Limit of Gate Oxide Thickness Scaling in MOSFETs due to Apparent Threshold Voltage Fluctuation Induced by Tunnel Leakage Current

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***Abstract*—We report on a new roadblock which will limit the gate oxide thickness scaling of MOSFETs. It is found that statistical distribution of direct tunnel leakage current through 1.2 to 2.8 nm thick gate oxides induces significant fluctuations in the threshold voltage and transconductance when the gate oxide tunnel resistance becomes comparable to gate poly-Si resistance. By calculating the measured tunnel current based on multiple scattering theory, it is shown that the device characteristics fluctuations will be problematic when the gate oxide thickness is scaled down to less than 1 nm.**

***Index Terms*—Device scaling, MOSFET, tunnel current, ultrathin gate oxides.**

I. Introduction

DEMONSTRATION of excellent performance for MOSFETs with a 1.5-nm thick gate oxide [1], [2] has stimulated extensive effort to further reduce the gate oxide thickness T_{ox}. Momose *et al.* [1], [2] have obtained a high transconductance of 1010 mS/mm for 90-nm gate length MOSFETs. The gate oxide was grown by rapid thermal oxidation (RTO) at 800 °C for 10 s. The source/drain (S/D) extensions of 30-nm junction depth were produced by solid-phase diffusion from a PSG film, achieving a sheet resistance of less than 10 k$\Omega/\square$. Recently the highest transconductance, 1120 mS/mm for 60-nm gate length MOSFETs has been obtained with a 1.3-nm thick gate oxide [3]. The oxide was grown by RTO at 1100 °C in pure oxygen at pressures from 1 to 500 torr. The shallow S/D junction was formed by low energy 2–4 keV As implantation with a dose ranging from 2–6×10^{14} cm^{-2}. The T_{ox} scaling limit has been argued in terms of stand-by power consumption due to the direct tunnel leakage current [4], the transconductance saturation due to a finite inversion layer thickness [5] and gate poly-Si depletion [6]. The influence of gate leakage tunnel current on the device characteristics has not yet been well examined except for the negative drain current offset problem [1], [2] which can be solved by scaling the gate length.

In this work, we have fabricated 0.1 to 20μm gate length nMOSFETs with 1.2 to 2.8-nm thick gate oxides to investigate the influence of direct tunnel leakage current I_g on the dc characteristics of MOSFET's. We have found that the statistical distribution of the direct tunnel leakage current through the ultrathin gate oxides induces significant fluctuations in the threshold voltage V_{th} and the transconductance G_m [7]. A simple model to quantitatively explain V_{th} and G_m fluctuations induced by I_g is proposed. The measured tunnel current through gate oxides has been in good agreement with theory, by which the T_{ox} scaling limit can be predicted.

II. Device Fabrication

Gate oxides with thicknesses of 2 to 3 nm were grown at 850 °C in 2% oxygen diluted with nitrogen on Si(100) substrates, whose surfaces were hydrogen-terminated by treatment in a 0.1% HF + 1% H_2O_2 solution [8]. For preparing oxides thinner than 2 nm, 2-nm thick oxides were etched-back by 0.1% HF. A schematic cross section of a fabricated MOSFET is shown in Fig. 1(a) together with the TEM picture [Fig. 1(b)]. The gate poly-Si was patterned with two-step electron cyclotron resonance (ECR) plasma etching. The anisotropic etching was first performed with Cl_2 and at a final stage of gate etch the etching gas was switched to a Cl_2/O_2 mixture to obtain a high etch selectivity. After the gate formation, 10 keV Sb ions were implanted at a dose of 1×10^{14} cm^{-2} through a 5-nm screen oxide to form S/D extensions with a junction depth of 20 nm [9]. The gate poly-Si was doped with 50-keV As ion implantation at a dose of 5×10^{15} cm^{-2} during the deep source and drain formation. The gate poly-Si sheet resistance was 800 $\Omega/\square$. in this case. Neither polycide nor salicide technique for low resistive gate was employed in order to enhance the influence of I_g on the device characteristics. The gate width W_g of evaluated MOSFETs was 10 μm and the distance between the gate pad and the device active region edge was also 10 μm. This structure is helpful to treat the gate poly-Si as a constant resistor in the model described in

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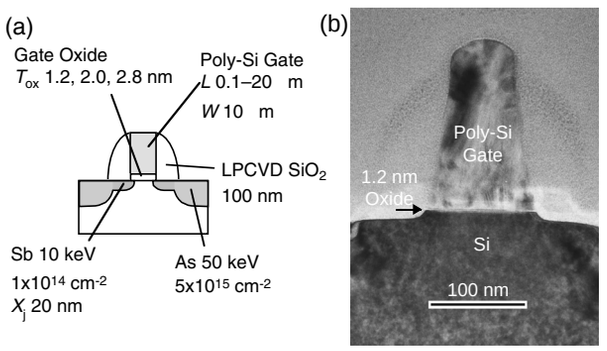

Fig. 1. (a) Schematic and (b) TEM cross sections of a fabricated MOSFET.

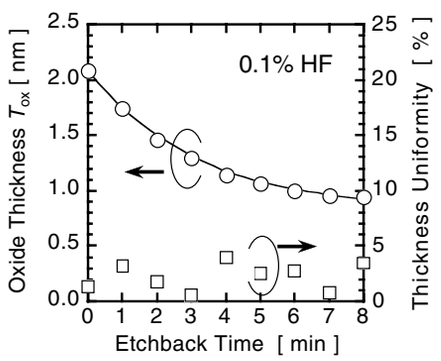

Fig. 2. Oxide thickness and uniformity versus etching time. Because of layer-by-layer etching mechanism of SiO_2 [11], [12], excellent thickness uniformity and thickness control are achieved.

the next section. The total thermal treatment time after extension formation was about 30 min at 850 °C.

The oxide thickness as a function of the wet etchback time is shown in Fig. 2. The etch rate decreases when the T_{ox} becomes thinner than 1.2 nm because the oxide layer within about 1 nm from the SiO_2/Si(100) interface is compressively strained [10], [11]. The thickness uniformity of the etched oxides is less than 5% over the entire wafer surface. This atomic scale thickness uniformity of the etched oxides is originated in a layer-by-layer etching mechanism, which was confirmed not only by atomic force microscopy (AFM) [12] but also by scanning reflection electron microscopy (SREM) [13] at each step of oxide stripping. Recently, it has been found that the oxide thinning by wet etchback significantly reduces SiO_2/Si interface states above midgap by employing photoelectron yield spectroscopy [14]. The oxide thickness was determined by ellipsometry using the refractive index of 1.460 and calibrated by X-ray photoelectron spectroscopy [15]. It has been demonstrated that the ellipsometric oxide thickness agrees well with the gate oxide thickness obtained from theoretical analysis of measured tunnel current based on multiple scattering theory (MST) [15], [16] and it also coincides with the thickness determined by *C-V* analysis of MOSFETs with taking into account the inversion layer quantization effects and gate poly-Si depletion [6].

III. Model of V_{th} Fluctuation Induced by Gate Tunnel Leakage Current

Here we propose a quantitative model to explain the relationship between the statistical distribution of I_g and fluctuations of

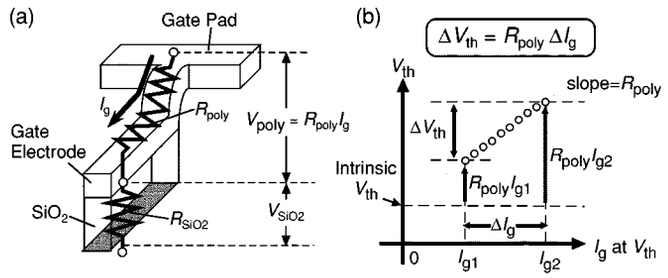

Fig. 3. Schematic explanation of V_{th} fluctuation induced by I_g distribution. (a) Equivalent circuit of I_g path, and (b) V_{th} shift and fluctuation caused by I_g variation. V_{th} is obtained by the constant current method ($I_d = (W_g/L_g)^* 10^{-7}$ A).

V_{th}. As illustrated in Fig. 3(a), the gate current flows into a channel via the gate poly-Si and gate oxide. When the gate oxide resistance R_{SiO2} is lowered by T_{ox} scaling, the voltage drop due to the gate poly-Si resistance R_{poly} can no longer be neglected. As a result, V_{th} apparently increases by the product of R_{poly} and I_g [Fig. 3(b)]. As depicted in Fig. 3(b), V_{th} fluctuates due to the statistical distribution of I_g over the range determined by the product of R_{poly} and ΔI_g. The slope of the dotted line and the y-axis-intercept correspond to R_{poly} and ideal V_{th}, respectively. For simplicity, the gate electrode is treated as a lumped resistance here. For more accurate modeling in real devices, effective local V_g shift due to the gate tunneling current on an active region is important. This local V_g shift problem is discussed in Section IV.

IV. Results and Discussion

The direct tunnel current I_g through 1.2 to 3.5-nm thick SiO_2 measured as a function of oxide voltage V_{ox} for MOSFETs and MOS diodes are compared with that calculated by the multiple scattering theory (MST) as shown in Fig. 4. Since the tunnel current measured for 1.0-μm gate length MOSFETs is quite consistent with that for the MOS diodes and the calculated one, no significant change in the tunnel current is induced by MOSFET fabrication processes such as gate patterning and ion implantation. Typical drain current-gate voltage (I_d–V_g) and gate current-gate voltage (I_g–V_g) characteristics for a 1.2-nm thick gate oxide MOSFET are shown in Fig. 5, where I_d is a few orders of magnitude larger than I_g and normal operation of the MOSFET is confirmed. I_g is relatively large with respect to I_d in the linear-mode turn-on region because electrons flow into the gate from both source and drain. The tunnel leakage current for 1.2–2.8 nm thick gate oxide MOSFETs at $V_g = 1.5$ V was measured as a function of gate length L_g as shown in Fig. 6, together with calculated results in which the oxide electric field strength at $V_g = 1.5$ V for each oxide thickness was evaluated by using device simulation. The measured I_g for $T_{ox} = 1.2$ nm is slightly lower than the theoretically calculated I_g, while those for $T_{ox} = 2.0$ and 2.8 nm agree with the calculated results. However, the experimental data for $T_{ox} = 1.2$ nm are in good agreement with the calculated result in which the voltage drop by poly-Si gate $R_{poly} I_g$ is taken into account. The result of [2], where $T_{ox} = 1.5$ nm and I_g at $V_g = V_d = 1.5$ V was measured as a function of L_g, is also shown in Fig. 6. Note that I_g for any cases increases in proportion to L_g because the gate width is kept constant, while the relationship as $I_g \propto L_g^{1.8}$ was obtained in [2].

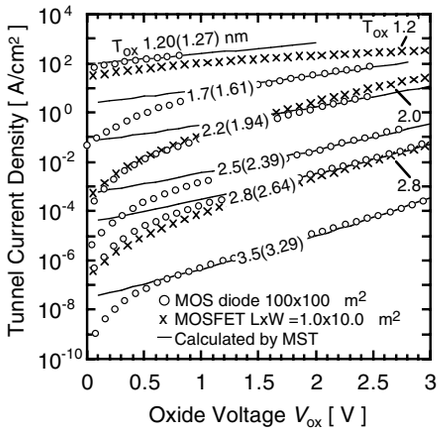

Fig. 4. Tunnel current density against oxide voltage for MOS diodes (solid circles) and MOSFETs (cross). The oxide thicknesses indicated in parenthesis are obtained by fitting theoretical *I–V* curves to measured ones, being in good agreement with the ellipsometric data.

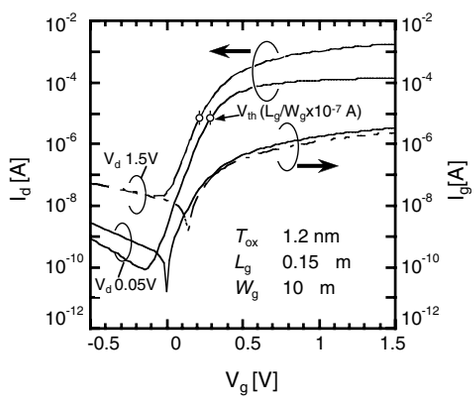

Fig. 5. I_d–V_g and I_g–V_g characteristics of 1.2-nm thick gate oxide MOSFET with $L_g = 0.15$ μm. The solid lines correspond to a linear mode *I–V* at $V_d = 0.05$ V, while dashed lines refer to a saturation mode I–V at $V_d = 1.5$ V.

The statistical distributions of I_g at $V_g = 1.5$ V for 1.2 to 2.8-nm thick gate oxides were measured. The average of I_g increases exponentially as T_{ox} is reduced as shown in Fig. 7. However, normalized I_g fluctuation defined as the standard deviation divided by the average of I_g is within 10% for all cases. The direct tunnel current is proportional to the exponent of T_{ox} [17] as follows:

$$I_g \propto \exp(-KT_{ox}). \tag{1}$$

Here, K is a constant value consisting of the electron effective mass, the barrier potential and the oxide voltage. Assuming the T_{ox} is the only factor which leads to I_g deviation, the following equation is obtained using the law of the error propagation.

$$\sigma I_g / I_g = \left[\left(\partial I_g / \partial T_{ox} \right)^2 \sigma T_{ox}^2 \right]^{1/2} / I_g = K \sigma T_{ox}. \tag{2}$$

Here, σI_g and σT_{ox} are deviations of I_g and T_{ox}, respectively. Therefore, the result that the normalized I_g is comparable for all T_{ox} means that σT_{ox} for the 1.2-nm oxide after the wet etch-back is also comparable to that for the thicker oxides grown by dry oxidation only. In the case of $T_{ox} = 1.2$ nm, the oxide thickness deviation estimated from the measured I_g deviation

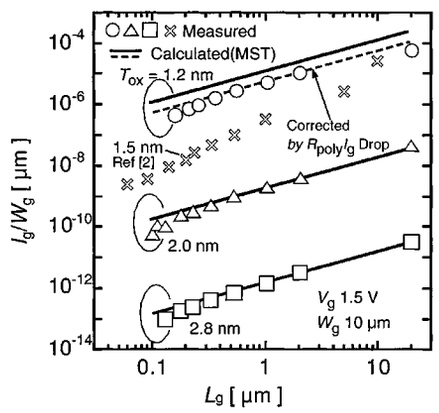

Fig. 6. I_g at $V_g = 1.5$ V versus L_g for MOSFETs. The I_g increases in proportion to L_g (solid squares, triangles and circles). The solid lines correspond to theoretical calculation without taking into account $R_{poly}I_g$ drop, while the dashed line for $T_{ox} = 1.2$ refers to the calculated result corrected by $R_{poly}I_g$ drop. Open circles refer to the result of Ref. [2], where $I_g \propto L_g^{-8}$ with a gate width of 10 μm.

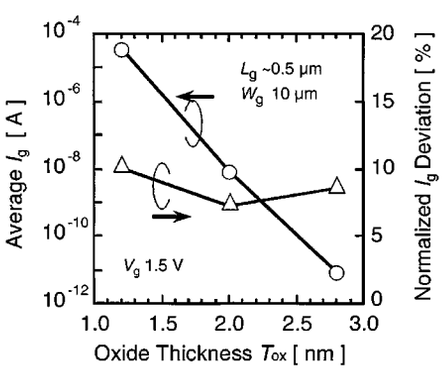

Fig. 7. Average of I_g at $V_g = 1.5$ V and normalized I_g deviation for 1.2 − 2.8 nm gate oxide MOSFETs with $L_g = 0.5$ μm.

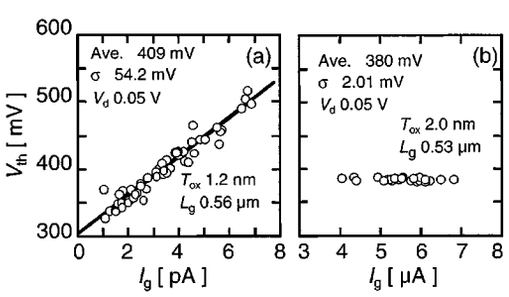

Fig. 8. Relationship between linear mode threshold voltage V_{th}(lin) and I_g distribution at $V_g = V_{th}$(lin) for (a) 1.2 nm, and (b) 2.0 nm gate oxide MOSFET's. V_{th} is obtained by the constant current method ($I_d = (W_g/L_g)^* 10^{-7}$ A).

is less than 0.1 nm, which is smaller than 1 molecular layer of the oxide. Such an extremely uniform, ultrathin gate oxide layer can be grown on the Si wafer because the layer-by-layer oxidation mechanism controls the oxide growth [18]. Fluctuation in gate-poly-Si resistance R_{poly} is also a possible cause of the I_g fluctuation, while no correlation was found between the I_g and R_{poly} fluctuations by a whole wafer measurement.

Different from I_g fluctuation, as shown in Fig. 8, V_{th} for 1.2-nm thick gate oxide MOSFETs significantly increases in proportion to I_g [Fig. 8(a)], while V_{th} remains nearly constant regardless of the I_g distribution for 2.0-nm thick gate oxide

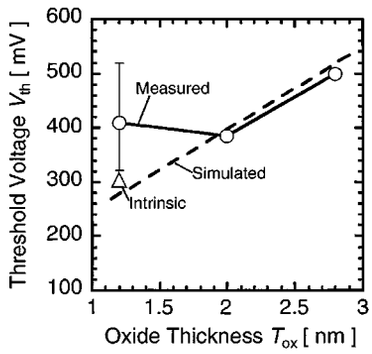

Fig. 9. Dependence of V_{th} on T_{ox}. The dashed line refers to V_{th} evaluated by device simulation without taking into account the gate leakage current. An open triangle for $T_{ox} = 1.2$ nm refers to V_{th} obtained from the y-axis intercept of Fig. 8(a).

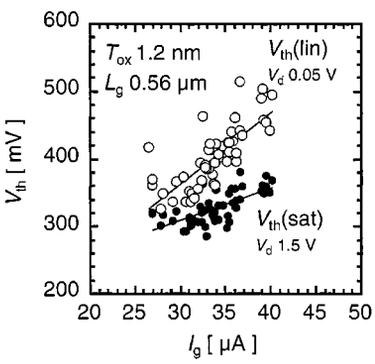

Fig. 10. Variation of V_{th}(lin) and V_{th}(sat) against I_g for $V_g = 1.5$ V. The difference between V_{th}(lin) and V_{th}(sat) seems to be increased by the increase of I_g, this is attributed to lowering of intrinsic V_{th} and the corresponding reduction of $R_{poly}I_g$ drop at apparent V_{th} at higher drain voltage.

MOSFETs [Fig. 8(b)]. A systematic variation of V_{th} with changes in I_g as indicated in Fig. 8(a) is over 200 mV, which is not acceptable for the circuit design. R_{poly} evaluated from the slope of V_{th} versus I_g curve [see Fig. 3(b)] is 800 Ω/□, which agrees with the measured poly-Si sheet resistance. The dependence of V_{th} on T_{ox} is shown in Fig. 9, where an average value of V_{th} for $T_{ox} = 1.2$ nm is larger than that for $T_{ox} = 2.0$ nm. However, an intrinsic value of V_{th} for $T_{ox} = 1.2$ nm as defined by the y-axis-intercept in Fig. 8(a) is very close to the result evaluated by device simulation as also indicated in Fig. 9.

The influence of $R_{poly}I_g$ drop depends on the operating bias point of MOSFETs. For example, under the saturation condition, I_g has a large gradient along the channel because of potential change along the channel and total I_g is smaller than that for the linear region. To confirm how the difference in the operating bias point affects FET characteristics, the I_g dependence of V_{th} in the linear mode region V_{th}(lin) is compared to that of V_{th} in the saturation region V_{th}(sat) as shown in Fig. 10, where V_{th} is plotted against I_g for $V_g = 1.5$ V and $V_d = 0.05$ or 1.5 V. Generally, the V_{th} lowers by increasing V_d because of the drain-induced barrier lowering (DIBL). In this figure, the difference in V_{th}(lin) and V_{th}(sat) seems to be larger as I_g becomes larger. In other words, DIBL seems to be enhanced by I_g. However, this tendency can be attributed to the variation of I_g caused by V_g change. As shown in Fig. 5, I_g increases exponentially as V_g increases. The small decrease in the intrinsic V_{th} due to the DIBL causes a significant

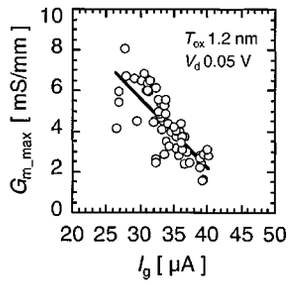

Fig. 11. Relationship between linear mode $G_{m\_\max}$ and I_g distribution at $V_g = 1.5$ V for 1.2 nm gate oxide MOSFETs with $L_g = 0.56$ μm.

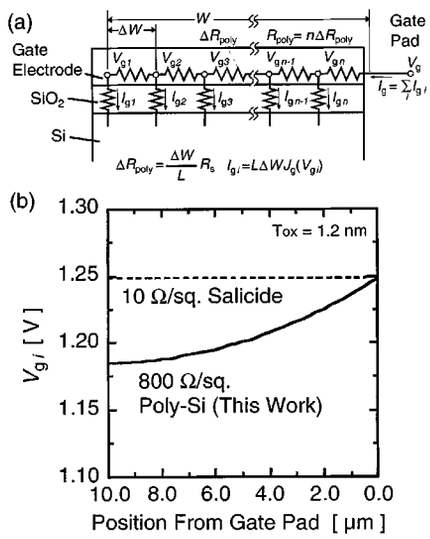

Fig. 12. (a) Equivalent circuit model for a MOSFET gate structure employed for estimating the influence of the gate tunneling current. (b) Variation in V_{gi} along the gate width direction.

reductions of I_g and the corresponding reduction of the gate voltage drop $R_{poly}I_g$. Thus, the apparent increase in DIBL is explained by the reduction of I_g at V_{th}.

As a result of V_{th} fluctuation due to I_g distribution, $G_{m\_\max}$ also fluctuates with the I_g distribution as shown in Fig. 11 for T_{ox} of 1.2 nm. This can be explained by a decrease in effective V_g applied to the gate oxide because of $R_{poly}I_g$ drop. Drain current-drain voltage (I_d–V_d) characteristics for 1.2 nm thick gate oxide MOSFETs exhibit the negative I_d offset for long L_g, while the offset disappears for $L_g = 0.56$ μm in consistent with a previous report [1]. In contrast, V_{th} and $G_{m\_\max}$ fluctuations for $T_{ox} = 1.2$ nm are similarly observed even for the shorter channel length MOSFETs. This is because the value of R_{poly} increases as L_g is scaled down. The observed fluctuation in V_{th} for $T_{ox} = 1.2$ nm MOSFET's makes the circuit design difficult. Also the fluctuation of $G_{m\_\max}$ by the I_g distribution spoils the merit of T_{ox} scaling.

In the above discussion, R_{SiO2} and R_{poly} have been treated as lumped constants for simplicity. In order to accurately evaluate the potential variation along the gate electrode, the gate structure is approximated with an equivalent circuit model as illustrated in Fig. 12(a). The tunnel current I_{gi} in the segmented portion of the gate structure was calculated from the measured J_g (gate current density) versus V_g characteristics. As shown in Fig. 12(b), in the case of the poly-Si gate with a 800-Ω/□ sheet resistance, the gate

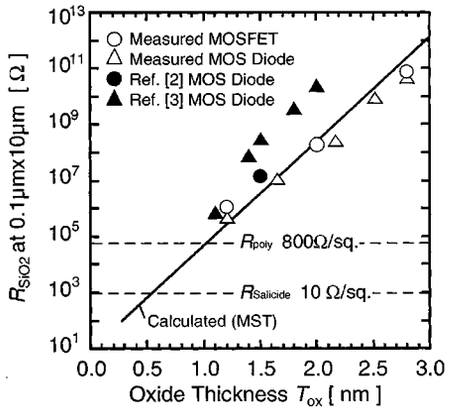

Fig. 13. Relationship between oxide resistance R_{SiO2} and oxide thickness T_{ox}. R_{SiO2} was obtained by $\partial V_{ox}/\partial I_g$, while R_{SiO2} for [2] was evaluated by V_g (= 1.5 V) divided by I_g.

potential falls by 65 mV at 10 μm from the gate pad where $V_g = 1.25$ V is applied. For the lower sheet resistance of 10 Ω/sq., the voltage drop is negligible. This result shows that a relatively large tunneling current harms the dc performance of MOSFETs with a large W. Concerning the influence on J_g variation, as indicated in Fig. 4, J_g for $T_{OX} = 1.2$ nm MOSFET very weakly depends on the oxide voltage V_{OX}. Therefore, the potential drop along the gate over the range of 0–65 mV shown in Fig. 12 hardly modifies the local tunnel current. This supports that the discussion based on the simple model in Fig. 3 is reasonable.

A proposed model of the V_{th} fluctuation due to the I_g distribution as shown in Fig. 3 indicates that the gate oxide tunnel resistance R_{SiO2} decreases with decreasing T_{ox} and when R_{SiO2} becomes comparable to the gate poly-Si resistance R_{poly}, the V_{th} fluctuation is significant. In Fig. 13, R_{SiO2} as defined by $\partial V_{ox}/\partial I_g$ at $V_g = 1.5$ V where I_g is the calculated tunnel current is plotted as a function of T_{ox} together with experimental data. In the calculation, the oxide electric field E_{ox} and gate area $L_g \times W_g$ were 5 MV/cm and 0.1×10 μm^2, respectively. Measured values of R_{SiO2} were obtained from I_g vs. oxide voltage curves in Fig. 4, being consistent with the calculated one. As references, resistances of poly-Si gate R_{poly} (this work) and salicided gate R_{salicide} are indicated in the figure. In this calculation, we employed sheet resistances of the poly Si gate and the salicided gate to be 1000 Ω/□ and 10 Ω/□, respectively. Considering that R_{salicide} for 0.1×10 μm^2 gate area is 1000 Ω, R_{SiO2} becomes comparable to R_{salicide} when T_{ox} is decreased to 0.8 nm. Namely, even if the gate electrode resistance is reduced by using salicide, V_{th} and G_m fluctuations will emerge when the T_{ox} is reduced to 0.8 nm. Though many alternative high-k materials are under investigation for such sub-1-nm equivalent-oxide-thickness generations, the fluctuation problem described in this paper should be taken into account. Because any materials have possibility to meet the same problem by the further reduction of thickness and increase of the gate current.

V. Summary

MOSFETs with 1.2 to 2.8 nm thick gate oxides have been fabricated. The gate tunnel leakage current has been evaluated both experimentally and theoretically. It is shown that the statistical distribution of gate tunnel leakage current causes significant fluctuations in V_{th} when the gate oxide tunnel resistance becomes comparable to the gate poly-Si resistance. Since this phenomenon is attributed to the voltage drop in the gate electrode, characteristics other than V_{th}, such as $G_{m\_\max}$, are also affected. The scaling limit of gate oxide thickness is discussed based on both measured and calculated results. It is predicted that when using a low-resistive salicide gate, these problems will not emerge until the oxide thickness is scaled to 0.8 nm.

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