Line-to-Ground Capacitance Calculation for VLSI: A Comparison

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Abstract-A **comparison is made between various approximations of the line-to-ground capacitance problem in a VLSI environment. It is shown that with up-to-date dimensions, the simple parallel-plate model is no longer adequate. However, easy-to-use and fast-to-compute formulas exist that result in accurate and reliable capacitance values.**

I. INTRODUCTION

THE PERFORMANCE obtained with VLSI is heavily influenced by parasitic effects,' such as interconnect resistance and capacitance. With increasing chip area and circuit complexity, the average interconnection length grows, making accurate consideration of these effects a necessity in order to produce working samples in the first run.

The parasitic capacitance problem is three-dimensional by nature. Three-dimensional calculations, however, are very expensive and thus seem to be an inadequate approach for VLSI. With sufficient accuracy the problem can be reduced to a set of two-dimensional ones. Capacitive couplings are described by three different components [l]:

1) line-to-ground capacitance (usually between a certain net on any layer and substrate);
2) line-to-line capacitance (between two nets on the same layer);
3) crossover capacitance (between two nets on different layers).

In advanced MOS technologies, where the interconnection pitch is near or less than 2 μm (i.e., the spacing is near or less than 1 μm), the line-to-line capacitance is comparable to or larger than the line-to-ground capacitance. Moreover, the line-to-ground capacitance is strongly affected by the spacing. This paper, however, deals only with the first component, which is still dominating the capacitance problem in many (e.g. bipolar) technologies.

II. PROBLEM AND SOLUTIONS

Calculating the capacitance of a rectangular conductor facing a ground plane (Fig. 1) is a well-known problem from basic electrostatic field theory. With respect to Fig. l(a), in which conservative design rules of a bipolar SBC (standard buried collector) process were used, a parallel-plate approximation seems to be well suited [2]. In fact, the parallel-plate result is about 33 percent apart from the true value. Using advanced design rules (Fig. l(b)), the error is 57 percent. Thus, parallel-plate approximations should no longer be considered.

Basically, calculating the capacitance of a given arrangement means solving Poisson's equation:

$$\Delta v = \mathrm{div}\,\mathrm{grad}\,v = -\frac{\rho}{\epsilon}$$

where v is the electric potential, ρ the space charge, and ϵ the dielectric constant.

There are a couple of approaches which can solve this problem numerically, for instance, finite difference or finite element methods [3]. Obtained results are fair, with accuracies up to 0.2 percent compared to the theoretically exact values. More recently, an integral method based on Green's function was proposed [4]. Reported discrepancies to measured data were smaller than 10 percent.

On the other hand, all numerical methods are computationally expensive, so that run times are prohibitive for VLSI layouts, even in the described two-dimensional case. The same is true for the exact analytical solution, which is difficult to derive (see electromagnetic field theory literature) and results in an extremely complicated description of this geometrically very simple configuration.

A possible solution to the problem is to use numerical methods to generate so-called look-up tables, which contain specific capacitance values to be used, e.g. during circuit extraction to compute the geometry-dependent absolute values,

Nevertheless, there is a strong need for simple and fast approximating formulas to calculate capacitance values directly, e.g. in the design phase.

The most accurate formula known to the author has been published by Chang [5], who used conformal transformation to derive relatively simple equations. Provided that $w \geq h$ holds, their accuracy is within 1 percent of the exact value. In the scope of this paper, Chang's approach is used as a reference. The original equations can be taken from [4]. Note that the first publication, in 1976, was completed and corrected in 1977.

Elmasry [6] proposed a greatly simplified analytical formula in 1981. Its first term describes the parallel-plate

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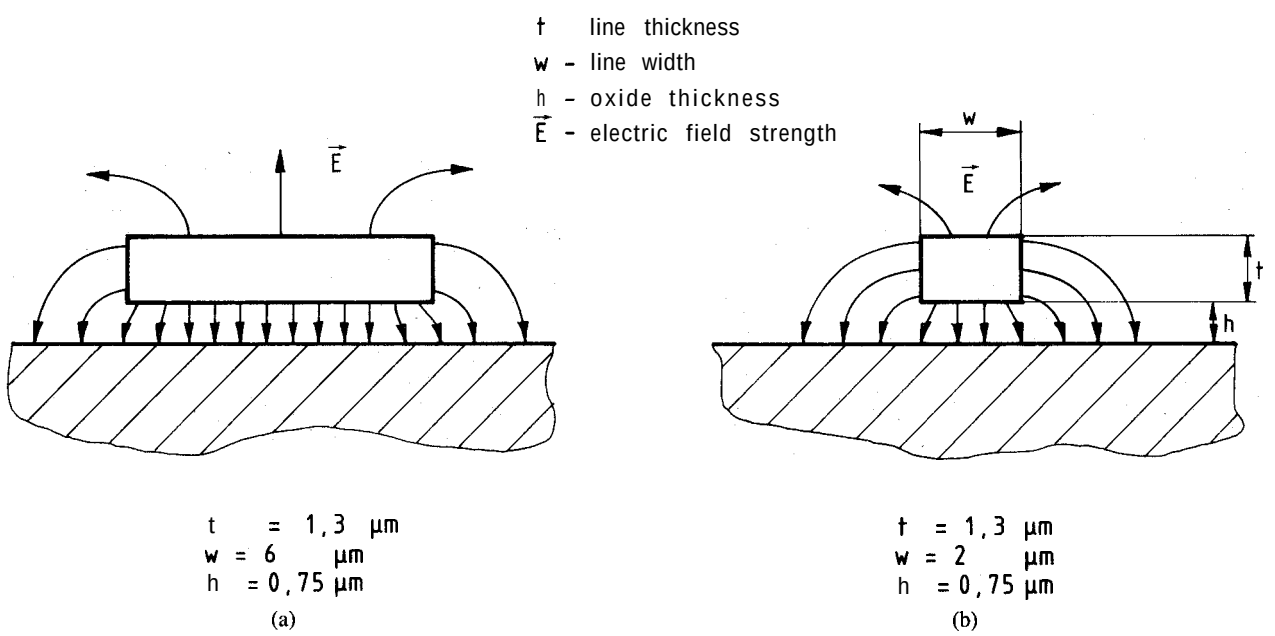

Fig. 1. An interconnection line facing substrate (the ground plane). (a) Conservative bipolar design rules. (b) Advanced bipolar design rules.

capacitor formed by the bottom plate of the interconnection line and ground, the second one additional contributions of the side walls, and the third one those of the top plate:

$$c = \epsilon\left[\frac{w}{h} + 2\ln\left(1 + \frac{t}{h}\right) + \frac{2t}{h}\ln\left(1 + \frac{w/2}{t+h}\right)\right] \tag{1}$$

where c is the capacitance per unit length.

In 1982 Yuan and Trick [7] presented another simple analytic approximation which has a direct physical interpretation. They replaced the rectangular line profile with an "oval" one, composed of a rectangle and two half-cylinders (Fig. 2). The resulting capacitance can be calculated as the sum of a parallel plate capacitor with width $w - t/2$ and a cylindrical one with $r = t/2$. This results in a capacitance c given by

$$c = \epsilon\left[\frac{w - t/2}{h} + \frac{2\pi}{\ln\left(1 + \frac{2h}{t} + \sqrt{\frac{2h}{t}\left(\frac{2h}{t} + 2\right)}\right)}\right]. \tag{2}$$

Provided that $w \geq t/2$ and $t \approx h$ hold, a maximum error of 10 percent with respect to Chang is stated. In the case of $w < t/2$, which is a more theoretical one, an empirical formula is suggested.

Sakurai and Tamaru [8] felt in 1983 that the accuracy of approximations such as [6] was not sufficient. Instead of improving the analytical approach, they evaluated a couple of numeric solutions and defined a sheer empirical

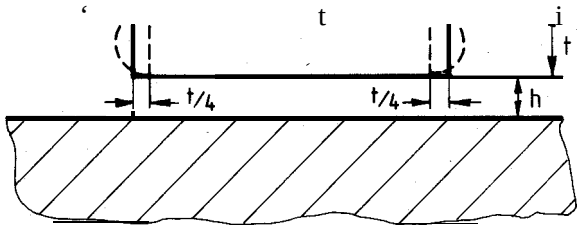

Fig. 2. Simplified arrangement of Yuan and Trick.

formula:

$$c = \epsilon\left[1.15\left(\frac{w}{h}\right) + 2.80\left(\frac{t}{h}\right)^{0.222}\right]. \tag{3}$$

The first term represents the (bottom and top) plates of the interconnection line and the second one considers the side walls. Within ranges of $0.3 < w/h < 30$ and $0.3 < t/h < 30$ an accuracy better than 6 percent is claimed.

In 1984 v.d. Meijs and Fokkema [9] improved Sakurai's approach by extending the empirical expression and simultaneously reducing the range of validity. The first term of their formula describes the parallel-plate capacitor and the other three allow for all side effects:

$$c = \epsilon\left[\left(\frac{w}{h}\right) + 0.77 + 1.06\left(\frac{w}{h}\right)^{0.25} + 1.06\left(\frac{t}{h}\right)^{0.5}\right]. \tag{4}$$

The maximum deviation from Chang's formula is given as 2 percent when $w/h \geq 1$, $0.1 \leq t/h \leq 4$ and as 6 percent when $w/h \geq 0.3$, $t/h \leq 10$ hold. All cited ranges seem to be adequate for practical applications. In bipolar technologies for instance t/h is within a 1.5 to 2.0 range.

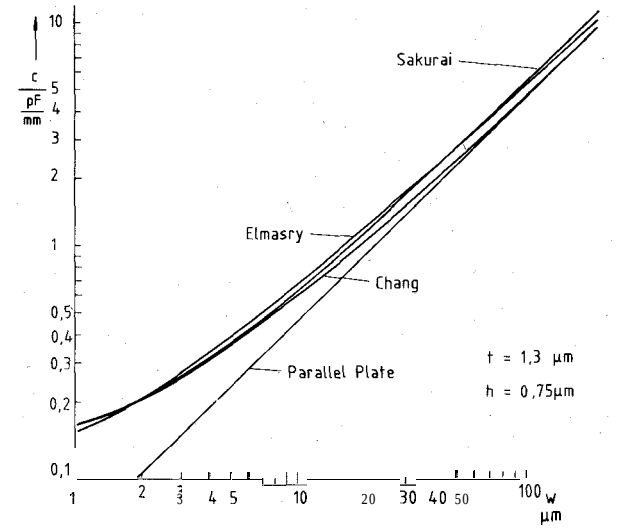

Fig. 3. Length-specific capacitances c versus line width *w*.

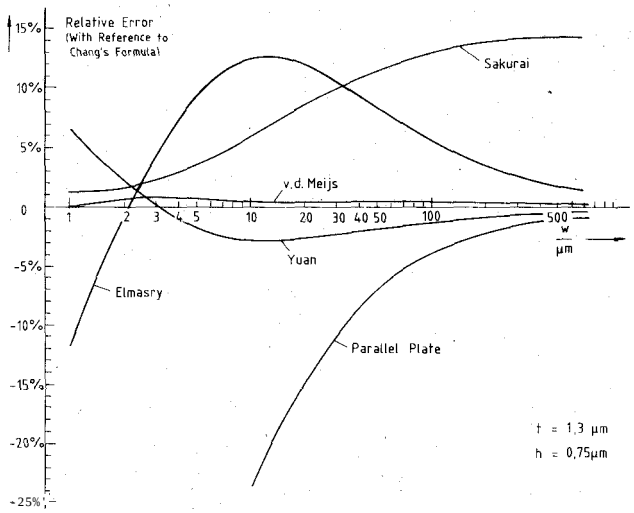

Fig. 4. Relative error versus line width *w*.

III. Comparison

Choosing the best approach for a specific application on the base of the published data is not an easy task. Accuracies are given only for certain ranges of w, t, and h and these ranges differ in all publications. As authors tend to notify the ranges of best approximation of their formulas (an understandable proceeding), an unbiased comparison is necessary.

For this purpose, a program has been written [10] that computes line-to-ground capacitances according to (1)-(4) and-as a reference-to Chang's formulas for a wide range of parameter values t, h, and w. Some results are given in Figs. 3 and 4. Because Chang's formula is a valid reference only for ratios w/h > 1, the comparison has been restricted to that region.

Fig. 3 shows length specific capacitances c versus line width w. For oxide and line thicknesses, values have been taken from a bipolar process as t = 1.3 μm and h = 0.75 μm. It is obvious that the parallel-plate approximation is totally inadequate for line widths below 20 μm (!) (i.e., *w/h* ratios $\leq$ 15). Moreover, it can be seen that the results of the Elmasry and the Sakurai/Tamaru approximations also differ significantly from the reference values, especially for small (≤ 2) and large (≥ 10) *w/h* values. On the contrary, the approximations by Yuan/Trick and v.d. Meijs/Fokkema are completely within the graphic resolution over the total w range.

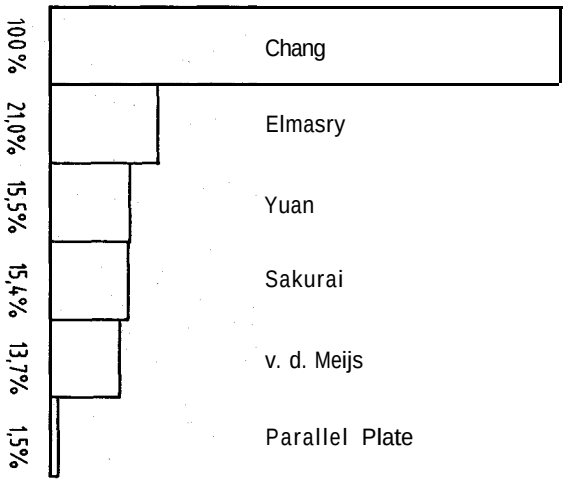

Fig. 5. Relative computing time.

A closer look at accuracies is given in Fig. 4. It proves that the v.d. Meijs/Fokkema approximation is superior to all others. Within a very broad w range, the accuracy is within 1 percent. This seems more than sufficient for layout verification purposes.

It is interesting to see that Sakurai's equation yields better results for smaller lines, making it a possible alternative for small geometries. On the other hand, Yuan's formula, which returns fairly good results for larger *w/h* ratios, is no longer usable when *w/h* gets smaller than 3.

Fig. 5 shows that the v.d. Meijs/Fokkema approximation is not only the most accurate but is also the fastest. Though (4) looks more complicated than (3), it is faster to compute, because in Pascal, which was used here, the exponentiation $y = a^b$ in (3) is slower than the multiple SQRT calls in (4).

IV. Conclusions

In this contribution, several methods for calculating the capacitance of an interconnection line facing the ground plane (substrate) have been examined and compared. Using up-to-date design rules, the formerly used parallel-plate approximation should be out of consideration, although it is indeed the fastest one. On the other hand, it is not necessary to apply expensive numerical methods to obtain accurate results for this geometrically simple problem. As shown here, there are relatively simple and fast formulas yielding satisfactory capacitance values even for small *w/h* ratios. Additional measurements on test structures using Fig. 1(b) design rules (w = 2 μm, t = 1.3 μm, h = 0.75 μm) were made in the context of another paper [11] to corroborate the calculated results. The measured value of c = 0.2 pF/mm proved that the approximation of v.d. Meijs/Fokkema is the best choice in every respect.

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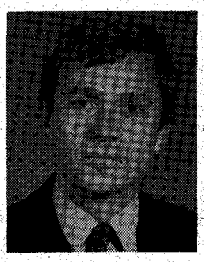

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