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Linear CMOS transconductance element for VHF filters — Source link

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Topics: Transconductance, Integrator, Linearity, CMOS and Differential amplifier

with ΔI_b denoting the observed bias current period and τ_x the external cavity round-trip time. Inserting the measured values ($\Delta I_b = 2{\cdot}69$ mA, $\partial f_{opt}/\partial I_b = 1{\cdot}67$ GHz/mA), the optical feedback location is determined to be at a distance

$$L_x = \frac{c}{2\Delta f_x} \simeq 33\,\text{mm} \tag{2}$$

Knowing this value, the location of the feedback could clearly be identified at the front face of the first optical isolator. Moving the isolator 10 mm further away gave the result depicted in Fig. 2. Comparison with eqns. 1 and 2 confirms the assumptions made.

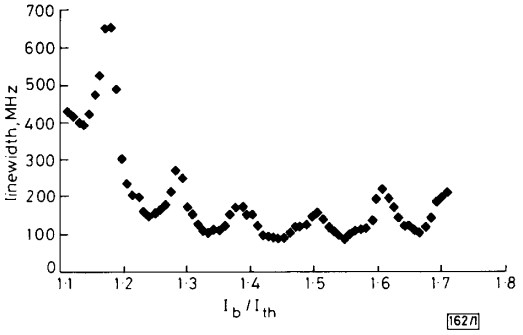

Fig. 1 *Measured linewidth Δv against CW bias current I_b normalised to threshold current I_{th}*

The strength of feedback can be estimated using single-frequency laser theory. The linewidth Δv changes with strength C and phase Φ_x of feedback according to[4]

$$\frac{\Delta v}{\Delta v_0} = \frac{1}{[1 + C\cos(\Phi_x + \text{constant})]^2} \tag{3}$$

Here Δv_0 denotes the linewidth without any feedback, and the feedback strength is given by the parameter C:[2,5]

$$C = a_x \frac{\tau_x}{\tau_D} \frac{1-R}{\sqrt{(R)}} \sqrt{(1+\alpha^2)} \tag{4}$$

with a_x denoting the total field attenuation per round-trip in the external cavity, $\tau_D = 4{\cdot}9$ ps is the round-trip delay of the laser cavity, $R = 0{\cdot}31$ is the power reflectivity of the laser facets, and $\alpha = 6{\cdot}6$ is the linewidth enhancement factor.[6] According to eqn. 3 the feedback parameter $C < 1$ is related to the measured linewidth maxima Δv_{max} and minima Δv_{min} as follows:

$$C = \frac{1 - \sqrt{(\Delta v_{min}/\Delta v_{max})}}{1 + \sqrt{(\Delta v_{min}/\Delta v_{max})}} \tag{5}$$

From Fig. 1, near $I_b/I_{th} = 1{\cdot}5$, one obtains about 155 MHz and 80 MHz for the maximum and minimum linewidths, respectively, leading to a feedback parameter $C = 0{\cdot}16$. In the same way one obtains from Fig. 2 about 160 MHz and 80 MHz, leading to $C = 0{\cdot}17$. With $C = 0{\cdot}16$ in eqn. 4 there results a total field attenuation per round-trip in the external cavity of $a_x = 4{\cdot}3 \times 10^{-4}$, corresponding to a feedback signal of about 67 dB below the laser output.

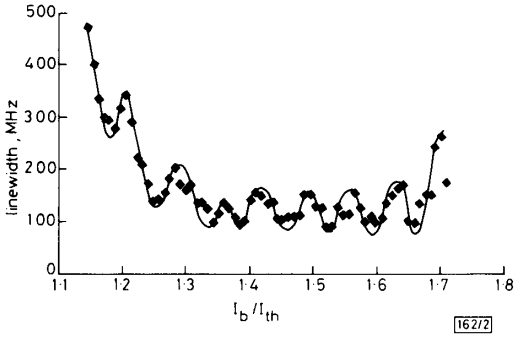

Fig. 2 *As Fig. 1, but with isolator front face distance increased by 10 mm*

Discussion: The method is very sensitive to low-level feedback signals. In view of the well collimated beam, it is not surprising that the two locations of the optical isolator gave the same strength of the optical feedback. Obviously, reflections from the collimating lens are of minor influence. The accuracy achieved here may be estimated roughly to be ± 1 dB. However, more closely spaced measurement points would have resulted in higher accuracy. After each current step the feedback phase undergoes increasing random disturbances. Therefore the measured linewidth/current functions in Figs. 1 and 2 lack the sufficient smoothness required for a highly accurate determination of the extrema. High measurement speed (here aided by a digital oscilloscope, HP 54501A) is important for good accuracy. For reading the maximum (minimum) from the Figures, we chose the upper (lower) envelope of the measured points.

Conclusion: The strength and location of low-level parasitic optical feedback are reflected by the amplitude and period, respectively, of the ripple in the measured linewidth/injection current curve of the diode laser used. The method is very sensitive. However, its accuracy depends on the availability of several laser parameters.

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LINEAR CMOS TRANSCONDUCTANCE ELEMENT FOR VHF FILTERS

Indexing terms: Circuit theory and design, Filters, Inverters

A differential transconductance element based on CMOS inverters is presented. With this circuit a linear, tunable integrator for very high-frequency continuous-time integrated filters can be made. This integrator has good linearity properties (THD < 0·04%, $V_{ipp} = 1{\cdot}8$ V), nondominant poles in the gigahertz range and a 40 dB DC gain.

Introduction: Most high-frequency transconductance-C filters which have been published so far are built with simple fully differential transconductors. These transconductors are (linearised) differential pairs with a common-mode feedback loop.[1,2] If no linearisation is applied, the linearity will be rather poor; if linearisation is applied, extra nodes will appear in the circuit, resulting in parasitic poles or zeros.[2] Better linearity can be obtained if the 'square-law principle'[3] is used. However, the published circuits using this principle also have internal nodes,[3–5] and hence show inferior high-frequency behaviour. Special techniques[4] can compensate for these effects in the low megahertz range.

The circuit presented here makes use of the square-law principle and has no internal nodes. This results in good linearity and a large bandwidth. Further, it has a tunable transconductance and DC gain.

Transconductor: The transconductor schematic diagram is given in Fig. 1*a*; it consists of six CMOS inverters, which are for the moment all presumed to be equal ($V_{dd} = V'_{dd}$). During the preparation of this letter it was discovered that the same circuit has independently been described as part of a voltage amplifier.[6]

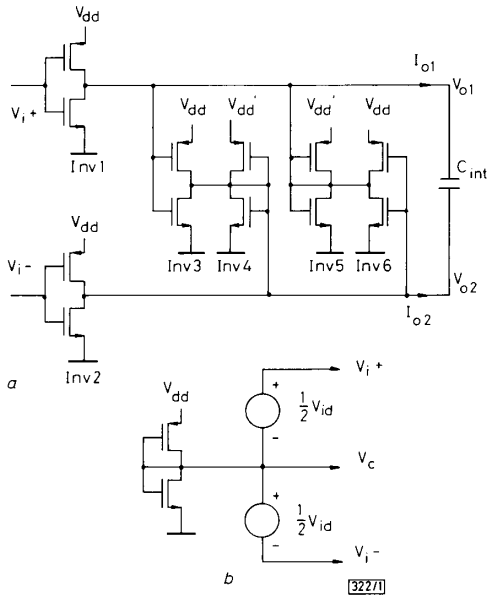

Fig. 1

a VHF linear transconductance element
b Definition of input voltages

The basic V/I conversion is performed by two CMOS inverters. If these inverters Inv1 and Inv2, are driven by a differential input voltage V_{id}, balanced around a certain common mode level V_c (see Fig. 1*b*), the differential output current will be proportional to the differential input voltage.

If the drain currents of an n-channel and a p-channel MOS transistor in saturation are written as

$$I_{dn} = \frac{\beta_n}{2}(V_{gs} - V_{tn})^2 \quad \text{and} \quad I_{dp} = \frac{\beta_p}{2}(V_{sg} - V_{tp})^2 \qquad (1)$$

the differential output current can be manipulated into the form

$$\begin{aligned} I_{od} &= I_{o2} - I_{o1} \\ &= V_{id}(V_{dd} - V_{tn} - V_{tp})\sqrt{(\beta_n \beta_p)} \\ &= V_{id} g_{md} \end{aligned} \qquad (2)$$

as long as the transistors operate in strong inversion and saturation.

Hence the differential transconductance (g_{md}) is linear, even with nonlinear inverters, i.e. if $\beta_n \neq \beta_p$. To reduce common-mode output currents however, β_n should be chosen close to β_p. The transconductance can be tuned by means of V_{dd}. For this purpose a tunable power-supply unit needs to be added.

Common-mode feedback: The common-mode level of the output voltages V_{o2} and V_{o1} is controlled by the four inverters Inv3–Inv6. For simplicity the transconductances g_m of these inverters are assumed to be linear ($\beta_n = \beta_p$). Inv4 and Inv5 are shunted as resistors connected between the output nodes and the common-mode voltage level V_o. The values of these resistors are $1/g_{m4}$ and $1/g_{m5}$. Inv3 and Inv6 inject currents $g_{m3}(V_c - V_{o1})$ and $g_{m6}(V_c - V_{o2})$, respectively, into these resistors.

The result for common signals is that the 'V_{o1}' node is virtually loaded with a resistor $1/(g_{m5} + g_{m6})$ and the 'V_{o2}' node with a virtual resistor $1/(g_{m3} + g_{m4})$. For differential signals the 'V_{o1}' node is loaded with a resistor $1/(g_{m5} - g_{m6})$ and the 'V_{o2}' node is loaded with a resistor $1/(g_{m4} - g_{m3})$. If the inverters have the same supply voltage and geometry, all the g_m will be equal. Thus the network Inv3–Inv6 forms a low-ohmic load for common signals and a high-ohmic load for differential signals, resulting in a controlled common-mode voltage level of the outputs.

If the inverters Inv3–Inv6 are not exactly linear ($\beta_n \neq \beta_p$), it can be shown that only for common-mode signals is the load resistance nonlinear.

DC gain enhancement: The DC gain of the transconductor-C integrator can be increased by loading the differential inverters with a negative resistance for differential signals. By choosing $g_{m3} > g_{m4}$, $g_{m5} = g_{m4}$ and $g_{m6} = g_{m3}$ this negative resistance, $1/\Delta g_m = 1/(g_{m4} - g_{m3}) = 1/(g_{m5} - g_{m6})$, is simply implemented, without adding extra nodes to the circuit. The width of the transistors in Inv4 and Inv5 can be designed slightly smaller than those of Inv3 and Inv6.

To obtain a more exact filter response, the DC gain of the integrators can be fine-tuned during operation (Q tuning) with a separate supply voltage V'_{dd} for Inv4 and Inv5. If in a filter only one value for V'_{dd} is used and the matching is ideal, then the DC gain of every integrator can theoretically become infinite if $\Delta g_m = -3/R_{out}$, where R_{out} is the output resistance of one inverter. However, it can be shown that the maximal DC gain of an integrator will be limited by mismatch. If transconductance mismatch occurs in Inv3–Inv6 of one integrator, the maximal DC gain will be less than infinite; 1% mismatch results in a maximal DC gain of 100 (40 dB).

If $\Delta g_m < -3/R_{out}$ the net load resistance will become negative. A stand-alone integrator then would become unstable owing to the right-half-plane pole. However, a more detailed analysis and practical experiments show that a gyrator or biquad section built with these building blocks will remain stable. This is owing to the feedback loops inherent to a filter structure constructed with gyrators or biquad sections.

Bandwidth: The circuit presented here has a large bandwidth due to the absence of internal nodes. In filter structures where all the parasitic capacitances are shunted parallel to the integration capacitors, the only parasitic poles are due to the finite transit-time of the carriers in the MOS channel, which are, according to Reference 7, located in the gigahertz range.

Experimental results: The differential transconductance g_{md} (2) of the transconductor was measured at different supply voltages using commercially available inverter arrays (CA3600). The results are given in Fig. 2. The nonlinearities in the normal operating range are mainly due to mobility reduction.

The total harmonic distortion of the differential voltage to current conversion, measured for $V_{dd} = 4$ V, was less than 0·04% for 1·8 V_{pp} input signals at 1 kHz. For $V_{dd} = 8$ V, the THD was less than 0·05% for 1·8 V_{pp} input signals.

A low-frequency, third-order elliptic lowpass filter breadboard has been built with 'digital' SCL4049 inverters. Without Q tuning the DC gain of the integrators was 20 dB ($V_{dd} = V'_{dd} = 5$ V), resulting in a poor filter characteristic. By means of V'_{dd} the DC gain was increased ($V_{dd} = 5$ V, $V'_{dd} = 4{\cdot}8$ V), resulting in a filter characteristic close to the theoretical response.

Simulations indicate that filters in the 20–100 MHz range should be possible.

Conclusions: The CMOS transconductor circuit presented here has a large bandwidth thanks to the absence of internal nodes. Owing to the square-law-principle the linearity is good and the transconductance can be tuned by means of the supply voltage V_{dd}. The DC gain can be designed via the MOSFET geometries and can be fine-tuned by means of a separate supply voltage V'_{dd} if necessary. Thus, Q tuning becomes possible.

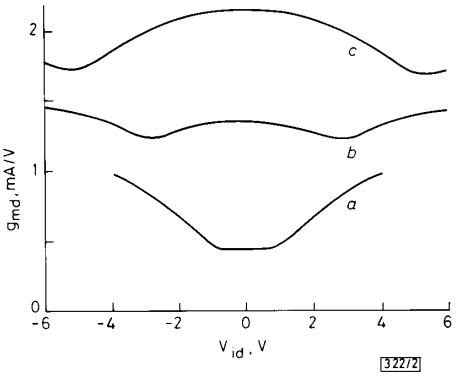

Fig. 2 *Measured transconductance against input voltage at various supply voltages*

a $V_{dd} = 4$ V *b* $V_{dd} = 6$ V *c* $V_{dd} = 8$ V

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ENTROPY CRITERION FOR PROGRESSIVE LAPLACIAN PYRAMID-BASED IMAGE TRANSMISSION

Indexing terms: Image processing, Data compression

Progressive image transmission under interactive user control is quite effective for low-bit-rate channels. The efficiency increases when significant details are transmitted first. A new criterion to extract them is presented, based on an entropy function which takes into account the features at different levels of a Laplacian pyramid. Results are compared with those given by existing algorithms.

Introduction: Progressive transmission has recently been considered in several applications such as telebrowsing, teleconferencing, remote teaching and security monitoring. In a preliminary step the most significant features of the image are transmitted; progressive refinements are obtained by further encoding the remaining finer details.

In this letter we report a new criterion based on the definition of an entropy function suitable for content-driven progressive image transmission in the framework of Laplacian pyramid coding.

Laplacian pyramid: Let $\{G_0(i, j), i, j = 0, \ldots, N-1\}$ be the original image with N a power of 2. It is defined as a Gaussian pyramid for the following set of subsampled images:

$$G_l(i, j) = \sum_{m=-2}^{2} \sum_{n=-2}^{2} w(m, n) G_{l-1}(2i + m, 2j + n) \quad (1)$$

for $i, j = 0, \ldots, (N/2^l) - 1$ and $l = 1, \ldots, L$, where l identifies the level in the pyramid, $L \leq \log_2 N$ and $G_0(i, j)$ is the basis of the pyramid.

The Laplacian pyramid is defined as

$$L_l(i, j) = G_l(i, j) - 4 \sum_{m=-2}^{2} \sum_{n=-2}^{2} w(m, n) \times G_{l+1}((i + m)/2, (j + n)/2) \quad (2)$$

for $i, j = 0, \ldots, (N/2^l) - 1$ and $l = 0, 1, \ldots, L-1$, and the sums are limited to only integer values of $(i + m)/2$ and $(j + n)/2$.

Note that $w(m, n)$, the kernel of the transformation, is assumed to be separable and symmetric.[1,2]

Encoding algorithm: This consists of transmitting the top image of the Gaussian pyramid followed by the Laplacian images at levels $L-1, L-2, \ldots, 1, 0$.

Each level of the Laplacian pyramid is divided into adjacent subimages of dimension 2×2. A 2×2 subimage at level l has one 'father' at level $l + 1$, and each element of the 2×2 subimage at level l is a father of a 2×2 subimage at level $l - 1$.

The transmission consists of a fixed number of steps. Each step is driven by a set of parameters; the parameters decrease with the level of the pyramid and with the transmission step.

The purpose is to identify those parts of the Gaussian pyramid which are more informative. For each step the pyramid is scanned in the breadth-first mode. On the 2×2 subimages an 'entropy' function is computed. If this measure is lower than the parameter which corresponds to the level of the pyramid, the current subimage is not transmitted, and the same happens for its 'sons' when they are successively encountered. If the entropy of the 2×2 subimage exceeds the parameter, the prediction errors (Laplacian 2×2 subimage) are quantised and coded with a Huffman code.

During each step, flag bits are transmitted for synchronisation and recorded to avoid unnecessary iterative operations. At the end of the breadth-first scan the values of the decision parameters are updated and the process repeated.

Entropy function: A highly critical point of the above scheme[3] is the choice of an efficient entropy function. As a 2×2 subimage result is too small to decide whether an important detail is present, we extended the entropy computation to its eight 2×2 neighbouring subimages.

Since consistent objects are expressed constantly at different spatial scales,[4] it seemed reasonable to involve at least two adjacent levels when computing the entropy function. The resulting weighted and normalised function is

$$H[S_l(i, j)] = 1/4\, H_2[S_l(i, j)] + 1/32 \sum_{\substack{m, n=-1 \\ m+n \neq 0}}^{1} H_2[S_l(i + 2m, j + 2n)] + 1/8 \sum_{m, n=0}^{1} H_2[S_{l-1}(2i + 2m, 2j + 2n)] \quad (3)$$

where

$$S_l(i, j) = \{L_l(i + ki, j + kj), ki, kj = 0, 1\} \quad \text{for } 0 \leq i \quad j < N/2^l \quad (4)$$