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Linear Current-Mode Active Pixel Sensor

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Keywords

CMOS analog integrated circuits, image sensors

Disciplines

Electrical and Computer Engineering

Linear Current-Mode Active Pixel Sensor

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I. Introduction

THE NEED FOR compact, low power devices provides an increasing impetus for sensors integrating imagers and processing circuits on a single die. Current mode active pixel sensors (APS) provide an attractive alternative to the traditional voltage mode APS for focal-plane image processing. The use of current output pixels has two main advantages over the use of their voltage-mode counterparts. First, they simplify many on-chip computation tasks; large scale computations can be performed on the focal plane using current mode computation-on-readout [1]–[3]. Second, many current mode pixels, including the proposed pixel, have fixed output voltages, eliminating the requirement to charge and discharge the column capacitances during readout, yielding the potential for significantly higher scan-out rates. Many proposed current mode active pixel sensors have suffered from high fixed pattern noise (FPN) [4] and have nonlinear transfer characteristics [5], [6]. These nonlinearities reduce the effectiveness of the typical offset-removal circuits used to improve FPN figures [7]. Other current mode pixels have had inverted light-to-output current relationships (producing the maximum output current at minimum light) [6]. The referenced current mode imagers have FPN figures between about 1% [6] and 4% [4]. Their nonlinear conversion characteristics make it difficult to further reduce this FPN using offset correction. First-order FPN cancellation techniques assume linearity; increasing pixel linearity increases the efficacy of those techniques. Ref. [8] proposes a technique to lower the power consumption of the technique proposed in [6], thereby allowing operation at higher bias current levels, which increases that pixel's linearity. Numbers for FPN were not provided. The current mode imagers in [6] and [8] require significant output currents in order to achieve linear operation; currents on the order of hundreds of microamps are required, values that are impractical when designing focal plane computation circuits to simultaneously read out multiple pixels.

Voltage mode CMOS image sensors have shown superiority in FPN figures, achieving better than 0.01% matching, or 12 bit image quality after offset correction [9]. A voltage mode technique of note is the active column sensor (ACS) [10], where the pixel's output transistor acts as half of a unity-gain amplifier. This technique retains the benefits of a standard APS design, but reduces the gain errors seen in the APS source-follower.

In this paper, we describe a current-mode imager with inherently low fixed-pattern noise. 10×10 μm^2 pixels were implemented in standard 3.3 V 0.35 μm and 1.8 V 0.18 μm CMOS processes. The pixel described in this paper has an uncorrected FPN of 0.7% without and 1.4% with column-parallel readout circuits (0.35 μm process) and 0.4% after offset correction (0.18 μm process).

The 0.35 μm process implementation included two 128×128 pixel image sensors, with 10×10 μm^2 pixels, that were used as part of a focal-plane image processing circuit. The description of the imager's application can be found elsewhere [1]; this paper describes the analysis of the imagers themselves. The 0.18 μm process implementation included a single 256×256 array of 10×10 μm^2 pixels. The authors have implemented the proposed pixel in two additional processes: 0.5 μm 5 V CMOS [11] and 0.18 μm 3-D integrated silicon-on-insulator [12].

In Section II of this paper, we describe the proposed pixel's design, operation, and light-to-output current transfer function. In Section III, we describe the generalized readout scheme for the pixel, as well as the readout scheme used in the 0.18 μm process imager. An analysis of temporal and fixed pattern noise is presented in Section IV. Results are given in Section V.

II. The Pixel

A. Pixel Operation

The pixel, shown in Fig. 1, along with its readout architecture, is operated as follows. Switch M1 resets the pixel's integrating node $V_{\rm pix}$ to a fixed voltage $V_{\rm reset}$. After the $\overline{\rm reset}$ signal is raised, turning M1 off, the photocurrent is integrated for a fixed period, producing a voltage directly proportional to the incident light intensity. $V_{\rm reset}$ is set so that it is slightly more than one P-threshold $|V_{tP}|$ below the positive supply V_{dd}

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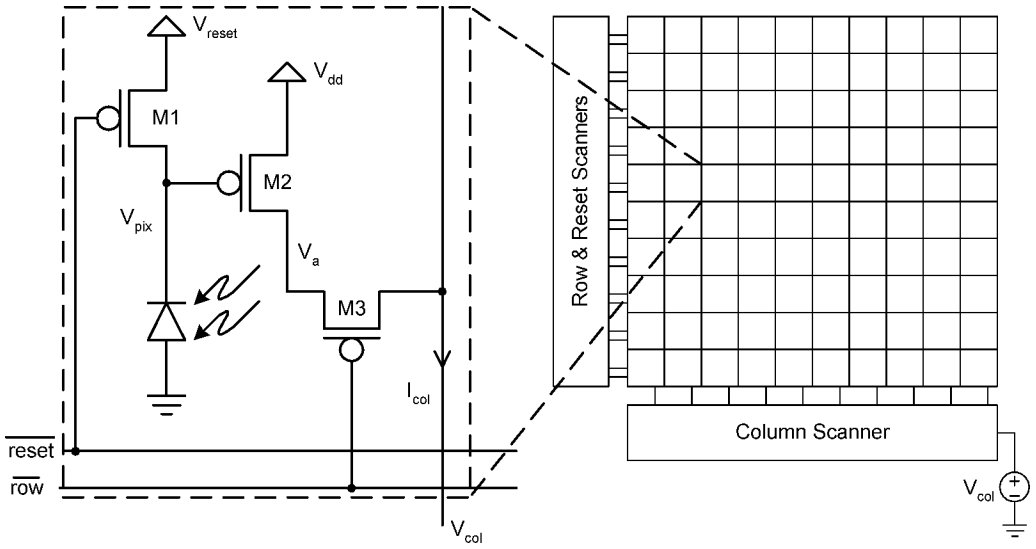

Fig. 1. Active pixel sensor and generalized imager schematic. Voltage source $V_{\rm col}$ is external to the pixel. All bulk terminals tied to V_{dd}.

(1) to ensure that the readout transistor M2 is always above threshold:

$$V_{\rm reset} < V_{dd} - |V_{tP}|\,. \tag{1}$$

The integrated voltage $V_{\rm pix}$ is converted to an output column current $I_{\rm col}$ by transistor M2, acting as a transconductance amplifier, as shown in (2). Under the assumption that $V_{\rm col}$ is constant and equal to V_a (4), the transconductance $G_{\rm pix}$, given by (5), is approximately linear. $G_{\rm pix}$ can be controlled by varying $V_{\rm col}$. An image sensor incorporating this pixel could vary $G_{\rm pix}$ to increase readout speed, lower power consumption, or to implement a scaling term in a spatial or temporal filter.

$$I_{\rm col} = \beta_2 \left[(V_{dd} - V_{\rm pix} - |V_{tP}|)\, V_{sd2} - \frac{V_{sd2}^2}{2} \right] \tag{2}$$

$$\beta_2 = \frac{\mu_{\rm eff2} C_{OX} W_2}{L_2} \tag{3}$$

$$V_a = V_{\rm col} + V_{sd3} \approx V_{\rm col} \tag{4}$$

$$G_{\rm pix} = \frac{\partial I_{\rm col}}{\partial V_{\rm pix}} \approx -\beta_2 \,(V_{dd} - V_{\rm col})\,. \tag{5}$$

The conversion gain from photo-generated electrons e^- to $I_{\rm col}$ is given by

$$\frac{\Delta I_{\rm col}}{e^-} \approx \beta_2 \frac{q}{C_{\rm pix}} \,(V_{dd} - V_{\rm col}) \tag{6}$$

where $C_{\rm pix}$ is the capacitance at the integrating node.

Switch M3 connects the pixel to the output bus, typically a column or row line of the image. Ideally, M3 has zero on-resistance $r_{\rm on3}$, meaning that the voltage drop across M3 ($V_a - V_{\rm col}$) is 0 V. This approximation, given by (4), becomes less valid at low supply voltages, owing to lower gate source voltages. The finite on resistance of M3 produces nonlinear effects that increase as the supply voltage is reduced. These effects can be ignored in a first-order analysis of the pixel's behavior, but provide a limit to the pixel's scalability. The analytical solution for the complete pixel transfer characteristic, including the effects of M3 on resistance, is provided in the Appendix. If the entire imager shares a single readout circuit, as shown in Fig. 1, the series resistance of any switches in the column scanner/decoder can be included in M3's series resistance.

The pixel's integration range at $V_{\rm pix}$ is from $V_{\rm reset}$ down to 0 V. Unlike a standard three–transistor (3T) voltage mode APS, the proposed pixel's lower integration limit is set by the photodiode, not the readout structure. The proposed pixel is capable of integrating to slightly below 0 V, to the point where the photodiode's forward current equals the photocurrent. The full integration range of the pixel is one pMOS threshold less than the power supply. For the 0.35 μm process used, $V_{dd} = 3.3$ V, $V_{tP} = -0.78$ V, and the integration range was 2.5 V, while for the 0.18 μm process used, $V_{dd} = 1.8$ V, $V_{tP} = -0.45$ V, and the integration range was 1.2 V. This compares favorably to a 3T APS, which loses two nMOS thresholds (including substantial body effect) and an nMOS $V_{\rm DSsat}$, which would provide an integration range of less than 2 V and 0.7 V for the same processes, respectively. A 3T APS employing a pMOS reset transistor, as seen in many modern APS pixels, loses an nMOS threshold and an nMOS $V_{\rm DSsat}$, providing a similar integration range to the proposed pixel.

B. Wells

The use of pMOS devices requires the use of an in-pixel n-well. Since the photodiode itself cannot reside in the n-well, the pixel's minimum size is constrained by n-well spacing requirements. The test imagers used 10×10 μm^2 pixels with 26% and 66% fill factors in standard 0.35 μm and 0.18 μm processes, respectively. The 0.18 μm process pixel's 10×10 μm^2 size was dictated by external system requirements unrelated to this work. The additional area was used solely for the photodiode; readout transistors were scaled with the process feature size. In a standard submicron process [13], the minimum pitch for a regular pixel layout is 32λ, where λ is approximately 1/2 the minimum gate length ($\lambda = 0.2$ μm, 0.1 μm and $32\lambda = 6.4$ μm, 3.2 μm for the 0.35 μm and 0.18 μm processes used, respectively).

Modifying the pixel to use nMOS devices would not eliminate the well requirement, as the photodiode would have to reside in an n-well (p+ diffusion to n-well). Well spacing requirements could be avoided by using an n+ to p-substrate diode with

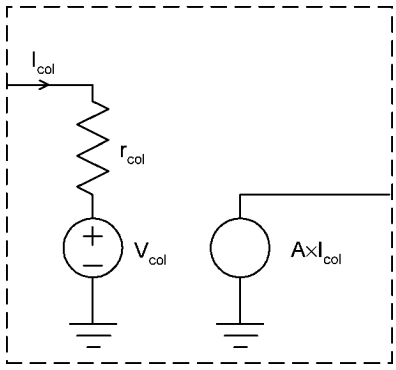

Fig. 2. Generalized image readout circuit. Note that A is in units of output unit per amp. $r_{\rm col}$ is the input impedance of the device.

nMOS devices. The pixel's layout would then be nearly identical to a standard 3T APS, as the reset could be to V_{dd} (no separate $V_{\rm reset}$ would be required). While this would significantly increase the pixel's fill factor or decrease its size, such a design would have several undesirable properties, including having the largest output current (highest noise) at the lowest light level, and reducing the available integration range by one threshold voltage.

III. Image Readout

A. Generalized Readout Circuit

Image readout from the pixel is accomplished using any circuit that applies a voltage $V_{\rm col}$ to the drain of M3 while providing a way to measure the pixel's output current (called $I_{\rm col}$, assuming a column parallel readout scan). The input impedance $r_{\rm col}$, ideally zero, should be less than the series resistance of the pixel's select transistors. The readout circuit's gain A is in units of readout unit per amp, where the readout unit would typically be amps or volts (meaning the circuit would be called a current conveyor or transimpedance amplifier, respectively). The general form of this readout circuit is shown in Fig. 2.

Linear pixel operation is achieved when $V_{\rm col}$ is close to, but below, V_{dd}, keeping M2 in the triode (linear) region of operation. The pixel operates with a nonlinear (quadratic) transfer characteristic when $V_{\rm col}$ is brought further away from V_{dd}, such that M2 is in the saturation region. The use of the pixel in this manner will not be discussed in this work.

It should be noted that many readout structures, such as the current conveyor discussed below, will require some steady-state input bias current to guarantee reliable operation (i.e., speed, stability). This can be achieved either by adding a bias current source, or by simply lowering $V_{\rm reset}$ so as to provide a sufficient current when $V_{\rm pix} = V_{\rm reset}$. This has the benefit of slightly increasing pixel linearity, as the pixel's behavior is least linear when M2 is just above threshold.

No double-sampling/offset correction of any kind was performed on the image outputs in the 0.35 μm design; the 0.18 μm design used a current memory unit to implement double-sampling offset removal. Methods of performing offset correction on currents are discussed in [5], and function much like voltage-domain offset correction.

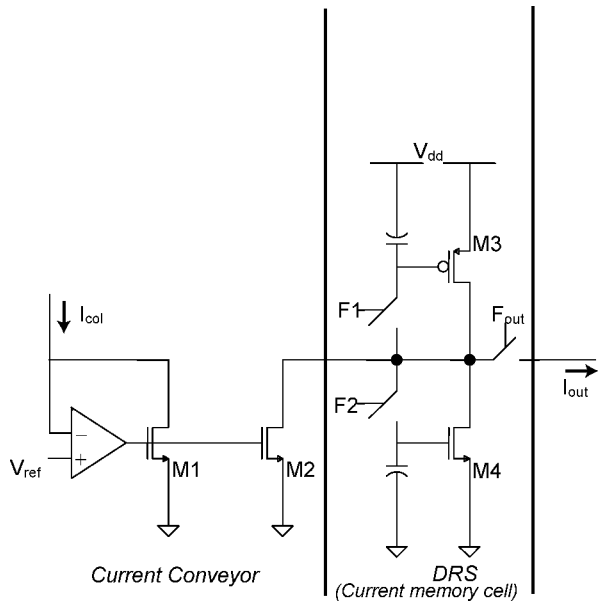

Fig. 3. Readout circuit used in 0.18 μm process. Current conveyor and delta-reset sampling.

B. Current Conveyor Readout

The proposed pixel implemented in the 0.35 μm process used column-parallel first-generation current conveyors (CCI+) to fix the pixel output voltage and provide a copy of the pixel output current. The input impedance of these circuits was simulated to be 100–200 Ω in the region of expected pixel output currents. This was significantly less than the 2.4 kΩ on-resistance of the pixel row select switch. The input impedance of the CCI+ "virtual ground" was therefore neglected; the virtual ground was considered perfect. The circuits used are described in [11]; however, the proposed imager's implementation was column parallel (one per column instead of one per chip) and did not include a double-sampling circuit.

The readout scheme for the 0.18 μm design is presented in Fig. 3. The readout scheme is composed of two parts. The first part employs a second-generation current conveyor circuit (CCII+) [12]. This circuit is composed of a two-stage operational amplifier with a Miller compensation capacitor operated in a negative feedback mode via transistor M1. The amplifier had a gain bandwidth product of 50 MHz and a DC gain A_0 of 80 dB. The negative feedback configuration pinned the inverting input terminal of the opamp to $V_{\rm col} \approx V_{\rm ref}$. The low-frequency input resistance of the current conveyor is given by

$$r_{\rm col} = \frac{1}{g_{m1} A_0} \tag{7}$$

in which g_{m1} is the transconductance of M1.

The minimum output current from the pixel in the 0.18 μm process was 1 μA during the reset interval and the measured input resistance of the current conveyor was 10 Ω. The input capacitance of the current conveyor consists of 256 drain capacitances (from M3 in the pixel) plus the line capacitance of the 2.5 mm long metal bus. With a total input capacitance of 300 fF, the time constant of the current conveyor circuit is 1 ns, giving

an operational bandwidth of 0.3 Grad/s or 53 MHz. The variations of the input terminal of the current conveyor over 10 μA input range have been measured to be less than 1 μV. The high readout bandwidth is desirable when analog processing units are implemented as part of the readout circuitry.

The second part of the 0.18 μm process readout circuitry is the delta-reset sampling (DRS) offset suppression circuitry, which is a modified version of the current memory cell described in [15]. A single offset suppression circuit is used for the entire image array, alleviating column FPN. The DRS cell is composed of coarse and fine sub-memory cells. During the memorization stage of the coarse memory cell, charge injection errors dependent on the input current level are introduced. These signal-dependent charge injections are memorized in the fine memory cell and subtracted from the coarse memory cell.

The DRS of the pixel is performed in two steps. Initially, the output current, after integration, is memorized in the memory cell. The pixel is then reset and the reset-phase output current is subtracted from the previously memorized uncorrected output current. The final current output is independent of the voltage threshold variations of the readout transistor M2 in Fig. 1.

IV. Noise

A. Pixel Temporal Noise

The pixel circuit uses a pMOS transistor to provide hard reset to a fixed voltage $V_{\rm reset}$. This has the advantage of eliminating image lag and guaranteeing reset to a precise voltage, but at the cost of increased reset noise versus a conventional soft reset. Pixels with hard reset exhibit kT/C noise, given by (8), whereas pixels with soft reset have reset noise as low as $kT/2C$ [16]. It should be noted that the DRS circuit used in the 0.18 μm process imager doubles the effect of kT/C noise, since noise power from two uncorrelated reset phases is added.

$$\overline{V_{n,\rm reset}^2} = \frac{kT}{C_{\rm pix}}. \tag{8}$$

During integration, the dark current $i_{\rm dark}$ and the photo-generated current $i_{\rm ph}$ contribute shot noise:

$$\overline{V_{n,\rm shot}^2} = \frac{q\left(i_{\rm ph}+i_{\rm dark}\right)}{C_{\rm pix}^2} t_{\rm int}. \tag{9}$$

Note that this assumes that the dark current, coming from the photodiode and the reset device, flows in the same direction as the $i_{\rm ph}$. The leakage at the drain of the reset device and the reset device's subthreshold off-current each contribute dark current opposite in direction to the photocurrent, thus increasing the magnitude of pixel shot noise. The use of a reset switch that is two threshold voltages away from "on" ensures that a minimum of subthreshold current flows through the reset device in the 0.35 μm process pixel.

The case where the all dark current components flow in the same direction as the photocurrent (or if there is no dark current), a "best case" situation, provides a lower limit (10) for the total shot noise power for a given integrated voltage:

$$\overline{V_{n,\rm shot}^2} \geq \frac{q\left(V_{\rm reset}-V_{\rm pix}\right)}{C_{\rm pix}}. \tag{10}$$

TABLE I
Input-Referred Random and Fixed Pattern Noise

Technology	0.35μm	0.18μm
Pixel Capacitance, C_{pix}	41 fF	80 fF
Saturation Charge	615,000 e^-	600,000 e^-
Dark Current	4fA (100mV/sec)	-80fA (-1V/sec)
Reset Noise	320 μV *	230μV #
Shot noise @ full scale †	3.1 mV *	1.6mV #
Readout noise†	4.8 mV *	8.0 mV #
Total random noise (ignoring 1/*f*) †	5.7 mV *	8.2 mV #
Dynamic Range	64dB†	53dB †
M3 on-resistance r_{ds3}	2.4kΩ	~10kΩ
Output capacitance C_{col}	900fF	300fF
Fixed-Pattern-Noise* (per-pixel, full-scale)	0.7% (17mV) (no correction)	0.4%, no correction: 1.6%
Fixed-Pattern-Noise * (with readout mismatch, full-scale)	1.4% (34mV)	N/A

*: at V_{col} = 2.9V, V_{reset} = 2.4V
#: at V_{col} = 1.7V, V_{reset} = 1.2V
†: Calculated

For a temperature of 300 K, the power in the photon and dark current shot noise is greater than the reset noise power when the integrated voltage is above 26 mV (11), or about 1% and 2% of full-scale integration voltage in the 0.35 μm and 0.18 μm process pixels, respectively. This demonstrates that the reset noise is of importance only at low integration (i.e., brightness) levels. Reset noise provides a lower limit on the resolvable pixel integration voltage (most important at short integration times), while dark current provides a lower bound on the resolvable light level (most important at long integration times).

$$\forall V_{\rm pix} > \frac{kT}{q} \rightarrow \overline{V_{n,\rm shot}^2} > \overline{V_{n,\rm reset}^2}. \tag{11}$$

The minimum detectable signal is determined by the power of the reset kT/C noise and dark current shot noise. The pixel's readout thermal noise is proportional to signal power and does not limit the dynamic range. Dark current shot noise power is proportional to integration time, as is the signal power; therefore the dynamic range (DR) remains constant regardless of integration time, as long as the reset noise dominates the dark current shot noise. This happens when the integration time $t_{\rm int}$ is less than

$$t_{\rm int} < \frac{C_{\rm pix}kT}{qi_{\rm dark}}. \tag{12}$$

The dark current was measured by resetting the pixels once and then reading multiple images in zero light. This measurement was repeated multiple times and the results were averaged. Calculated and measured noise values are summarized in Table I.

B. Readout Temporal Noise

The small-signal circuit in Fig. 4 was used to compute the readout noise from thermal sources. Readout noise was referred

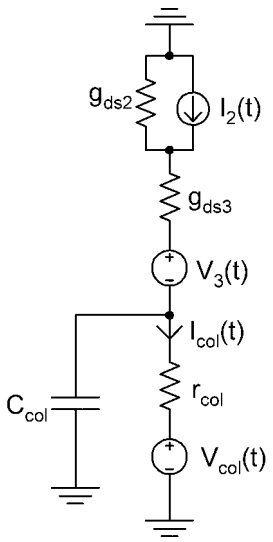

Fig. 4. Readout temporal noise sources, including generalized readout circuit. Noise is measured at $I_{\rm col}$. $C_{\rm col}$ is the column (pixel output) capacitance.

to the circuit's output $I_{\rm col}$. The output (typically column or row) -3 dB bandwidth is given by (13). This bandwidth was sufficient in both imagers to assume steady-state conditions for readout noise analysis.

$$f_{-3\rm dB} \approx \frac{1}{2\pi r_{\rm col} C_{\rm col}}. \tag{13}$$

The output ($I_{\rm col}$) referred noise due to transconductor M2 and row select switch M3 are given by

$$\overline{I^2_{n,\rm M2,col}} = \frac{2kT}{C_{\rm col}} \frac{g_{ds2} g^2_{ds3}}{r_{\rm col}\left(g_{ds2}+g_{ds3}\right)\left(g_{ds2}+g_{ds3}+g_{ds2}g_{ds3}r_{\rm col}\right)} \tag{14}$$

$$\overline{I^2_{n,\rm M3,col}} = \frac{2kT}{C_{\rm col}} \frac{g^2_{ds2} g_{ds3}}{r_{\rm col}\left(g_{ds2}+g_{ds3}\right)\left(g_{ds2}+g_{ds3}+g_{ds2}g_{ds3}r_{\rm col}\right)}. \tag{15}$$

By definition, the total power of the output-referred thermal noise due to the readout circuit (excluding M2 and M3) is not band-limited; the noise power is limited only by temperature. The circuit's input impedance is inherently low (on the order of tens to hundreds of ohms), and a wide variety of possible circuit architectures exist. The contribution of the output noise source itself is therefore ignored.

The readout temporal noise amplitude produced in M2 (16) is proportional to the square-root of its drain-source conductance, which is proportional to the integrated pixel voltage (17).

$$\overline{I^2_{n,M2}(t)} = \gamma 4kT\Delta f \; g_{ds2}|_{V_a=V_{dd}} \qquad 1>\gamma>\frac{2}{3} \tag{16}$$

$$g_{ds2} = \beta_2\left[\left(V_{dd}-V_{\rm pix}-|V_{tP}|\right)-2\left(V_{dd}-V_a\right)\right]. \tag{17}$$

The maximum output temporal noise occurs at a full-scale integration voltage of 2.4 V and 1.2 V ($V_{\rm pix}=0$ V) in the 0.35 μm and 0.18 μm process pixels, respectively. The calculated output temporal noise for the 0.35 μm process pixel at full scale (with $V_{\rm col}=2.9$ V) is 56 $\rm nA_{rms}$. Referred back to the pixel, this is approximately 5.7 $\rm mV_{rms}$, or 1500 $\rm e^-$. Since the output current is linearly proportional to the integrated voltage, the output noise power is roughly proportional to the light level. At 10% full-scale, the input-referred output noise is about 2.2 $\rm mV_{rms}$. The 0.18 μm process pixel was calculated to have 8.2 $\rm mV_{rms}$ of total (excluding $1/\rm f$) input-referred temporal noise at full-scale (with $V_{\rm col}=1.7$ V). The resulting calculated full-scale signal-to-noise ratios (SNR) are 42 dB and 39 dB for the 0.35 μm and 0.18 μm process imagers, respectively.

Lowering the pixel output voltage, and thus increasing the pixel transconductance, decreases the input-referred readout noise and increases the SNR. For a given pixel voltage, the rms readout noise grows only slightly with increasing transconductance, but the noise level, when referred back to the pixel, is divided by a larger number. $V_{\rm col}=2.8$ V was calculated to have 4 mV of input referred noise at full-scale. This comes at the price of increased power consumption and a smaller linear integration range.

C. Fixed Pattern Noise

The pixel, operating without FPN, is considered to follow the model:

$$I_{\rm col,ideal} = G_{\rm ideal} V_{\rm pix} + I_{\rm DC,ideal}. \tag{18}$$

where the integrated light level $V_{\rm pix}$ is converted to a current $I_{\rm col,ideal}$ by the ideal linear transconductance $G_{\rm ideal}$. An offset current $I_{\rm DC,ideal}$, uniform across the pixel array and independent of light level, is considered part of the ideal transfer characteristic.This analysis considers pixel FPN to consist of additive offset ($I_{\rm DC,fpn}$) and multiplicative gain ($G_{\rm fpn}$) errors, both normalized:

$$I_{\rm col} = G_{\rm ideal} V_{\rm pix}\left(1+G_{\rm fpn}\right) + I_{\rm DC,ideal}\left(1+I_{\rm DC,fpn}\right). \tag{19}$$

The proposed APS utilizes a hard reset to a fixed voltage; therefore reset transistor threshold mismatch does not contribute significantly to pixel FPN. However, readout transconductor M2 threshold mismatch contributes directly to the pixel output current mismatch. This mismatch is part of the additive $I_{\rm DC,fpn}$ term, meaning that $V_{\rm pix}$ does not appear in (20), and can be removed using double-sampling techniques.

$$\frac{\partial I_{\rm col}}{\partial V_{tp2}} = \beta_2\left(V_{dd}-V_{\rm col}\right). \tag{20}$$

Unlike the standard 3T APS, the proposed pixel's transfer function includes a significant nonunity gain term (5) that is set by the transistors in the pixel. Mismatch in this gain term contributes directly to observed fixed pattern noise at nonzero output. This gain term is proportional to β_2, which includes the size ratio of M2 (3). This multiplicative mismatch is not removed by standard mismatch-correction (offset-removal) circuits; a minimum 2-point correction is required to remove this error. The use of a separate reset voltage enables such a 2-point correction by allowing all pixels' $V_{\rm pix}$ to be set to the same fixed voltage, thereby extracting slope information. This technique would also permit *in situ* acquisition of the data necessary for readout gain correction without the need for uniform illumination or complex spatiotemporal processing schemes [18], and

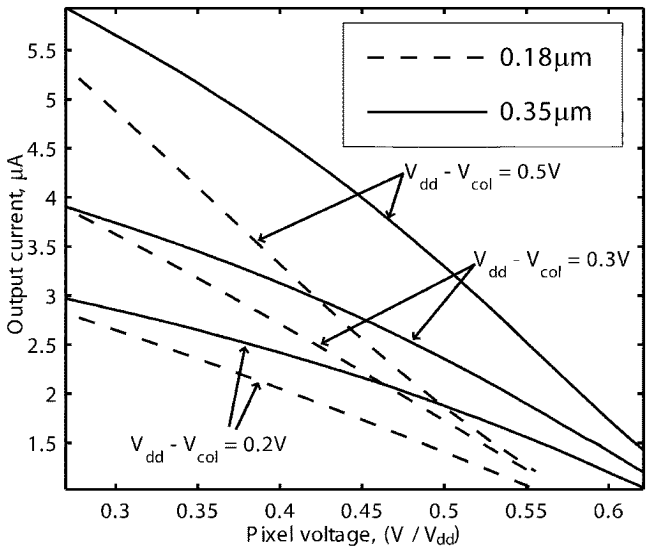

Fig. 5. Pixel transfer characteristics: integrated voltage to output current. $V_{dd} =$ 3.3 V for 0.35 μm pixel, $V_{dd} =$ 1.8 V for 0.18 μm pixel.

was used below to characterize the pixels' transfer function, but was not implemented for image readout.

$$\frac{\partial I_{\rm col}}{\partial \beta_2} = V_{sd2}\left(V_{dd} - V_{tp} - V_{\rm pix}\right) - \frac{V_{sd2}^2}{2} \propto -V_{\rm pix}V_{sd2}. \quad (21)$$

Due to the sensitivity to transistor characteristics described by (20) and (21), the test imagers' readout transconductors M2 were made significantly larger than minimum size: a square device of roughly triple the minimum width in the 0.35 μm process and a rectangular device of $\mathrm{W/L} = 0.3$ for the 0.18 μm process.

The 0.35 μm process test imager contained a column-parallel readout structure, which introduced significant inter-column mismatch. To remove the effects of this mismatch, which would not be present if a global readout circuit were used, FPN calculations were performed along the column. The individual column FPN values were then combined (root-mean-square) to compute the FPN. This method makes the assumption that the pixel itself does not have any inherent column-to-column bias in its mismatch; the mismatch is assumed to be random over the imager [19]. The measured pixel FPN was 0.7% at full scale. The FPN, when including the effects of the column circuit mismatch, was 1.4% at full scale.

The FPN in the gain term was also evaluated by forcing each pixel to a range of reset voltages and reading the output current. The relationship between $V_{\rm pix}$ and $I_{\rm col}$ for various output voltages $V_{\rm col}$ is plotted in Fig. 5. Note that direct manipulation of $V_{\rm pix}$ takes into account neither variations in the pixels' quantum efficiency nor the variations in pixel capacitance. Neither of these two considerations is unique to this pixel, which uses a standard n+ diffusion to p-substrate diode.

Linear curve fits were performed on measured transfer curves between $V_{\rm pix}$ and $I_{\rm col}$ to acquire $G_{\rm fpn}$ and $I_{\rm DC,fpn}$ (multiplicative and offset FPN values). The deviation of each pixel's first-order fit from the global first-order fit was obtained. The distribution of these deviations ($1+I_{\rm DC,fpn}$ and $1+G_{\rm fpn}$) is shown in Fig. 6(a) and (b) for the 0.35 μm and 0.18 μm process imagers, respectively. It can be seen that the pixel mismatch sees similar amounts of offset FPN and gain FPN. Note that these data, taken at $V_{\rm pix}$ values from 0 to 50% saturation, exhibit higher mismatch levels than the imager operating at full scale (down to 0 V); the use of a pMOS reset transistor did not permit directly controlling $V_{\rm pix}$ below 1.1 V and 0.5 V for the 0.35 μm and 0.18 μm process imagers, respectively.

The calculated and measured results for temporal and fixed pattern noise in the 0.35 μm and 0.18 μm process pixels are summarized in Table I.

V. Results

A. 0.35 μm Process

The 0.35 μm process pixel was implemented in a 3.3 V n-well 0.35 μm CMOS process with four metal and two polysilicon interconnect layers. The pixel was 10×10 μm^2 in size and had a 26% fill factor. The test chip included two 128×128 pixel imagers with column parallel readout and on-chip analog current-mode computation circuitry. Offset correction circuits such as correlated double-sampling (CDS) or delta-reset sampling (DRS) were not used on the chip.

The measured rms dark current was 4 fA (100 mV/s), or 4.2% of full-scale per second. The resulting dynamic range, including the effects of calculated reset noise and measured dark current shot noise, as well as readout thermal noise on the integrated dark current, is 64 dB at $t_{\rm int} = 33$ ms. The tested pixel's dynamic range is constant at 67 dB up to approximately 25 ms of integration time, at which point it begins to decrease because of dark current shot noise.

The imager's power consumption is determined primarily by the pixel output current and the readout circuit, which was not individually measurable in the test chip. By design, the image readout power consumption is proportional to output current, and therefore proportional to light intensity. The test chip used column-parallel readout circuitry to read an entire row of 128 pixels simultaneously for use in analog current-mode computation circuits. The simulated power consumption, with all 128 columns active pixels illuminated at 50% of saturation brightness, was 4 mW. Scanning one pixel requires approximately six times the pixel output current, or approximately 60 μW (assuming 50% saturation) plus the power consumption of the digital scanning circuits.

A sample image is shown in Fig. 7. The imager's characteristics are summarized in Table II.

B. 0.18 μm Process

The 0.18 μm process pixel was implemented in a 1.8 V n-well 0.18 μm CMOS process with six metal and one polysilicon interconnect layers. The pixel was 10×10 μm^2 in size and had a 66% fill factor. The test chip included a 256×256 pixel imager with global readout and offset correction circuits.

The 0.18 μm image sensor was tested for linearity, FPN, and memory unit (DRS unit) accuracy. The image sensor was composed of 256×256 photo elements, with pixel size of 10×10 μm^2 and a fill factor of 66%. The transfer characteristics of the photo pixels were measured and presented in Fig. 8. The horizontal axis presents the output current as a function

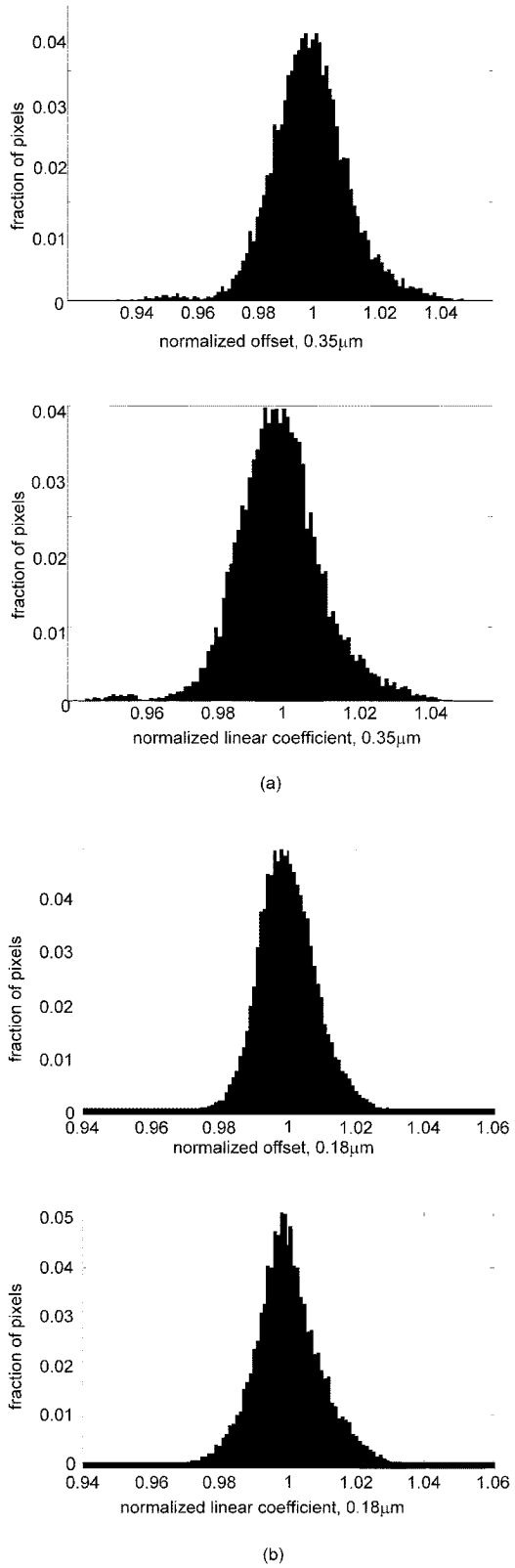

Fig. 6. (a) Offset and gain error distributions (0.35 μm process pixel). (b) Offset and gain error distributions (0.18 μm process pixel, after double-sampling).

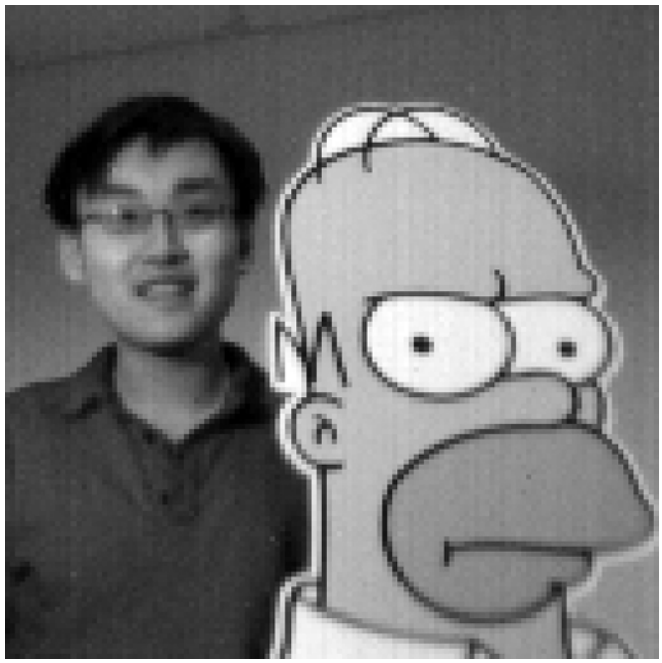

Fig. 7. Sample image. 0.35 μm process: 128 $\times$ 128 pixels. No offset correction. Note that the majority of the FPN is the form of readout column mismatch.

TABLE II
IMAGE SENSOR CHARACTERISTICS

Technology	0.35μm, 4m2p	0.18μm, 6m1p
Supply voltage	3.3V	1.8V
$\|V_{tP}\|$	~0.78V	~0.45V
Pixel array size	128 × 128	256 × 256
Pixel size	10 × 10μm^2	10 × 10μm^2
Fill factor	26%	66%
Maximum frame rate	> 30 frames/s	> 30frames/s
Total input-referred random noise	5.7 mV$_{rms}$ *†	8.2 mV$_{rms}$ #†
Fixed-pattern-noise (per-pixel)	0.7% (17mV$_{rms}$) * (no correction)	0.4% (2 mV$_{rms}$) * (after CDS)
Signal to Noise Ratio (full-scale, no 1/*f* noise)	42dB *†	39dB #†
Dynamic Range	64dB *†	53dB #† (t_{int} = 33ms)

*: at V_{col} = 2.9V, V_{reset} = 2.4V, t_{int} = 33ms.
#: at V_{col} = 1.7V, V_{reset} = 0.8V, t_{int} = 60ms.
†: Calculated, (ignoring 1/*f* noise)

of integration time. The set of curves was recorded at different light intensities from 0 μW/cm^2 to 36 μW/cm^2. The power supply voltage (V_{dd}) was 1.8 V, column voltage ($V_{\rm col}$) was 1.7 V, and reset voltage ($V_{\rm reset}$) was 0.8 V. The photo pixels were held in reset mode from 0 s to 20 ms, at which point the reset transistor was turned off, allowing the pixel to begin integrating the photocurrent for an integration time $t_{\rm int} = 60$ ms. Given the bias voltages ($V_{\rm reset}$ and $V_{\rm col}$), the pixel output current remained linear within 99% for light intensities up to 9 μW/cm^2. For this light intensity, the measured FPN after DRS was 0.4%.

For the higher light intensity of 36 μW/cm^2, the linearity of the output current was reduced to 88%. This nonlinearity is due to several factors. First, the pixel integration voltage was below 0 V, near its lowest possible value. Additionally, the high output current creates a large voltage drop across the switch transistor M3; the approximation given by (4) becomes less valid. Hence,

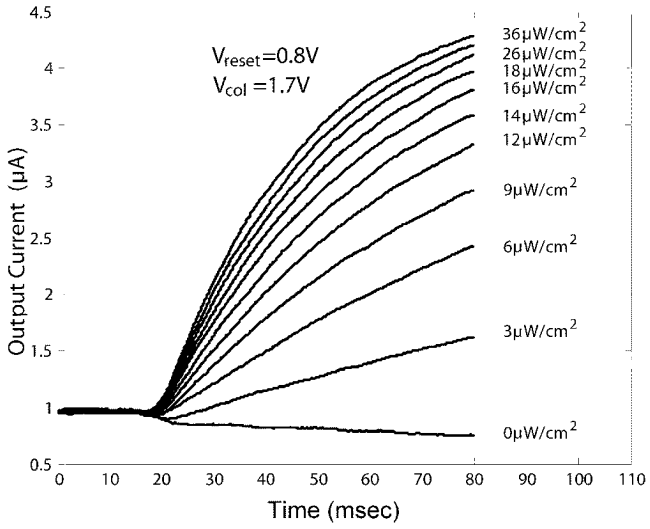

Fig. 8. Output current as a function of time and light intensity for 0.18 μm process imager (reset at 20 ms).

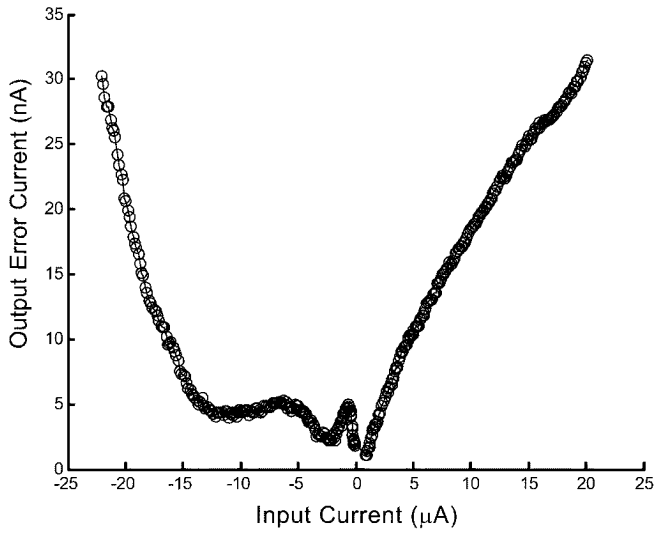

Fig. 9. A memory unit is used to implement a DRS unit. The output error current is measured as a function of the input current.

readout transistor M2 sees substantially different drain voltages, and thus transconductances, during the reset and readout phases. This voltage difference causes nonlinear current output, which reduces the effectiveness of the DRS circuit.

The third contribution to the nonlinear output is the mobility degradation due to the high V_{sg} of transistor M2, which is more pronounced in technologies with smaller feature sizes. The FPN figure for this light level increases to 0.85%. For high intensities, the image sensor can be biased with a reset voltage closer to V_{dd}, or a higher column voltage, which will decrease the output current. Hence, the pixel's linearity can be increased, which in turn will decrease the FPN, at the cost of decreased SNR.

A large dark current $i_{\rm dark}$ can also be observed in Fig. 8; the output current under zero illumination decreases with time. This indicates that the dark current, coming from the reset transistor, flows in the reverse direction of the photocurrent. An average of $i_{\rm dark} = -80$ fA (1 V/sec) dark current was measured, with a standard deviation of 30 fA. In addition, less than 0.5% of the total number of pixels exhibited very large dark current ($|i_{\rm dark}| > 800$ fA). These "dead" pixels were excluded from the FPN measurement. The large negative dark current, from transistor off-current and gate leakage, was attributed to the use of a standard 0.18 μm CMOS process.

Comparing Figs. 5–8, it can be seen that the 0.18 μm process pixel is least linear at high levels of integration and high output currents. The effects for high light levels reflect pixel saturation, which are not unique to this imager. The behavior at lower light levels (12 μW/cm^2 and lower) is far more linear, and reflects the transfer characteristics shown in Fig. 5.

Offset correction was performed using a current memory unit. The memory unit was tested for various input currents at a sampling rate of 10 MHz; the results are presented in Fig. 9. For a current range of ± 20 μA, the maximum measured error current was less than 20 nA. This indicates that the memory unit can replicate/memorize a current over a ± 20 μA range with 10 bit accuracy at a 10 MHz sampling rate. The bidirectional input current can be memorized in the memory cell due to a constant bias current flowing through the memory transistors. As long as the input current is smaller than the bias current, the memory cell can memorize the current. In the measurements shown in Fig. 9, the bias current was set to 22 μA, allowing for successful memorization of an input current of $\sim$ 21.5 μA. The bidirectional current memory cell can be easily used as a part of a processing unit, where the input current can be scaled with both positive and negative coefficients. The offset currents can be cancelled out by memorizing a scaled version of an input current and subtracting it from a scaled version of a reference current.

The total power consumption of the 0.18 μm process imager was simulated to be 0.6 mW, including the double-sampling unit. The tested chip included three double sampling units, which, together with the 256×256 pixel imager, consumed 2.5 mW, excluding digital scanning circuits.

C. Comparison

The 0.35 μm and 0.18 μm process imagers exhibited linear transfer characteristics shown in Fig. 5. Both were within 6% of linear (worst case) for integrated values up to 50% of full-scale integration. Both imagers' linearity worsened at the extremes of integration (Figs. 5 and 8); by lowering the reset voltage, linearity could be increased at the cost of reduced dynamic range. The 0.18 μm process imager exhibited worse uncorrected FPN than the 0.35 μm process imager (1.4% versus 0.7%), but was equipped with double-sampling circuits that reduced FPN to 0.4%.

Using standard CMOS rules, directly scaling the 0.35 μm process pixel's layout to the 0.18 μm process would result in a 5×5 μm^2 pixel size. This would quadruple the imager spatial resolution, but the reduced well capacity would decrease the dynamic range and SNR.

The high subthreshold leakage in the 0.18 μm process pixel's reset transistor created a large dark current, which was about 20 times larger than $i_{\rm dark}$ in the 0.35 μm process pixel. This issue could be addressed in future work through the use of a 3.3 V thick-oxide nMOS reset transistor [20].

$$I_{\mathrm{col}} = \frac{\beta_2\beta_3}{2\left(\beta_2+\beta_3\right)^2}\cdot\left(\begin{array}{l}\beta_3\left(V_{dd}^2 - V_{\mathrm{out}}^2 + 2V_{\mathrm{col}}V_{tP} + 2V_{\mathrm{pix}}V_{tP} - 2V_{dd}\left(V_{\mathrm{pix}}+V_{tP}\right)\right) \\ \quad +\beta_2\left(\begin{array}{r} V_{dd}^2 - V_{\mathrm{col}}^2 + 2V_{\mathrm{col}}V_{tP} + 2V_{\mathrm{pix}}\left(V_{\mathrm{pix}}+V_{tP}\right) \\ -2V_{dd}\left(V_{\mathrm{pix}}+V_{tP}\right)\end{array}\right) \\ +2V_{\mathrm{pix}}\sqrt{\left(\begin{array}{l}\beta_3^2\left(V_{\mathrm{col}}-V_{tP}\right)^2 + \beta_2^2\left(V_{\mathrm{pix}}-V_{dd}+V_{tP}\right)^2 \\ +\beta_2\beta_3\left(\begin{array}{l} V_{\mathrm{col}}^2 + V_{dd}^2 \\ -2\left(\begin{array}{c} V_{\mathrm{col}}V_{tP} + V_{dd}\left(V_{\mathrm{pix}}+V_{tP}\right) \\ -V_{tP}\left(V_{\mathrm{pix}}+V_{tP}\right)\end{array}\right)\end{array}\right)\end{array}\right)}\end{array}\right)$$

VI. Conclusion

A current mode active pixel sensor with low fixed pattern noise, implemented in both 0.35 μm and 0.18 μm standard CMOS processes, has been presented. The image sensors' characteristics are summarized in Table II. The underlying pixels in the 0.35 μm process imager exhibited only 0.7% FPN, a result that was achieved without on-chip correction of any kind. The 0.18 μm process imager attained 0.4% FPN after delta-reset sampling. The imagers' light-to-output current transfer characteristics were within 6% of linear. The current output pixels are suitable for use in focal plane computation-on-readout image processing tasks.

Appendix

The analytical solution for the pixel transfer characteristic (from integrated voltage V_{pix} to output current I_{col}) is shown in the equation at the top of the page.

Using linear triode transistor models, ignoring the quadratic drain–source dependence, yields the following simplification, which is valid for small drain–source voltages:

$$I_{\mathrm{col}} = \frac{\beta_2}{2}\left(V_{\mathrm{pix}} - V_{dd} + V_{tP}\right) \times\left(\frac{\left(V_{\mathrm{col}} - 2V_{dd} + V_{tP}\right) + \frac{\beta_2}{\beta_3}\left(V_{\mathrm{pix}} - V_{dd} + V_{tP}\right) + \sqrt{\left(\begin{array}{l}\left(\frac{\beta_2}{\beta_3}\right)^2\left(V_{\mathrm{pix}} - V_{dd} + V_{tP}\right)^2 \\ +2\frac{\beta_2}{\beta_3}\left(V_{\mathrm{pix}} - V_{dd} + V_{tP}\right)\left(V_{\mathrm{col}} - 2V_{dd} + V_{tP}\right) \\ +\left(V_{\mathrm{col}} - V_{tP}\right)^2\end{array}\right)}}{}\right).$$

References

[1] R. M. Philipp and R. Etienne-Cummings, "A 128x128 33mW 30frames/s single-chip stereo imager," in *2006 IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, Feb. 2006, pp. 2050–2059.

[2] R. Etienne-Cummings, S. Mehta, R. Philipp, and V. Gruev, "Neuromorphic vision systems for mobile applications," in *Proc. 2006 IEEE Custom Integrated Circuits Conf. (CICC)*, San Jose, CA, Sep. 2006, pp. 531–534.

[3] V. Gruev, J. Van der Spiegel, and N. Engheta, "Image sensor with focal plane extraction of polarimetric information," in *Proc. IEEE ISCAS*, May 2006, p. 4.

[4] R. M. Philipp and R. Etienne-Cummings, "Single-chip stereo imager," *Analog Integrat. Circuits Signal Process.*, vol. 39, pp. 237–250, Jun. 2004.

[5] J. Nakamura, B. Pain, T. Nomoto, T. Nakamura, and E. R. Fossum, "On-focal-plane signal processing for current-mode active pixel sensors," *IEEE Trans. Electron Devices*, vol. 44, no. 10, pp. 1747–1758, Oct. 1997.

[6] L. G. McIlrath, V. S. Clark, P. K. Duane, R. D. McGrath, and W. D. Waskurak, "Design and analysis of a 512x768 current-mediated active pixel array image sensor," *IEEE Trans. Electron Devices*, vol. 44, no. 10, pp. 1706–1715, Oct. 1997.

[7] A. El Gamal, "High dynamic range image sensors," presented at the IEEE Int. Solid-State Circuits Conf.–Tutorial, San Francisco, CA, 2002.

[8] F. Boussaid, A. Bermak, and A. Bouzerdoum, "An ultra-low power operating technique for mega-pixels current-mediated CMOS imagers," *IEEE Trans. Consum. Electron.*, vol. 50, no. 1, pp. 46–53, Feb. 2004.

[9] J. Yang, K. Fife, L. Brooks, C. Sodini, A. Betts, P. Mudunuru, and H. Lee, "A 3 megapixel, low-noise flexible architecture CMOS image sensor," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, 2006, pp. 496–497.

[10] T. L. Vogelsong, J. Zarnowski, M. Pace, and T. Zarnowski, "Scientific/industrial camera-on-a-chip using active column sensor CMOS imager core," in *Proc. SPIE*, May 2000, vol. 3965, pp. 102–113.

[11] V. Gruev, R. Etienne-Cummings, and T. Horiuchi, "Linear current mode imager with low fix pattern noise," in *Proc. IEEE ISCAS*, May 2004, vol. 4, pp. 860–863.

[12] V. Gruev, R. M. Philipp, J. van der Spiegel, and R. Etienne-Cummings, "Image sensor with general spatial processing in a 3D integrated circuit technology," in *Proc. IEEE ISCAS*, May 2006, p. 4.

[13] *Design Rules: MOSIS Scalable CMOS Edition 8*, [Online]. Available: http://www.mosis.org/Technical/Designrules/scmos/scmos-main.html

[14] A. M. Ismail and A. M. Soliman, "Wideband CMOS current conveyor," *Electron. Lett.*, vol. 34, no. 25, pp. 2368–2369, Dec. 1998.

[15] J. Hughes and K. Moulding, "S^{3}I: The seamless S^{2}I switched-current cell," in *Proc. IEEE ISCAS*, Hong Kong, Jun. 1997, vol. 1, pp. 113–116.

[16] H. Tian, B. Fowler, and A. El Gamal, "Analysis of temporal noise in CMOS photodiode active pixel sensor," *IEEE J. Solid-State Circuits*, vol. 36, no. 1, pp. 92–101, Jan. 2001.

[17] B. Wang, J. R. Hellums, and C. Sodini, "MOSFET thermal noise modeling for analog integrated circuits," *IEEE J. Solid-State Circuits*, vol. 29, no. 7, pp. 833–835, Jul. 1994.

[18] S. Lim and A. El Gamal, "Gain fixed pattern noise correction via optical flow," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 4, pp. 779–786, Apr. 2004.

[19] A. El Gamal, B. Fowler, H. Min, and X. Liu, "Modeling and estimation of FPN components in CMOS image sensors," in *Proc. SPIE*, San Jose, CA, Jan. 1998, vol. 3301, pp. 168–177.

[20] S. Kleinfelder, S. Lim, X. Liu, and A. El Gamal, "A 10,000 frames/s CMOS digital pixel sensor," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 2049–2059, Dec. 2001.

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