Linear Vt-based Temperature Sensors with Low Process Sensitivity and Improved Power Supply Headroom

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Abstract— **A new on-die temperature sensor that operates at low supply voltages and exhibits low process sensitivity and good linearity over a wide temperature range is introduced. When compared to conventional structures which have limited supply voltage headroom at the slow-n process corner, the new structures have sufficient headroom to practically operate well over all process corners. When implemented in a TSMC 0.18um process with a nominal supply voltage of 1.8V, simulation results show the maximum temperature linearity error is reduced from 1.5˚C to less than 0.3˚C at the NMOS slow process corner and with negative 10% Vdd variation.**

I. INTRODUCTION

On-chip thermal monitoring is a becoming increasingly important as VLSI circuits become more complex and more dense. On-chip the thermal monitors provide critical input to the power and thermal management structures that are necessary to prevent excessive chip temperatures from destroying the device or reducing the expected lifetime to unacceptable levels. In applications where on-chip heating is of concern, multiple built-in temperature sensors are distributed throughout the chip to monitor temperature at critical positions on the die. These on-chip temperature sensors must be compatible with the technology available in the process, must not consume a large area, and must be highly accurate with low power consumption over standard process variations and over typical supply voltage variations. The circuit shown in Fig.1 can be used for on-chip temperature sensing [1]. A startup circuit is needed for this temperature sensor but has been omitted for notational convenience. For the same reason, startup circuits are required for the other temperature sensors that will be introduced but they will not be shown in the schematics either. This circuit is compact in size, is insensitive to V_{DD} variations, and it has good linearity with temperature thus making it well suited for emerging on-chip temperature measurement applications. The sensor expresses the MOS threshold voltage at both the Vo1 and Vo2 outputs. Since the threshold voltage is highly linear with temperature, the output voltages of this circuit can be highly linear with temperature. With a combined analytical and numerical design approach, simulation results show that sizing optimization can effectively reduce the second- and third-order temperature non-linearity of this circuit to achieve a typical temperature INL error of about 0.05˚C using typical/typical process models. This is about ten times better than the current state of the art in CMOS based on-die temperature sensors [2]-[5].

Table 1 The sizes of Circuit A in reference [1]

	M1	M2	M3	M4	M5
W/L(μm)	0.3/0.8	2×5/0.4	2×7/0.4	4.5/0.9	4.5/0.9

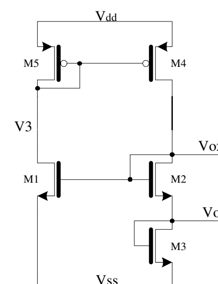

Fig. 1 Circuit A, the emperature sensor in reference [1]

However, under different process corners and power supply variations, the linearity of this circuit degrades. This degradation in linearity is due to headroom limitations on both the left and right sides of the circuit. At the slow NMOS corner, the headroom degradation is most severe on the right side of the circuit. At the slow NMOS, slow PMOS corner, the headroom limitations on the left side of the circuit are also problematic but of approximately the same magnitude as on the right side of the circuit. For this reason, we will restrict our discussion of headroom limitations to the right side of this circuit. Thus, the worst temperature nonlinearity of this reference occurs at low supply voltages in the slow NMOS process corner [1]. This can be attributed to the increase in the threshold voltage in this process corner when the temperature is low. This increase in threshold voltage reduces the Vds voltage of M4, and thus drives M4 towards the triode region, thus reducing the Vdd headroom on M4. Correspondingly, the increase in threshold voltage of the n-channel devices reduces the headroom on M1at low supply voltages since V3 also decreases but as stated previously, these effects are no worse than the headroom degradation on the right side.

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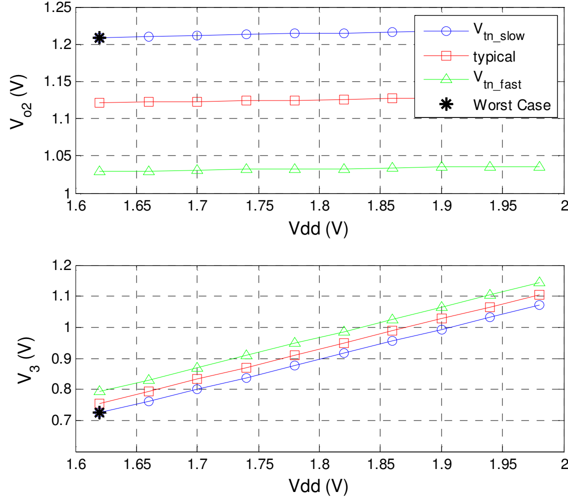

Fig. 2 Vo2 and V3 in Circuit A in different process corners the worst case is marked in black start markers

An implementation of this circuit was made in the TSMC 0.18u process with a nominal supply voltage Vdd designated with upper case subscripts of VDD=1.8V. Device sizes used in this simulation appear in Table 1. Low temperature -20C simulation results of Vo2 and V3 for different process corners and different supply voltages are shown in Fig. 2. The headroom is most severely limited when operating at the Vtn-slow process corner designated with the blue curves marked with circles. At the low supply voltage (10% below nominal) of Vdd=1.62V point, Vo2 is higher and V3 is lower when compared with the values at the other process corners. Naturally, the headroom is most limited at the low supply voltage and N_slow corner, and this worst case is marked with black stars. A sensitivity analysis is useful for characterizing how the headroom of a circuit is impacted by process variations. The sensitivity of Vo2 with respect to the NMOS threshold voltage is given in (1).

$$s_{V_{tn}}^{V_{o2}} = \frac{\partial V_{o2}}{\partial V_{tn}} = \frac{\sqrt{\frac{(W/L)_3}{(W/L)_2}} + 1 - 2\sqrt{\frac{(W/L)_3}{(W/L)_1}}}{\sqrt{\frac{(W/L)_3}{(W/L)_2}} + 1 - \sqrt{\frac{(W/L)_3}{(W/L)_1}}} \quad (1)$$

The change in the voltage headroom of M4 for this circuit,

$$\Delta HR = -s_{V_{tn}}^{V_{o2}} \times \Delta V_{tn} \quad (2)$$

It will now be assumed that the threshold voltages of M2 and M3 are the same and the excess bias voltage (sometimes termed the drain-source saturation voltage) of transistors M2, M3, and M4 are the same and given by Veb. The designed headroom with typical parameters is given by, VDD-(2Vtn+3Veb) where Vtn is the typical n-channel threshold voltage. In order to keep this temperature sensor working normally at 90% of the nominal voltage supply, the minimum headroom is 10% of VDD. If ΔHR is the change in headroom due to process variations, it follows that this requirement can be expressed as

$$V_{dd} - (2V_{tn} + 3V_{eb}) + \Delta HR > 0.1 \times V_{dd} \quad (3)$$

It follows from (2) and (3) that when the sensitivity increases, it becomes more difficult to satisfy (3), headroom requirement. saturation condition. In the design described in Table 1, the drain currents of all transistors are about the same. With the same values for Veb, it follows that M2 and M3 are close to the same size and $\sqrt{(W/L)_3/(W/L)_1}$ approximately 8.5. In the actual design it is 9.6. It thus follows from (2) that the sensitivity of Vo2 with respect to Vtn is around 2.3. Thus, if Vtn increases by 0.1V at the NMOS_slow corner, the voltage headroom will be squeezed down by about 0.23V because of Vo2 increasing.

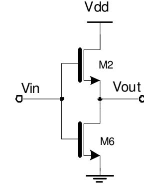

Fig. 3 Active attenuator

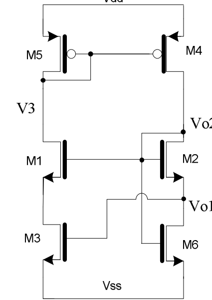

Fig. 4 Circuit B, the first proposed temperature sensor

II. DESCRIPTION OF PROPOSED CIRCUIT

In this section, two different temperature sensor circuits are described. The sensitivity values of these circuits when operating under low Vdd and slow threshold voltage process corners will be discussed and compared with that of Circuit A of Fig. 1.

Both circuits incorporate an active attenuator [6] as shown in Fig. 3. In this attenuator, M2 operates in the saturation region while M6 operates in the ohmic region. The transfer characteristics of this active attenuator can be written as:

$$V_{out} = \theta \left(V_{in} - V_{tn}\right) \quad (4)$$

where θ is a constant dependent upon device dimensions and where V_{tn} is the threshold voltage of the transistors.

A. Circuit B

The first proposed circuit is shown in Fig. 4. Compared with Circuit A in Fig.1, the active attenuator replaces the previous transistor M2 and M3 is moved to the left branch in the circuit. In this circuit, if channel length modulation and output conductance effects are neglected, and if it is assumed that M6 is operating in the triode region and the remaining devices are operating in the saturation region, it follows from the basic square-law model that the four equations (5)~ (8) describe the operation of the circuit.

$$I_{b1} = 1/2 \cdot \mu_n C_{ox} (W/L)_3 (V_{o1} - V_{tn3})^2 \quad (5)$$

$$I_{b2} = 1/2 \cdot \mu_n C_{ox} \cdot (W/L)_2 \cdot (V_{o2} - V_{o1} - V_{tn2})^2 \quad (6)$$

$$I_{b2} = I_{b1} \quad (7)$$

$$V_{o1} = \theta (V_{o2} - V_{tn2}) \quad (8)$$

Solving these equations for the two output voltages, it follows that the output can be expressed as a linear function of the NMOS threshold voltage as shown in (9) and (10). Thus the output voltage of this circuit also varies linearly with temperature. In order to compare the headroom of Circuit B with that of Circuit A, the sensitivity of Vo2 with respect to Vtn can also be calculated and it is given in (11). With a value of θ close to 1, it follows that $s_{V_{tn}}^{V_{o2}}$ equals 2.

It can be shown that the headroom equation of Circuit B can be expressed as (12). Thus in addition to a Veb increase in headroom, the **Δ**HR is reduced from 0.23V to 0.2V giving Circuit B an additional 30mV of headroom. Thus with 10% lower Vdd this circuit has better linearity at the Vtn-slow process corner than Circuit A.

$$V_{o1} = \frac{1}{1-\sqrt{\frac{(W/L)_2}{(W/L)_3}}(\frac{1}{\theta}-1)} \cdot V_{tn3} \tag{9}$$

$$V_{o2} = \frac{1}{\theta-\sqrt{\frac{(W/L)_2}{(W/L)_3}}(1-\theta)} \cdot V_{tn3} + V_{tn2} \tag{10}$$

$$s_{V_{tn}}^{V_{o2}} = \frac{\partial V_{o2}}{\partial V_{tn}} = \frac{(1+\theta)-\sqrt{\frac{(W/L)_2}{(W/L)_3}}(1-\theta)}{\theta-\sqrt{\frac{(W/L)_2}{(W/L)_3}}(1-\theta)} \tag{11}$$

$$V_{dd} - (2V_{tn} + 2V_{eb}) + \Delta HR > 0.1 \times V_{dd} \tag{12}$$

B. Circuit C

Fig. 5 shows a second Vdd independent temperature sensor that also expresses the n-channel threshold voltage at the Vo1 and Vo2 outputs. Again comparing with Circuit A, an active attenuator is substituted for M2of Circuit A and the

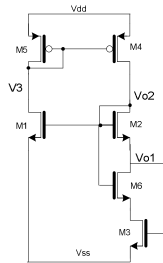

Fig. 5 Circuit C, the second proposed temperature sensor

gate of M3 is connected with the output of this attenuator instead of the drain of M3.

The expressions given in (13)~(16) mathematically characterize the operation of this circuit. As before, channel length modulation and output conductance effects were neglected when writing these equations.

$$I_{c2} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W_2}{L_2 + L_6} \cdot (V_{o2} - V_{d3} - V_{tn2})^2 \tag{13}$$

$$I_{c1} = \frac{\mu_n C_{ox}}{2} \cdot (\frac{W}{L})_1 \cdot (V_{o2} - V_{tn1})^2 \tag{14}$$

$$I_{c1} = \frac{\mu_n C_{ox}}{2} \cdot (\frac{W}{L})_1 \cdot (V_{o2} - V_{tn1})^2 \tag{15}$$

$$I_{c2} = I_{c1} \tag{16}$$

These 4 equations can be solved to obtain Vo1 and Vo2. These solutions are given in (17) and (18). It is apparent from (17) and (18) that the output voltages Vo1 and Vo2 both express the n-channel threshold voltage. The sensitivity function is also shown in (19). Its approximation value is 2.13. For Circuit C, the headroom equation is shown as (20), and its headroom is one Veb more than Circuit A. When Vtn increase 100mV, Vo2 will increase by 213mV. Thus, this circuit has about 13mV more voltage headroom compared with that of Circuit A. This headroom provides better linearity at the Vtn slow corner and with lower Vdd.

$$V_{o1} = \frac{[(1-\theta)\sqrt{\frac{(W/L)_3}{W_2/(L_2+L_6)}} - \sqrt{\frac{(W/L)_3}{(W/L)_1}}] \cdot V_{tn3} + (V_{tn1} - V_{tn2})}{(1-\theta)\sqrt{\frac{(W/L)_3}{W_2/(L_2+L_6)}} - \sqrt{\frac{(W/L)_3}{(W/L)_1}} + 1} \tag{17}$$

$$V_{o2} = \frac{V_{o1} - V_{tn3}}{\sqrt{\frac{(W/L)_1}{(W/L)_3}}} + V_{tn1} \tag{18}$$

$$s_{V_{tn}}^{V_{o2}} = \frac{\partial V_{o2}}{\partial V_{tn}} = \frac{(1-\theta)\sqrt{\frac{(W/L)_3}{(W/L)_2}} + 1 - 2\sqrt{\frac{(W/L)_3}{(W/L)_1}}}{(1-\theta)\sqrt{\frac{(W/L)_3}{(W/L)_2}} + 1 - \sqrt{\frac{(W/L)_3}{(W/L)_1}}} \tag{19}$$

$$V_{dd} - (2V_{tn} + 2V_{eb}) + \Delta HR > 0.1 \times V_{dd} \tag{20}$$

III. SIMULATION RESULTS

To demonstrate the temperature linearity of Circuit B and Circuit C and their performance at low Vdd at the slow threshold voltage process corner, two circuits were designed in a TSMC 1P5M 0.18um process. In these designs, emphasis was placed on obtaining a linear relationship between Vo2 and temperature since Vo2 provides a wider voltage range than Vo1.The device sizes used for these designs are included in Table 2. The nominal supply voltage is 1.8V.

Table 2The sizes of design examples for Circuit A and B

W/L(μm)	M1	M2	M3	M4,M5	M6
Circuit B	4X1.5/1	4/0.4	20/0.8	10X9/1	3.5/10
Circuit C	1.3/0.6	2X5/0.68	20X3.3/0.4	4X2/0.9	4X5/8

Simulation results for the output voltage Vo2 versus temperature are presented in Fig 6 for Circuit B and in Fig. 7 for Circuit C. The overall performances of these two circuits at node Vo2 are summarized in Table 3. These two structures were simulated at the four process corners, SS, FS, SF, and FF. It can be observed that Circuit B has a peak nonlinearity of 0.38˚C over all process corners, while simulation results of Circuit C show that it has a peak nonlinearity of 0.65˚C over all corners. This linearity is obtained without any INL trimming for process variations.

To verify the reduction in headroom with Circuit B and Circuit C, simulations were made with voltage drops down to a Vdd of 1.62V (10% reduction from nominal 1.8V). Simulations for both circuits were made at the problematic high NMOS threshold voltage corner and compared with the simulation results for Circuit A. The simulation results at 27˚C are shown in Fig.8. Circuit B and Circuit C have lower voltage levels at the Vo2 node. Thus, these two circuits do a better job of keeping M4 in the saturation when Vdd drops at the high NMOS threshold voltage corner. This correspondingly improves the linearity of these sensors over process corners. Fig. 9 shows a comparison of the three circuits' temperature linearity of node voltage Vo2 at the problematic low VDD and high NMOS threshold voltage corner. Circuits B and C are still able to maintain temperature error within 0.3°C, while circuit A has more than 1°C temperature error due to process variations at this corner. The maximum temperature errors

at the low Vtn corner and under low Vdd are compared with the sensitivity values of these three circuits in Table 4. Circuit B and C have lower Vo2 sensitivity values with respect to Vtn and the voltage headroom decrease less at NMOS_slow corner.

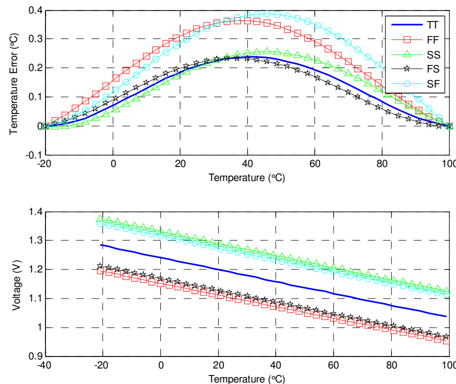

Fig. 6 Under nominal voltage supply (1.8V) Temperature Error of Circuit Bat different process corners (TT: typical; FF: fast NMOS fast PMOS; FS: fast NMOS slow PMOS; SS: slow NMOS slow PMOS; SF: slow NMOS fast PMOS)

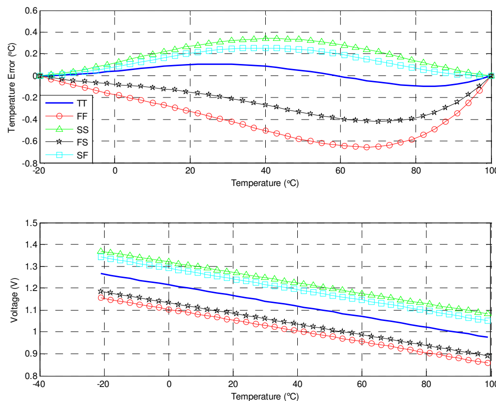

Fig. 7 Under nominal voltage supply (1.8V) Temperature Error of Circuit Bat different process corners (TT: typical; FF: fast NMOS fast PMOS; FS: fast NMOS slow PMOS; SS: slow NMOS slow PMOS; SF: slow NMOS fast PMOS)

Table 3 Performance summary of Circuit B and Circuit C

Parameters	*Performance of Circuit B*	*Performance of Circuit C*
Process	0.18 μm	0.18 μm
Temperature Range	-20℃~100℃	-20℃~100℃
Maximum Temp Error at typical condition	0.23℃	0.1℃
Maximum Temp Error at worst condition	0.38℃	0.65℃
Total area	270 μm²	185 μm²
Output Voltage Coefficient	-2.39 mV/℃	-2.11 mV/℃
Power consumption	95μW	65μW

IV. Conclusion

In this paper, two new Vdd-independent threshold-based temperature sensors were introduced. Simulation results for implementations in a 0.18u CMOS process show a worst case nonlinear temperature error of 0.38°C and 0.65°C respectively over all process corners with no nonlinearity trimming. This is a significant reduction in nonlinearity over process corners from what has been previously reported.

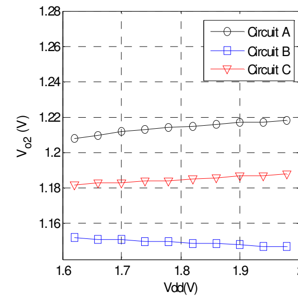

Fig. 8 Vo2 in Circuit A, B and C at high NMOS threshold voltage corner

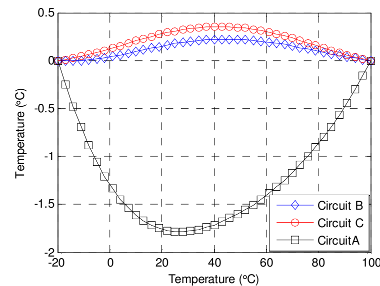

Fig.9 Temperature Errors of Circuit A, B and C at high NMOS threshold voltage corner

Table 4 Sensitivity and ΔHR(Voltage Headroom change) of Circuit A,B and C

	Circuit A	**Circuit B**	**Circuit C**
$S_{V_{tn}}^{V_{o2}}$ **(V/V)**	**2.3**	**2**	**2.13**
ΔHR (V) if ΔVtn=+0.1V	**-0.23**	**-0.2**	**-0.213**

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