Linearity and Mobility Degradation in Strained Si MOSFETs with Thin Gate Dielectrics

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Abstract-As gate dielectrics are scaled to a few atomic layers and the channel doping is increased to mitigate short channel effects, high vertical electric fields cause considerable mobility degradation through surface roughness scattering in silicon MOSFETs. This high field mobility degradation is known to influence the harmonic distortion through higher order drain current derivatives. Failure to take these higher order derivatives into account can cause significant error in the predictive evaluation of linearity (V_{IP3}) in MOSFETs. Electrical measurements are used to extract the 2nd order mobility degradation factor (θ_2) from strained silicon MOSFETs with different germanium contents. Linearity and high-field mobility degradation are shown to be independent of strain in spite of atomic force microscopy measurements showing that the surface roughness root-mean-square amplitude increases with the germanium content. It is also shown that θ_2 is required for the accurate modelling of linearity. The impact of oxide thickness on linearity is also investigated through θ_2. In this paper, an analytical relationship between θ_2 and the effective oxide thickness is developed and validated by electrical measurements on MOSFETs with different oxide thicknesses and θ_2 values from the literature. Using the extracted θ_2 values as inputs to analytical MOSFET models, a correlation between the oxide thickness and linearity is analyzed.

***Index Terms* – Distortion, Linearity, Mobility degradation, Strained Silicon.**

INTRODUCTION

The miniaturization of the metal oxide on semiconductor field effect transistor (MOSFET) has made complimentary metal oxide on semiconductor (CMOS) devices considerable radio frequency (RF) contenders where bipolars and high-electron-mobility-transistors are traditionally dominant [1, 2]. Strain engineering in deep submicrometer CMOS devices has further improved the high speed performance required for RF implementation [3]. However in analog/mixed-signal applications, other metrics like noise and linearity are important [4-6]. Linearity is particularly of interest in CMOS devices since MOSFETs exhibit better linearity than bipolars [2]. In a perfectly linear MOSFET, a signal with a single harmonic at the input would yield an output signal at the same frequency. However, since MOSFETs are not perfectly linear, the output signal usually contains higher order harmonics that may interfere with the fundamental. These higher order harmonics are related to the higher order derivatives of the drain current with respect the terminal voltages according to

$$i_{DS} \approx g_m v_{GS} + \frac{\partial g_m}{\partial v_{GS}} v_{GS}^2 + \frac{\partial^2 g_m}{\partial v_{GS}^2} v_{GS}^3 + \ldots\ldots\ldots \frac{\partial^{n-1} g_m}{\partial v_{GS}^{n-1}} v_{GS}^n \qquad (1)$$

where i_{DS} is the drain-source current, g_m is the transconductance and v_{GS} is the small signal gate-source voltage. Distortion analysis is important for analog MOSFETs since higher order harmonics at the output can cause interference with fundamental harmonic thereby resulting in inter-modulation distortion and degrading the signal integrity of the system. Of the higher order harmonics, the most important is the 3rd order harmonic due to the fact that a signal close in frequency to the fundamental signal at the input of a MOSFET will have a third order intermodulation harmonic at

the output of the MOSFET that will be close in frequency to the fundamental. Various figures of merit have been developed to quantify the linearity of RF transistors. The third order intercept point (*IP3*) is defined as the input power level at which the fundamental harmonic and the third order harmonic have equal power levels at the output. This is usually determined from extrapolations of RF power measurements. Another indicator of linearity is the V_{IP3} which is defined as the extrapolated gate voltage (V_{GS}) bias at which the amplitudes of the 1st and 3rd order derivatives of I_{DS} are equal [2, 7-11]. The V_{IP3} can be measured from MOSFET DC I_{DS} *vs.* V_{GS} characteristics and is given by

$$V_{IP3} = \sqrt{24\left[\frac{\partial g_m}{\partial V_{GS}}\right] \times \left[\frac{\partial^2 g_m}{\partial V_{GS}^2}\right]^{-1}} \tag{2}$$

It has been shown that accounting for mobility degradation accurately is essential for understanding the distortion characteristics of MOSFETs [7]. Since applications that require low distortion use strongly inverted MOSFETs (where linearity is highest), surface roughness scattering becomes the important mobility limiting mechanism in the determination of linearity. Gate dielectric scaling and higher substrate doping has increased the transverse electric fields and hence, mobility degradation from surface roughness scattering. A 2nd order mobility degradation model was developed to account for mobility reduction related to $(V_{GS}\text{-}V_{TH})^2$ at high vertical fields where V_{TH} is the threshold voltage [12]. The effective mobility, μ_{EFF} can be expressed as

$$\mu_{EFF} = \frac{\mu_O}{1 + \theta_1 (V_{GS} - V_{TH}) + \theta_2 (V_{GS} - V_{TH})^2} \quad (3)$$

where θ_1 is the 1st order mobility degradation factor (MDF), θ_2 is the 2nd order MDF and μ_O is the low field mobility. Previous accounts of modelling mobility degradation from surface roughness scattering used only the 1st order MDF model which can be derived from equation 3 by assuming θ_2=0 [13-15]. However, as the gate dielectric is thinned, the amplitude of the semiconductor surface asperities at the dielectric interface becomes a larger proportion of the total dielectric thickness hence 2nd order effects become non-negligible. The model in equation 3 was shown to account more accurately for mobility degradation in thin gate dielectric MOSFETs and has been used in other studies [16-18]. In this paper, the linearity of strained Si nMOSFETs is assessed, the 2nd order MDF (θ_2) is extracted for 2.5 nm thick oxides and a MOSFET model is used to assess the importance of θ_2 in the predictive modelling of linearity for CMOS devices. Also, an analytical model is developed relating θ_2 to the oxide thickness and is validated by experimental measurements of θ_2 together with values taken from literature.

DEVICE FABRICATION

Si control and strained Si nMOSFETs on $Si_{1-x}Ge_x$ strain relaxed buffers (SRBs) with x=0.15, 0.20 and 0.25 are co-fabricated in a CMOS process flow. The SiGe SRBs where grown by low-pressure chemical vapour deposition with SiH_4 and GeH_4 as pre-cursors. The total thickness of the SiGe SRBs was 4 μm with the compositional grading done to a thickness of 2.5 μm and a 1.5 μm layer of constant composition SiGe upon which 10 nm of tensile strained Si layers are deposited. The

tensile strain is confirmed by Raman spectroscopy. Atomic force microscopy (AFM) measurements with different scan sizes were performed on the strained Si wafers. Table 1 shows the results of the AFM scan. The rms roughness amplitude is proportional to the germanium content. It is known that cross-hatching resulting from strain relaxation in the underlying virtual substrate increases the surface roughness amplitude in strained Si MOSFETs hence, these results are not surprising [19, 20]. The gate oxide is grown by thermal oxidation to an effective oxide thickness (EOT) of 2.5 nm which is confirmed by gate-bulk capacitance measurements. The gate polysilicon was deposited; after which source-drain arsenic LDD and boron anti-punch-through pocket implantation was performed. The next process steps were the silicon nitride side wall spacer formation, source-drain HDD implantation and cobalt silicidation done at 1000 °C for 30s. Contact was made with the MOSFET through tungsten plugs with titanium nitride barriers lining the contact via. The back end metallisation consisted of aluminium and copper.

RESULTS AND DISCUSSION

Using the split CV technique with series resistance corrections, the effective mobility is extracted for the Si control and strained Si nMOSFETs [21]. Fig. 1 shows the effective mobility as a function of the vertical effective field for all the devices. It can be seen from Fig. 1 that the effective mobility is proportional to the Ge content (strain) over the entire range of vertical field. The gate-channel capacitance and gate-bulk capacitance measurements used in the calculation of the inversion charge density and vertical effective fields were done on 10 μm (W) by 10 μm (L_G) nMOSFETs biased at 25 mV drain voltage.

The 2nd order mobility degradation factor is extracted using a technique introduced by McLarty et al [12]. The starting point of the technique is the drain current linear model (low V_{DS} and high V_{GS}) for strongly inverted MOSFETs

$$I_{DS} = \frac{W\mu_{EFF}C_{OX}}{L_G}(V_{GS} - V_{TH})V_{DS} \tag{4}$$

where W is the gate width, L_G is the gate length, C_{OX} is the gate dielectric capacitance density and V_{DS} is the drain voltage. Substituting equation (3) into (4), the 1st order and 2nd order derivatives of the inverse of the drain current (I_{DS}^{-1}) with respect to V_{GS} is calculated as

$$\frac{\partial}{\partial V_{GS}}\frac{1}{I_{DS}} = \frac{L_G}{W\mu_O C_{OX}V_{DS}}\left(\theta_2 - \frac{1}{(V_{GS} - V_{TH})^2}\right) \tag{5}$$

$$\left(\frac{\partial^2}{\partial V_{GS}^2}\frac{1}{I_{DS}}\right)^{-\frac{1}{3}} = \left(\frac{W\mu_O C_{OX}V_{DS}}{2L_G}\right)^{\frac{1}{3}}(V_{GS} - V_{TH}) \tag{6}$$

θ_2 is extracted from equation 5 as the x-axis intercept of the linear plot of $\partial\left(I_{DS}^{-1}\right)/\partial V_{GS}$ against $(V_{GS}\text{-}V_{TH})^{-2}$ whereas μ_0 is extracted from the slope of the straight line. The threshold voltage can be extracted by calculating the 2nd derivative of the inverse of the drain current (I_{DS}^{-1}) with respect to V_{GS} and plotting $(\delta^2(I_{DS}^{-1})/\delta V_{GS}^2)^{-1/3}$ as a linear function of V_{GS}. The threshold voltage is the intercept of the extrapolated linear plots with the V_{GS} axis.

Fig. 2(a) and Fig. 2(b) show the plots of $\partial\left(I_{DS}^{-1}\right)/\partial V_{GS}$ against $(V_{GS}\text{-}V_{TH})^{-2}$ for 0.5 μm (L_G) Si control and strained Si nMOSFETs biased at 50 mV V_{DS}. A low drain

voltage is used because the MOSFET channel must be biased in strong inversion (linear mode) for the model in equation 4 to be applicable. It can be seen from Fig. 2(a) that the slopes of the lines reduce as the Ge composition (or strain content) increases. This observation correlates with equation 5 where it can be seen that the slope $L_G/(W\mu_O C_{OX} V_{DS})$ is inversely proportional to the low field mobility. The extracted low field mobility, shown in table 2, is proportional to strain and is on average 100% higher than the effective mobility. The 2nd order MDF and low field mobility are respectively extracted from the x-axis intercepts and slopes in Fig. 2 (a). Fig. 2(b) is an enlarged version of Fig. 2(a), showing how the values of θ_2 are read off from the x-axis intercepts. When calculating the slope and intercept from Fig. 2(a), it is important to only consider measurement points at least 500 mV above the threshold voltage. This corresponds to $(V_{GS}-V_{TH})^2 < 4\ V^2$ in Fig. 2. This is because the MOSFET model in (4) applies to only MOSFETs in strong inversion and mobility degradation from the vertical effective field applies only at high V_{GS}. It can be seen from Fig. 2(b) that the values of θ_2 vary from 0.28 V^{-2} to 0.29 V^{-2} for the Si control and strained Si nMOSFETs. θ_1 is also calculated by substituting the experimentally extracted values of μ_{EFF}, μ_O and V_{GS}-V_{TH} (which is approximately 1.5 V at an E_{EFF} of 1.8 $MVcm^{-1}$) into equation 3. The values of θ_1, θ_2 and μ_{EFF} can also be seen in table 2.

Fig. 2(b) and Table 2 show that the values of θ_2 for the Si control and strained Si nMOSFETs are within 2% of each other, hence it can be assumed that θ_2 is independent of strain. Since the MOSFETs under investigation here are co-processed (the same EOT, pocket implant and substrate doping), the only factor that may influence mobility degradation differently would be the different surface morphological properties (rms roughness amplitude and correlation length). However, in spite of the increasing AFM measured surface roughness with Ge content (strain),

the mobility enhancement is maintained in the strained Si devices. High mobility enhancement in strained Si MOSFETs at high vertical fields (in the surface-roughness scattering regime) has led researchers to propose that strained Si MOSFETs have "smoother" surfaces compared with Si control MOSFETs [22, 23]. Lower surface roughness amplitudes and longer correlation lengths were required to match simulated high field mobilities with measured high field mobilities in strained Si MOSFETs [22]. Smoother surfaces in strained silicon are assumed because the mobility enhancement mechanism (reduced phonon scattering from Δ_2-Δ_4 conduction band splitting) can explain mobility enhancement at medium vertical fields (where phonon scattering is the dominant mobility limiting mechanism) but not at high vertical fields (where surface roughness scattering is the dominant mobility limiting mechanism). Furthermore, the band-splitting due to quantum confinement at high vertical fields renders the band splitting from tensile strain redundant [23]. Although the measurements here indicate that mobility degradation is independent of strain, more advanced MOSFET models than (1) and more advanced mobility models than (2) would be needed to understand the impact of strain/germanium-related surface morphological properties on the high field mobility in strained Si layers.

Fig. 3 shows the extraction of V_{TH} for the Si control and strained Si nMOSFETs based on equation 6. Since, the devices are process matched, it is expected that the V_{TH} will reduce as the Ge content in the $Si_{1-x}Ge_x$ SRB increases. This is due to the increase in the electron affinity with tensile strain. Table 2 also shows the V_{TH} values extracted from Fig. 3. The V_{TH} values extracted from Fig. 3 agree well with V_{TH} values extracted using the linear transconductance method.

The linearity (V_{IP3}) of the Si control and strained Si nMOSFETs is measured according to (2). The transconductance (g_m) and the 2nd derivative of the

transconductance (g_{m3}) are used to calculate the linearity. Fig. 4 shows the V_{IP3}^2 as functions of the gate voltage overdrive for the 0.5 μm gate length Si control and strained Si nMOSFETs with 50 mV V_{DS}. The characteristic peak in the V_{IP3}^2 plot of Fig. 4 indicates when the 2nd order derivative of the transconductance (g_{m3}) crosses the zero mark [8, 9]. V_{IP3} is low in weak inversion (left side of the peak) due to the exponential relationship between I_{DS} and V_{GS} (I_{DS} is a diffusion current). V_{IP3}^2 increases in strong inversion because the exponential relationship between I_{DS} and V_{GS} becomes parabolic (I_{DS} is a drift current). The peaks in the V_{IP3}^2 characteristics of the measured devices in Fig. 4 occurs at V_{GS}=V_{TH}, thereby indicating the change from a diffusion current to a drift current i.e. the onset of moderate inversion or the triode part of the I_{DS} *vs.* V_{GS} characteristic. As can be seen from Fig. 4, there is no difference in the V_{IP3}^2 characteristics hence V_{IP3} is independent of strain. This is not surprising since mobility is proportional to both g_m and g_{m3}, hence, it is removed by the ratio in equation 2. Also, it has already been shown in Fig. 2 that mobility degradation is independent of strain. It has been shown that V_{IP3}^2 depends on the oxide thickness and substrate doping, (i.e. the body factor) both of which affect the vertical electric field [5]. Fig. 5 shows the measured g_m and g_{m3} for the Si control MOSFET illustrating the positive and negative peak of g_{m3}. The region to the right of the maximum transconductance in Fig. 5 is dominated by surface roughness scattering hence, the magnitude of mobility degradation determines the slope of the negative transconductance.

The importance of taking the 2nd order MDF into account in the predictive modelling of V_{IP3}^2 is shown by using a single-piece semi-empirical MOSFET model which is valid from weak inversion to strong inversion [9, 24].

$$I_{DS} = I_{D0}\left[\left(\ln\left(1+\exp\left(\frac{V_{GS}-V_{TH}}{2m\Phi_{TH}}\right)\right)\right)^2 - \left(\ln\left(1+\exp\left(\frac{V_{GS}-V_{TH}-mV_{DS}}{2m\Phi_{TH}}\right)\right)\right)^2\right] \quad (7)$$

where $I_{D0} = \dfrac{2W\mu_O C_{OX}\Phi_{TH}^2 m}{L_G\left(1+\theta_1\left(V_{GS}-V_{TH}\right)+\theta_2\left(V_{GS}-V_{TH}\right)^2\right)}$

m is the body factor (m =1.16 for an oxide thickness of 2.5 nm and for a substrate doping of 5x10^{17} cm^{-3}), L_G is 500 nm, V_{DS}=50 mV and Φ_{TH} is the 300 K thermal voltage (26 mV). Fig. 6 shows g_m and g_{m3} calculated using the model in equation 7 with θ_1=0.6 V^{-1} and θ_2=0.3 V^{-2}. The similarity between the calculated characteristics of Fig. 6 and the measured characteristics of Fig. 5 was obtained by tuning θ_2 to the measured value. Fig. 7 shows a comparison between the measured V_{IP3}^2 characteristic and the calculated V_{IP3}^2 characteristics with θ_2=0 V^{-2} and θ_2=0.3 V^{-2}. It can be seen in Fig. 7 that the calculated characteristic matches the measured characteristic only with θ_2 taken into account (θ_2=0.3 V^{-2}). The calculated V_{IP3} with θ_2=0 V^{-2} exhibits high V_{IP3} in strong inversion which is not representative of the measured characteristic. Fig. 8 shows the calculated V_{IP3}^2 as a function of V_{GS} for different values of θ_2. It can be seen in Fig. 8 that V_{IP3}^2 reduces significantly as θ_2 increases. Fig. 7 and Fig. 8 show that it is necessary, in the predictive modelling of linearity, to take θ_2 into account as linearity can easily be over-estimated.

The effective mobility of a carrier in a MOSFET is determined by coulomb scattering from ionized impurities, phonon scattering from lattice vibrations and surface roughness scattering from surface asperities at the Si/SiO_2 interface [25]. This can be expressed, according to the Matthiessen' rule, as

$$\mu_{EFF} = \frac{\mu_O'}{1 + \theta_{PH} E_{EFF}^{1/3} + \theta_{SR} E_{EFF}^{n}} \tag{8}$$

where θ_{PH} and θ_{SR} are empirical parameters [7]. The interface between the silicon channel and the gate dielectric is not atomically smooth; hence, carriers scatter against surface asperities in strong inversion conditions. These Si channel surface asperities can be characterised by the root-mean-square roughness and the correlation length [26]. Surface roughness can be modelled as variations in oxide thickness, hence carriers transiting along the channel will be perturbed by a change in potential that is proportional to the average roughness amplitude [26, 27]. According to the Fermi golden rule, the scattering rate is proportional to the square of the perturbation potential resulting from the surface roughness [28]. Under high vertical fields, *n* in equation 8 is usually 2 for electrons and 1 for holes [7, 25, 26, 28, 29]. Under such conditions, equation 8 can be re-written for electrons as

$$\mu_{EFF} = \frac{\mu_O'}{1 + \theta_{SR} E_{EFF}^{2}} \tag{9}$$

The vertical effective field for a MOSFET in inversion can be expressed as

$$E_{EFF} = \frac{1}{\varepsilon_{Si}} \left(Q_B + \eta C_{OX} \left(V_{GS} - V_{TH} \right) \right) \tag{10}$$

where $Q_B = \sqrt{4 q \varepsilon_{Si} N_A \left(\frac{k_B T}{q} \ln\left(\frac{n_i}{N_A} \right) \right)}$

Q_B is the depletion charge density (0.39 μC.cm^{-3} for a substrate doping, N_A, of 5x10^{17}cm^{-3}), ε_{Si} is the dielectric constant of silicon, C_{OX} is the gate dielectric capacitance density (1.42 μF.cm^{-2} for an EOT of 2.5 nm) and η is 0.5. Substituting equation 10 into 9, the effective mobility can be re-written in the form of equation 3 with the following expressions for the low field mobility, the 2nd and 1st order MDF.

$$\mu_O = \mu_O^{/}\left(1+\frac{\theta_{SR}}{\varepsilon_{Si}^2}Q_B^2\right)^{-1} \tag{11}$$

$$\theta_2 = \frac{\theta_{SR}}{\varepsilon_{Si}^2}\eta^2 C_{OX}^2\left(1+\frac{\theta_{SR}}{\varepsilon_{Si}^2}Q_B^2\right)^{-1} \tag{12}$$

$$\theta_1 = 2\frac{\theta_{SR}}{\varepsilon_{Si}^2}Q_B\eta C_{OX}\left(1+\frac{\theta_{SR}}{\varepsilon_{Si}^2}Q_B^2\right)^{-1} \tag{13}$$

In the pioneering work of mobility degradation analysis by Fu [13], a similar expression to equation 13 was developed for θ_1 as shown below

$$\theta_1 = \frac{B}{4\varepsilon_{Si}}C_{OX}\left(1+\frac{B}{\varepsilon_{Si}}Q_B\right)^{-1}$$

where $B=2bql/3KT$.

l is the mean free path, T is the temperature, K is Boltzmann's constant and b is a constant that depends on the ratio of the mean free path to the inversion layer depth. B in [13] was found to be 6.41×10^{-6} cm.V^{-1} assuming a mean free path and inversion layer depth of 5 nm. Comparing equation 13 with the formulation in [13], the following expression can be derived for θ_{SR}

$$\theta_{SR} = N\left(\frac{2bql}{3\eta KT}\right)\frac{\varepsilon_{Si}}{Q_B} \tag{14}$$

N accounts for the numerical constant difference between the derivation of θ_1 in this study and that in [13]. Solving equation 14 using the value of B calculated in [13], θ_{SR} is calculated to be approximately 17×10^{-12} cm^2.V^{-2}. Substituting θ_{SR}=17×10^{-12} cm^2.V^{-2} into equations 12 and 13, solving for θ_1 and θ_2 yields 2.5 V^{-1} and 2.3 V^{-2} respectively. This is much higher than what was measured. Adjusting N to 0.34 and θ_{SR} to 0.8×10^{-12} cm^2.V^{-2}, solving for θ_1 and θ_2 yields 0.6 V^{-1} and 0.3 V^{-2} respectively (much closer to the measured values). For θ_{SR} = 0.8×10^{-12} cm^2.V^{-2},$Q_B^2\theta_{SR}/\varepsilon_{Si}^2 << 1$, hence, equations 11, 12 and 13 can be approximated as

$$\mu_O = \mu_O' \tag{15}$$

$$\theta_2 = \frac{\theta_{SR}}{\varepsilon_{Si}^2}\eta^2 C_{OX}^2 \tag{16}$$

$$\theta_1 = 2\frac{\theta_{SR}}{\varepsilon_{Si}^2}Q_B\eta C_{OX} \tag{17}$$

It can be observed that in equations 12 and 13 that θ_1 and θ_2 are inversely related to the gate dielectric thickness. This is expected since the vertical effective field increases as the gate dielectric is scaled. What is also interesting to note is that the dielectric constant of the gate insulator is directly proportional to θ_1 and θ_2. This is important for advanced technology nodes that used high-k gate dielectrics. To experimentally characterise the dependence of on θ_2 on t_{OX}, θ_2 is extracted from a 1.4 nm and a 6 nm thick gate oxide nMOSFET. Although the MOSFETs were not

fabricated in the same process flow, the comparison serves as the first approximation of the θ_2 vs. t_{OX} relationship. Fig. 9 shows the measured θ_2 as a function of t_{OX} for the 1.4 nm, 2.5 nm and 6 nm nMOSFETs together with measurements taken from 3.5 nm and 10 nm gate oxide MOSFETs in literature [12]. It should be noted that since these MOSFETs are not co-fabricated, they will exhibit different θ_{SR} values due to different surface roughness amplitudes and correlation lengths i.e. θ_{SR} will be unique for each process. However, a universal trend can be observed with θ_2 increasing as t_{OX} is reduced. Also shown in Fig. 9 is the θ_2 vs. t_{OX} calculated by equation 12 with θ_{SR} = 1×10^{-12} $cm^2.V^{-2}$ and Q_B =0.39 $\mu C.cm^{-3}$. It can be seen in Fig. 9 that there is good agreement between the measured and modelled θ_2 vs. t_{OX} relationship.

The linearity of the 6 nm and 1.4 nm oxide MOSFETs is also measured. It has been shown in Fig. 7 and Fig. 8 that V_{IP3} reduces as θ_2 increases. Fig. 10 shows the V_{IP3}^2 as a function of V_{GS}-V_{TH} for 1.4 nm, 2.5 nm and 6 nm oxide MOSFETs. It can be seen in Fig. 10 that V_{IP3}^2 reduces with the oxide thickness. At V_{GS}-V_{TH} =1.25 V, there is a difference of at least an order of magnitude between the V_{IP3}^2 of the MOSFETs.

CONCLUSIONS

The results in this paper show the importance of the 2nd order MDF in the predictive modelling of linearity in ultra-thin gate dielectric MOSFETs. The 2nd order MDF and low field mobility has been extracted from strained Si MOSFETs with 2.5 nm silicon dioxide gate dielectrics and varying germanium composition. The results indicate that mobility degradation and linearity is independent of strain and is dominated by oxide thickness. A semi-empirical MOSFET model calibrated with the measured parameters is used to further understand the impact of the 2nd order MDF on linearity. It was shown that linearity reduces substantially as the 2nd order MDF is

increased. An analytical relationship between the 2nd order MDF and the gate dielectric thickness is developed. It is shown that the 2nd order MDF is inversely proportional to the oxide thickness. Measurements of the 2nd order MDF from MOSFETs with different oxide thicknesses and values taken from literature are used to validate the accuracy of the model. The model also indicates that linearity will be reduced in MOSFETs with high-k dielectrics due to the increased dielectric constant. MOSFET models must take account of the 2nd order MDF as these results show that linearity can easily be over-estimated.

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TABLE 1
AFM MEASUREMENTS

AFM Scan size	Ge=15% RMS (nm)		Ge=20% RMS (nm)		Ge=25% RMS (nm)	
	Max	St dev	Max	St dev	Max	St dev
1x1 μm^2	0.20	0.01	0.23	0.04	0.23	0.04
3x3 μm^2	0.21	0.02	0.40	0.12	0.43	0.06
10x10 μm^2	0.28	0.05	0.39	0.09	0.83	0.14
30x30 μm^2	0.40	0.09	0.61	0.15	0.89	0.10
100x100 μm^2	0.70	0.05	0.90	0.09	1.20	0.22

TABLE 2
PARAMETERS EXTRACTED

Device	μ_O ($cm^2V^{-1}S^{-1}$)	μ_{EFF} ($cm^2V^{-1}S^{-1}$)	θ_2 (V^{-2})	θ_1 (V^{-1})	V_{TH} (V)
Si	230	125	0.28	0.63	0.40
Ge=15%	515	250	0.29	0.59	0.34
Ge=20%	569	280	0.28	0.61	0.30
Ge=25%	594	310	0.28	0.57	0.28

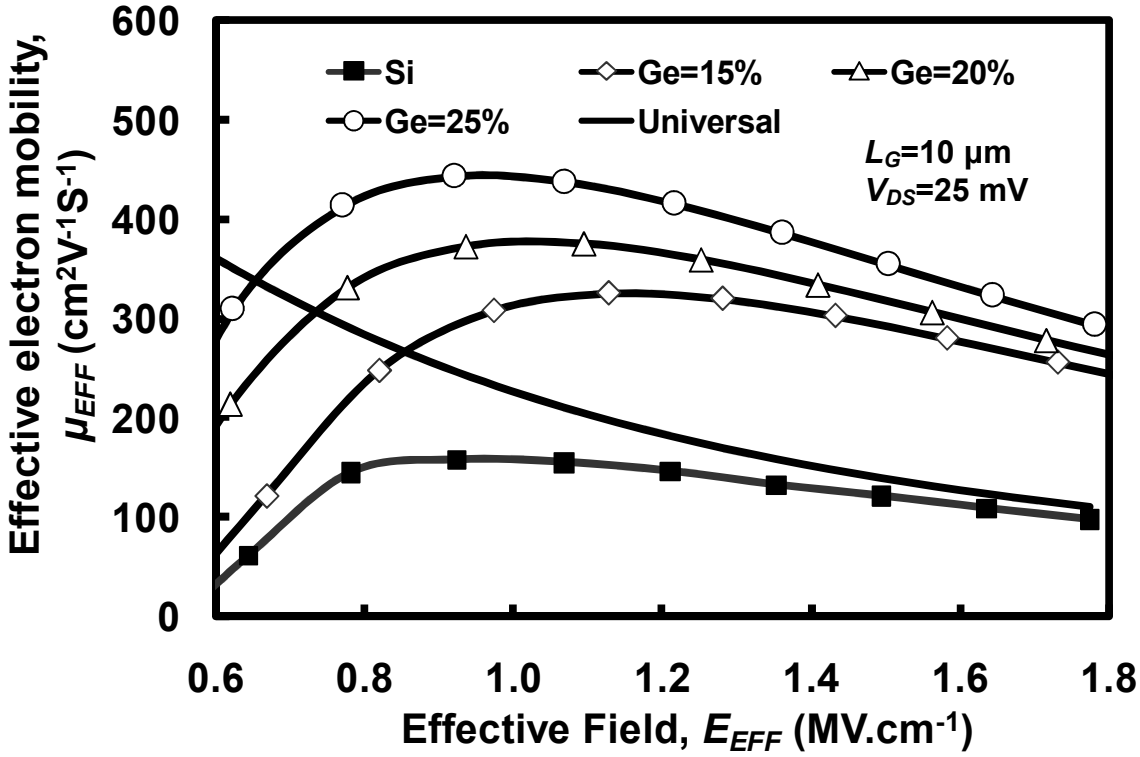

Fig. 1. The effective mobility as a function of the vertical effective field for the Si control and strained Si nMOSFETs on $Si_{1-x}Ge_x$ SRBs for x=0.15, 0.20 and 0.25. The effective mobility is proportional to strain.

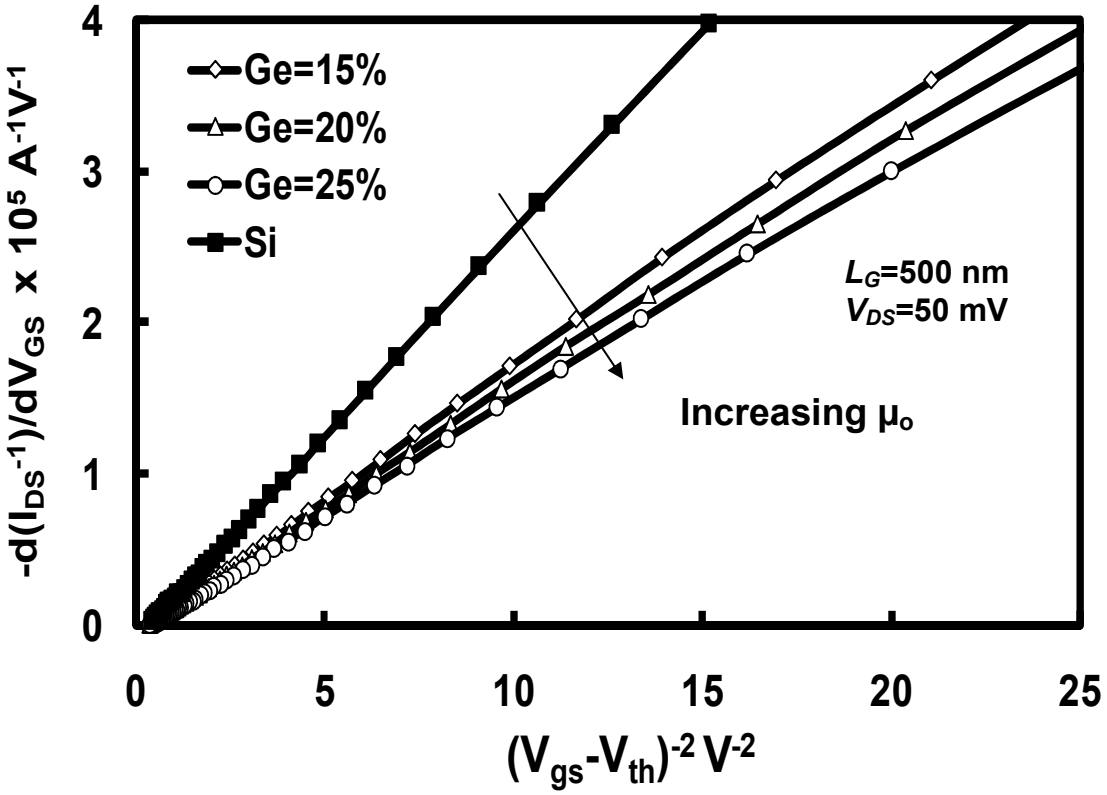

Fig. 2(a). $\partial\left(I_{DS}^{-1}\right)/\partial V_{GS}$ plotted as a function of $(V_{GS}-V_{TH})^{-2}$ for Si control and strained Si nMOSFETs. The low field mobility is inversely proportional to the slope of the line and θ_2 can be extracted from the x-axis intercepts.

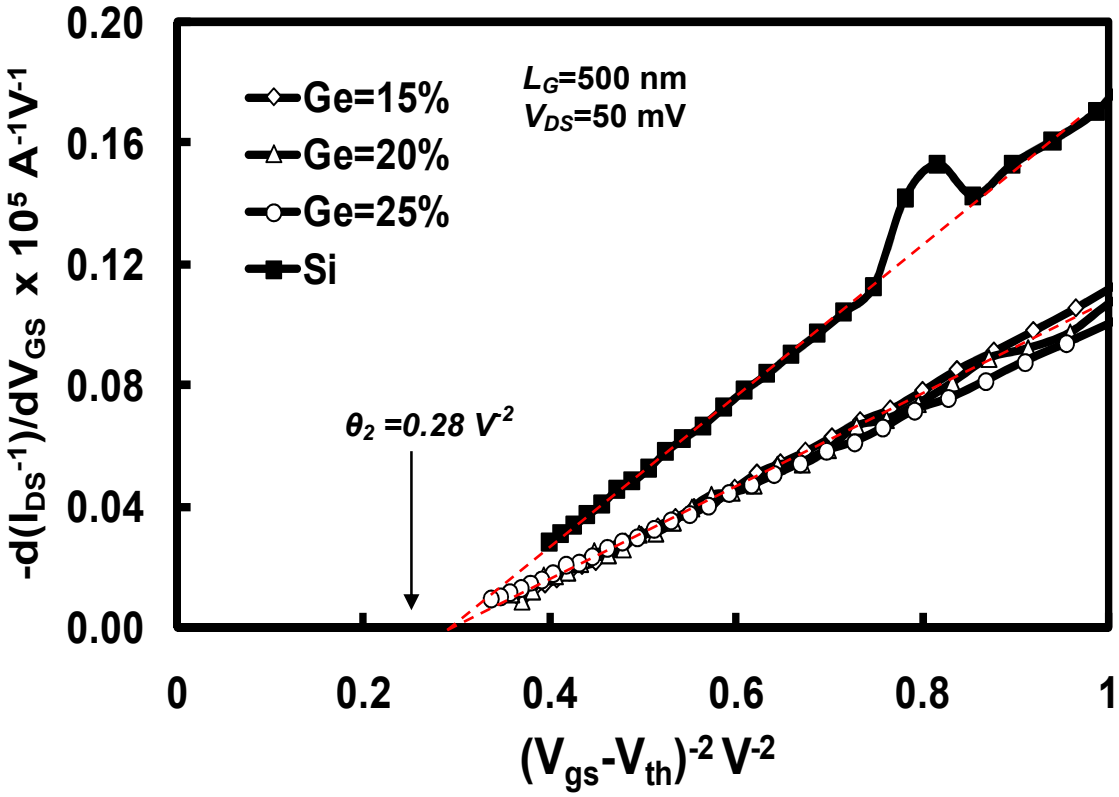

Fig. 2(b). An enlarged version of Fig. 2(a) showing the intercepts of the straight lines with the x axis. The 2nd order MDFs extracted for all the MOSFETs is approximately 0.29 V^{-2}.

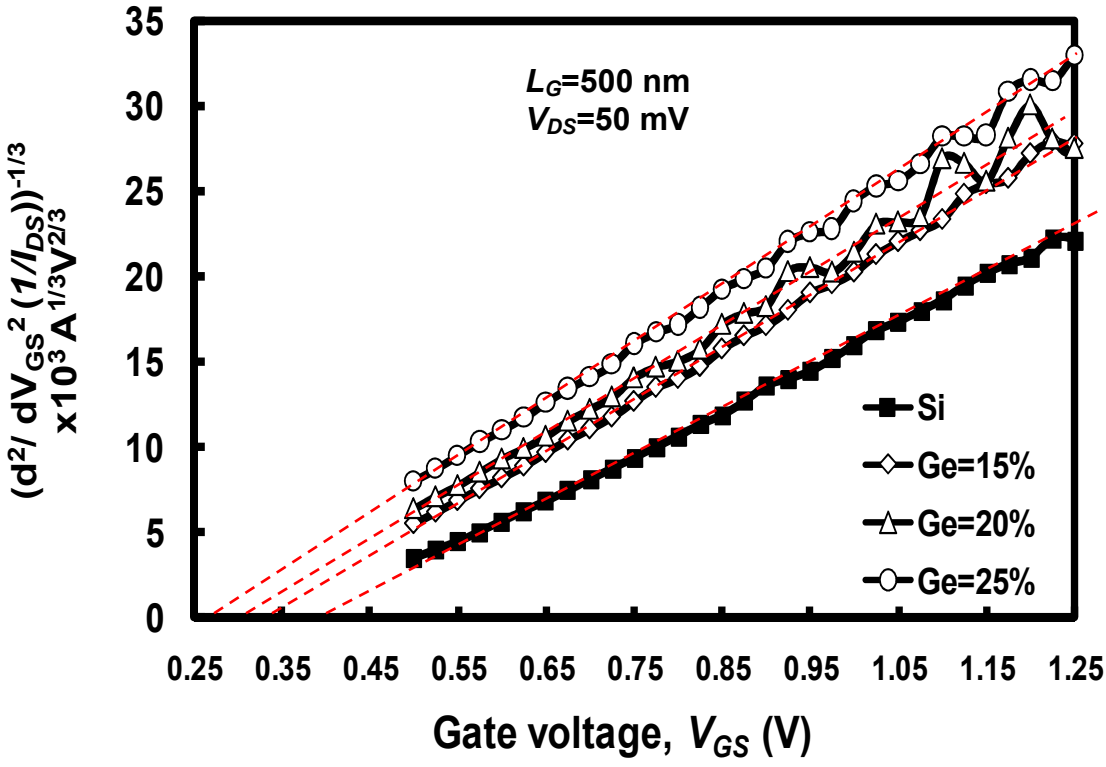

Fig. 3. The extraction of the threshold voltage from the x axis intercepts. The V_{TH} extracted reduces as the strain content increases. V_{TH} extracted agrees with values extracted using linear transconductance.

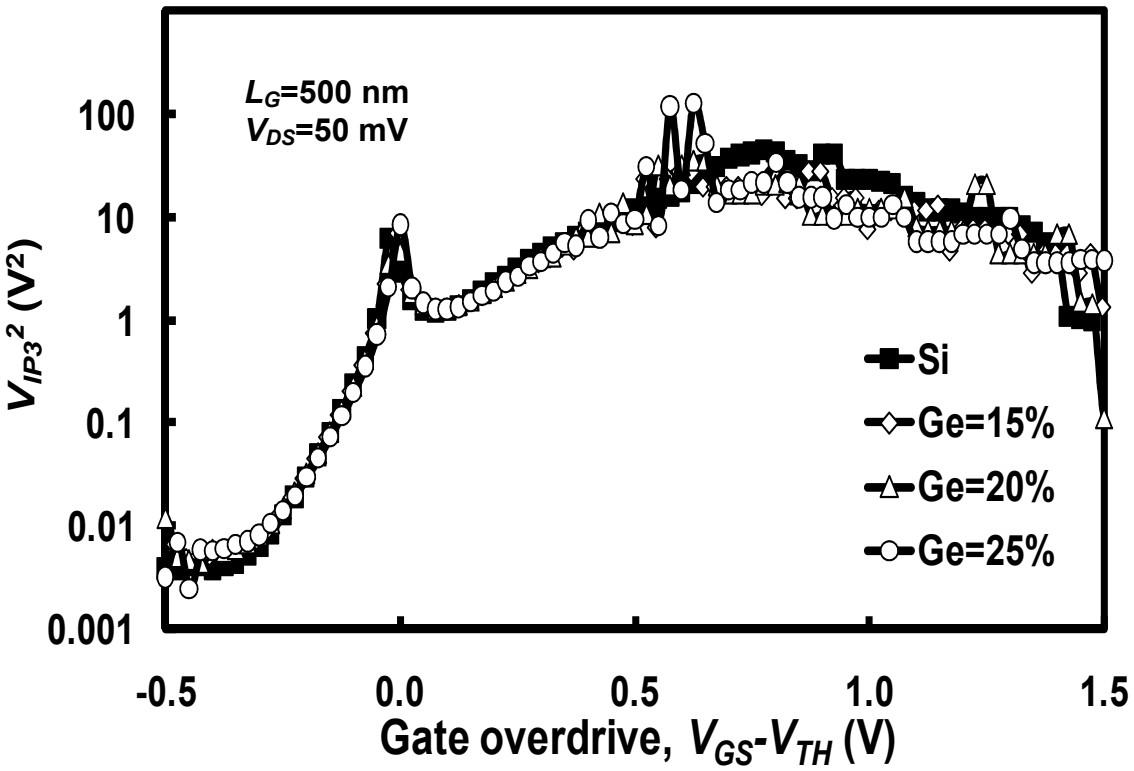

Fig. 4. V_{IP3}^2 as a function of the gate voltage overdrive for strained Si and Si control nMOSFETs. There is no impact of strain on the V_{IP3}^2.

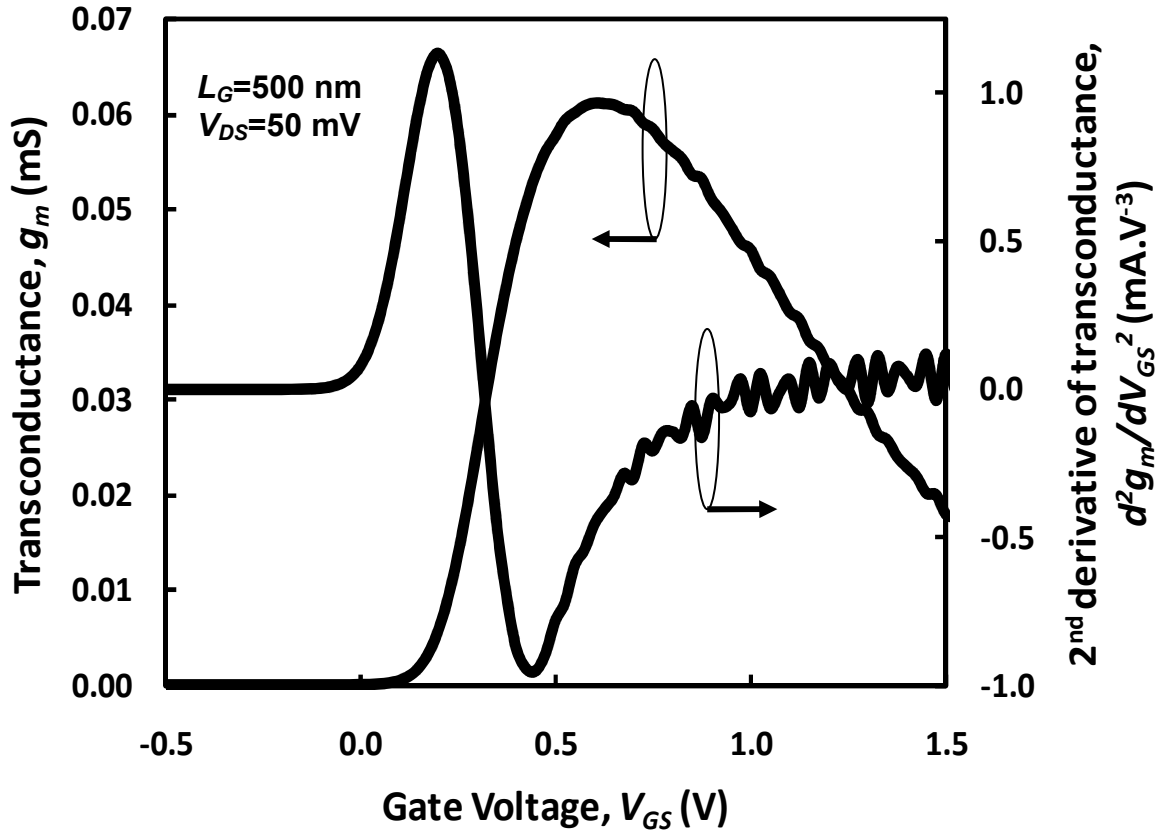

Fig. 5. Measured g_m and $\delta^2 g_m/\delta V_{GS}^2$ as functions of V_{GS}-V_{TH} for the Si control MOSFET.

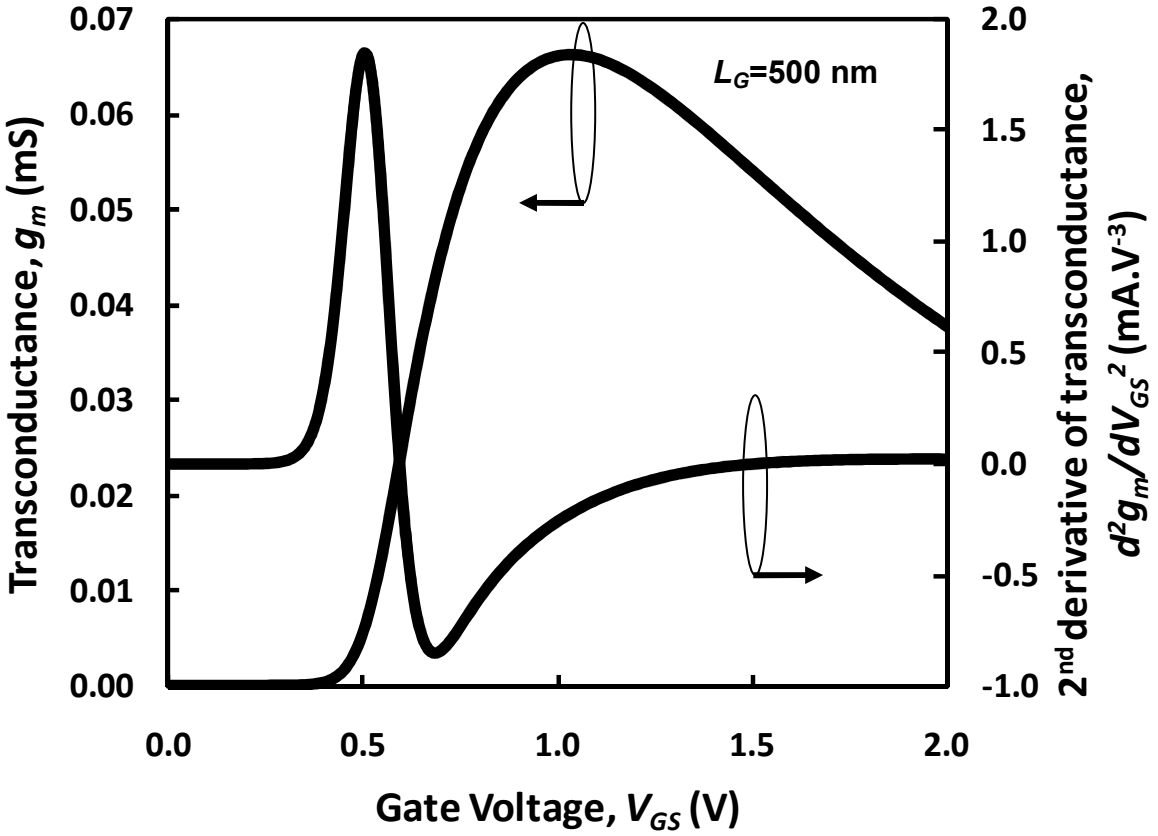

Fig. 6. Calculated g_m and $\delta^2 g_m/\delta V_{GS}^2$ as functions of V_{GS}-V_{TH}. The semi-empirical MOSFET model is calibrated with measured parameters. A θ_2 of 0.3 V^{-2} is required to match the shape of the calculated characteristics with the measured one.

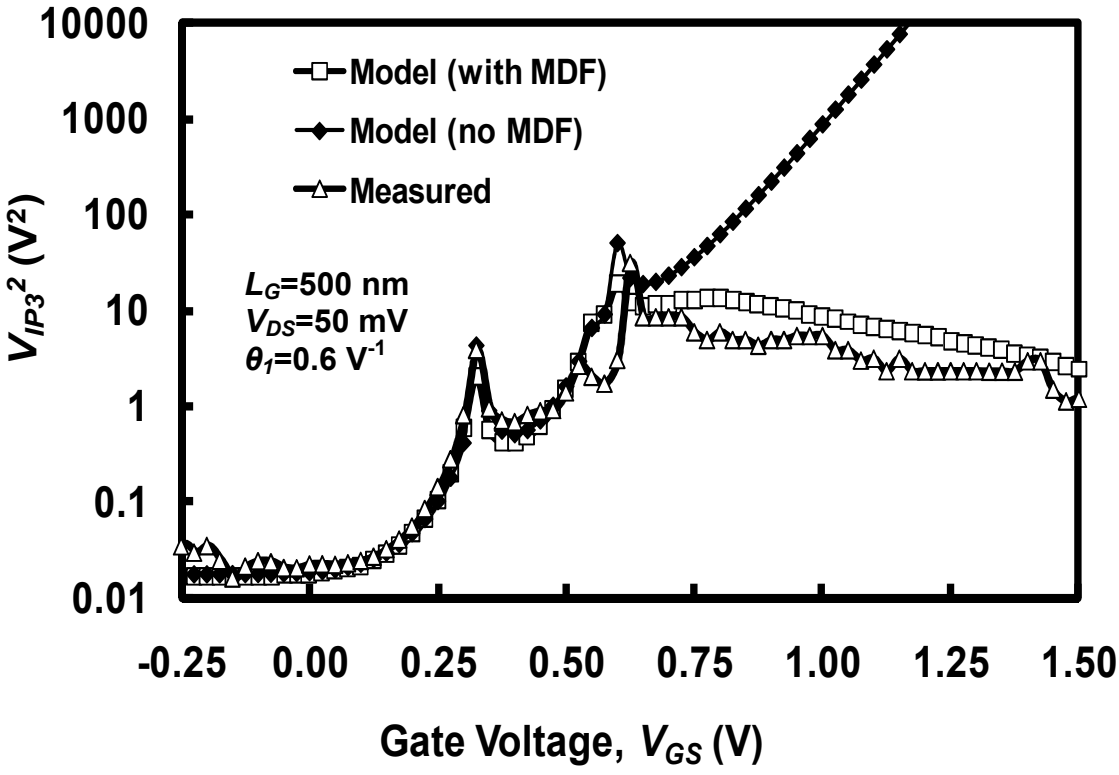

Fig. 7. A comparison of measured V_{IP3}^2 characteristics and calculated V_{IP3}^2 characteristics with θ_2=0.28 V^{-2} and θ_2=0 V^{-2}. There is a match between the calculated V_{IP3}^2 and measured V_{IP3}^2 only when θ_2 is tuned to the measured value.

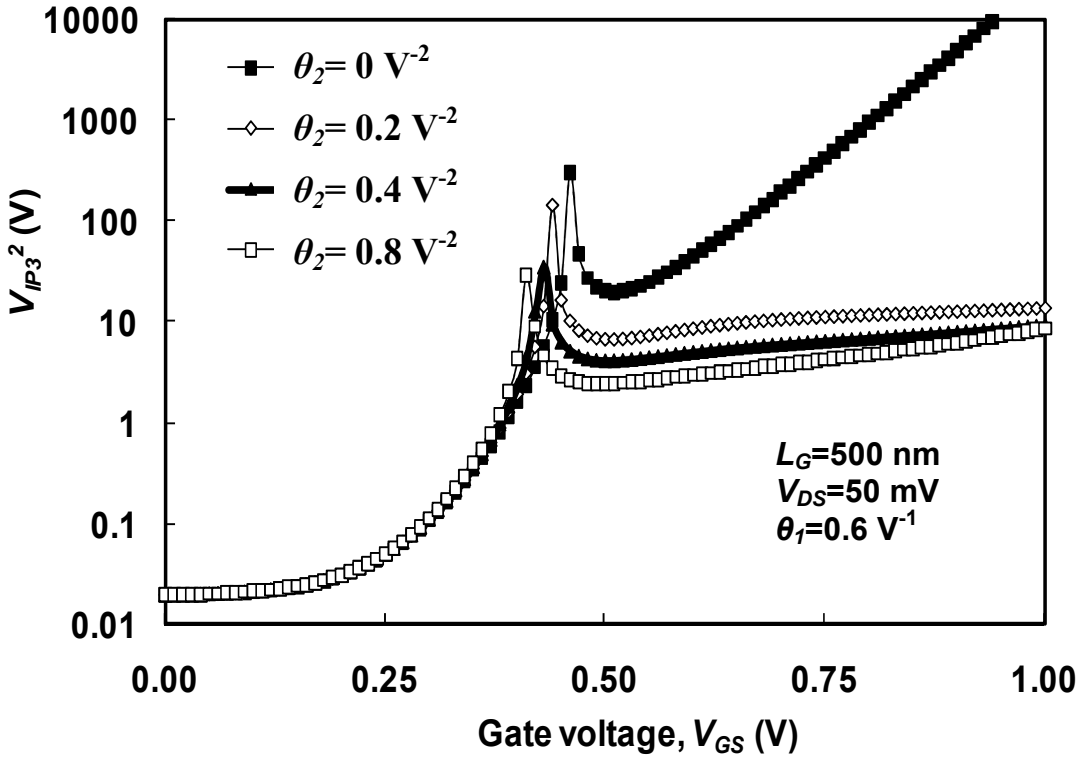

Fig. 8. The calculated V_{IP3}^2 characteristics shown as functions of θ_2. V_{IP3}^2 reduces significantly as θ_2 increases. The linearity can be overestimated without taking θ_2 into account.

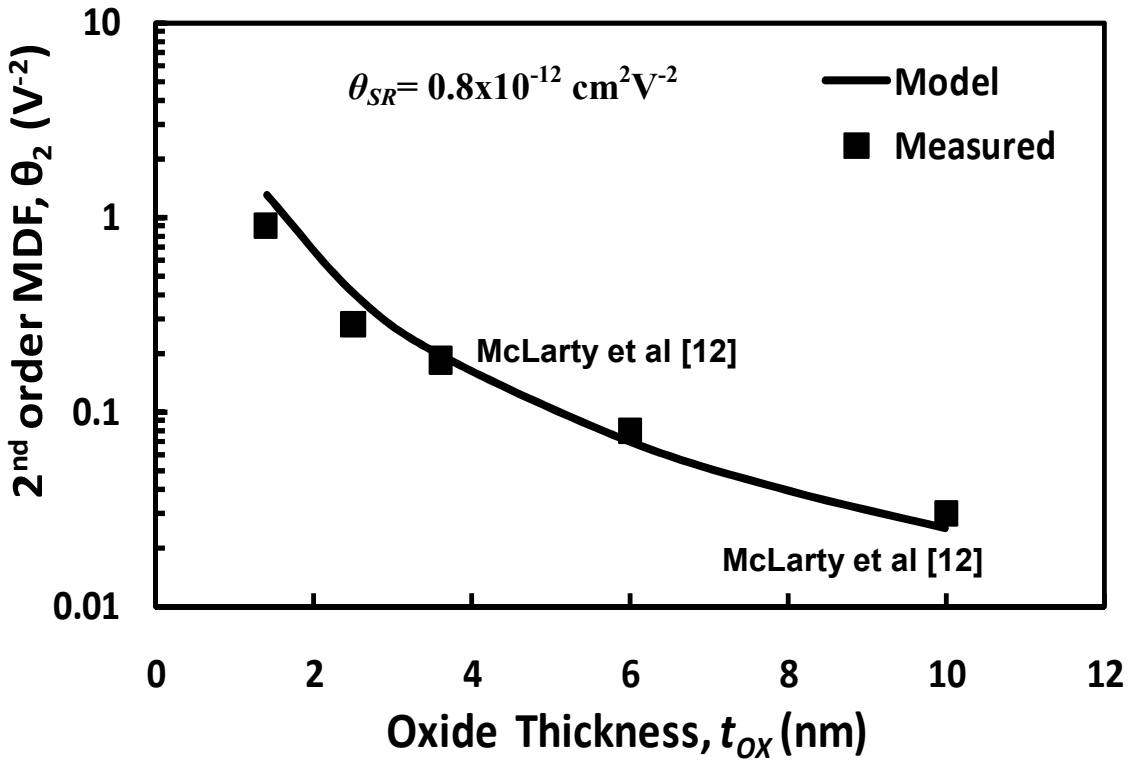

Fig. 9. The calculated and measured θ_2 values shown as functions of the oxide thickness. θ_2 increases as the oxide thickness is decreased and there is good matching between the calculated and measured data.

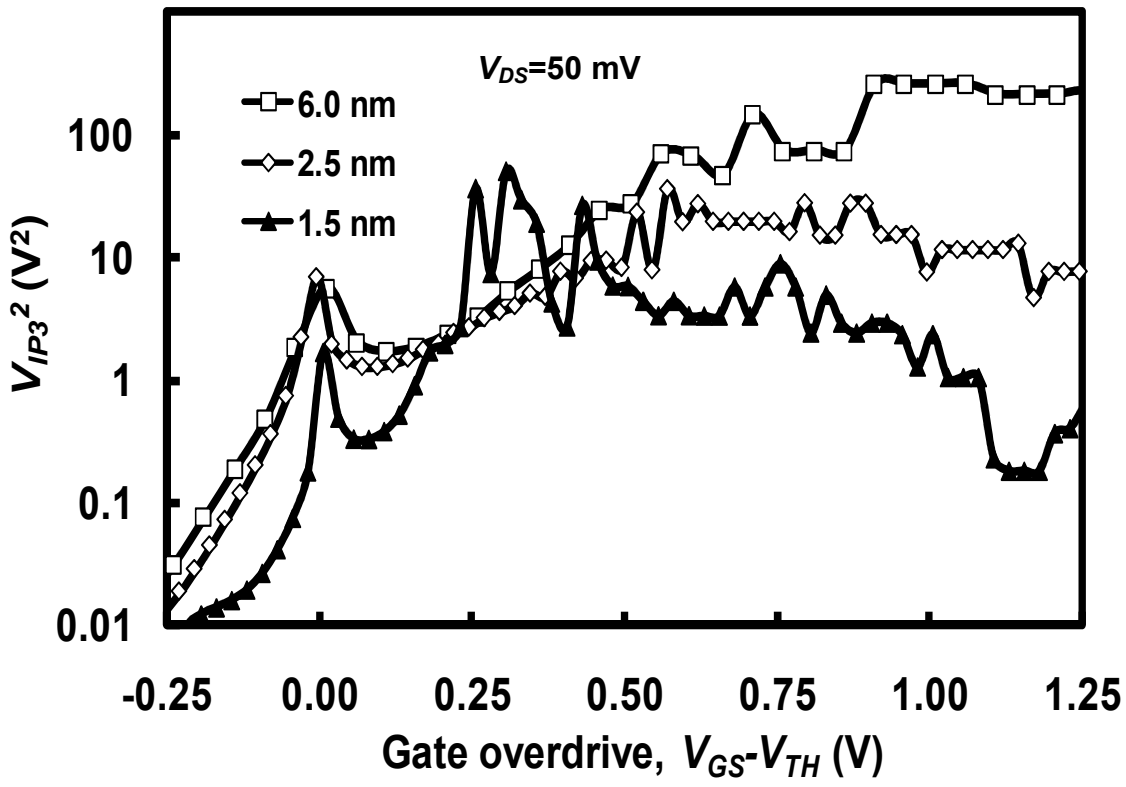

Fig. 10. V_{IP3}^2 as functions of V_{GS}-V_{TH} for 1.4 nm, 2.5 nm and 6 nm gate oxide MOSFETs. V_{IP3}^2 increases with the oxide thickness because θ_2 reduces as oxide thickness increases.

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