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PAPER

Linearity Improvement of VCO-Based ADC via Complementary Bias Voltage Control for IoT Devices

Pitchayapatchaya Srikram[1], Masayuki Ikebe[2] and Masato Motomura[3]

[1]Graduate School of Information Science and Technology, Hokkaido University
Kita14, Nishi 9, Sapporo 060-0814, Japan
[2]Research Center for Integrated Quantum Electronics, Hokkaido Univerisity
Kita13, Nishi 8, Sapporo 060-8628, Japan
[3]Institute of Innovative Research, Tokyo Institute of Technology
Tokyo 226-8502, Japan
E-mail: {srikram.pt,ikebe} @ist.hokudai.ac.jp, motomura@artic.iir.titech.ac.jp

Abstract **Ring-VCO (Voltage controlled oscillator)-based ADCs are suitable for the data acquisition in embedded sensors which are at the core of AI enabled IoT (Internet of Things) devices. Fundamentally, the ring-VCO can generate digital code by counting frequency from its voltage-controlled oscillation. However, the ring-VCO has some issues related to non-linearity and power dissipation due to the voltage-to-frequency (V-to-F) tuning characteristics. Particularly, for low power operation with low voltage supply, the linearity further degrades. This paper presents a complementary bias voltage control approach to attain a linear V-to-F characteristics with low-power dissipation. The novel voltage-to-current (V-to-I) conversion provides the linear bias current source and sink matching for current-starved inverter-based delay elements. Furthermore, the proposed circuit can be extended to optimize nonlinearity error by selecting an optimal transistor size. Simulation results with a 0.5V power supply circuit designed in TSMC 180nm CMOS technology shows that maximum nonlinearity error is below 0.24% for 4-stage and below 0.49% for 8-stage ring-VCO.**

Keywords: voltage-controlled oscillator (VCO), voltage-to-frequency linearity, low voltage supply, analog-to-digital converter (ADC)

1. Introduction

Recently there is an increased interest in smart devices and that has resulted in development of embedded sensing applications for healthcare, home automation and transportation. The smart sensors used in the IoT devices, rely on energy provided by batteries or energy harvesters, and connect billions of edge devices in the multidisciplinary paradigm via wireless communication. Additionally, IoT devices are expected to have long operational lifetime. Ideal design objective when developing such sensor is to have ultra-low-power operation which is realized by using energy-efficient circuits for both communication and computing part [1]. For data acquisition, analog-to-digital converter (ADC) is indispensable, and is utilized in the pre-processing stage as analog interface circuits [2].

Continuous-time (CT) $\Delta\Sigma$ ADC has proven to be a great candidate for IoT edge devices [3]. Their advantageous properties include simplicity in circuit implementation by removing the sample/hold circuit with continuous sampling in each sampling period. Furthermore, this continuous sampling generates anti-aliasing characteristics, and it can even make analog prefilter dispensable. VCO based ADC belongs to the class of the CT $\Delta\Sigma$ ADC. Here, the counter performs continuous integrating pulse density in each sampling period while counting frequencies, and it reuses the phase condition of the VCO as the quantization error for the next conversion. Ring-VCO is important part of VCO-based ADC, and is composed of a chain of inverters or delay elements, where an analog input is continuously converted from voltage to frequency. In VCO based ADCs, power dissipation is an issue, because high frequency oscillation increases power dissi-

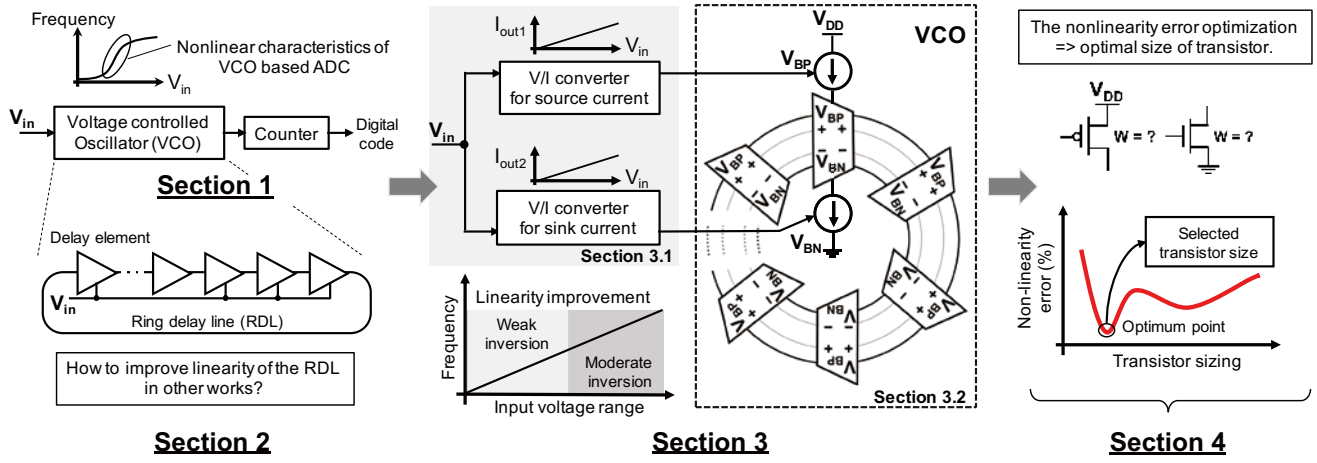

Fig. 1 Conceptual block diagram of complementary bias voltage controls for linearity in voltage-to-frequency tuning characteristic improvement in weak and moderate inversion input range

pation of its delay elements and counter. Also, the linear V-to-F tuning characteristic is important for VCO based ADC design because high linearity can directly achieve lower harmonic distortion with high signal-to-noise-ratio (SNR) and signal-to-noise-distortion-ratio (SNDR). However, V-to-F tuning gain of ring-VCO has some non-linearity. Particularly, for low power operation with low voltage supply, the linearity further degrades because of characteristics of delay elements. The current-starved delay element is well-known as part of the VCO for the frequency tuning by transconductance. Optimal current control in low-voltage supplies may improve the linearity of VCOs with low power operation. Therefore, this paper proposes a novel voltage-to-current (V/I) conversion to improve the linearity V-to-F tuning curve under low power supply condition. This provides for driving even-stage of the differential current-starved inverter-based ring-VCO-based ADC. Following are our main contributions:

- A low power supply and low leakage current V/I converters for current source/sink using a negative feedback transconductance amplifier without body-bias technique.
- Apply a linear bias current sink and source for control of ring-VCO instead of the current-mirrors with the large process variation in sub-threshold operation.
- Simplify the traditional methodology used for optimization of transistor sizing, and demonstrate its use in the proposed circuit.

Our paper is organized as follows (refer Fig. 1): In section 2 recent linearity improvement techniques are surveyed. Section 3 presents the complementary bias voltage control approach and its circuits for the V/I converters, including the current starved inverter. Section 4 discusses the analysis and simulation results for optimum design, including performance comparison with other related works. Section 5 concludes the paper.

2. Related Work

Watanabe et al. proposed basic VCO based ADC which consists of a ring-delay-line (RDL). The ADC circuits were implemented using digital circuit components only, and the supply voltage to the delay line were directly controlled [4]. Applying 2^n stage delay elements for RDL, pulse position in the RDL, which corresponds to phase of the oscillation, directly indicates additional lower bits. However, since the delay was controlled using supply voltage, non-linearity was not essentially improved.

For the delay control of RDL in the VCO, a current-starved inverter is used which is a well-known technique to realize delay elements with current tuning by transconductance. However, the delay elements rely on stacking MOSFETs, whose structure decrease the input voltage range, resulting in low voltage operation which is difficult. Therefore, the design of current-starved delay element at low nominal voltage supply degrades its linearity in the sub-threshold region. In contrast, linear operation of the current-starved inverter is challenging, which is related to both the linearity in V-to-F conversion and the wide tuning range of the current-starved inverter-based ring-VCO. In general, an inverter-based delay element suffers from non-linearity due to the relationship between input voltage (i.e., either the source voltage as its power supply voltage or gate voltage) and delay. Moreover, if a VCO-based ADC is designed as an open-loop archi-

tecture, where there is no need for DACs, it may result in poorer VCO linearity. Thus, the researchers developing VCO-based ADCs using open-loop architecture, in addition try to suppress non-linearity. Different approaches have been proposed both at an architecture level, for instance, digital calibration [5] and two identical pseudo- differential VCO-based ADCs, and a digital subtraction for distortion cancellation [6].

The proposed linearization technique at the circuit level tends to mitigate additional circuits, resulting in small area realization. With reference to circuit approach, researchers have been exploring several techniques based on the controllable current ring oscillator. The preliminary approaches can be categorized into two groups according to the modified inverter-based delay element and additional resistance. Voelker et al. presented a break-before-make delay cell using five-stacked series transistors [7]. The modified delay elements generate synchronized waveform using controller signal and are applicable to reduce the short current for linearity improvement. Alvero-Gonzalez et al. proposed a new delay model consisting of two parts. In their proposed design, first, the supply-controlled inverter-based delay element requires to increase voltage-controlled current source. Therefore, they use the second part which consists of two inverters-based delay elements as the buffer with nominal supply voltage in cascade. Additionally, their study has further discussed about obtaining higher linearity in V-to-F characteristic of their modified delay model depending on the highly linear input current. To generate the linear current, they apply additional resistance-based method, and this is beneficial for differential inverter-based delay elements and current-starved delay elements in nominal supply voltage.

The baseline case of a conventional linearity in voltage to frequency conversion of the current-starved VCO [9] is shown in Figure 2 (a), in which resistance is compensated linearly, and the current relates to the input voltage. However, this operation neglects input voltage range in the sub-threshold region. References [10, 11], discuss a compromised current control and voltage control technique which enables the current source in the ring oscillator to be linear. Figure 2 (b) shows the proportional resistive input circuit which converts the input voltage to current depending on bias current. Likewise, [14] played a role in determining non-linearity, which affects the current source flowing through the ring oscillator. Consequently, the linearized control mechanism has been established, as shown in Figure 2 (c), by subtracting proportional resistive voltage-to-current (V/I) conversion with complementary behavior. The bias current serves the current mirror technique, which may affect the phase noise performance of the current amplifier. AL-Tamimi et al. in contradiction to [14], pre-

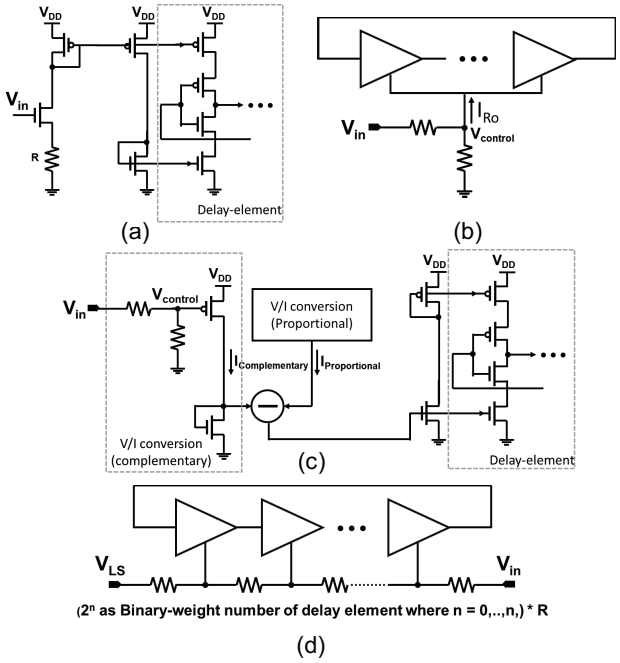

Fig. 2 Linearity improvement techniques: (a) Conventional voltage-to-current converter for current-starved inverter [9]. (b) Voltage-to-current converts by using resistance [10, 11] (c) Linearized current control mechanism [14] (d) Scaled resistance network at their input [15]

sented a binary pre-weighted resistor network connected between the input which adjusted the voltage at every delay element [15]. Figure 2 (d) shows the circuit where resistance values are increased exponentially based on the number of stages. Hence, the accumulating different time delay is attained to correct the amount of time delay, using which linearity transfer curve can be expanded over rail-to-rail input. This circuit suffered from a huge area and power consumption; however, the author presented an alternative pre-weighted resistance network called inverse R-2R [16]. The topology is equivalent to a prior art [15] with some modifications, which have resistors with constant value. Although this approach improved power consumption efficiency and the area when compared to prior art, but it increased the nonlinearity error percentages.

The studies of VCO-based ADC, as mentioned above, have been focused only on one established linearization techniques. Some of these researches suffer from the area and power consumption from a low-power device point of view, including high resistance value. Furthermore, those proposed techniques cannot operate at low power supply voltage. Our approach proposes a solution that can be categorized as circuit technique for linearity improvement of VCO at

low power supply voltage, and it is suitable for AI-enabled IoT devices.

3. Linearity Improvement under Ultra-Low Supply Voltage

The current-starved ring-VCO requires a highly linearized biasing current source for its supplement due to characteristically degrading linearity of the delay cell. By this motivation, many design strategies have been served with bias current based on the current-mirrored technique, as shown in Figure 2 (a) and (c). Considering the bias circuit is affected by various transistor operations with the input voltage, the nMOSFET could perform inefficiently in the triode region. In contrast, the pMOSFET maintains operation in the saturation region by the given high input voltage. At the same time, the nMOSFET requires to relieve the saturation region until input voltage is corresponding to supply voltage. Thus, the operation region of those transistors could influence the linearity of ring-VCO [17]. As far as we know, no approaches have been presented apart from serving the biased current source and sink realization using a current mirror.

With the demand for low-power (battery-operated) applications, there is a dilemma between linearity improvement and power dissipation reduction. Since input voltage in weak and moderate inversion leads to non-linear bias current. The bias current yields the drain current which is computed exponentially as shown in equation 1. [18].

$$I_D = I_{bias} = \frac{2K'W}{L} \cdot \left(\frac{nkT}{qe}\right)^2 \cdot exp\left(\frac{q(V_{GS}-V_{th})}{nkT}\right) \quad (1)$$

Where, n is the sub-threshold slope factor, k is the Boltzman constant, q is the electronic charge, V_{th} is the threshold voltage and T is the temperature.

To realize linearity improvement in low supply volage operation, we propose a novel complementary biasing voltage technique for current-starved inverter-based ring-VCO, as conceptually shown in the block diagram of Figure 1. The complementary bias voltage control scheme combines two V/I conversion circuits for the current source and the current sink; which is described in section 3.1 provides the required linear biased current matching. Furthermore, both V/I conversion circuits simultaneously convey input voltage (V_{in}), i.e., control voltage, to current, preventing nonidentical region operation. The proposed current-starved inverter-based delay element configuration is described in section 3.2. Besides, emphasizing linear bias current can improve the linearity of V-to-F characteristics. The bias input voltage of the V/I converter can minimize nonlinearity error by finding the optimal size of the transistor as described in section 4.

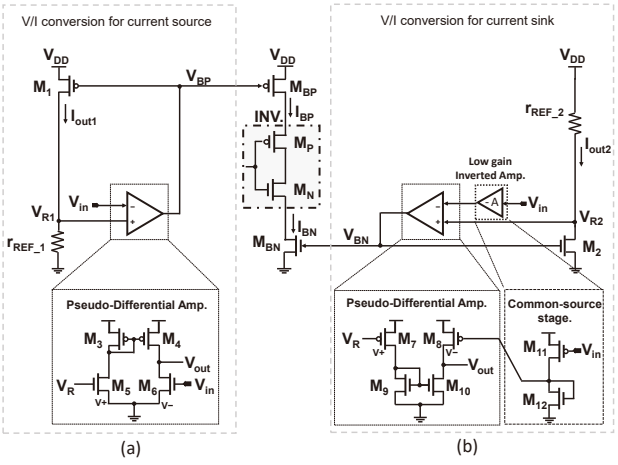

Fig. 3 Schematics for the proposed V/I, (a) Current source and (b) Current sink: Generate bias voltage and replica- biased current for current-starved inverter-based ring-VCO.

3.1 Proposed voltage-to-current (V/I) conversion

3.1.1 V/I conversion topology and its operation

The schematic of the proposed complementary bias voltage control approach is shown in Figure 3. The main circuit relies on a transconductance amplifier with a negative-feedback loop through a common-source amplifier. However, the ultra-low-power supply restricts circuit configuration due to its current flow limitation. We apply a pseudo-differential amplifier [19], which simplifies the number of transistors and minimizes power dissipation resulting in a low supply voltage operability. This configuration lacks a tail current; it degrades common-mode rejection ratio (CMRR) by increasing common-mode gain of pseudo-differential circuits. However, our designed amplifiers maintain negative common-mode gains (Maximum common-mode gain, Fig.3(a) $-8.7dB$, (b) $-30dB$). Thus, we can ignore the disadvantages of pseudo-differential amplifier.

In the source-side V/I converter (in Fig. 3(a)), negative feedback loop controls gate voltage of M_1 for leading V_{R1} is close to V_{in}. Thus V_{R1}, which is nearly equal to V_{in}, is given to r_{REF_1}; I_{out1} along with the V_{in} can flow. On the other hand, in the sink-side V/I converter (in Fig. 3(b)), since I_{out2} is based on the current of r_{REF_2} with $V_{DD} - V_{R2}$, if V_{R2} is along with V_{in}, will result in reverse current. Therefore, in our sink-side V/I converter design, we apply the low gain inverted amplifier with diode-connected nMOSFET for inverting V_{in}. The simulated result of absolute current (I_{out1}) with a corresponding current value of I_{out2} illustrated in Figure 4. Before adding the inverted amplifier, absolute current I_{out2} decreases

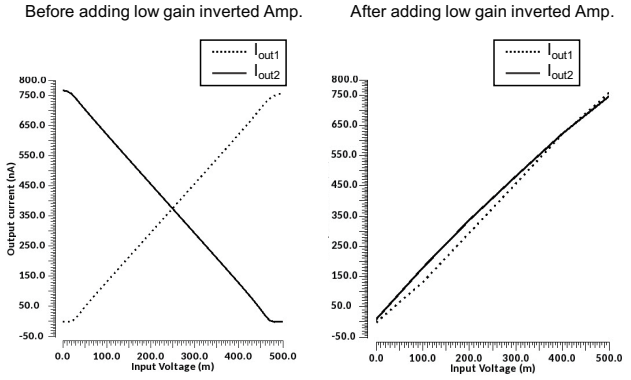

Fig. 4 Simulation results of output current characteristic of $I_{out1,2}$ variation over input voltage range, (a) Before adding low gain inverted Amp. and (b) After adding low gain inverted Amp.

along with the V_{in}. However, after inverting V_{in}, I_{out2} increases along with the V_{in} like I_{out1}. Proportional V_R can cause a linearized current through r_{REF}, which is approximately given by equation 2.

$$I_{out1,2} \approx \frac{V_{R1,2}}{r_{REF\_1,2}} \tag{2}$$

3.1.2 Relationship between V/I conversion and delay time

The operation of those V/I conversions can be performed as a replica-biasing circuit. The conceptual operation and the schematic of the single current-starved inverter are illustrated in Figure 3, V_{BP} and V_{BN}, which are generated by negative feedback networks, are given to current source (M_{BP}) and sink (M_{BN}). Consequently, I_{out1} (I_{out2}) behaves identical to current source. In particular, the values of both sides are similar; thus, the load of M_{BP} (M_{BN}) is the equivalent value of $r_{REF\_1,2}$. The inverter sandwiched between M_{BP} and M_{BN} behaves like a switch limiting the current I_{BP} (I_{BN}).

The propagation delay of the delay element is controlled low-to-high (T_{plh}) and high-to-low (T_{phl}) transient times by a current source and sink [21], and can be expressed as:

$$\begin{aligned} T_{plh} &= \frac{C_{eff}V_{trp}}{I_{BP}} \\ T_{phl} &= \frac{C_{eff}(V_{DD}-V_{trp})}{I_{BN}} \end{aligned} \tag{3}$$

Where C_{eff} is the effective load capacitance of each inverter stage, V_{DD} is the supply voltage, and V_{trp} is the inverter trip voltage.

Even though we apply the constraints of ultra-low-power supply, the proposed V/I conversion can provide sufficient current source and current sink (that is to say $I_{BP} = I_{BN}$=I_{Bias} (bias current)); and therefore, the overall propagation delays can nullify V_{trp}. This can be expressed as:

$$T_{plh} + T_{phl} = \frac{C_{eff}V_{DD}}{I_{Bias}} \tag{4}$$

Hence, the frequency oscillator of ring-VCO is inversely proportional to sum of propagation delay of n-stage delay elements and is given by

$$F_{osc} = \frac{I_{Bias}}{n(C_{eff}V_{DD})} \tag{5}$$

As far as near-threshold voltage condition is concerned, the current-starved inverter operates in the sub-threshold region; therefore, the delay is assumed by corresponding to the resistance of the current source (R_{BP}) and current sink (R_{BN}) along with the inverter ($R_{P,N}$) in each stage, which can be written [15] by

$$T_d \propto (R_{BP,BN} + R_{P,N}) * C_{eff} \tag{6}$$

In particular, the nonlinearity V-to-F tuning characteristics caused by bias current is inefficient in the sub-threshold operation. As mentioned earlier, the proposed V/I converters replicate their linearized output current as biasing current of current-starved delay elements, where the transistors are approximately equivalent as corresponding reference resistors $r_{REF\_1,2}$ which are constructed as feedback network. Therefore, this study has utilized this characteristic and the resistance behavior of current-starved delay element in sub-threshold operation to improve the linearity V-to-F tuning characteristics of ring-VCO.

3.2 Circuit configuration of ring-VCO

Figure 5 shows circuit configuration of the proposed ring-VCO, which consists of two main current-starved inverters and two auxiliary current-starved inverters which adjust delay time, as shown in Figure 5 (a). The current source (sink) of these inverters are controlled by the V/I converters explained in section 3.1. This configuration has efficient linearity in the current to frequency conversion rather than voltage [18].

Generally, in an inverter-based delay line, odd number of inverter stages are required. However, applying differential delay elements, oscillator can be implemented using even number of stages (in Fig.5 (b)). Furthermore, using differential outputs, the oscillator can increase phase resolution twice that of a single-ended delay element. When we apply 2^n stages to the ring-VCO, our ADC has the capability to add more lower bits by picking up the pulse edge position in the RDL, which is like Watanabe et al 's method [4].

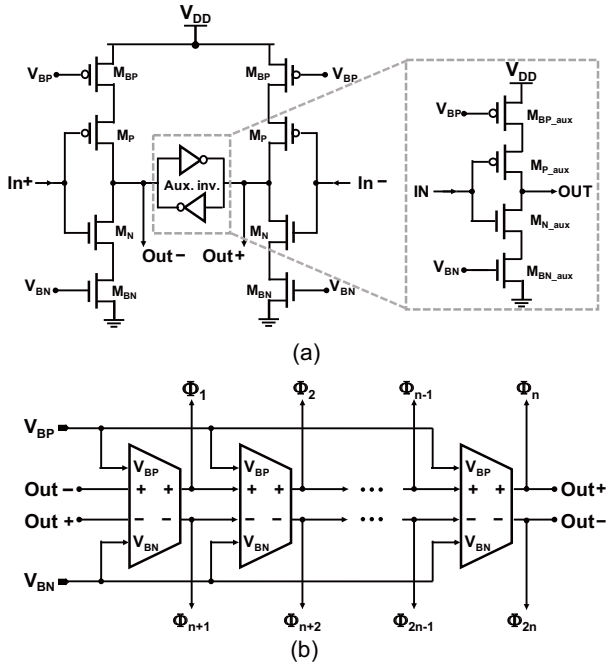

Fig. 5 Block diagram of proposed (a) Schematic of current-starved cross-coupled inverter-based delay element with the auxiliary inverters, (b) Even-stage pseudo-differential delay elements

4. Analysis and Simulation Results

The proposed current-starved ring-VCO-based ADC was designed and simulated to confirm the proposed conceptual linearity improvement. The implementation of this circuit is simulated in 180-nm TSMC process technology at 0.5 V supply voltage. Table 1 shows the optimal transistors sizing of the proposed V/I converters and differential delay elements, which are implemented in 4-stage and 8-stage configurations. The resistance reference of V/I converters has value of $r_{REF\_1} = 640$ KΩ and $r_{REF\_2} = 560$ KΩ in 4-stage, whereas in 8-stage, the resistance reference of V/I converters has value of $r_{REF\_1,2} = 640$ KΩ. The transistor sizing and resistor values are optimally determined by considering the minimal nonlinearity error, which can be observed from the linearity curve of V-to-F tuning characteristic results.

Cadence Spectre (Virtuoso® Design Environment version IC6.1.8-64b) was used to perform following experiments: (i) output waveform as a transient response, (ii) voltage-to-frequency tuning characteristics, (iii) curve fitting, (iv) frequency error curve, and (v) phase noise analysis. The simulation results is based on typical process corner and temperature of 27 ℃. Furthermore, a discussion on performance comparison with other techniques are provided in the following section.

Table 1 The size of the transistors

V/I conversion for current source		V/I conversion for current sink	
Transistor	W (um)	Transistor	W (um)
M_1	5.4	M_2	1.55/2.7†
M_3/M_4	2.7	$M_7/M_8/M_{11}$	2.7
M_5/M_6	0.33	$M_9/M_{10}/M_{12}$	0.33
Inverter		Aux. inverter	
Transistor	W (um)	Transistor	W (um)
M_{BP}	5.4	M_{BP_aux}	1.35
M_{BN}	1.55/2.7†	M_{BN_aux}	0.38/0.675†
M_P	1.76	M_{P_aux}	0.44
M_N	1.34	M_{N_aux}	0.335

†size of transistors for 8-stage

4.1 Transient analysis

The transient analysis was simulated to confirm corresponding output waveform of proposed ring-VCO as shown in Figure 6; here, Figure 6 (a) shows a single output waveform of 4-stage ring-VCO, and Figure 6 (b) shows the waveform of 8-stage ring-VCO for four different input voltage (V_{in}) as 0.1V, 0.2V, 0.3V, and 0.4V respectively.

The ring-VCO implemented by the proposed technique generates a square wave as the transient response with an the output rail-to-rail swing. Moreover, the waveform as the transient response is utilized to convert the delay time (Δt) to the oscillating frequency by tuning the input voltage (V_{in}), then those frequency values are transformed to the V-to-F tuning characteristic.

4.2 Linearity of V-to-F tuning characteristic

The linearity of the V-to-F tuning characteristics is directly related to INL (integral non-linearity) of VCO-based ADC and can represent how harmonic distortion limits obtaining high resolution of this ADC. Thereby, the V-to-F tuning curve of ring-VCO can be expressed using equation (7).

$$\begin{aligned} F_{vco} &= K_{vco}V_{in} + f_o \\ where, K_{vco} &= \frac{\delta f_{vco}}{\delta V_{in}} \end{aligned} \tag{7}$$

where, ring-VCO sensitivity or gain (K_{vco}) is defined as derivative of transfer function with respect to input signal, and the free-running frequency of ring-VCO is defined as f_o.

The V-to-F tuning characteristics of our proposed ring-VCO for 4-stage and 8-stage designs are presented in Figure 7 (a). The actual value refers to simulation result of output frequency over the input voltage range along with its ideal value, which fits the curve of actual value which is obtained from equation (7). The difference between the actual value and the

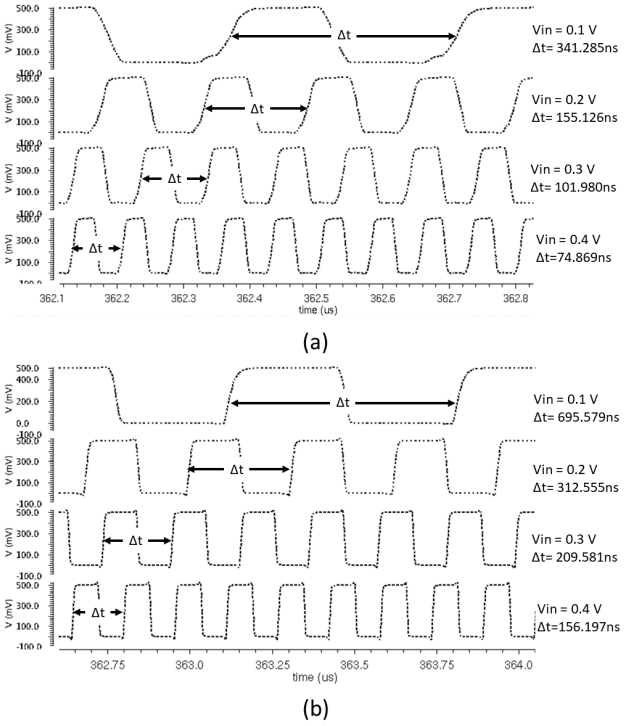

Fig. 6 Transient response of a single output phase, (a) 4-stage and (b) 8-stage ring-VCO with the coarse tuning input voltage range (0.1 -0.4 V)

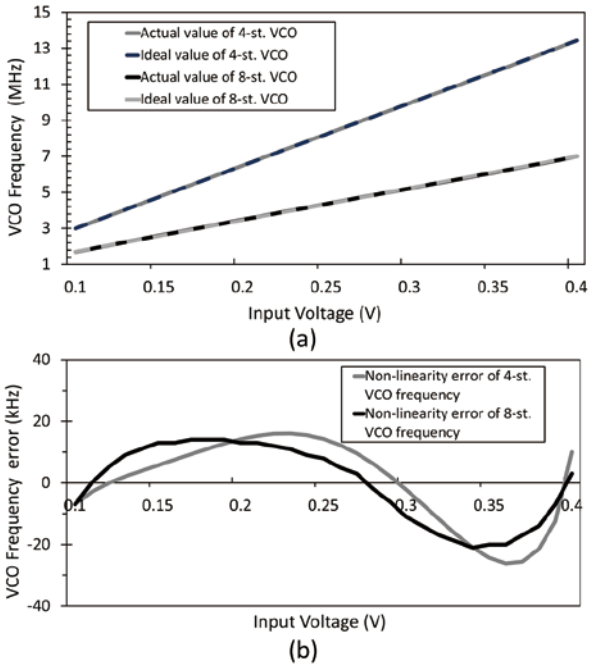

Fig. 7 Voltage-to-frequency tuning characteristic of (a) Proposed ring-VCO comparison of the actual and ideal value of 4-stage and 8-stage with (b) Its frequency error

ideal value is called frequency error, and it is shown in Figure 7 (b).

The linearity performance can be evaluated using the nonlinearity error or relative error given by equation (8). The maximum nonlinearity error of our proposed 4-stage and 8-stage ring-VCOs are 0.2325% and 0.4898%, respectively.

$$Nonlinearity\_error[\%] = \left\{ \frac{F_{actual} - F_{ideal}}{F_{ideal}} \right\} \times 100 \quad (8)$$

Additionally, linear regression coefficients is utilized to estimate the linearity V-to-F characteristics, i.e., for r-square, linearity error is 1-R^2 [19]. The output frequency and input value are normalized to calculate the linear regression coefficient. Our proposed 4-stage and 8-stage ring-VCO results are shown in Figure 8 (a) and Figure 8 (b), respectively. The linearity error computed by Python programming for our proposed ring VCOs are 0.004%.

As aforementioned, the transistor sizing, as listed in Table 1, is determined by optimized nonlinearity error. Even though a proper resistor value of proposed V/I converter can generate linear current source and sink matching, and actual fine tuning of the bias voltages control of current sink and source (V_{BP} and V_{BN}) are optimized by nonlinearity error adjusted using transistor sizing. Figure 9 shows bias voltage

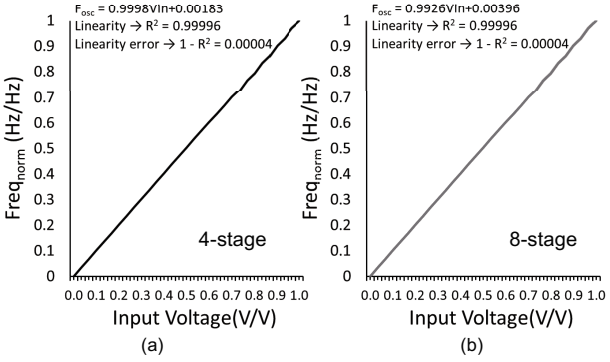

Fig. 8 Linearity error of V-to-F tuning characteristics, (a) Proposed 4-stage ring-VCO and (b) 8-stage ring-VCO determines normalized output frequency and normalized input voltage to compute the r-square value (R^2)

control variation on input voltage along with different transistor sizing. The transistor sizing of current sink from 1 to 4 of the $\beta 1$ value, referred to as the pMOS (M_1, M_{BP})-to-nMOS (M_2, M_{BN}) width ratio scenario over an input voltage of 4-stage ring-VCO.

Additionally, Figure 10 shows the results of $\beta 1$ value versus nonlinearity error. As far as nonlinearity error as defined in equation (8) was used to compare the frequency error among variations for the $\beta 1$ value,

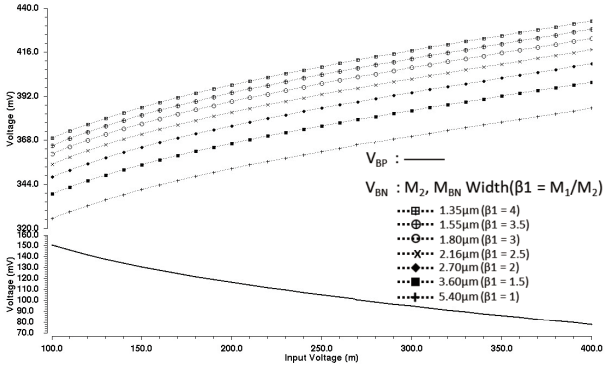

Fig. 9 Bias voltage control variation of V_{BP} (current source) and V_{BN} (current sink) on input voltage with difference transistor sizing M_2, M_{BN} (current sink) of 4-stage ring-VCO, and shows current source(M_1, M_{BP})-to-current sink width ratio by $\beta 1$

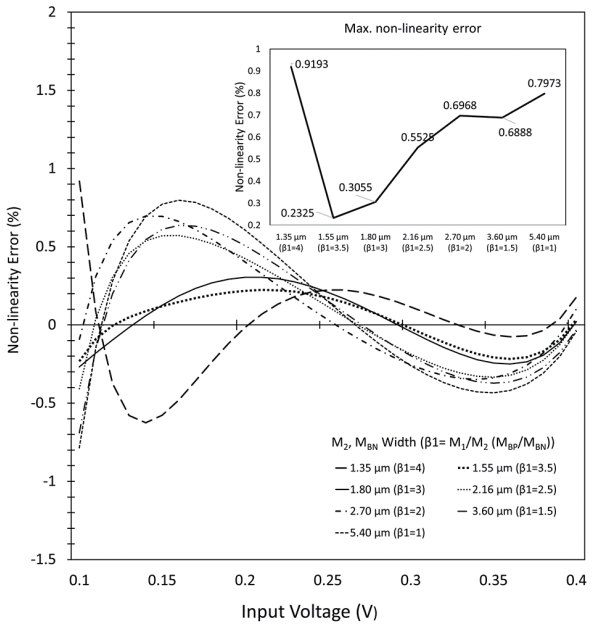

Fig. 10 Nonlinearity error variation of dependence output frequency on input voltage with difference transistor sizing M_2, M_{BN} (current sink) of 4-stage ring-VCO, and shows current source (M_1, M_{BP})-to-current sink width ratio by $\beta 1$, Besides, insert a graph to summarize maximum nonlinearity error versus those sizing design scenarios.

this metric indicates a significant difference error value between 4-stage and 8-stage ring-VCO. Therefore, the optimal nonlinearity error obtained from $\beta 1$ is 3.5, in which the current-source width is applied on 5.4 μm, and current-sink width is applied on 1.55 μm. This optimization method is analogous to implementing current sink on the 8-stage ring-VCO.

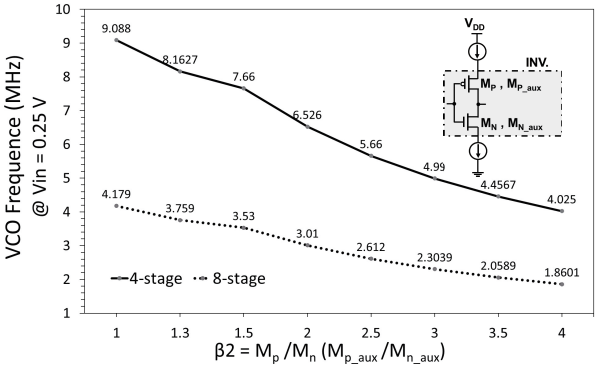

Fig. 11 The comparison between pMOS-to-nMOS width ratio by $\beta 2$ of 4-stage and 8-stage ring-VCO versus its output frequency at 0.25 input voltage

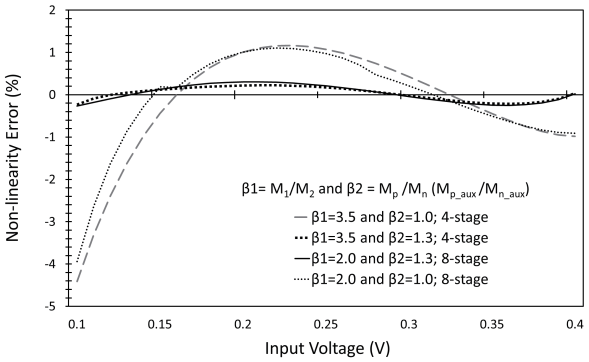

Fig. 12 The comparison of nonlinearity error variation of dependence output frequency on input voltage between 1 and 1.3 of pMOS-to-nMOS width ratio $\beta 2$ on 4-stage and 8-stage ring-VCO

Subsequently, the optimal inverter sizing selected by comparing output frequency over the variation of the $\beta 2$ referred to as the pMOS (M_p, M_{p_aux})-to-nMOS (M_n, M_{n_aux}) width ratio scenario of 4-stage and 8-stage ring-VCO at 0.25V input voltage is shown in Figure 11. In this case, the value of 0.25V is selected as input voltage by the majority of overlapping nonlinearity error from Figure 10, even though the minimized $\beta 2$ obtained the best output frequency; this ratio has a higher nonlinearity error. Therefore, inverter sizing is selected as one with high output frequency, and at the same time with minimum of the maximum nonlinearity error value. With this constraint $\beta 2$ ratio = 1.3 is the chosen value and this result is shown in Figure 12.

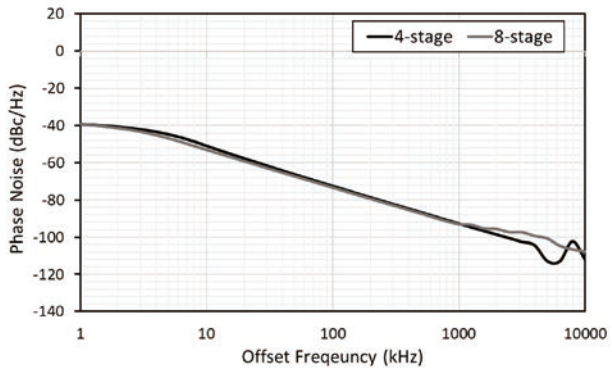

Fig. 13 Simulated phase noise results for proposed 4-stage and 8-stage ring-VCO

4.3 Phase noise analysis

The ring-VCO-based ADC produces non-ideal output waveforms in the time domain due to jitter corresponding to phase noise in the frequency domain. Phase noise is caused by active/passive-device noises such as thermal and flicker noise. The phase noise refers to the power ratio at a specified offset from the carrier frequency to the power at the center frequency. This study's phase noise simulation results from the periodic steady-state analysis (PSS) on Cadence simulation.

Figure 13 shown the simulated phase noise performance of the 4-stage ring-VCO with output phase noise of -50.85dBc/Hz, - 72.49dBc/Hz, and -92.71dBc/Hz at 10kHz, 100kHz, and 1MHz offset frequency, respectively. Concurrently, the simulation results showed phase noise performance of the 8-stage ring-VCO with output phase noise of -53.06dBc/Hz, -73.43dBc/Hz, and - 93.1dBc/Hz at 10kHz, 100kHz, and 1MHz offset frequency, respectively. The offset frequency of 1MHz is selected to compare the performance with results in other related works, as shown in Table 2.

Maezawa et al. has mentioned that offset frequency depends on -20dB/dec, and phase noise performance was difficult to evaluate under 1kHz [12]. In actual use of our ADC (e.g., 2kS/s), the effect of low frequency noise is important. Thus we evaluate the effect of phase noise within range from 1kHz to 1MHz. The phase noise in this range can be converted to RMS jitter [13]. The obtained RMS jitter are 0.77ns and 1.1 ns for 4-stage and 8-stage ring-VCO, respectively. Thus, The jitter yields in our ADC are ±2 LSB and ±3 LSB fluctuation at 10 bit ADC operation (V_{in} = 0.25V, 2kS/s sampling rate).

4.4 Comparisons with results in other work

The proposed ring-VCO is targeted for IoT devices which are to be operated at low supply voltage. Therefore, the nonlinearity error of our ring-VCO is compared with other works which may not feature in high frequency application. The related works are emphasized on low-frequency and low power consumption improvement in addition to bulk-driven technique. Thus, comparison with other works are categorized by dominant performance into three groups. The other works that reported the phase noise result are listed in Table 2, whereas Table 3 lists those related works that did not reveal the phase noise analysis. According to the ring-VCO, linearity improvement is crucial for evaluating the wide frequency tuning range and their stability in output waveform. Thus, in Table 2 the results of [14],[17], and [26] have been evaluated by power-frequency-turning-normalized (FOM_{TR}) [22] which is dominate the tuning range of ring-VCO as given by equation (9).

$$FOM_{TR} = 10\log\left[\left(\frac{F_{max}-F_{min}}{F_m}\right)^2 \frac{1}{P_{(mW)}}\right] - L\{F_m\} \tag{9}$$

where $L\{F_m\}$ is phase noise of an oscillator at F_m, F_{max} and F_{min} that are offset, the maximum and minimum frequency oscillator, respectively, and P is the total dissipated power.

The power dissipation in [17] is prominent in a ring-VCO that was operated over nominal supply voltage group. It is worth noting that its design methodology is based on conventional current-starved ring-VCO, whereas in [14], [15], and [16] they achieved the high linearity owing to a resultant resistance network at their inputs despite huge power consumption. However, the variation of linearity error in [14] depends on the process corner and temperature condition. The comparison with [14] and [17] reveals that resistance at their input could be limited by the phase noise performance and wide frequency tuning range as according to FOM_{TR}.

Alternately linearity improvement is achieved by bulk-driven control or bulk input technique, while operating at ultra-low supply voltage. The performance in [23], [24], and [25] obtained a lower tuning input range than other works. The nonlinearity error metrics of [23] and [24] were evaluated by their proposed metric, whereas other works in Table 2 and Table 3 were evaluated by equation (8). However, a limitation of the bulk-input voltage is that it may cause leakage current.

Ring-VCOs in low frequency application are ideally low power devices. Even though those works [27]-[29] are remarkable in low power consumption, their nonlinearity error could be significant. In [26], the phase

noise is dominant due to the inclusion of a phase detector and other reported ring-VCOs were not evaluated for their phase noise performance. In [30] ring-VCO is utilized in machine learning applications, and linearity is essential for this application. Thus, they propose to extend the input voltage range technique to preserve the ring-VCO in linear operating range and then obtain accurate digital code.

According to the comparison with other works, the proposed scheme satisfies with high linear V-to-F characteristics. The frequency tuning range and power consumption results reveal that our proposed ring-VCO based ADC can operate in low-power, and is suitable for low-frequency applications like AI-enabled IoT devices. Furthermore, 4-stage and 8-stage ring-VCO-based ADC achieve 12 bits and 13 bits of resolution with the sampling frequency of 1kS/s, respectively.

5. Conclusion

Linearized bias current plays an essential part in linearity improvement in ring-VCO-based ADC, relying on current-starved inverter-based delay elements. With the proposed V/I converter for the current source and sink, we find that the bias voltage control is practical to improve its linearity at 0.5 supply voltage. The evaluation results based on TSMC 180nm CMOS technology show that maximum nonlinearity error is below 0.24% for 4-stage ring-VCO and below 0.49% for 8-stage ring-VCO which were obtained from the optimized error based on adapted transistor sizing. Furthermore, the proposed ring-VCO consumes low power; therefore, it applies to a wide range of ring-VCO applications from IoT-device to machine learning.

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Table 2 Comparison of results and FOM_{TR} with other works

Ref.	Tech.	Supply	Input Range	Number of Stages	Error	Power (mW)	Output Freq.	Phase Noise	FOM_{TR}
	nm	V	V		%	mW	MHz	@1 MHz dBc/Hz	
Linearity improvement at nominal supply voltage									
[14]	180	1.8	0 - 1.8	5	0.02-0.9	0.965	574-852.8	-77‡	126
[17]	180	1.8	0.6 - 1.8	N/A	5.567	0.26	66-875	-82.25‡	146
Ring-VCO for Ultra-low-power application									
[26]	65	0.9	N/A	13	N/A	0.09	0.001 - 3	-106.8§ @0.43 MHz	161
Our proposed technique									
Our	180	0.5	0.1 - 0.4	4	0.24	0.000465	2.99 - 13.44	-92.71‡	146
				8	0.49	0.000466	1.69 - 7	-93.1‡	140

‡: Phase Noise from simulated results
§: Phase Noise from measurement results

Table 3 Comparison of results with other works

Ref.	Tech.	Supply	Input Range	Number of Stages	Error	Power	Output Freq.
	nm	V	V		%	mW	MHz
Linearity improvement at nominal supply voltage							
[15]	65	1	0 - 1.0	8	0.50	N/A	4000-5000†
[16]	65	1	0 - 1.0	8	1	3.1	340 - 460†
Linearity improvement by bulk-driven controlled technique							
[23]	N/A	0.6	-0.6 - 0	5	0.50	N/A	580 - 860
		0.2	-0.2 - 0		2.40		1 - 1.4†
[24]	130	0.25	0.1 - 0.15	3	0.33	0.000590	0.37- 0.55
[25]	130	0.4	0 - 0.1	N/A	2.7	0.078	0.033 - 3.48
Ring-VCO for ultra-low-power application							
[27]	180	0.5	0 - 0.5	N/A	N/A	0.000152	6.3 - 12.5†
[28]	180	0.4	0 - 0.4	N/A	N/A	0.000011	0.0000975 - 0.0004285
[29]	130	0.14	0.09-0.16	N/A	N/A	0.0000036	0.45-9.2
Our proposed circuits							
Our	180	0.5	0.1 - 0.4	4	0.24	0.000465	2.99 - 13.44
				8	0.49	0.000466	1.69 - 7

†: Approximate from frequency tuning curve

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Pitchayapatchaya Srikram received her B.Eng. degree from Silpakorn University, Thailand, in 2012, and her M.Eng. degree from Chulalongkorn University, Thailand, in 2016. She is currently pursuing her Ph.D. degree in information science and technologies at Hokkaido University, Japan, with support from the Royal Thai Government. She has been a Lecturer with Rajamangala University of Technology Thanyaburi (RMUTT), Thailand, since 2018. She worked on the asynchronous control circuits design methodology based on signal transition graphs. Her current research interests are delay elements, analog-to-digital converters, and mixed-signal circuits.

Masayuki Ikebe received his B.S., M.S., and Ph.D. degrees in electrical engineering from Hokkaido University, Sapporo, Japan, in 1995, 1997, and 2000, respectively. During 2000-2004, he worked for the Electronic Device Laboratory, Dai-Nippon Printing Corporation, Tokyo, Japan, was engaged in researching and developing wireless communication systems and image processing systems. Presently, he is a Professor and leads the Functional Communication Devices and Circuits Laboratory at the Research Center For Integrated Quantum Electronics (RCIQE), Hokkaido University. His current research interests are analog and mixed-signal IC design, emphasizing CMOS image sensors, THz imaging devices, and intelligent image processing systems. He is a member of IEICE and IEEE.

Masato Motomura received his B.S., M.S., and Ph.D. degrees in electrical engineering from Kyoto University, Kyoto, Japan, in 1985, 1987, and 1996, respectively. In 1987, he joined NEC Central Research Laboratories, Kawasaki, Japan, where he worked on various hardware architectures, including string search engines, multi-threaded on-chip parallel processors, embedded DRAM-field-programmable gate array (FPGA) hybrid systems, memory-based processors, and reconfigurable systems. From 2001 to 2008, he was with NEC Electronics, Kawasaki, where he led the research and business development of dynamically reconfigurable processor (DRP) that he invented. He was a Visiting Researcher with the MIT Laboratory for Computer Science, Cambridge, MA, USA, from 1991 to 1992. He has been a Professor with Hokkaido University, Sapporo, Japan, since 2011. He has been a Professor with the Tokyo Institute of Technology, Tokyo, since 2019, where he is leading the artificially intelligent computing (ArtIC) research unit. He is actively working on reconfigurable and parallel architectures for deep neural networks, machine learning, annealing machines, and intelligent computing in general. Dr. Motomura is a member of the Institute of Electronics, Information, and Communication Engineers (IEICE), Information Processing Society of Japan (IPSJ), and the Engineering Academy of Japan (EAJ). He was a recipient of the IEEE JSSC Annual Best Paper Award in 1992, the IPSJ Annual Best Paper Award in 1999, the IEICE Achievement Award in 2011, and the ISSCC Silkroad Award as the corresponding author in 2018.

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