01 Aug 2008

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Francesco de Paulis

Jun Fan
Missouri University of Science and Technology, jfan@mst.edu

Jay Diepenbrock

Samuel Connor

et. al. For a complete list of authors, see https://scholarsmine.mst.edu/ele_comeng_facwork/1703

Recommended Citation

F. de Paulis et al., "Link Path Design on a Block-by-Block Basis," *Proceedings of the 2008 IEEE International Symposium on Electromagnetic Compatibility, 2008*, Institute of Electrical and Electronics Engineers (IEEE), Aug 2008.
The definitive version is available at https://doi.org/10.1109/ISEMC.2008.4652140

Link Path Design on a Block-by-Block Basis

Francesco de Paulis, Jun Fan
EMCLab, Missouri University of Science and Technology, Rolla, MO, USA

Jay Diepenbrock, Bruce Archambeault, Samuel Connor
IBM Corporation, USA RTP, NC, USA

Antonio Orlandi
EMCLab, University of L'Aquila, L'Aquila, Italy

***Abstract*—In high-speed data communication systems, the complexity of link path between transmitters and receivers present a challenge for designers to maintain an acceptable bit error rate. An approach is presented in this paper to design the link path on a block-by-block basis. The unique advantage of this approach lies on the physics-based model of each block, which relates performance to geometry and makes design improvement and optimization possible. An example link path involving a backpanel is investigated using the approach. The via stubs and the dielectric materials in the backpanel are demonstrated to be critical factors for link performance in certain situations.**

***Keywords*—link path design, block-by-block approach, via stub, backpanel**

I. Introduction

In high-speed communication systems, link path may involve many different components. Understanding the effects of each component is critical to design a link path that can meet the design specifications with a minimum cost and a high reliability. For example, in a backpanel application, high-speed signals need to be transferred between daughter cards through backpanel traces. The link involves the traces, vias, connectors, and dielectric materials in both the daughter cards and the backpanel. All these parameters, to some extent, affect the performance of the entire link.

Due to cost considerations, through-hole vias are used in most of the PCB designs to move signals from one signal layer to another. Depending on the signal-layer locations, these vias can present open-ended stubs, which may significantly affect signal transmission depending on the stub length, the capacitive loading, and the signal bit rate. The via-stub effects are more significant in backpanels since they are normally much thicker than daughter cards.

The dielectric loss is another issue that the designer needs to take into account in the backplane designs where the length of the signal traces can reach tens of inches. Using an exotic dielectric material may improve the performance. But cost may increase significantly. Quantification of the performance improvement is obviously necessary to make an educated engineering decision.

This paper presents an approach to design a link path on a block-by-block basis. In other words, the entire link is divided into multiple blocks, and the contribution of each block to the overall link performance such as eye diagram is investigated. In this approach, every block can be modeled with a physics-based equivalent circuit if needed, so that geometry is linked with circuit elements. This unique feature can relate a geometrical parameter to its effects on the overall link performance; thus improvement and optimization become intuitive. The approach is described in Section II. Obtaining S-parameters from physics-based models in an example backpanel link is illustrated in Section III. Section IV presents results and discussions.

II. Link Path Analysis

To analyze a link path on a block-by-block basis, the entire link path is divided into multiple blocks, and frequency-domain S-parameters are obtained for each block so the blocks can be easily cascaded in the frequency domain. A link path analysis tool has been developed to generate an output waveform in the format of an eye diagram based on the frequency-domain S-parameters and an input waveform. The tool can calculate the eye openings and jitter to quantify the performance of a link. The high-level structure of the tool is shown in Fig. 1.

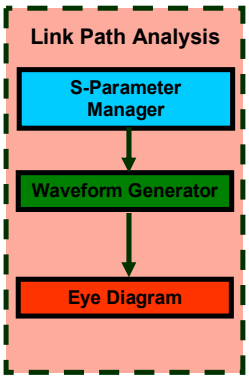

Figure 1. Block Diagram of the link path analysis tool.

A. S-Parameter Manager

The S-Parameter Manager allows the user to load up to 24 S-parameter data sets related to 2-port, 4-port, and 8-port

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systems. They are then cascaded together in the user defined sequence.

Once the S-parameter data are loaded, a necessary study is required to make sure that they are correct and that they represent properly the system under test. This is critical to ensure a meaningful result. The tool checks and enforces, if needed, the causality and passivity in the input data.

For causality, the tool extracts the causal imaginary part from the real part and compares it to the original imaginary part according to the procedure shown in [1]. When the two imaginary parts are overlapped, the input data can be considered causal. For passivity, the tool computes the 2-norm of the S-parameter matrix [2-3]. The data represent a passive system when the computed 2-norm is less than one.

Once these checks are passed the cascaded S-parameter can be exported, continuing the procedure for generating the eye diagram.

B. Waveform Generator

The Waveform Generator constructs a time domain waveform characterized by several basic parameters such as data rate, rise/fall time, number of samples per bit, voltage logic levels. The user can specify the sequence of bits according to some predefined bit patterns commonly used in different types of links such as K28.5+, D21.5, CJTPAT, PRBS, etc.

In order to have a more physical waveform, a procedure enforcing continuity of the first derivative has been used. Once an ideal trapezoidal waveform is generated, a low-pass filter is applied to remove the very high frequency components of the spectrum Therefore the signal shape does not have sharp transitions while going from high to low and low to high logic state.

Two additional features allow the user to emulate some "real" input signals often seen in a practical design: pre-emphasis and driver jitter. The pre-emphasis can be set to increase the magnitude of the high frequency components of the signal in order to balance the higher link path losses at high frequencies. The driver jitter can be added to the input signal, emulating noise effects that can be present inside the driver.

The Waveform Generator gives a wide flexibility for creating a waveform; this helps matching the emulated waveform as well as possible with the real one from an IC driver.

C. Eye Diagram Generator

The input waveform is first transformed to the frequency domain using the Fast Fourier Transform, and then multiplied with the cascaded S-parameters to generate the frequency domain output waveform. This frequency-domain output waveform is further transformed back to the time domain. An eye diagram is then generated by overlapping the bits together.

The eye diagram parameters such as eye width, eye height and peak-to-peak jitter are computed. These parameters quantify the overall link performance.

III. AN EXAMPLE BACKPANEL LINK PATH

The S-parameters of each block can be obtained from a physics-based model. This can be better explained by looking at an example backpanel link path. The entire link connects two daughter cards through a backpanel. More specifically, it starts with a microstrip trace on the first daughter card, continues with a via in the first daughter card, a backpanel connector pair, a backpanel via, a backpanel stripline, a second backpanel via, a second backpanel connector pair, a via in the second daughter card, and ends with a microstrip line on the second daughter card. Fig. 2 shows the block diagram of this link, neglecting the daughter card vias and the backpanel connector pair for simplicity.

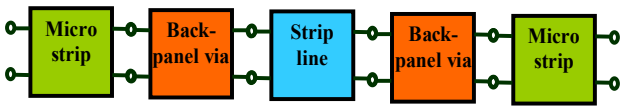


Figure 2. Block diagram of the example backpanel link.

The microstrip lines on the daughter cards are 5 inches long with a 50Ω characteristic impedance. The stripline in the backpanel is 18 inches long. Its characteristic impedance is also 50Ω. These traces can be well modeled with transmission lines; therefore, the following discussions will mainly focus on the backpanel via modeling.

The stack-up of the backpanel is shown in Fig. 3. The dimensions of the board are 20″ by 16″. All the dielectric layers are assumed to be FR-4 with a dielectric constant of 4.0, and a loss tangent of 0.02.

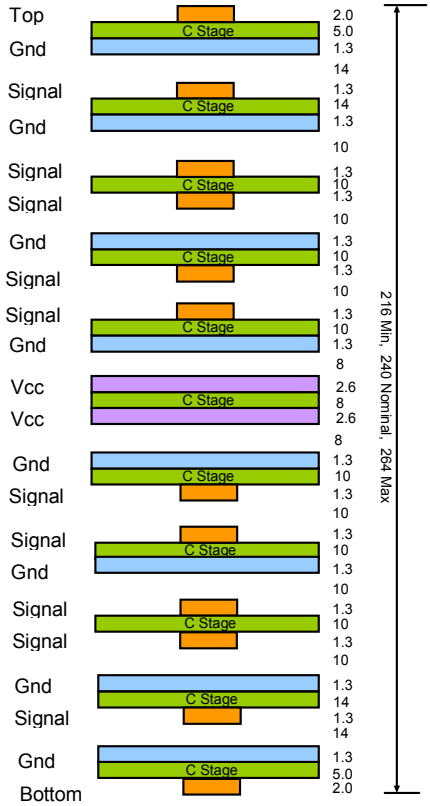


Figure 3. Backpanel stack-up.

A. Design Cases

Three different via transition designs in the backpanel, as illustrated in Fig. 4, are investigated:

1. the backpanel stripline is on S1 and the backpanel vias are through-hole vias;
2. the backpanel stripline is on S10 and the backpanel vias are through-hole vias;
3. the backpanel stripline is on S1 and the backpanel vias are blind vias.

In addition, one more design using a Rogers material in the backpanel is also studied:

4. the backpanel stripline is on S1, the backpanel vias are blind vias, and the backpanel material is a Rogers material with a low loss tangent (dielectric constant 3.8, loss tangent 0.008).

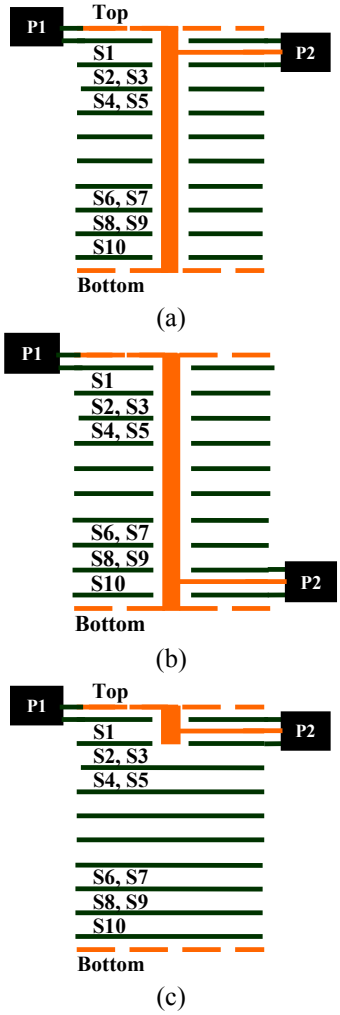


Figure 4. Design cases under investigation: (a) case 1; (b) case 2; and (c) cases 3 and 4.

Fig. 5 shows the $|S_{21}|$ of the daughter card microstrip traces, as well as the backpanel stripline trace with the two different dielectric materials. The data shown in Fig. 5 come from VNA measurements.

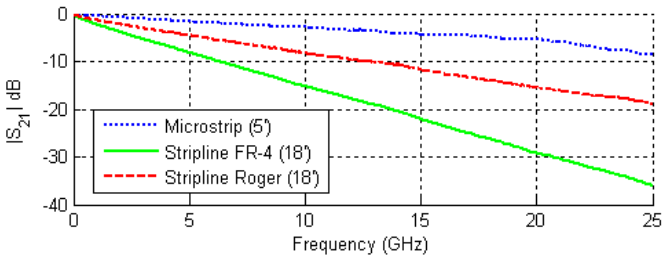


Figure 5. The $|S_{21}|$ for the microstrip and stripline traces.

B. Backpanel Via Modeling

Every signal via shown in Fig. 4 is accompanied with two closely spaced ground vias, as shown in Fig. 6. The diameter of the vias is 23mils, and the diameter of the antipads is 48 mils.

The backpanel via geometry is modeled using a segmentation approach combined with a via-capacitance model and a plane-pair cavity model [4-5]. The entire backpanel geometry is divided into multiple blocks at the middle of every ground plane. Every block includes a pair of planes and portions of the signal and ground vias. The pair of the planes is modeled as a multi-port impedance matrix that is obtained using a cavity method [6], while the via portions are modeled with via-plane capacitances. Then, all the blocks are connected together by enforcing the current and voltage continuity conditions. The complete via circuit models are shown in Fig. 7.

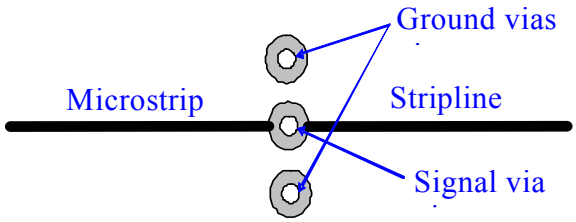


Figure 6. Top view showing the position of the signal and the two ground vias.

The circuit models for the backpanel vias are analyzed and their S-parameters are obtained. Fig. 8 shows the transfer function $|S_{21}|$. As clearly shown, a resonance at 6.5 GHz is present in Case 1. It is due to the open stub generated by the unused portion of the signal via between the layer S1 and the bottom layer. At the same frequency the phase of the S_{21} does not have a linear trend, showing a phase jump instead, as shown in Fig 9. This behavior is completely absent in the responses of the other designs where the stub length is very short.

After the S-parameters for the backpanel via blocks are obtained, the 5 S-parameter blocks in Fig. 2 are cascaded together through the S-Parameter Manager, as shown in Fig. 10. The overall $|S_{21}|$ results are shown in Fig. 11 for the four designs under investigation.

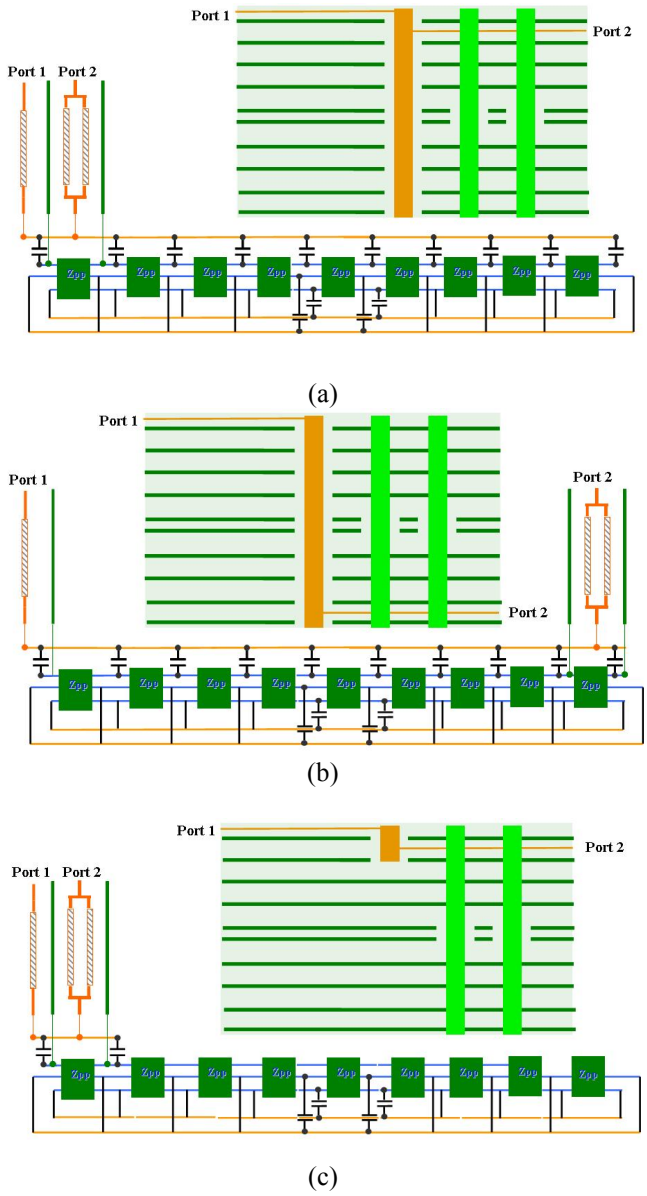


Figure 7. Geometry versus equivalent circuit model for: (a) Case 1; (b) Case 2; (c) Case 3 and 4.

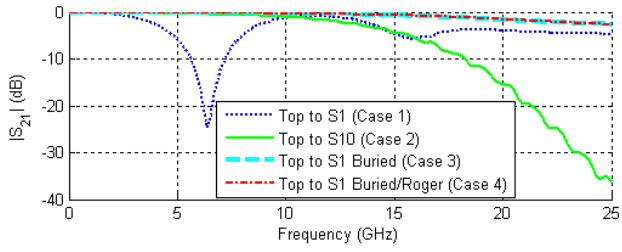


Figure 8. Magnitude of the transfer function S_{21} for each backpanel via block.

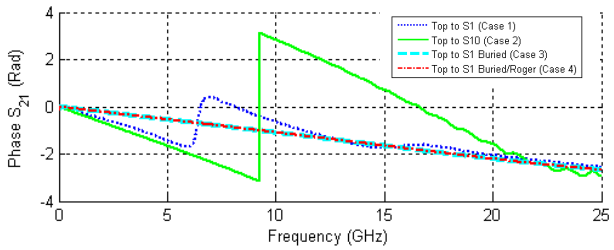


Figure 9. Phase of the transfer function S_{21} for each backpanel via block.

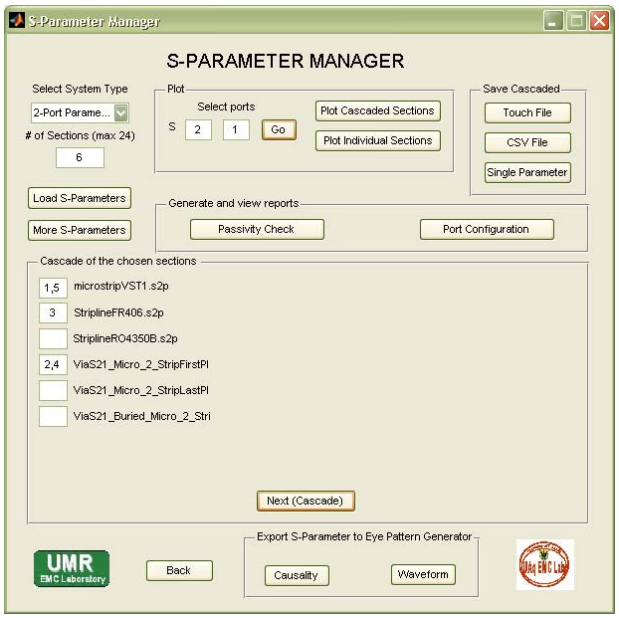


Figure 10.S-Parameter Manger window for cascading the S-parameters.

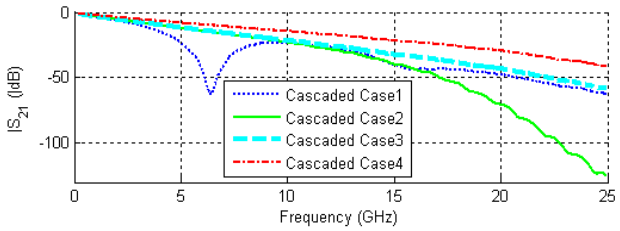


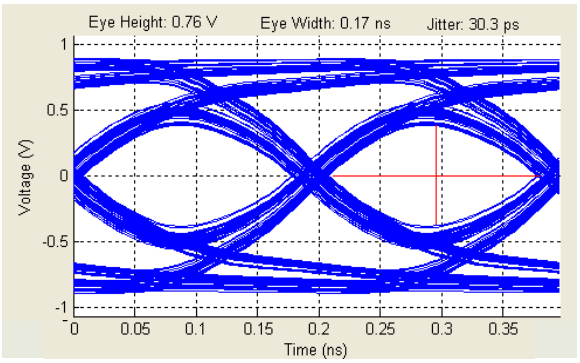
Figure 11. $|S_{21}|$ for the entire link path including traces.

IV. Link Performance

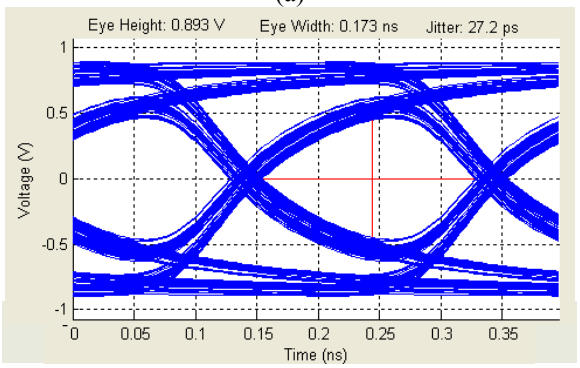
Eye diagrams are generated for the backpanel link path described in the previous section for a data rate of 5 Gb/s, and are shown in Fig. 12. Case 1 has the smallest eye opening and the largest jitter value due to the effect of the long stub present in the geometry, even though the fundamental frequency, 2.5GHz, is pretty far away from the stub resonance at approximately 6.5 GHz. In Case 2, signal flows through almost entire portion of the vias, leaving very short stubs. The performance of the entire link slightly improves over Case 1. Case 3 is further slightly better than Case 2, due to the fact that signal only travels a shorter distance in the vias and the stub length is very short as well. The best performance is

achieved in Case 4, where the dielectric loss is further reduced compared to Case 3.

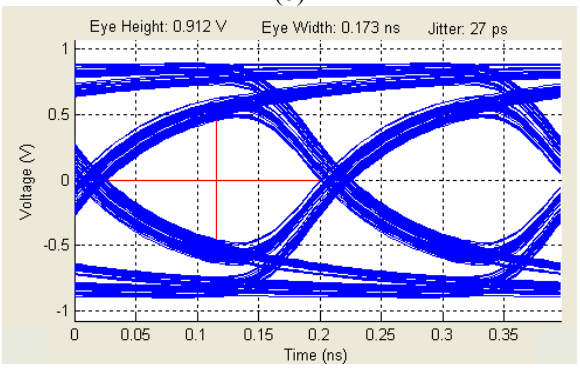
It's worth mentioning that Cases 3 and 4 do incur more cost by introducing non-conventional manufacturing processes such as blind via or via back-drilling, as well as non-conventional board materials. In this particular case, since the performance improvement in Cases 3 and 4 is only marginal compared to Case 2, the optimal design choice could be Case 2.



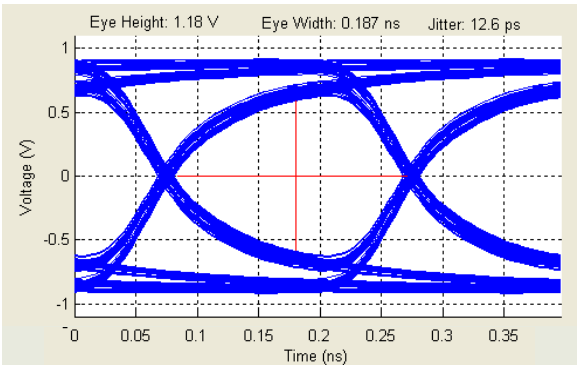
(a)



(b)



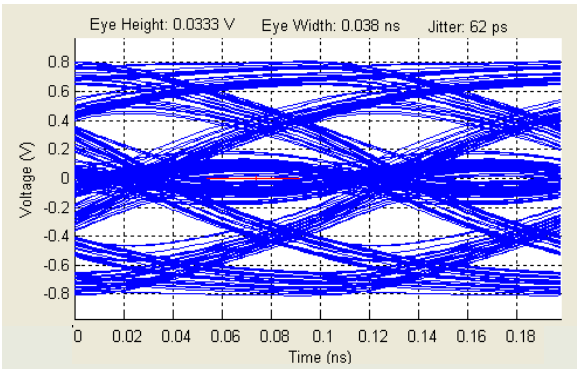
(c)



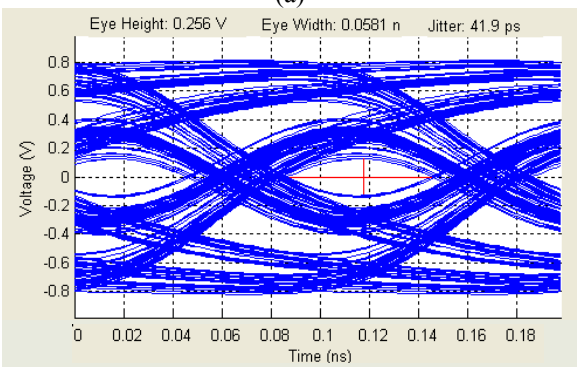
(d)

Figure 12: Eye diagrams at 5Gbps. (a) Case 1; (b) Case 2; (c) Case 3; (d) Case 4.

If the data rate increases to 10 Gb/s, the fundamental frequency increases to 5GHz, which is close to the stub resonance. A second set of the eye diagrams are simulated and they are shown in Fig. 13.



(a)



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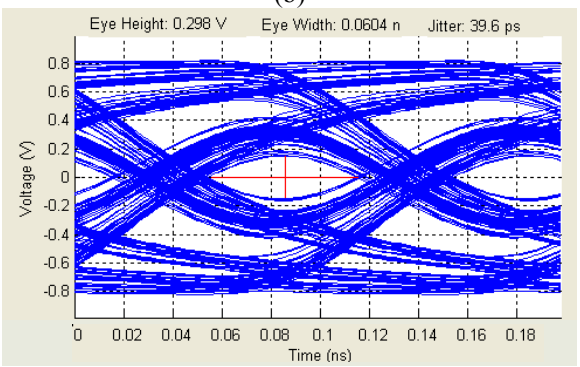

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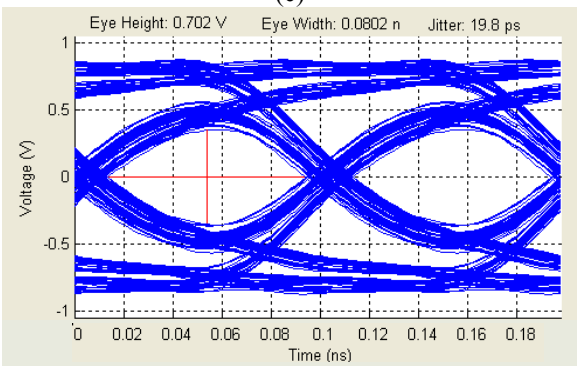

(d)

Figure 13: Eye diagrams at 10Gbps. (a) Case 1; (b) Case 2; (c) Case 3; (d) Case 4.

The eye openings at 10Gbps are much smaller than those at 5Gbps because the channel attenuation is higher at the higher frequencies. In Case 1, the eye is completely closed, demonstrating that the effects of the via stub is much more significant at this data rate. Cases 2 and 3 are slightly better due to the shorter stubs. The eye diagram in Case 4 is widely open, providing the best performance among the four designs. At this data rate, the best choice might be Case 4 even it is the most expensive solution, if the requirements for link performance are relatively high.

V. CONCLUSION

A design approach on a block-by-block basis is introduced in this paper to characterize high-speed link paths. It relates geometry to performance, and has been shown to be very efficient for investigating the effects of every block on the entire link performance.

Via stubs in a thick backpanel can cause unintentional resonances that could significantly affect the transmission of high-speed signals. The dielectric loss can also play an important role in determining the high-frequency link performance. Engineering compromises shall be carefully made with the considerations of cost, performance, manufacturing easement, etc.

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