INVITED PAPER

Lithography and Other Patterning Techniques for Future Electronics

As integrated circuits continue to go smaller, laying down circuit patterns on semiconductor material becomes more expensive and new techniques are needed.

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ABSTRACT | For all technologies, from flint arrowheads to DNA microarrays, patterning the functional material is crucial. For semiconductor integrated circuits (ICs), it is even more critical than for most technologies because enormous benefits accrue to going smaller, notably higher speed and much less energy consumed per computing function. The consensus is that ICs will continue to be manufactured until at least the "22 nm node" (the linewidth of an equal line-space pattern). Most patterning of ICs takes place on the wafer in two steps: a) lithography, the patterning of a resist film on top of the functional material; and b) transferring the resist pattern into the functional material, usually by etching. Here we concentrate on lithography. Optics has continued to be the chosen lithographic route despite its continually forecast demise. A combination of 193-nm radiation, immersion optics, and computer-intensive resolution enhancement technology will probably be used for the 45- and 32-nm nodes. Optical lithography usually requires that we first make a mask and then project the mask pattern onto a resist-coated wafer. Making a qualified mask, although originally dismissed as a "support technology," now represents a significant fraction of the total cost of patterning an IC largely because of the measures needed to push resolution so far beyond the normal limit of optical resolution. Thus, although optics has demonstrated features well below 22 nm, it is not clear that optics will be the most economical in this range; nanometer-scale mechanical printing is a strong contender, extreme ultraviolet is still the official front runner, and electron beam lithography, which has demonstrated minimum features less than 10 nm wide, continues to be developed both for mask making and for directly writing on the wafer (also known as "maskless lithography"). Going from laboratory demonstration to manufacturing technology is enormously expensive (> $1 billion) and for good reason. Just in terms of data rate (mask pattern to resist pattern), today's exposure tools achieve about 10 Tb/s at an allowable error rate of about 1/h; this data rate will double with each generation. In addition, the edge placement precision required will soon be 30 parts per billion. There are so many opportunities for unacceptable performance that making the right decision goes far beyond understanding the underlying physical principles. But the benefits of continuing to be able to manufacture electronics at the 22-nm node and beyond appear to justify the investment, and there is no shortage of ideas on how to accomplish this.

KEYWORDS | Electron beam lithography; imprint lithography; ion beam lithography; laser beam lithography; lithography; nanofabrication; nanoimprint; nanotechnology; patterning; phase separation; photolithography; self-assembly

I. DRIVING FORCES IN PATTERNING

In the past 40 years, the minimum dimension of integrated circuits (ICs) has been shrinking at a rate of 30% smaller feature size every three years, following the so-called Moore's law. The International Technology Roadmap for Semiconductors (ITRS), an industrial consensus of future technology largely based on Moore's law, is a ~100 page document that suggests that features of complementary metal–oxide–semiconductor (MOS) circuitry will continue to shrink down to at least the "22 nm node" [38]. At that node, the half of the center-to-center (pitch) of first level of interconnect is 22 nm and the width of the resist feature for the gate electrode is 15 nm; the etched gate electrode is even smaller, about 9 nm (Fig. 1).

Manuscript received April 18, 2007; revised October 2, 2007. This work was supported by the DARPA Advanced Lithography Program.
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Digital Object Identifier: 10.1109/JPROC.2007.911853

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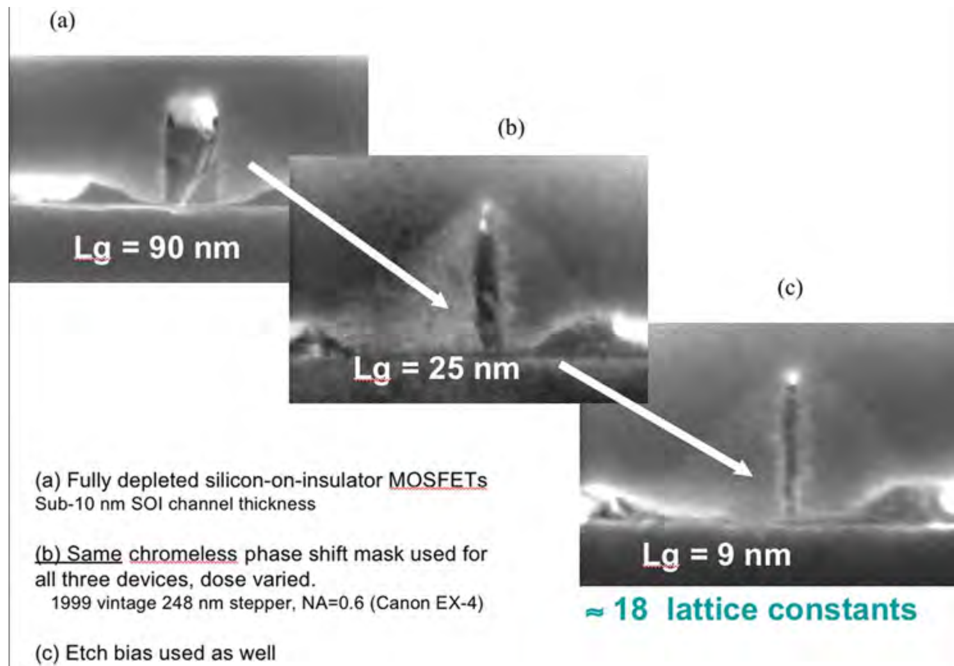


Fig. 1. ***Experimental example of results achieved with a combination of phase-shifting mask imaging and etch slimming showing gate lengths down to 9 nm [17]. (a) Fully depleted silicon-on-isulator (SOI) MOS field-effect transistors (FETs) with sub-10-nm SOI channel thickness. (b) Same chromeless phase-shift mask used for all three devices, dose varied. A 1999 vintage 248-nm stepper, NA = 0.6 Canon (EX-4). (c) Etch bias used as well.***

There is very good reason for this continued drive to shrink dimensions. Until recently, scaling down all linear dimensions L along with applied voltages led to a proportionate increase in speed and a reduction in energy per computing function to L [3]. Although the former advantage is the most frequently touted, the latter is probably the more significant; even more so as electronics increasingly will be hand-carried.

Although the classical scaling laws [1], [74], [75] may not apply quantitatively as we continue to scale down dimensions, it appears that we will get more computing per unit time and per unit energy. Scaling to 22 nm will bring advantages in terms of energy per computing function as well as speed.

There may be other ways to reduce power per computing function. For example, just about all transistors operate by modulating the height of a thermal barrier. Thence it follows that to change the current tenfold at room temperature, the change in voltage applied to the control electrode must be at least 60 mV; in current jargon we say that we need 60 mV/decade [2]. But as we scale down dimensions we must also scale down signal and supply voltages to avoid breakdown. Thus, at finer dimensions, the current in transistors that are "off" will become appreciable and will increase the dissipated power. Some newer devices operate on different principles and may well not suffer this problem. These and other exotic devices (e.g., spintronics [3]) and strategies [e.g., three-dimensional (3-D) integrated circuitry and quantum computing[1]] are being pursued and are described elsewhere as well as in separate papers in this issue.

But even with these exotic devices and structures, the power and speed advantages of scaling down dimensions remain and compel us to invest in appropriate patterning technologies. At least one prominent speaker (Shahidi, IBM) claims that the limit to system performance is directly related to density [9] and thus the limit to system performance is set by the technology to generate and replicate dense patterns.

II. BRIEF HISTORY OF SEMICONDUCTOR IC PATTERNING

In the early 1960s, the first integrated circuits were patterned by *contact lithography*, which places a mask directly on top of the resist. The masks were made in the following steps (Fig. 2).

i) Fabricate an enlarged layout (reticle) by cutting a thin plastic sheet ("Rubylith") that blocked blue light.
ii) Expose the reticle pattern at reduced magnification onto a master mask blank that comprised a glass or quartz substrate coated with 80-nm

[1]http://www.cs.caltech.edu/~westside/quantum-intro.html.

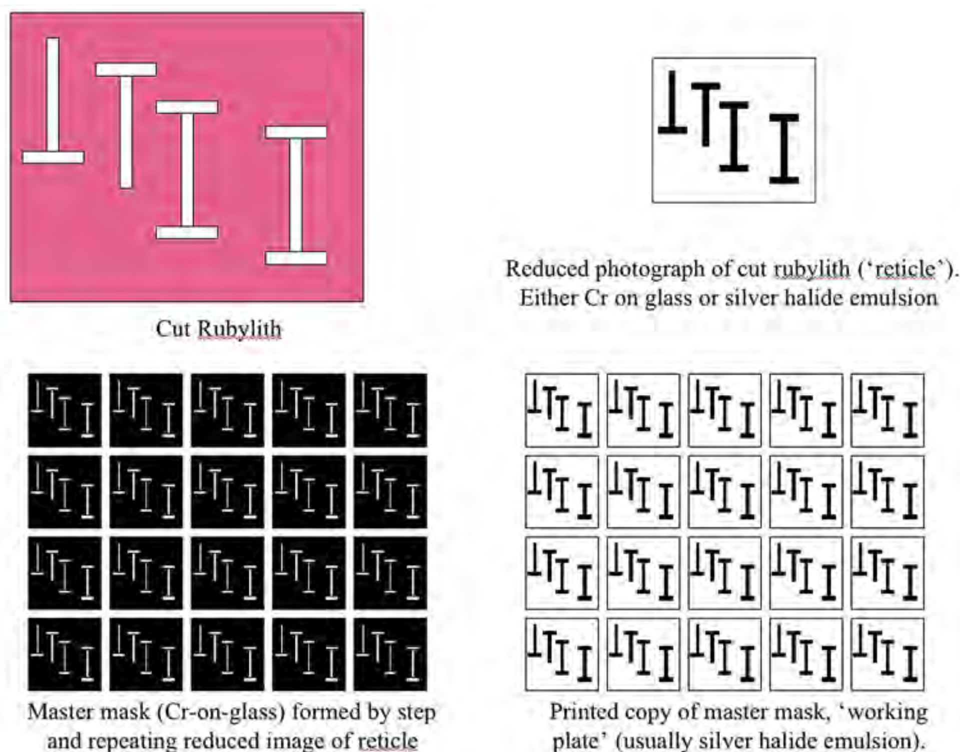


Fig. 2. ***Original process for making photolithographic masks.***

chromium and a photosensitive polymer (resist) on top.

iii) Repeat the exposure across the entire master plate to build up an array of identical patterns on the mask (the instrument used was, fairly obviously, referred to as a "step and repeat camera").

iv) Develop the resist and etch the chromium.

v) Replicate the master mask onto silver halide emulsion plates ("daughter masks" or "working plates").

The daughter masks were used to contact print the required pattern onto the resist film on the wafer. The underlying functional layer was then etched into the required pattern. The resolution of this process was typically > 10 μm set by the emulsion.

But the main problem of contact lithography is that the repeated contact of the masks while overlaying the image to the prior pattern layers gives rise to defects in the plate, thus lowering yield and limiting the economic scale of integration that could be achieved. So the next step, *proximity printing*, was developed in which there is a gap (of width g) between the emulsion and the wafer. The resulting resolution, discussed more fully in the next section, is on the order of $(g\lambda)^{1/2}$. So if $\lambda = 436$ nm (a strong line on a mercury arc), for a 2-μm blur resolution, the gap should be no more than 9 μm. As the whole wafer was exposed simultaneously, this placed a stringent requirement on the flatness of the wafer and limited the useful minimum features to larger than 5 μm.

To improve the lithography resolution and overlay while keeping no contact with the wafer, *projection printing lithography* tools were developed. The Perkin Elmer Micralign (circa 1973) was the first practical tool to employ focusing optics so that a sharp image of the pattern on the mask could expose the resist-coated wafer without mechanical contact, thus reducing defects and improving yield [10]. The 3x cost increase (to $100 000) in the cost of the tool was easily justified on grounds of yield alone. Furthermore, mask life was greatly improved, so there was no need to generate cheap emulsion working plates; and the master, with its higher resolution chromium pattern, could be used directly. To compensate for the lower contrast on the projected optical (aerial) image (see contact or proximity printing), the resist used was a positive, novolac-based resin with much higher contrast (gamma of about three; this is discussed more in Section III-D) and better resolution than original negative photoresists. The optics of the Micralign was an ingenious arrangement of three mirrors and one prism (Fig. 3) that allowed aberration-free imaging over a ring-shaped field of view 75 mm long by about 1 mm wide. Because the optics had unity magnification of +1 (i.e., an erect image), a simple mechanical scanning mechanism allowed complete

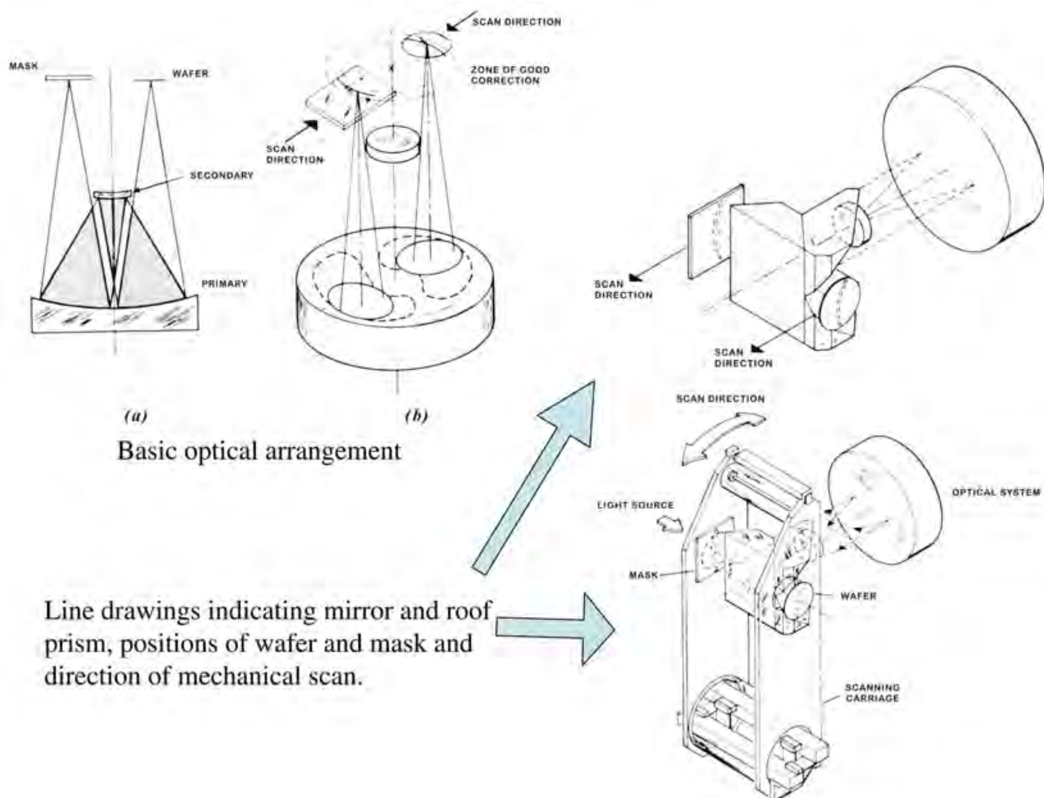


Fig. 3. *The first successful wafer exposure tool using optical projection; the Perkin–Elmer Micralign (1973). This tool made possible very large-scale integration by directly exposing the reticle onto the wafer with no mechanical contact to either image surface.*

exposure of a (3-in diameter) wafer in less than 1 min. This patterning technology offered the winning combination of sub-5-μm resolution with high yield and high throughput (1 wafer/min) and made possible the economical manufacturing of very large-scale integrated circuits.

Unfortunately, the optical arrangement of the Micralign limited the numerical aperture to 0.167, which, as described in the next section, limited the smallest features to about 2 or 3 μm. So the next family of exposure tools was to use a step and repeat camera, employing a multiple-element refractive lens, to expose the wafer directly from the reticle. The first such *steppers* were expensive ($500 000) and slow (1 wafer/3 min) but were able to generate 1.25-μm features, and by 1985 steppers had replaced the Micralign for the critical patterning steps. During the next 20-plus years, steppers evolved such that the numerical aperture is now close to one, the wavelength dropped from 436 to 193 nm (using an excimer laser), and the resist technology improved so that features can be less than 100 nm. A further advantage of the stepper was improved overlay because alignment could be carried out die-by-die or to some less dense array of marks to correct for the most serious spatial frequency components of distortion of the wafer. Moreover, the introduction of "chemically amplified" resist allows a throughput exceeding one 300-mm-diameter wafer per minute. The most recent versions employ scanning as well as stepping to cover the large fields of the ultra-large-scale interated (ULSI) chips, and liquid immersion optics are being introduced to reduce the wavelength [i.e., increase the numerical aperture (NA)] further so that the minimum features will be less than 50 nm. All this comes at a price; the current "scanners" have a price tag of about $30 000 000. But despite this high price, the cost per patterned minimum feature has continued to drop.

Needless to say, the *mask making* technology has also been changing. In the mid 1970s, Bell Labs introduced and licensed to ETEC Corporation commercial electron beam technology for mask making, and initially the product was the master masks used in the Micralign; only one patterning step was needed to generate the master. With the introduction of steppers, the e-beam tools were used to generate reticles (i.e., only one to four chip patterns) whose features were four to ten times those on the wafer. So, despite the shrinking of features on the wafer, the original electron beam tools continued to be used with little modification until about 2000. Since then, new generations of electron beam tools have been introduced, not simply because the wafer features have become smaller

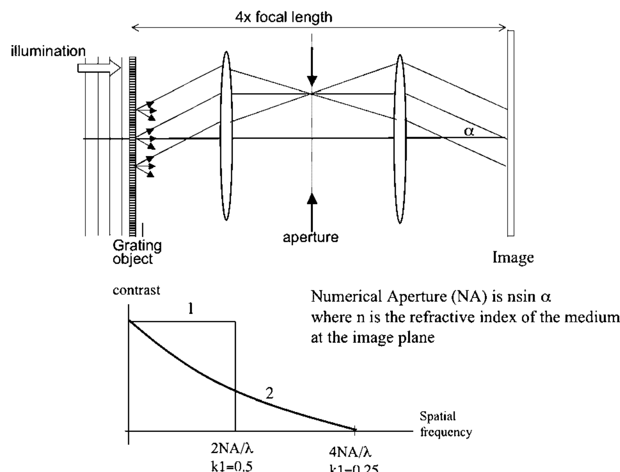


Fig. 4. ***Resolution limitation of optical imaging of a grating object; for simplicity the system is shown for unity magnification. Top diagram shows the object illuminated by a collimated monochromatic light at normal incidence. The aperture in the optics just allows the undiffracted and both first-order diffracted rays to reach the image plane, so the grating pattern is just resolved. This corresponds to curve 1 (lower diagram) of contrast versus spatial frequency that goes abruptly to zero when the spatial frequency reaches 2NA/1. If the illumination is tilted or arrives at many angles, then the aperture can accept the undiffracted rays and one of the first-order diffracted rays so spatial frequencies up to 4NA/λ can be resolved but at lower contrast (curve 2). In current parlance, we say that the feature size is $k_1\lambda/$NA.***

but also because of the need to put on the mask subresolution assist features (SRAFs) to enhance the fidelity of the projected image to the design layout (Fig. 8).

Less publicized has been the accompanying *inspection, metrology, and repair tools* needed to qualify the patterns on the reticles, masks, and wafers. Inspection for defects is mostly done with highly automated high-speed optical microscopy, whereas the scanning electron microscope (SEM) is used to measure the feature sizes. Inspection, repair, and metrology of the reticle have now become an appreciable factor in the total cost of patterning a wafer and must be considered when assessing the introduction of a new patterning technology.

III. PHOTOLITHOGRAPHY

A. Limit to Resolution Set by the Wavelength

If you focus an image of a point object using an aberration-free lens, the result will be an "Airy" disk of radius 0.61 $\lambda/\sin\alpha$, where λ is the wavelength (at the image) and α the convergence semi-angle at the image.[2] In light optics, this is frequently written as 0.61 $\lambda/nsin\alpha$, where *n* is the refractive index of the medium at the image, λ the free-space wavelength, and the quantity $nsin\alpha$ the *numerical aperture* (NA) of the lens. Lord Rayleigh suggested that the criterion for resolution of a microscope should be the radius of the Airy disk. That is, two (self-luminous) points separated by 0.61 λ/NA can just be resolved when using a perfect (i.e., aberration-free) lens. This criterion is often referred to, incorrectly, as the Rayleigh "limit," largely because is it is a practical limit for two points emitting radiation with no coherence between the pencil beams from the different points.

However, an IC pattern is very far from being a pair of points, and we can use many different kinds of illumination to achieve different levels of coherence between rays from neighboring points in the object. Often we use a (equal line-space) grating object for analyzing optical system performance. For example, if we illuminate coherently a grating object and project its image through a perfect lens system (Fig. 4 top), there will be two diffraction spots, as well as the undiffracted spot, at the aperture plane (assume that higher order spots will be outside the aperture) and so the resulting aerial image will be a periodic wave of unity (maximum) *contrast* defined by $(\mathrm{I_{max}} - \mathrm{I_{min}})/(\mathrm{I_{max}} + \mathrm{I_{min}})$. This value will hold as we shrink the grating (increase spatial frequency) until the diffraction spots go outside the aperture, at which point the contrast abruptly goes to zero. If the illumination is incoherent, usually realized by impinging over a solid angle up to 2π steradians, from an extended source, then the curve of contrast versus spatial frequency drops gradually with increasing spatial frequency (Fig. 4 bottom); note that the highest spatial frequency for which there is nonzero contrast is twice that of the corresponding value when coherent illumination is used.

In practice, the illumination is partially coherent, so the curves are somewhere between the two, but the trend of monotonically decreasing contrast for smaller features is usually true.

Thus, except for perfectly coherent illumination, there is no sharp criterion for resolution of the grating object, so today we replace the factor 0.61 with k1 for the minimum (half-pitch) feature that is resolved by the projection

[2]See any optics book. Also see [5].

system imaging into a resist film. As we shall see below, k1 depends on several factors and can be much less than 0.61. We should also point out that the optics of present-day scanners and steppers has become much more involved than those used in the Perkin–Elmer Micralign because of the need to cover large fields of view at high numerical apertures and with negligible aberrations; an example is shown in Fig. 5.

Proximity printing, in which a shadow of the mask pattern is cast onto the nearby resist film, is still used for noncritical patterns, and here the wavelength is still key. The nonsharpness of the edge of the shadow is caused not only by a noncollimated illumination but also by *Fresnel diffraction*. For collimated illumination, the Fresnel diffraction width is approximately $(\lambda g)^{1/2}$ where g is the gap between the object (mask) and image (resist film on wafer). Values of $g < 5\ \mu$m are difficult in practice because of nonflatness of the wafer; hence achieving submicrometer resolution with visible and ultraviolet wavelengths is also difficult. However for X-rays, ions, and electrons, this limitation is much less serious but, as described below, other factors limit the utility of proximity printing with these technologies.

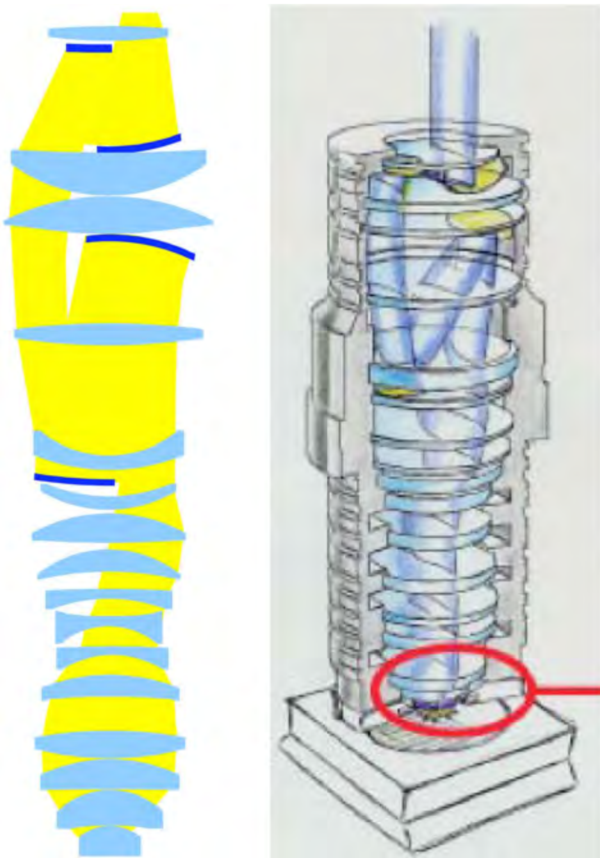


Fig. 5. ***Cutaway view showing an example of a design of projection optics for wafer exposure tools employing 193-nm immersion optics. Even with the use of mirrors, the design still features many different elements that must be fabricated and positioned to tolerances much less than the wavelength of the light. (Courtesy of ASML Corporation.)***

From the above, it is clear that lowering the wavelength is key to better resolution. Hence during the last 20 years, the industry has moved from 436–365 nm (two strong lines, *g* and *i*, of the mercury arc) to 248–193 nm (KrF and ArF excimer lasers). It is proving extremely difficult to go further. One reason is that a unique advantage of ultraviolet and visible wavelengths is the existence of "glass," or, more precisely, material that is transparent and mechanically rigid (usually fused silica in the case of ultraviolet wavelengths) for both the mask substrates and refractive lenses. An attempted move to 157 nm was aborted because the "glass" required, crystalline calcium fluoride, proved to have residual birefringence, which made it impractical. Obviously no equivalent of glass exists for electrons or ions, and this has proved a major difficulty in making the required masks, and nearly all electron- and ion-beam lithography is now "maskless."

X-rays (whose use is described more fully in a later section) present a more interesting case. There certainly exist materials that are transparent to the harder wavelengths (< 4 nm), and for many years X-ray proximity lithography was developed intensively. The difficulty was that for masks we need an opaque, patternable film (for which softer X-rays are desirable) on top of the transparent rigid substrate (for which harder are better), and finding the right combination of materials and wavelength proved uneconomical. A soft X-ray technology, now termed extreme ultraviolet lithography (EUVL), has been equally intensively developed over the last ten years; it uses both reflective masks and mirrors for focusing and has still to surpass 193-nm-based lithography in terms of overall performance. But it is still the favorite candidate of the industry for the 22-nm node, and the projected cost (per wafer exposure) of these tools easily exceeds that of 193-nm lithography (for which the capital tool cost is now more than \$30 million); this investment (more than \$1 billion so far) is a measure of importance of continuing to increase the density of ICs.

So although reducing wavelength is important, this is limited by the necessity for "glass," and so we have had to at least pause at 193 nm. To keep reducing the minimum features, the industry is pushing optical lithography well beyond the Rayleigh criterion. That is, k1 is well below 0.61. For example, the industry is now developing pilot production at the 45-nm node using 193-nm radiation. There are several developments that enabled this advance: better resist chemistry, imaginative optics, and the application of intensive computing.

B. Limitations to Speed and Resolution Set by Resists

Resists have to be sensitive to the imaging radiation, yield a sharp and faithful relief image on development, withstand the etching (or other pattern transfer) step, and

have some tolerance to variations in exposure level and development process. The *sensitivity* of a resist is usually quoted as the dose in millijoules per centimeter squared required to bring about the required response to the developer. Thus if we plot the thickness remaining after development versus $\log_{10}$ (exposure dose), we get curves for both negative (exposed areas insoluble in developer) and positive (Fig. 6). Usually, for a positive resist, the required dose is a bit above the minimum dose required to remove all the resist and similarly for a negative tone. The (mean) slope of the curve between full thickness and zero thickness is the *contrast* or *gamma* of the resist; a gamma of one means that we need a tenfold change in dose to go from full thickness to zero thickness; a gamma of two, only $10^{1/2}$ or about threefold; and so on. Clearly the higher the better (assuming we want a binary image). Early resists had a gamma of about one, and so the optical image at the wafer ("aerial image") had to have high contrast (i.e., $(I_{max} - I_{min})/(I_{max} + I_{min})$ close to unity) to compensate.

But as we have seen, such high contrast in the aerial image is not available for small features (high spatial frequency), so the resist chemists have come to the rescue of the optical physicists by providing resist with gamma values of ten or more and at the same time increasing speed. Fig. 6 (bottom) shows a representative curve of current resists corresponding to contrast values exceeding six; there is little to be gained by going higher. The chemistry used to bring this about is beyond the scope of this paper, but books by Levinson [5] and by Thompson *et al.* [4] are good introductions.

In the quest to improve the throughput of optical lithography, chemical techniques, notably chemical amplification [4], [5], have been developed in which the exposure gives rise to an acid that on subsequent heating catalyzes the desired chemical reaction. This has proved invaluable for features down to 65 nm, but it appears that at 45 nm, the diffusion of the acid is setting a limit to the sharpness of the features; it is not yet clear if this represents a fundamental limitation to the tradeoff between speed and resolution in optical lithography [28], [82]. For EUVL, the statistics of the exposure process due to the small number of exposing quanta and the variation in the number of acid molecules generated by each 13-nm photon may set a more fundamental limit [31].

C. Resolution Enhancement Technology (RET)

This takes many forms but the key idea is that in lithography, unlike microscopy, we know what image we are trying to project, so in principle we can determine the best distribution of amplitude and phase of the impinging wavefront to give the desired image (i.e., distribution of light intensity across the field of view). The term "wavefront engineering" was coined to describe this process. For low-resolution patterns (e.g., $k1 > 0.61$), the most effective technique is simply to use a mask pattern that is the same as the desired pattern on the wafer. For higher resolution patterns, we have already seen that the contrast

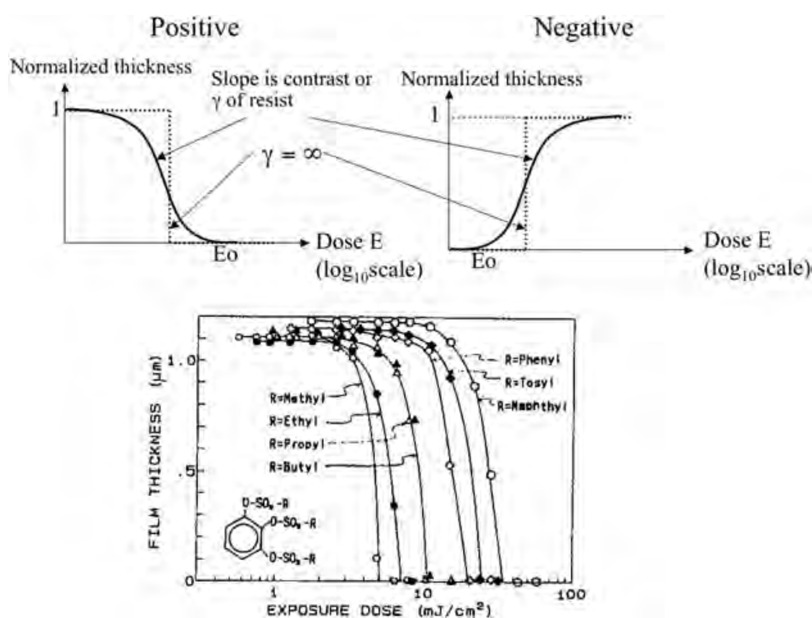


Fig. 6. ***Resist materials are often characterized by curves (top) of fractional thickness remaining after development (normalized) versus $\log_{10}$ (dose). Early resists had a contrast (gamma) of about one, so that a tenfold change in dose was needed to achieve a relief image of areas of full thickness and zero thickness. Current resists have gamma values exceeding six, so that the aerial image can be of much lower contrast (lower curve) [5].***

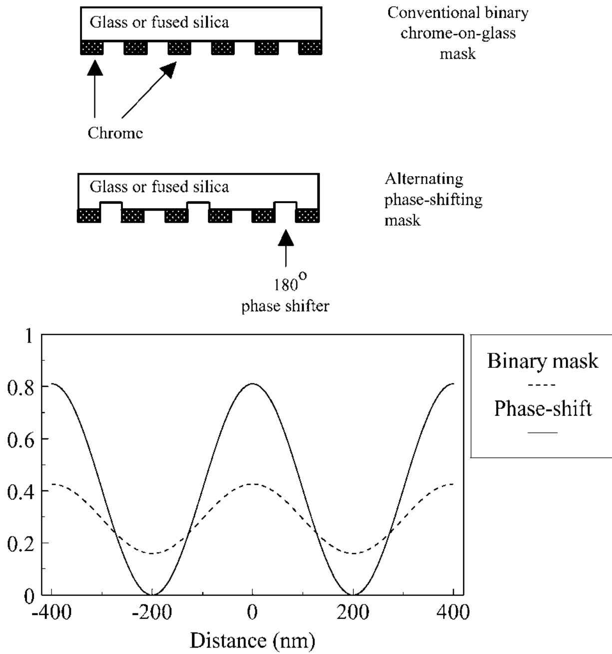


Fig. 7. *The alternating area PSM (M. D. Levenson, IEDM 1982) compared with the conventional binary mask. The resultant intensity curves show clearly the better contrast in the image of the PSM. This was probably the earliest example of treating the mask as a diffractive element rather than an object to be faithfully imaged.*

falls off as the lines and spaces shrink. One of the first wavefront engineering techniques was the *phase-shifting mask* [7], [11], [12] (Fig. 7) in which alternate clear features have a π phase change in the transmitted light so that they destructively interfere and give rise to a region of zero intensity between them, thus restoring contrast. This is very effective for line-space patterns but in general there were pattern topologies (e.g., the letter M) that made the application of alternating phase shifting challenging. There have been many variations on this original idea. Related to this is the technique of concentrating the illumination at certain angles *(tilted illumination)* so that contrast of the characteristic spatial frequency of a periodic mask pattern is maximized. One literal shortcoming of images for $k1 < 0.5$ is that the ends of lines become rounded and shortened, and this can often be compensated by making the mask pattern for a short line in the form of a "dogbone."

Such semiempirical techniques were effective for a time, but as features became smaller, k1 continued to drop and more and more effects due to nearby features (hence the term "proximity effects") became significant and there were more neighbors to take into consideration. The complexity of arriving at an acceptable mask pattern soon became a computational nightmare. This was exacerbated by the more complex physics that needs to be invoked for

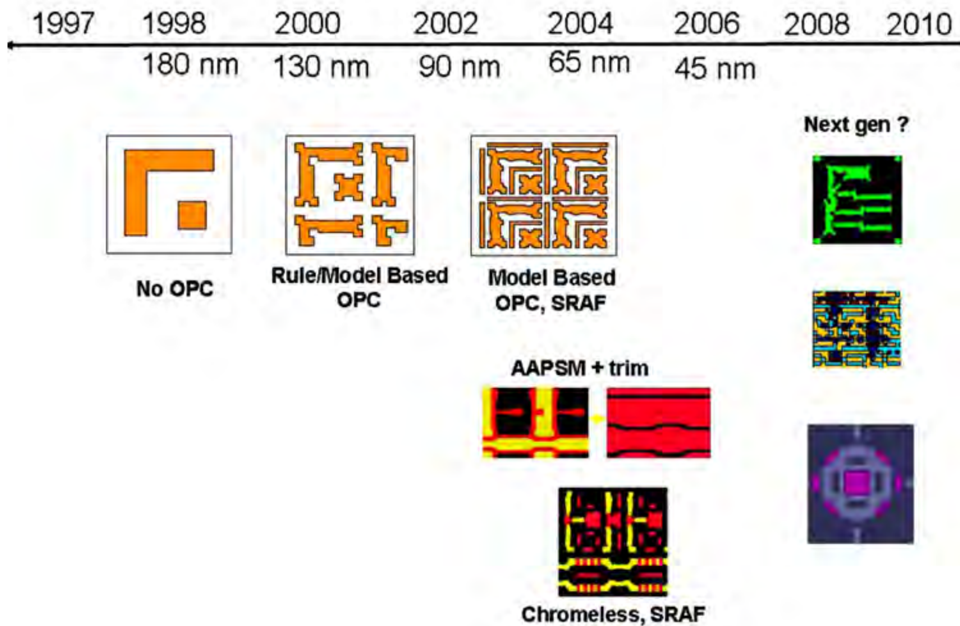


Fig. 8. *Transition of mask pattern from simple binary to a complex diffractive element showing optical proximity correction and SRAFs as well as alternating area PSMs. The computation, fabrication, and inspection required for generating a qualified mask for a complex chip pattern with 1×10^{10} features at 65 nm and below has become a major challenge.*

modeling the imaging process when features are smaller than the wavelength of the radiation and the numerical apertures are so high that the obliqueness of zonal rays becomes appreciable. Use of the scalar model for optical imaging ceases to be adequate, and Maxwell's equations have to be solved for each case ("vector" model). This nightmare was partially ameliorated by the introduction of model-based correction for these optical proximity effects [13], [14]. The principle of the model-based approach is that an IC pattern can be thought of as made up of a finite menu of basic patterns, and knowing thoroughly the behavior of these basic patterns simplifies the task of computing the proximity effects for the complete pattern; the evolution of optical masks is shown in Fig. 8. In more recent versions, the development response of the resists is also taken into account. Several companies have been formed that devote their entire efforts to improving the speed and accuracy of predicting completely the optical lithography process, including the tolerance to variations in exposure level and focus level, and identifying "hotspots" where such variations can reduce yield; the term *computational lithography* has recently been coined to describe this activity. Again, this is a large topic, and more complete descriptions can be found in [6]. Applying such techniques has led to the ability to manufacture ICs at the 65-nm node using 193-nm radiation at an NA of 0.9. This corresponds to a k1 of 0.3.

D. Immersion Optics [15], [76]

The arrangement is shown schematically in Fig. 9. By using water for the fluid filling the space between the lens and wafer surface, we can increase the numerical aperture to more than one. Although the principle is simple and the technique has been used for microscopy since the nineteenth century, the practical difficulties are challenging. For example, in a modern scanner, the wafer is moving past the lens at up to 1 m/s so droplets are often left on the surface and bubbles can form; but despite these difficulties, this technique is now being introduced to manufacturing for 45-nm (half-pitch) features and is slated to be extended to 32 nm. Some of the arrangements for maximizing the numerical aperture with this technique are described in [15] and [76] and illustrated in Fig. 9.

E. How to go Beyond $k1 = 0.25$

How low can k_1 go? Looking at Fig. 4(b), we can see that the contrast drops to zero at $k1 = 0.25$. However, that is for a single exposure, and we have already pointed out that we can overetch to achieve arbitrarily finer features.

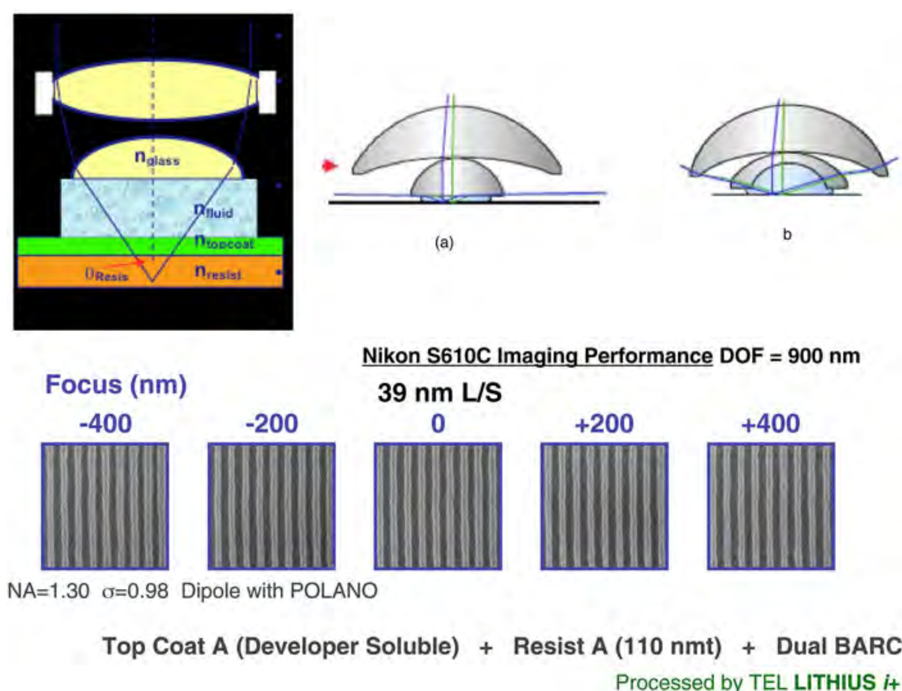


Fig. 9. *Immersion optics has been used for more than 100 years in microscopy but its application to deep ultraviolet has spawned major challenges arising from the lack of transparent and high index fluids and solids at 193-nm wavelength and from the difficulty of maintaining the fluid in place while the wafer moves at up to 1 m/s past the final surface of the lens. Top left shows the general principle in which a topcoat is used to match the refractive indices of the fluid (e.g., water) and resist. To achieve numerical apertures >1 at 193 nm, we either need (a) a fluid and a "glass" with respective refractive indexes greater than those of water and of fused silica or (b) a combination of a curved lens final surface and a thick (i.e., highly transparent) fluid [76]. The lower figure shown some preliminary results with NA >1 [15].*

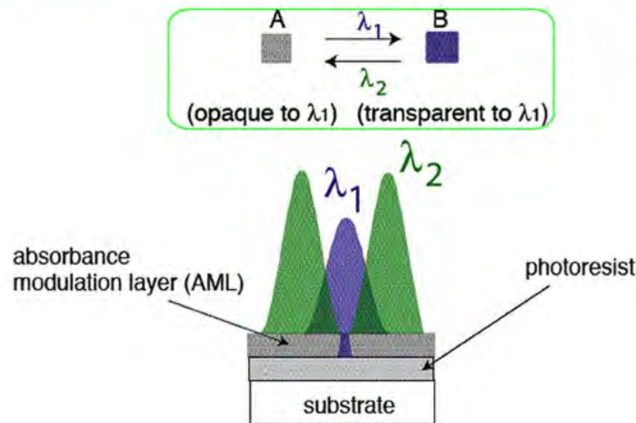


Fig. 10. ***An example of an ambitious approach to achieving features sizes for k1 < 0.25, AMOL. Under exposure at one wavelength, the absorbing modulation layer (AML) turns opaque and transparent at the other. Thus a simultaneous exposure at l_1 and l_2 can achieve an arbitrarily small transparent opening in the AML, which is then transferred to the photoresist by the same exposure at l_1. To achieve closely packed features, the operation must be repeated prior to developing. (Courtesy of H. I. Smith.)***

So we could expose, develop, and overetch one grating pattern and then pattern an identical grating pattern offset so that the combination is now a grating of double the spatial frequency of the original. A huge number of variations of such *double exposure* techniques are being described. In some, there is no need to remove the wafer from the scanner, so registering the second exposure to the first is less of a problem. However, most of the techniques do require a second registration operation, and achieving sufficiently accurate overlay has now become a major issue. Whereas for single exposure techniques an overlay accuracy of linewidth/three was regarded as adequate, with double exposure, an accuracy of a few nanometers is now desirable for 32-nm half-pitch.

One particularly ambitious approach to overcoming the wavelength limitation on resolution in optical lithography is *absorbance modulation optical lithography* (AMOL) [16]. AMOL employs simultaneous exposure at two different wavelengths and is shown schematically in Fig. 10. Twenty-nanometer lines and spaces have been reported corresponding to a k1 value of 0.05.

The bottom line is that ultraviolet lithography has demonstrated features below 22 nm, so the issue is not fundamental physics but technology (including economics). A

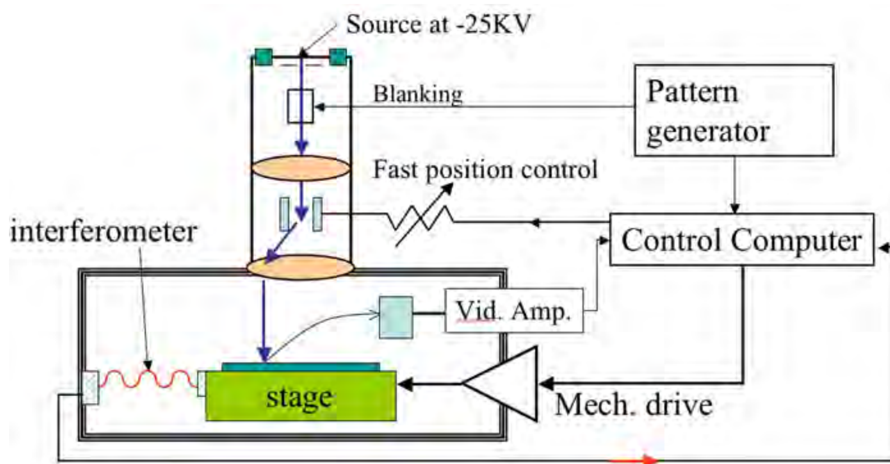


Fig. 11. ***Schematic of scanning electron beam lithographic tool featuring continuous feedback on stage position and sporadic feedback of landing position on workpiece (see [20]). Schemes to provide continuous feedback from the beam landing position have also been reported but are not yet in commercial use. (Courtesy of H. I. Smith.)***

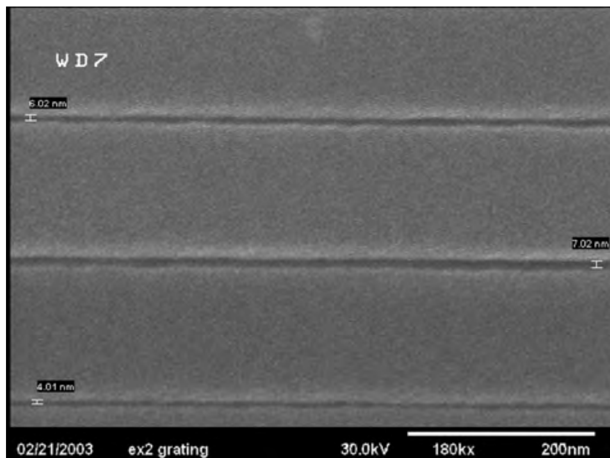


Fig. 12. *Example of electron beam lithography showing sub-10-nm features. (Courtesy of G. Bernstein, University of Notre Dame.)*

particularly telling example is that a 9-nm transistor was made using 248-nm radiation [17] (Fig. 1).

IV. ELECTRON AND ION BEAM LITHOGRAPHY

At the energies used (> 2 KeV), the wavelengths of both ions and electrons are so short as to be of negligible concern. Much the most popular is electron beam direct write (EBDW) and is essentially a computer-controlled SEM with means for blanking the beam. The simplest versions employ the scanning circuitry of the SEM and a stationary workpiece, and rely on the computer pattern generator to blank the beam at the appropriate intervals. More sophisticated systems use an interferometer to monitor continuously the position of the stage and often write while the stage is moving (this was the key feature of the Bell Labs

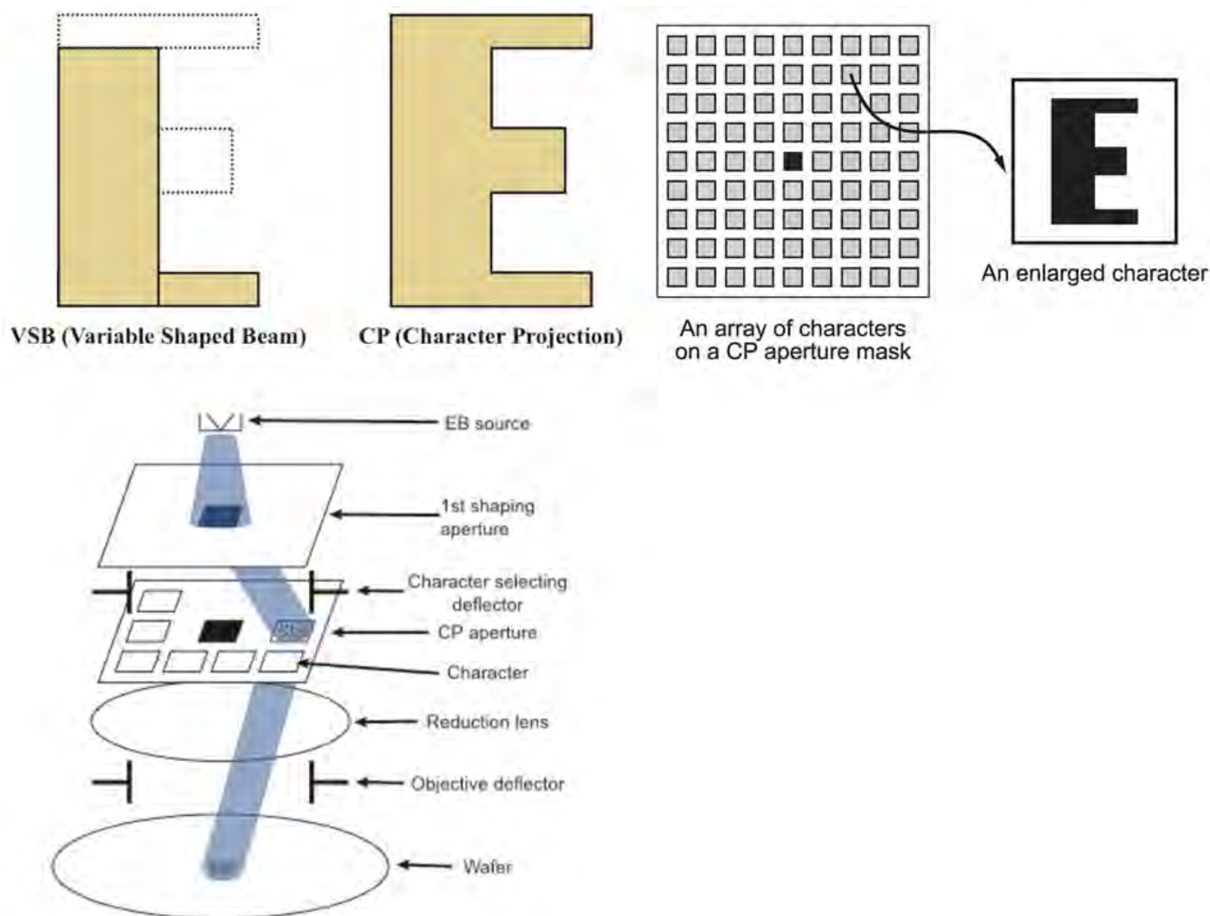


Fig. 13. *Improvement in the throughput of electron beam lithography can be achieved by exposing many pixels simultaneously. The simplest approach is to project an image of the first shaping aperture directly onto the wafer (not shown). In more elaborate schemes (shown), this shape is first projected onto a second stencil pattern so that only the overlap regions are projected onto the wafer. The overlap can be in the form of a rectangle of arbitrary format (top left, variable shape) or a selectively illuminated complete shape (character projection, top right). However, even these schemes suffer from limitations on resolution and throughput arising from electron–electron interactions because they employ a single electron optical axis [22].*

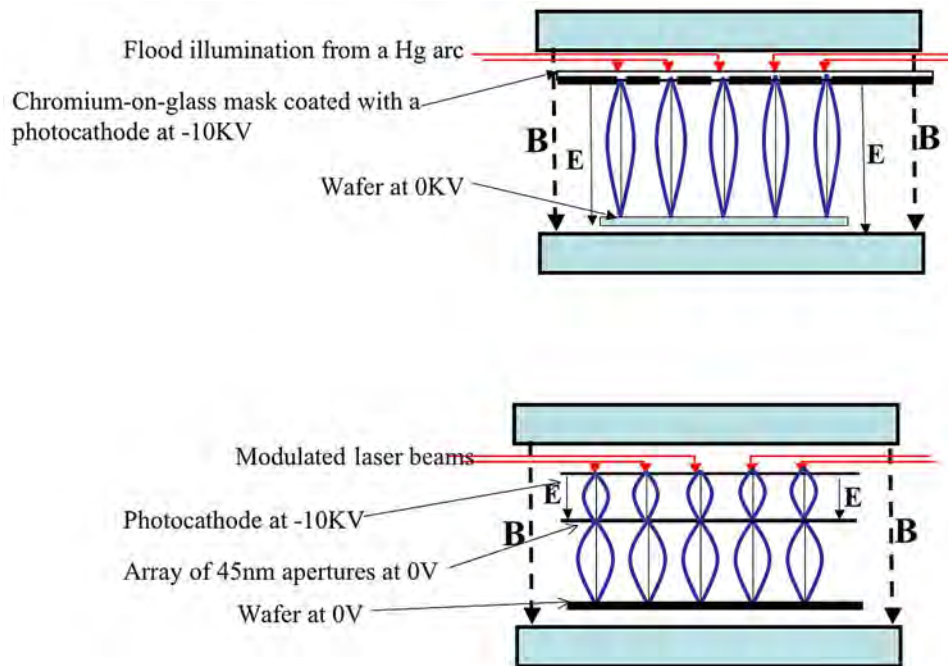


Fig. 14. *For further enhancement of electron beam lithography, we can employ multiple axes so that the beams are completely separated. The use of multiple columns has so far proved impractical because of the difficulty of matching the different columns. An early scheme (top) [26] employed parallel uniform E- and B-field to accelerate and focus photoelectrons emitted from a photocathode deposited on top of a chromium-on-glass mask. The high E-field at the wafer led to contamination of the photocathode and to poor overlay. The scheme shown below has negligible E-field at the wafer and employs only a uniform magnetic field to bring about simultaneous focusing of the different beams and so can be indefinitely extended. Sub-50-nm beam diameters have been demonstrated [81]; developing an array of suitable photoelectron sources is continuing.*

"EBES" [20]; see Fig. 11). With one pencil beam, the pattern is built up one picture element (pel) at a time. A minimum feature has at least $5 \times 5 = 25$ pels. A current chip pattern containing, say, 1×10^{11} rectangles has 2.5×10^{12} pels. If the maximum blanking rate is 100 MHz, then it will take 8 h to write one chip pattern; this is unacceptable for writing directly on the wafer but might be just acceptable for patterning a reticle. Even so, the versatility and resolution (better than 10 nm) (Fig. 12) of EBDW has led to at least two commercial systems (VISTEC and JEOL) that are used for prototyping a wide range of individual devices.

The slowness of this single pencil process was recognized from the start [18], and various approaches have been used to mitigate the problem. The shaped beam approach is the most successful. By imaging a square aperture as the object, we can project a complete square simultaneously. When introduced in about 1976 [19] by IBM for the personalization of gate arrays, the minimum feature size was 2.5 μm and it was possible to expose 22 wafers of 2.25-in diameter in 1 h. But today, with 65-nm minimum features and 300-mm wafers, the same system would take several months to pattern one wafer. So more elaborate approaches have been tried such as the variable-shape [21], [77]–[79] and cell projection [22] (Fig. 13). These schemes are faster than the fixed shape and are still being used for mask making and prototyping complex circuits. A related system with the same advantages in principle is the dot matrix configuration [24]. As can be inferred from Fig. 13, even though the object and image are extended, all rays pass through a common aperture centered on a single axis. At currents above about 1 μA, the coulomb forces between electrons usually introduce not only first-order defocusing but also third-order aberrations and stochastic blurring of the beam [23], [80] so large-scale manufacture of ULSICs is not economical.

To get around this, the idea of many electron beam columns has repeatedly surfaced [25] but this has not yet proved practical, largely because of the difficulty of matching the different columns. Perhaps the most promising idea has been one that has its origins in the early days of electron lithography [26]; the principle is shown in Fig. 14(a). That particular idea failed because of contamination of the photoelectron emissive film by the resist being bombarded and because any nonflatness of the wafer distorted the electric field and caused misalignment of the projected image. However, its reincarnation [Fig. 14(b)] overcomes those problems and is being researched by at least one institution [27], [28], [81], [82]. The main difficulty now appears to be achieving an array of adequately intense, uniform, and stable photoelectron sources. A similar scheme, MAPPER [29], ran into the same problem but now employs a different approach that brings about

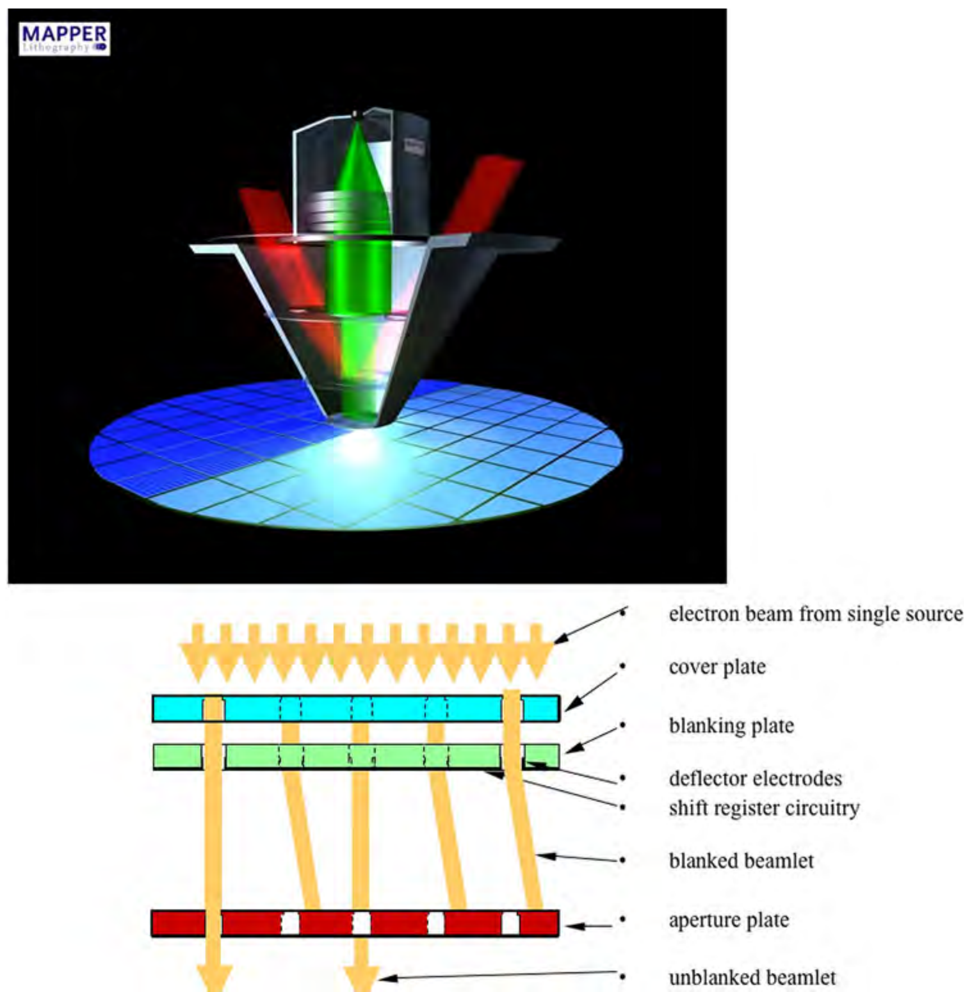


Fig. 15. *The MAPPER concept also employs multiple-axes within one vacuum envelope. A thermionic cathode illuminates an array of apertures. The emerging beamlets are then focused by an array of simple electrostatic lenses, and each is modulated by deflecting across its own aperture. The individual deflecting signals are brought through the vacuum wall as light beams that activate the deflection of each beamlet. A similar arrangement (but not using light-based deflecting signals) is used in the IMS PML-2 design (lower). (Courtesy of P. Kruit and MAPPER Lithography NV; and H. Loeschner, IMS.)*

individual blanking of the beamlets using a complicated micromachined assembly that is activated optically to facilitate bringing a large array of switching signals through the vacuum wall (Fig. 15). Another European project is PML2, which features electron optics optimized to minimize space charge interactions and also employs a micromachined assembly for blanking individual beamlets.[3]

One scenario that is becoming more popular is a throwback to the original IBM work on personalizing gate arrays; this is a hybrid approach in which EBL is used only for the high-resolution features and the remainder is done with optical lithography. One company, e-ASIC, employs a process in which only vias are patterned to personalize application-specific integrated circuits (ASICs); in this way only about 1% of one level need be exposed[4] (Fig. 16). This not only saves time, thus making EBL viable, but also greatly reduces design costs, without the overhead of the switching and routing circuitry associated with field-programmable gate arrays.

Multiple ion beams and ion projection lithography have also been suggested [30] because there is reduced lateral scattering within the resist film and the resists are about 100 times more sensitive to ions than to electrons; but because of shot noise in the beam, we cannot take advantage of this increased sensitivity at features sizes below 100 nm. Present estimates are that we need about 10 000 exposure quanta to achieve 10% feature area tolerance (6-sigma) [20], [31]. For 45-nm^2 features, this is about 40 μC/cm^2 and for 22-nm features 160 μC/cm^2;

[3]IMS, http://www.rimana.org/project_description.htm.

[4]www.easic.com.

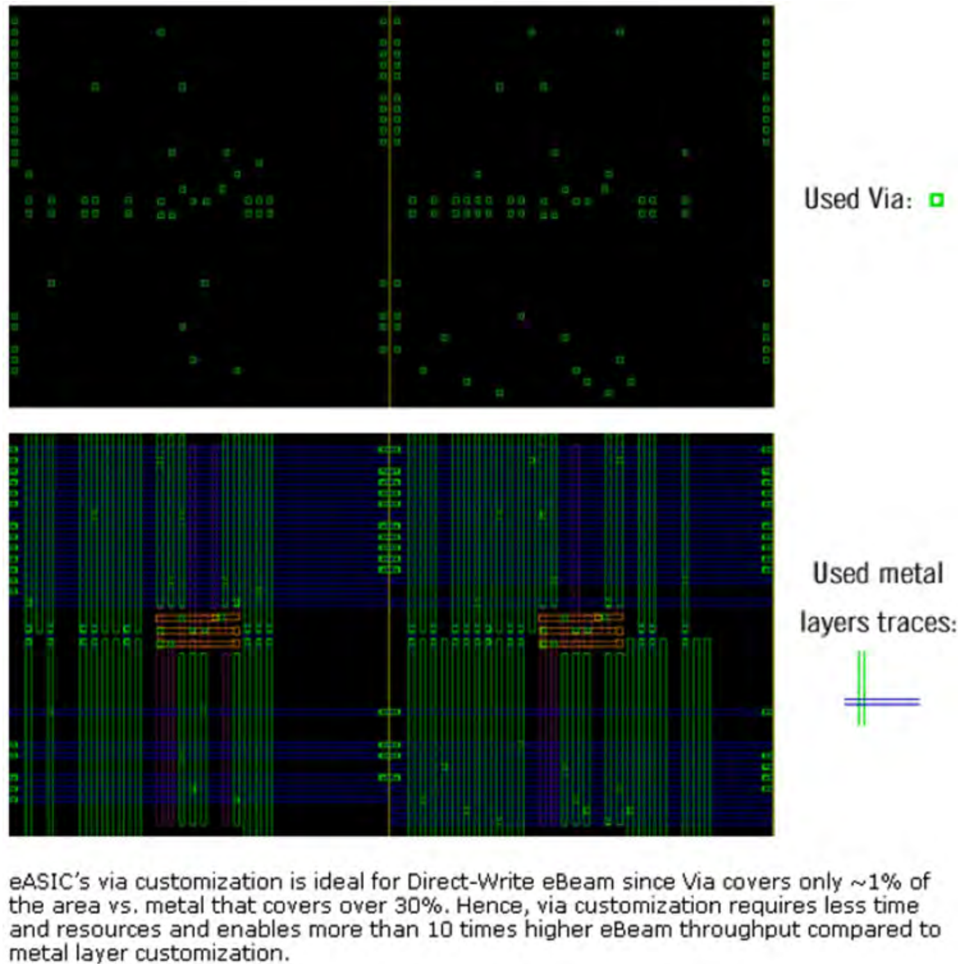


Fig. 16. *One promising application of electron beam lithography is for personalizing ASICs. Traditional personalization features custom patterning of a complete metallization level (bottom) but can also be accomplished by patterning only selected vias such that only 1% of the area (or less) need be exposed (top). (Courtesy of e-ASIC.)*

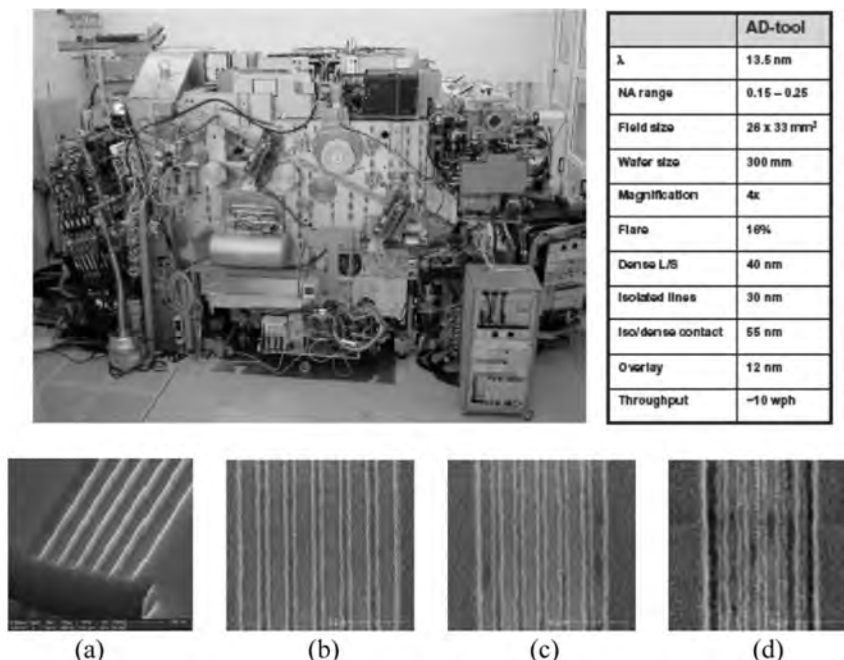
both figures are characteristic of required doses of high-resolution resists to electrons so there is no advantage in using ions under these conditions. To try to avoid space-charge problems, proximity printing through a stencil mask has been demonstrated [32], but despite the high quality of patterns the difficulty of making qualified stencil masks has precluded serious development. Thus ion beam patterning is now restricted to applications using a pencil beam in which only very small throughput is needed such as repair of photomasks [33] and preparing samples for examination in the transmission electron microscope[5] and for making ambitious devices one at a time; some spectacular structures have been built in this way[6] (Fig. 18). For researching new devices, this focused ion beam is a wonderful tool especially when combined in the same instrument as a scanning electron beam [34].

[5]http://www.uga.edu/caur/SampPrep.pdf.

[6]http://www.nanopicoftheday.org/2004Pics/May2004/Nanowine-glass.htm.

V. X-RAY LITHOGRAPHY

As mentioned earlier, X-ray lithography (XRL) [35] has a choice of a large range of wavelengths, from about 0.4 to 100 nm. In its first incarnation, proximity printing was used with a wavelength of about 1 nm and the gap was about 20 μm, giving a Fresnel diffraction blur of about 140 nm. At this wavelength membranes of, for example, silicon 4 μm thick were reasonably transparent and absorbers of, say, gold needed to be about 400 nm thick to be adequately opaque (these numbers are approximate as it is advantageous to tune the wavelength on opposite sides of the absorption edges of the substrate and absorber materials). Despite determined industrial efforts and significant technical success, XRL never was able to demonstrate circuits that could not be made more economically by ultraviolet lithography. The blame for this failure was laid at the door of the mask houses who had failed to furnish adequate masks; in particular it was the fact that these masks had to be unity magnification (rather than 4, 5, or 10 times



	AD-tool
λ	13.5 nm
NA range	0.15 – 0.25
Field size	26 x 33 mm^2
Wafer size	300 mm
Magnification	4x
Flare	16%
Dense L/S	40 nm
Isolated lines	30 nm
Iso/dense contact	55 nm
Overlay	12 nm
Throughput	~10 wph

Fig. 17. ***(Top) Photograph of ASML EUV alpha demonstration tool together with a list of key characteristics. (Bottom) Examples of resist patterned with EUV lithography. The term σ refers to the ratio of the NA of the illumination optics/NA projection optics [37]. (a) Resist profile cross-section by an FEI dual-beam SEM. (b)–(d) Top-down SEM images of 50-nm hp, 40-nm hp, and 35-nm hp lines, respectively (MET-2D resist, dose= 19 mJ/cm^2; NA = 0.25; σ = 0.5 conventional illumination.***

larger, as in the case of reticles for steppers) that was widely blamed. Others, including one of the authors, believe the real problem was the membranous nature of the substrate and the thick absorber layers that were needed; a 4× mask would have had to have 16× the area of a 1× mask. However a variant, originally dubbed "soft X-ray lithography," appeared in the early 1990s. It offers a way around the difficulty of making X-ray lithographic masks by offering reduction optics and a thick mask substrate. To make the introduction of this technology more palatable, it was renamed extreme ultraviolet lithography [36].

EUVL is now the favorite technology to supplant optical lithography. The wavelength is 13 nm. For this wavelength, mirrors can be made with up to 70% reflectivity by using a multilayer (e.g., about 70 alternating layers several nanometers thick of Si and Mo) structure with tolerances of a few atomic layers. All-reflective optics are used (including the mask substrate), and building the appropriate focusing elements and defect-free mask blanks have been major challenges that, somewhat to the surprise of several authorities, appear to have been successfully met. Coming up with an appropriately powerful source now appears to be the main problem. At this wavelength, the shot noise limitations begin to appear, which could make the source problem even more daunting. Until now, the only published sub-30-nm features that look acceptable have been made in very insensitive resist such as polymethylmethacrylate (PMMA) or hydrogen silsesquioxane (HSQ) but it is possible that more sensitive resists will be adequate. Some early results are shown in Fig. 17. Two prototype EUV exposure tools have recently been delivered (Fig. 17) [37], and it will be interesting to see how well the technology performs. Assuming they are successful, this approach may be more economical than immersion 193 nm using double exposure because, at the 22-nm half-pitch, the relative simplicity of the process allows greater tolerance for each step. The annual meeting on microlithography sponsored by

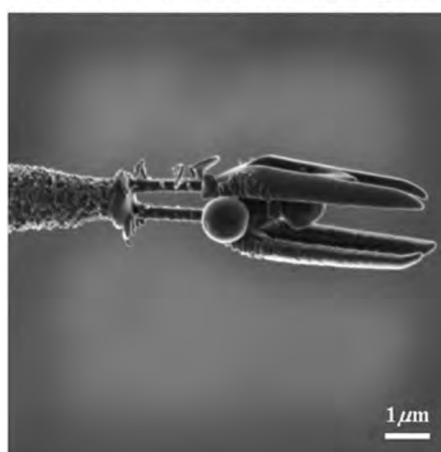


Fig. 18. ***Example of fashioning a 3-D nanostructure using a focused ion beam.***

The International Society for Optical Engineering is the best source of current progress on this and other patterning techniques for semiconductor manufacturing.

VI. NON-RADIATION-BASED PATTERNING

Unlike the above forms of patterning that employ radiation (photons, electrons, or ions) to delineate a pattern in a resist, non-radiation-based patternings delineate features in a resist primarily using mechanical or chemical means or both. *Mechanical patterning* uses a mechanical mold (also called template) that shapes a material into features (i.e., nanoimprinting [39]) or a stamp that transfers an ink onto a surface (nanoprinting or soft-lithography [40]). *Chemical patterning* techniques use a local chemical energy minimum of a material system, hence called "self-assembly," since in a thermal equilibrium a system always goes to its energy minimum and the patterns form themselves. Chemical patterning techniques include self-assembly of a monolayer of molecules on the local surface and the phase-separation of diblock polymers. *Mixed patterning* techniques combine mechanical and chemical means, such as guided self-assembly, that use a larger mechanical or chemical patterns to guide the self-assembly of much small patterns, so that the self-assembled patterns have predetermined locations and large domain size rather than random locations and small domain sizes in unguided self-assembly.

Compared with radiation-based nanopatternings, non-radiation-based patternings have three major advantages due to fundamentally different physical principles. First, they do not have a diffraction limit in resolution; secondly, they are easy for 3-D patterning; and thirdly, they can directly pattern functional materials to reduce fabrication steps and cost. (They also eliminate expensive, complicated particle source and optical systems.) Although non-radiation-based patterning is far less mature and has its drawbacks (as discussed below), it potentially offers a high resolution and low cost unmatchable by radiation-based patterning.

Nonradiation patternings have their own challenges. For example, mechanical patterning (such as nanoimprint or nanoprint) is a form of contact lithography, facing issues of defect density, 1x mask cost, mask damage, and wafer throughput (for step-and-repeat). It is to be seen whether all of these issues can be solved, to what degree, and for what applications. Unlike radiation-based patterning, which has been used by the semiconductor industry for more than 30 years and has had tens of billions dollars investment (in today's money) for research and development, non-radiation-based patterning is just introduced to industry from laboratory research and has received several orders of magnitude less funding for research and development. It is of great interest to see if, when given sufficient funding and time, the previous issues will be solved and the potential of nonradiation patterning will be fully utilized.

Here our discussion focuses on nanoimprint, since it may be the most promising non-radiation-based patterning for electronics applications due to its ultrahigh resolution and high pattern transfer fidelity. Nanoimprint has been put on the roadmaps of many industries, including ITRS, as

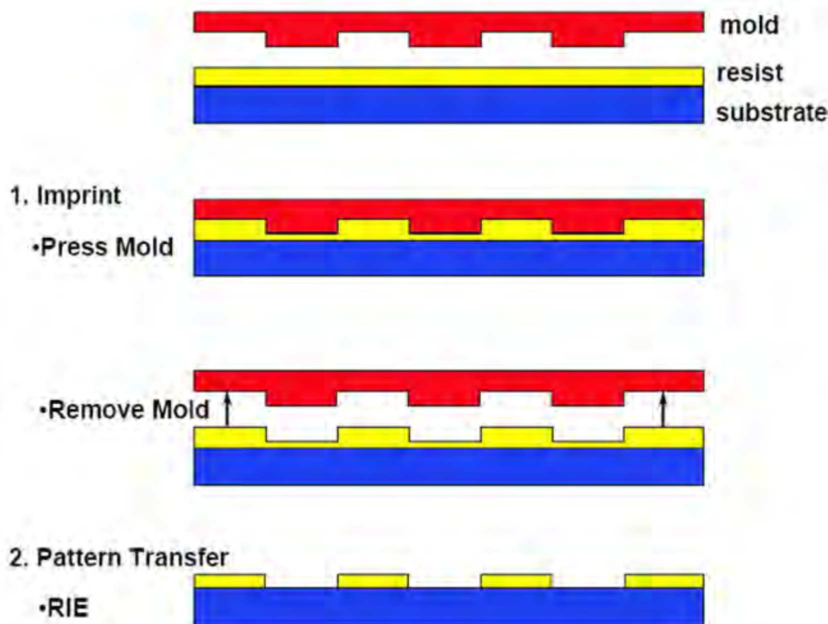


Fig. 19. *Schematic of the earliest nanoimprint technology—nanoimprint lithography. (a) Imprinting using a mold to create a thickness contrast in a resist. (b) Pattern transfer using anisotropic etching to remove residue resist in the compressed areas [39], [40]–[43].*

a next-generation patterning method for manufacturing semiconductor integrated circuits [38] and the roadmap for manufacturing magnetic data storage disks.

A. Nanoimprint Technologies

Principle: Nanoimprint patterns nanostructures by physical deformation of a material using a mold, creating a pattern in the material (rather than by changing the local chemical properties of the material using radiation) (Fig. 19) [39], [41]–[43]. The imprinted material can serve as a resist for pattern transfer (as in conventional lithography and being removed later) or can be a part of the devices to be built and stay on the wafer (direct imprint of functional materials).

Different Forms of Nanoimprint: There are various forms of nanoimprint technology. The earliest is thermal nanoimprint lithography (thermal-NIL), originated in 1994, that imprints a thermoplastic resist and removes the residual layers of the imprinted materials to expose the substrate. (A thermoplastic material starts as a solid film, becomes a viscous liquid when its temperature is raised higher than its glass transition temperature (T_g), and returns to a solid when its temperature is brought below T_g.) The imprint resists also can be photo (often ultraviolet light) or thermal curable materials, which are initially in liquid state and become solid by curing them with photons or heat, respectively [43], [44]. An entire wafer can be imprinted by a single step or multiple steps with one imprint step on one die and repeat. *Step-and-flash imprint lithograph* (SFIL) is a photo-NIL process in which drops of a resist liquid are dispensed and imprinted on one single die area at a time. This process is repeated as the imprint mold is "stepped" from die to die across the wafer, repeating the resist drop and imprint cycle [45]. Other forms of nanoimprint include "roller nanoimprint" that can offer ultra-high throughput and low cost of nanopatterning [46]; and transfer nanoimprint and casting nanoimprint, where a material is imprinted outside a wafer and later is transferred on the wafer (by a bonding processes).

The imprinted material can serve as a resist for subsequent processing and be removed afterwards or stay as a part of the device. For simplicity, we call all imprinted materials "resists" in either case.

NIL Capability: Because its working principle is fundamentally different from radiation-based patterning technology, nanoimprint has many advantages over conventional lithography, particularly in patterning resolution, high pattern transfer fidelity, 3-D patterning, larger area (full wafer if needed), ability of reducing other fabrication steps, high throughput, and low cost.

Patterning resolution: Since pattern delineation in nanoimprint lithography is not based on the modification of the chemical structure of a resist by radiation, its resolution is not limited by the factors that limit the resolution of conventional lithography: wave diffraction, scattering and interference in a resist, backscattering from a substrate, and the chemistry of resist and of its development. In fact, photocurable NIL has demonstrated 6-nm half-pitch imprinted into a resist [Fig. 20(a)] [47], [48] and thermal-NIL has demonstrated arrays of 10-nm-diameter dots separated by 40 nm (400 dots/in^2) [Fig. 20(b)] [49]. Yet, these features are not the limits of NIL, but the limits of our ability in making the features on the mold; NIL can achieve even smaller features if a mold can be made. From the faithful duplication of nanometer variations on a sidewall of a mold, it is clear that imprinting of sub-3-nm features is possible [50].

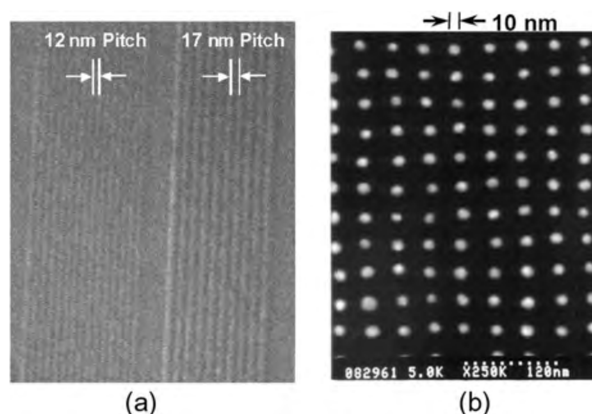


Fig. 20. *SEM of (a) imprinted resist grating with a minimum 6-nm half-pitch [47], [48] and (b) 10-nm-diameter and 40-nm period of metal dot array by nanoimprint and a liftoff [49].*

High pattern transfer fidelity: NIL has been demonstrated to have high fidelity in pattern transfer, accurately reproducing original mold patterns and maintaining smooth vertical sidewalls in the imprint resist. For example, repeated imprinting of SRAM metal interconnect patterns of 20-nm half-pitch has achieved a standard deviation of 1.3 nm in the variation of the imprinted feature width (Fig. 21) [47]. High aspect ratio patterns with smooth sidewalls on the mold are transferred to the resist faithfully (Fig. 22), unlike in conventional lithography, which can produce sloped sidewalls and line edge roughness due to a Gaussian shape of the light profile, light scattering, and other noise [48].

3-D patterning: The third unique feature of NIL is 3-D patterning, rather than the two-dimensional patterning as in conventional lithography. Three-dimensional features are very desirable for certain applications such as microwave circuits and microelectromechanical systems. For example, the T-gate for microwave transistors has a narrow footprint for high-frequency operation but wide top for lower resistance. Fabrication of a T-gate often requires two electron beam lithography steps: one for the footprint and one for the wide top. Each electron beam exposure could take more than 2 h to pattern a single 4-in wafer. With NIL, the entire 4-in wafer can be patterned in

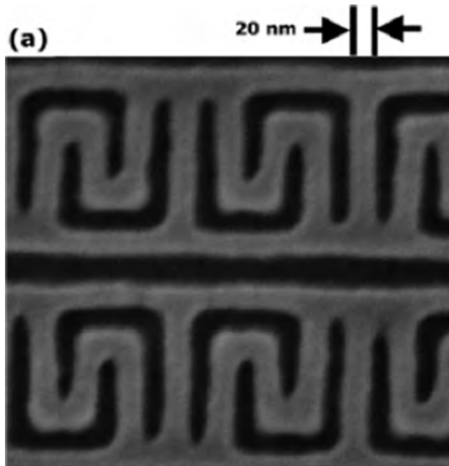


Fig. 21. *SEM image of 20-nm half-pitch resist pattern for SRAM metal contacts fabricated by NIL [47].*

one step in less than 10 s. Fig. 23 shows a 40-nm T-gate fabricated by a single NIL step and liftoff of metal [51]. Nanoimprint is also used to create 3-D damascene oxide patterns for metal interconnect using SFIL (Fig. 24) [52].

Large patterning area: The NIL exposure area (area patterned in a single step) can be much larger that the exposure field of a conventional photolithography stepper ($\sim$1 in^2) because NIL does not require high precision optics nor a well-conditioned monochromatic light source. Today, full 4- or 8-in wafers are routinely imprinted at once over a full wafer scale. When air cushion press is used, which press wafers and mold by pressured air (or fluid) creating uniform pressure everywhere, excellent imprint uniformity has been achieved [53].

Reducing fabrication steps: When replacing imprinting resist with functional materials that will stay on devices as a part of the device structure, nanoimprint can in fact reduce multiple fabrication steps into one (imprint). For

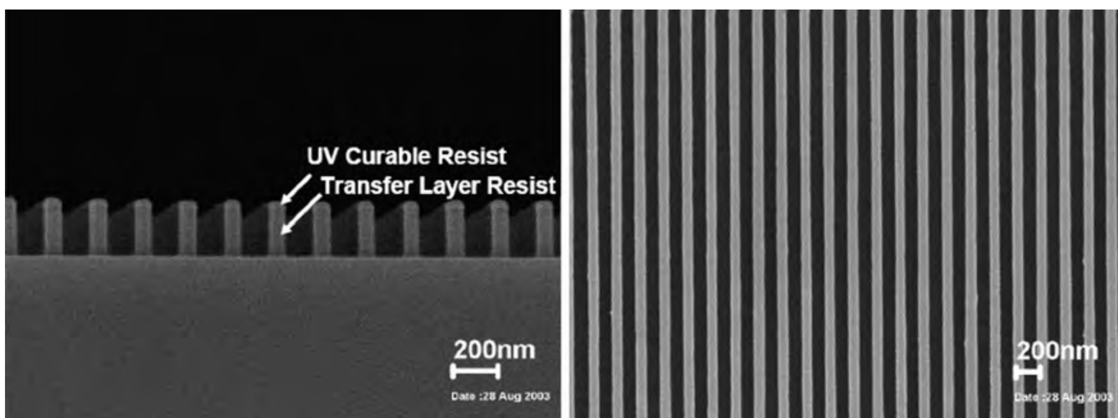


Fig. 22. *Resist profile by nanoimprint showing smooth vertical sidewalls [15], [76].*

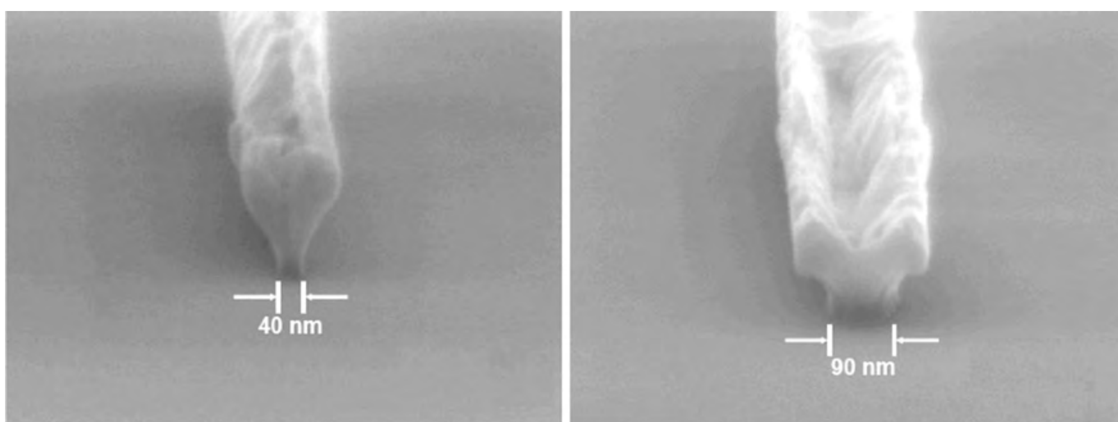


Fig. 23. *Three-dimensional patterning. SEM of two T-gates of 40- and 90-nm footprint, respectively, fabricated by a single NIL and a liftoff of metal [51].*

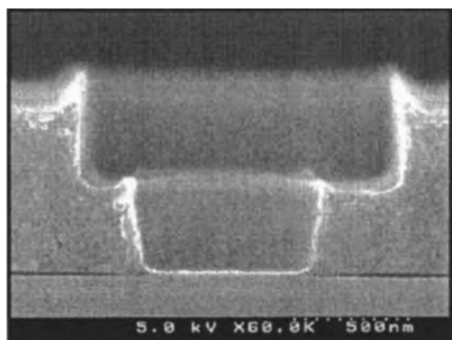


Fig. 24. ***Three-dimensional dielectric patterns for metal interconnect damascene using SFIL [53].***

example, for the T-gate in microwave devices or the interconnects in ICs, the conventional approaches to create a 3-D dielectric structure require multiple steps of depositions, lithography, etching, but nanoimprint needs one step because the imprint material is already the dielectrics and the 3-D shape can be made by one imprint.

Low cost and high throughput: Because NIL does not use complicated and expensive optics systems and laser sources, NIL tools can be much cheaper than conventional photolithography. The overall cost of a lithography needs to factor in the cost of masks and wafer throughput. A 1x mask for NIL is intrinsically more expensive than a 4x mask for photolithography, unless some low-cost 1x masking will be developed. For a single full wafer imprint, its throughput should be higher than photolithography (currently some 600 wafer per hour full-wafer imprint tools are under development). For step-and-repeat, NIL throughput can be comparable to photolithography (as discussed below).

Challenges in Manufacturing by Nanoimprint

Defect density: The contact between a imprint mask and a wafer makes the technology susceptible to more defects than projection photolithography. However, the situation of today's nanoimprint is quite different from the problems faced by old contact lithography, which were one key reason of having migrated to projection lithography. In the old contact lithography, the mask would pick up some "dirt" at each contact, hence accumulating the dirt, becoming worse each time, and eventually going over a certain defect density limit. In contrast, in nanoimprint, the mold is coated with a thin antisticking layer, which prevents dirt from sticking on a mold while the resist behaves more like a glue that will take a dirt away from a mold. Therefore, in each imprint, a dirt on the mold will be picked up by the resist and comes off from the mold, making a mold cleaner after each imprint. Such mold "self" cleaning in nanoimprint was long observed in its early date [54] and was further documented recently [55]. Recently, a defect density of 1.2 defects per square centimeter has been reported [56]. The belief is that the defect density can be further reduced.

Mask damage: Mask damage is another issue in a contact printing. A variety of technologies have been devised for avoiding and reducing mask damages. For example, before imprinting a die on a wafer, the die can be previewed by a microscope and will be skipped from imprinting if a "significant" dust is observed, avoiding a mold damage. A "soft" mold also can be used to reduce the mold damaging.

1X masks (mold): In today mask making technology, 1x masks cost much more than 4x mask. However, the difference in mask costs is getting smaller as 4x masks use more and more optical proximity corrections (for improving the patterning capabilities) which has a feature size near or the same as that in a 1x masks. In parallel, some new ways of making 1x masks (nanoimprint molds) are being explored.

Wafer throughput: Wafer throughput for SFIL tools is ~5 wafers (8-in diameter) per hour commercially available[7] and 20 wafers per hour is under development. Although these tools can produce feature sizes five to seven times smaller, they have a throughput slower than current 65-nm photolithography tools, which have a throughput of 60–80 wafers per hour. It should be clearly understood that just imprinting a pattern into a resist itself can be done in less than a microsecond. In fact, sub-200-nm imprinting in either liquid silicon or resists has been demonstrated [57], [58]. The slow throughput of current SFIL tools primarily comes from the time for dispensing resist on a die, alignment on each die, and resist curing. There is no doubt that with further development, these times can be reduced and the throughput of step-and-repeat tools improved.

Nanoimprint Applications: Because of its unmatchable advantages over the existing nanopatterning technology, nanoimprint technology, as soon as it was invented, was applied quickly and increasingly to a broad range of disciplines, including magnetic data storage, optics, optoelectronics, displays, biotechnology, semiconductor integrated circuits, advanced materials, and chemical synthesis, to name just a few [54], [59]–[63]. Initially, nanoimprint technology was used in laboratory demonstrations; but in recent years, nanoimprint technologies have been pushed by various industry sectors to become key in industrial manufacturing. Working Si nanotransistors have been fabricated on 4-in wafers using nanoimprint at each of four lithography levels (Fig. 25) [63].

B. Other Mechanical Patterning Methods

Other mechanical patterning include *micro/nanoprinting (or soft lithography)*, where a stamp with surface patterns transfers an ink onto a surface [64]. Soft lithography is one of the earliest forms of mechanical patterning introduced. It is mainly for patterning of micrometer sizes or features greater than 100 nm because it is very difficult to control the amount and flow of a liquid ink and the stamps are not

[7]Imprio-250, Molecular Imprint Inc., 2006.

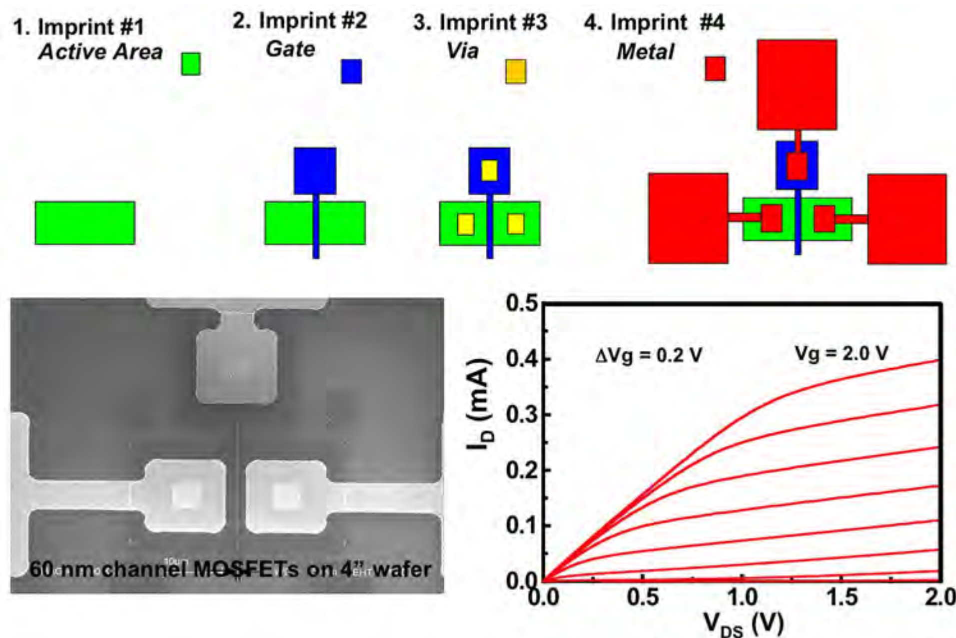


Fig. 25. *Sixty-nanometer channel length MOSFET fabricated on 4-in wafer using nanoimprint in all four lithography levels [63].*

sufficiently rigid. The feature resolution of the printing is poorer than nanoimprint, where a hard mold and embossing are used. Soft lithography has been widely used in microfluidic devices and biology due to its low cost, flexible, and fast prototyping nature. To overcome the problem of ink flow and amount control, *nanotransfer printing* is used, where a solid material (ink) pattern is created on a hard stamp by nanoimprinting or material deposition, and then is transferred to a substrate by bonding the solid material pattern to the substrate and peel off (separate) the mold from the solid material pattern [65].

C. Chemical Patterning (Self-Assembly—Unguided and Guided)

Self-Assembly (SA): Patterning refers to the process where the materials form patterns themselves. This is because the final formed patterns are a local chemical energy minimum of the material system, while the initial material state has a higher energy. In unguided SA, a single domain where self-formed patterns are in a uniform desired regularity often has a small area (several micrometer ranges) and the orientations between the different domains are random. The reason is that the self-assembly occurs simultaneously in many locations of a substrate without any correlation between different sites. This can be solved by putting some guiding patterns on a substrate prior to an SA. The guiding pattern, often much larger than that formed by an SA, serves as a guide to teach an SA where to start and end and to establish a desired correlation between different SA sites. Another type of guided self-assembly (GSA) is a "carbon-copy" GSA, where the self-assembled patterns follow the exact patterns that were prefabricated on a substrate, except having smoother edges and/or different pattern thickness. So a carbon-copy GSA is not for creating a lithography pattern, but for improving it. Presently, self-assembly approaches are still in the research phase and have issues such as defect density, placement accuracy, and materials compatibility.

Self-Assembled Monolayers (SAMs): SAM is a process where only one monolayer molecules are attached to the substrate surface (for a review, see [66]). The principle of SAMs, based on the fact that each molecule used for assembly has two end functional groups, one end group, called head functional group, preferentially attaches to the material on the substrate surface and the other end functional group, called terminal functional, does not attach to the substrate material nor the head functional group. Hence once one layer of molecules has attached to the substrate surface, the rest of the molecules stop attaching to the surface, and hence only layer of molecules is attached. For examples, thiol (SH) can be used as the head functional group for attaching a gold surface, and hydroxyl (OH) can be used as a head functional group for attaching to SiO2. Methyl (CH3) can be used as terminal functional group. Often, a SAM is coated on nanoparticles with its terminal functional group attractive to a substrate, so that a monolayer of the nanoparticles can be coated on the a surface and the monolayer of nanoparticles can self-form certain patterns.

Phase Separation of Block Copolymers: Block copolymers are a special type of polymer where different polymer blocks are connected. For examples, a diblock copolymer has a block $A - A \ldots A$ connected to another block $B - B \ldots B$, namely, $A - A \ldots A - B - B \ldots B$, where A and B are different monomers. An example is polyisoprene (PI)-polystyrene (PS) diblock copolymer that has monomer of isoprene and styrene, respectively. In general, block A mixes well with block B, and the film is uniform. But when the copolymer is heated at the order–disorder temperature (e.g., $\sim$140 °C for PI-PS copolymer), the two polymer blocks phase-separate (because a nonmixing state has a lower energy). However, since the two blocks are connected at their ends, the phase separation only can be in microscopic regions, forming periodic patterns of A and B blocks, with the length of each A and B block region about two times the block A and B molecular length, respectively [67]. By controlling the initial molecular length of each block, we can varyeach A and B block region from a few to hundreds of nanometers. Furthermore, depending upon the relative size of the two blocks, the final phase separation structures can be spheres, cylinders (HEX), lamellae (LAM), bicontinous, or perforated layers [67]. Because each polymer block has a different reactive ion etching (RIE) rate, the RIE of a phase-separated diblock copolymer film will convert its original composition difference into topology difference, hence carving out the pattern formed by phase separation [68].

Guided Self-Assembly (GSA): Also called templated self-assembly, uses patterns much larger than that formed in the assembly to guide self-assembly. The guiding patterns allow fixing a SA starting location and ending location, and establish the orientation relation with SA in the other areas of the substrate. For examples, patterned substrates have been used for guided the phase separation of diblock copolymers (Fig. 26) [69]–[71]. Such GAS has been used to fabricate multiple 1D channel MOSFETs [72]. The diblock copolymer phase-separation is also being used as a carbon-copy GSA to remove edge roughness caused by original lithography [72].

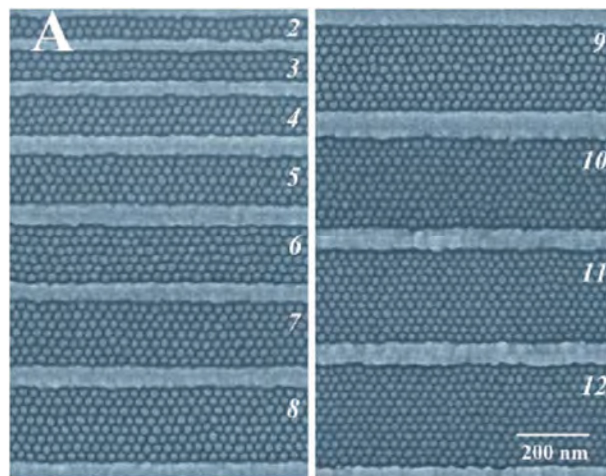


Fig. 26. ***Phase separation of diblock copolymer (polystyrene-b-polyferrocenyldimethylsilane) guided by the substrate strips. [69], [70].***

VII. CONCLUSIONS

Patterning is fundamental to advancing (almost) any technology.

For many applications, most notably electronic circuitry, smaller is better in terms of speed, power consumption, and cost. According to classical scaling laws, the energy consumed per computing function varies as the cube of the linear dimension, i.e., halving linear dimensions, results in an eightfold reduction in energy consumed for a given amount of computation. Judging by the continued investment by industry leaders in new patterning technology, significant advantages will continue at least down to 20-nm features.

Patterning of features to 20 nm and below has been demonstrated by a variety of techniques. So the issues are now technological (including economics) rather than fundamental. Although even 248-nm radiation has been used to make 9-nm devices, the complexity of the processes involved may well render this approach uneconomical. Many authorities believe that EUVL will be more economical despite the complexity and cost of the exposure tool. However nonradiation patterning techniques such as nanoimprint lithography also appear very attractive but presently lack the investment needed to make them attractive for semiconductor IC manufacturing. It is possible that they will be used initially for patterning the less critical levels and later migrate to more critical levels, i.e., behave as a classical disruptive technology. Self-assembly of structures is an appealing approach particularly when periodic patterns that do not require overlay accuracy to a small fraction of a minimum feature are required. One example might be to increase the surface area of capacitors through the fabrication of high aspect ratio holes or pillars.

Inspection and metrology of the fabricated patterns do not often feature in the discussions of patterning technology, yet these steps are now becoming a significant contributor to total cost and merit more attention from the research community. In many cases, the tecniques used for writing may well be used for high speed, high resolution inspection. One example could be a multiple-beam SEM using multiplexed secondary electron detectors. ■

Acknowledgment

The authors acknowledge valuable discussions with Prof. H. Smith of the Massachusetts Institute of Technology and the encouragement of Dr. J. Zolper and D. Radack of the Defense Advanced Research Projects Agency.

REFERENCES

[1] T. J. Riley, "Scaling of IGFET circuitry," 1971, Bell Labs Tech. Memo., unpublished.

[2] S. M. Sze and K. K. Ng, *Phys. Semiconduct. Devices*, 3rd ed. New York: Wiley, 2007, ch. 6.

[3] D. D. Awschalom, M. E. Flatté, and N. Samarth, *Sci. Amer.*, Jun. 2002.

[4] L. F. Thompson, C. G. Willson, and M. J. Bowden, *Introduction to Microlithography*. Washington, DC: Oxford Univ. Press, 1983.

[5] H. J. Levinson, *Principles of Lithography*, vol. PM146, 2nd ed. Bellingham, WA: SPIE.

[6] A. Kwok-Kit Wong, *Optical Imaging in Projection Microlithography*, ser. Tutorial Texts in Optical Engineering. Bellingham, WA: SPIE, 2001.

[7] M. D. Levenson, N. S. Viswanathan, and R. A. Simpson, "Improving resolution in photolithography with a phase-shifting mask," *IEEE Trans. Electron Devices*, vol. ED-29, pp. 1828–1836, 1982.

[8] [Online]. Available: http://www.cs.caltech.edu/~westside/quantum-intro.html

[9] G. G. Shahidi, "SOI technology for the GHz era," in *Int. Electron Devices Meeting Tech. Dig. (IEDM 95)*, 1995, pp. 59–62.

[10] A. Offner, "Unit power imaging catoptric anastigmat," U.S. Patent 3 748 015, 1973.

[11] M. Shibuya, "Projection master for transmitted illumination," Japanese Patent Showa 62-50811, Oct. 27, 1987.

[12] D. C. Flanders and H. I. Smith, "Spatial period division exposing," U.S. Patent 4 360 586, Apr. 14, 1980.

[13] Y. C. Pati, A. A. Ghazanfarian, and R. F. W. Pease, *IEEE Trans. Semiconduct. Manufact.*, vol. 10, pp. 62–75, 1995.

[14] D. Van Den Broeke, K. Wampler, X. Shi, R. Socha, and K. Gronlund, "Model-based RET using interference maps, algorithms for random contacts at 65 nm," *Solid State Technol.*, Sep. 1, 2004.

[15] S. Owa, H. Nagasaka, K. Nakano, and Y. Ohmura, "Current status and future prospect of immersion lithography," *Proc. SPIE*, 2006, vol. 6154, 61 5408-1.

[16] R. Menon and H. I. Smith, "Absorbance modulation optical lithography (AMOL)," *J. Opt. Soc. Amer.*, vol. A 23, p. 2290, 2006.

[17] M. Fritze *et al.*, "Fully depleted SOI transistors with sub-10 nm channel thickness," *J. Vac. Sci. Technol.*, vol. B22, p. 2366, 2001.

[18] S. J. Angello, "The tyranny of numbers," U.S. Air Force Avionics Lab, 1969.

[19] H. J. Yourke *et al.*, *IEDM Tech. Dig.*, Washington, DC, 1976.

[20] D. R. Herriott *et al.*, "EBES, a practical electron lithographic system," *IEEE Trans. Electron Devices*, vol. 21, pp. 385–392, Jul. 1975.

[21] M. G. R. Thompson *et al.*, "Double aperture method of producing variably-shaped writing spots for electron lithography," *J. Vac. Sci. Technol.*, vol. 15, pp. 891–895, 1978.

[22] M. Sugihara, T. Takata, K. Nakamura, R. Inanami, H. Hayashi, K. Kishimoto, T. Hasebe, Y. Kawano, Y. Matsunaga, K. Murakami, and K. Okumura, "Technology mapping technique for throughput enhancement of character projection equipment," in *Proc. SPIE*, vol. 6151, X. Michael and J. Lercel, Eds., 2006, Emerging Lithographic Technologies, paper 61 510Z-1.

[23] G. I. Winograd *et al.*, "Space-charge induced aberrations," *J. Vac. Sci. Technol.*, vol. B17, pp. 2803–2807, 1999.

[24] T. H. Newman and R. F. W. Pease, "Dot-matrix electron beam lithography," *J. Vac. Sci. Technol.*, vol. B1, pp. 999–1002, Nov./Dec. 1983.

[25] T. H. P. Chang, M. G. R. Thomson, E. Kratschmer, H. S. Kim, M. L. Yu, K. Y. Lee, S. A. Rishton, B. W. Hussey, and S. Zolgharnain, "Electron-beam microcolumns for lithography and related applications," *J. Vac. Sci. Technol.*, vol. B14, pp. 3774–3781, 1996.

[26] T. W. O'Keefe and R. M. Handy, "An electron imaging system for the fabrication of integrated circuits," *Solid State Electron.*, vol. 12, pp. 841–855, Nov. 1969.

[27] T. R. Groves and R. A. Kendall, "Distributed, multiple variable shaped electron beam column for high throughput maskless lithography," *J. Vac. Sci. Technol.*, vol. B16, pp. 3168–3173, 1998.

[28] W. D. Hinsberg, F. A. Houle, M. I. Sanchez, and G. M. Wallraff, "Chemical and physical aspects of the post- exposure baking process used for positive-tone chemically amplified resists," *IBM J. Res. Develop.*, vol. 45, pp. 667–673, 2001.

[29] P. Kruit, "High throughput electron lithography with the multiple aperture pixel by pixel enhancement of resolution concept," *J. Vac. Sci. Technol.*, vol. B16, pp. 3177–3180, 1998.

[30] R. Kaesmaier, H. Löschner, G. Stengl, J. C. Wolfe, and P. Ruchhoeft, "Ion projection lithography: International development program," *J. Vac. Sci. Technol.*, vol. B17, pp. 3091–3097, 1999.

[31] P. Kruit *et al.*, "Predicted effect of shot noise on contact hole dimensions in e-beam lithography," *J. Vac. Sci. Technol.*, vol. 2931, pp. 2931–2935, 2006.

[32] J. N. Randall, L. A. Stern, and J. P. Donnelly, "The contrast of ion beam stencil masks," *J. Vac. Sci. Technol.*, vol. B4, pp. 201–204, 1986.

[33] L. R. Harriott, J. G. Garofalo, and R. L. Kostelak, "Focused-ion-beam repair of phase-shift photomasks," in *Proc. SPIE*, vol. 1671, M. C. Peckerar, Ed., 1992, pp. 224–233.

[34] M. Yamabe, "Present status of x-ray lithography," in *Proc. SPIE*, vol. 3412, N. Aizaki, Ed., 1998, pp. 88–98.

[35] J. Warlaumont, "X-ray lithography; on the road to manufacture," *J. Vac. Sci. Technol.*, vol. B7, pp. 2934–2938, 1989.

[36] J. P. H. Benschop, A. J. J. van Dijsseldonk, W. M. Kaiser, and D. C. Ockwell, "EUCLIDES: European EUVL Program," *J. Vac. Sci. Technol.*, vol. B17, pp. 2978–2981, 1999.

[37] H. Meiling, H. Meijer, V. Banine, R. Moors, R. Groeneveld, H.-J. Voorma, U. Mickan, B. Wolschrijn, B. Mertens, G. van Baars, P. Kürz, and N. Harned, "First performance results of the ASML alpha demo tool," presented at the SPIE Conf., vol. 6151, 2006, paper 61 5108-10.

[38] ITRS, *ITRS roadmap*, (2005). [Online]. Available: http://www.itrs.net/

[39] S. Y. Chou, P. R. Krauss, and P. J. Renstrom, "Imprint of sub-25 Nm vias and trenches in polymers," *Appl. Phys. Lett.*, vol. 67, no. 21, pp. 3114–3116, 1995.

[40] A. Kumar and G. M. Whitesides, "Features of gold having micrometer to centimeter dimensions can be formed through a combination of stamping with an elastomeric stamp and an alkanethiol ink followed by chemical etching," *Appl. Phys. Lett.*, vol. 63, no. 14, pp. 2002–2004, Oct. 4, 1993.

[41] S. Y. Chou, P. R. Krauss, and P. J. Renstrom, "Imprint lithography with 25-nanometer resolution," *Science*, vol. 272, no. 5258, pp. 85–87, 1996.

[42] S. Y. Chou, "Nanoimprint lithography," U.S. Patent 5 772 905, 1998.

[43] S. Y. Chou, "Release surfaces, particularly for use in nanoimprint lithography," U.S. Patent 6 309 580, 2001.

[44] J. Haisma *et al.*, "Mold-assisted nanolithography: A process for reliable pattern replication," *J. Vac. Sci. Technol. B*, vol. 14, no. 6, pp. 4124–4128, 1996.

[45] T. Bailey *et al.*, "Step and flash imprint lithography: Template surface treatment and defect analysis," *J. Vac. Sci. Technol. B*, vol. 18, no. 6, pp. 3572–3577, 2000.

[46] H. Tan, A. Gilbertson, and S. Y. Chou, "Roller nanoimprint lithography," *J. Vac. Sci. Technol. B*, vol. 16, no. 6, pp. 3926–3928, 1998.

[47] M. D. Austin *et al.*, "6 nm half-pitch lines and 0.04 μm^2 static random access memory patterns by nanoimprint lithography," *Nanotechnology*, vol. 16, no. 8, pp. 1058–1061, 2005.

[48] M. T. Li *et al.*, "Pattern transfer fidelity of nanoimprint lithography on six-inch wafers," *Nanotechnology*, vol. 14, no. 1, pp. 33–36, 2003.

[49] S. Y. Chou *et al.*, "Sub-10 nm imprint lithography and applications," *J. Vac. Sci. Technol. B*, vol. 15, no. 6, pp. 2897–2904, 1997.

[50] M. T. Li, L. Chen, and S. Y. Chou, "Direct three-dimensional patterning using nanoimprint lithography," *Appl. Phys. Lett.*, vol. 78, no. 21, pp. 3322–3324, 2001.

[51] S. Y. Chou, P. R. Krauss, and P. J. Renstrom, "Nanoimprint lithography," *J. Vac. Sci. Technol. B*, vol. 14, no. 6, pp. 1–5, 1996.

[52] H. Gao, H. Tan, W. Zhang, K. Morton, and S. Y. Chou, "Air cushion press for excellent uniformity, high-yield, fast nanoimprint across 100 mm field," *Nano Lett.*, 2006.

[53] G. M. Schmid *et al.*, "Implementation of an imprint damascene process for interconnect fabrication," *J. Vac. Sci. Technol. B*, vol. 24, no. 3, pp. 1283–1291, 2006.

[54] W. Wu, B. Cui, X. Y. Sun, W. Zhang, L. Zhunag, and S. Y. Chou, "Large area high density quantized magnetic disks fabricated using nanoimprint lithography," *J. Vac. Sci. Technol. B*, vol. 16, no. 6, pp. 3825–3829, 1998.

[55] M. D. Stewart, S. C. Johnson, S. V. Sreenivasan *et al.*, "Nanofabrication with step and flash imprint lithography," *J. Microlith. Microfab. Microsyst.*, vol. 4, no. 1, Jan.–Mar. 2005, 011002.

[56] I. McMackin, W. Martin, J. Perez, J. Maltabes, S. Johnson, K. Selinidis, D. Resnick, and S. V. Sreenivasan, "Patterned wafer defects density analysis of step-and flash imprint lithogrpaphy," in *Proc. EIPBN*, Denver, CO, May 2007.

[57] S. Y. Chou, C. Keimel, and J. Gu, "Ultra fast and direct imprint of nanostructures in silicon," *Nature*, vol. 417, pp. 835–837, 2002.

[58] Q. F. Xia, Z. N. Yu, H. Gao, and S. Y. Chou, "In situ real time monitoring of nanosecond imprint process," *Appl. Phys. Lett.*, vol. 89, no. 7, 2006.

[59] Z. N. Yu *et al.*, "Fabrication of large area 100 nm pitch grating by spatial frequency doubling and nanoimprint lithography for subwavelength optical applications," *J. Vac.*

Sci. Technol. B, vol. 19, no. 6, pp. 2816–2819, 2001.

[60] M. T. Li *et al.*, "Large area direct nanoimprinting of SiO2-TiO2 gel gratings for optical applications," *J. Vac. Sci. Technol. B*, vol. 21, no. 2, pp. 660–663, 2003.

[61] Z. N. Yu *et al.*, "Fabrication of large area subwavelength antireflection structures on Si using trilayer resist nanoimprint lithography and liftoff," *J. Vac. Sci. Technol. B*, vol. 21, no. 6, pp. 2874–2877, 2003.

[62] M. T. Li *et al.*, "Pattern transfer fidelity of nanoimprint lithography on six-inch wafers," *Nanotechnology*, vol. 14, no. 1, pp. 33–36, 2003.

[63] W. Zhang and S. Y. Chou, "Fabrication of 60-nm transistors on 4-in. wafer using nanoimprint at all lithography levels," *Appl. Phys. Lett.*, vol. 83, no. 8, pp. 1632–1634, 2003.

[64] B. D. Gates *et al.*, "New approaches to nanofabrication: Molding, printing, and techniques," *Chem. Rev.*, vol. 105, no. 4, pp. 1171–1196, 2005.

[65] Y. L. Loo *et al.*, "Additive, nanoscale patterning of metal films with a stamp and a surface chemistry mediated transfer process: Applications in plastic electronics," *Appl. Phys. Lett.*, vol. 81, no. 3, pp. 562–564, 2002.

[66] G. M. Whitesides, J. P. Mathias, and C. T. Seto, "Molecular self-assembly and nanochemistry—A chemical strategy for the synthesis of nanostructures," *Science*, vol. 254, no. 5036, pp. 1312–1319, 1991.

[67] G. H. Fredrickson and F. S. Bates, "Dynamics of block copolymers: Theory and experiment," *Annu. Rev. Mater. Sci.*, vol. 26, pp. 501–550, 1996.

[68] M. Park *et al.*, "Block copolymer lithography: Periodic arrays of similar to 10(11) holes in 1 square centimeter," *Science*, vol. 276, no. 5317, pp. 1401–1404, 1997.

[69] J. Y. Cheng *et al.*, "Templated self-assembly of block copolymers: Effect of substrate topography," *Adv. Mater.*, vol. 15, no. 19, p. 1599, 2003.

[70] J. Y. Cheng *et al.*, "Pattern registration between spherical block-copolymer domains and topographical templates," *Adv. Mater.*, vol. 18, no. 5, p. 597, 2006.

[71] C. T. Black and O. Bezencenet, "Nanometer-scale pattern registration and alignment by directed diblock copolymer self-assembly," *IEEE Trans. Nanotechnol.*, vol. 3, pp. 412–415, Sep. 2004.

[72] C. T. Black, "Self-aligned self assembly of multi-nanowire silicon field effect transistors," *Appl. Phys. Lett.*, vol. 87, no. 16, p. 163 116, 2005.

[73] M. P. Stoykovich, M. Muller, S. O. Kim *et al.*, "Directed assembly of block copolymer blends into nonregular device-oriented structures," *Science*, vol. 308, no. 5727, pp. 1442–1446, 2005.

[74] B. Honeisen and C. A. Mead, "Fundamental limits of scaling electronics II MOS," *Solid State Electron.*, Jul. 1972.

[75] R. H. Dennard, F. H. Gaensslen, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *J. Solid-State Circuits*, vol. SC-9, pp. 256–268, 1974.

[76] H. Sewell, J. Mulkens, D. McCafferty, L. Markoya, B. Streefkerk, and P. Graeupner, "The next phase for immersion lithography," in *Proc. SPIE*, vol. 6154, D. G. Flageilo, Ed., 2006, Optical Microlithography XIX, paper 615 406-1.

[77] H. C. Pfeiffer *et al.*, "Variable spot shaping for electron-beam lithography," *J. Vac. Sci. Technol.*, vol. 15, pp. 887–890, 1978.

[78] E. Goto, T. Soma, and M. Idesawa, "Design of a variable-aperture projection and scanning system for electron beam," *J. Vac. Sci. Technol.*, vol. 15, pp. 883–886, 1978.

[79] J. Trotel, "Dynamic beam shaping," *J. Vac. Sci. Tech.*, vol. 15, pp. 872–873, 1978.

[80] L. Han, R. F. Pease, W. D. Meisburger, G. I. Winograd, and K. Takahashi, "Scaled measurements of global space-charge induced image blur in electron beam projection system," *J. Vac. Sci. Technol.*, vol. B18, pp. 2999–3003, 2000.

[81] D. S. Pickard, T. R. Groves, W. D. Meisburger, T. Crane, and R. F. Pease, "Distributed axis electron beam technology for maskless lithography and defect inspection," *J. Vac. Sci. Technol.*, vol. B21, pp. 2834–2838, 2003.

[82] U. Okoroanyanwu and J. H. Lammers, "Resist road to the 22 nm technology node," *Future Fab Intl.*, vol. 17, Jun. 21, 2004. [Online]. Available: http://www.future-fab.com/documents.asp?d_ID=2614

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