Load-Independent Class E/EF Inverters and Rectifiers for MHz-Switching Applications

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***Abstract*—This paper presents a unified framework for the modeling, analysis, and design of load-independent Class E and Class EF inverters and rectifiers. These circuits are able to maintain zero-voltage switching and, hence, high efficiency for a wide load range without requiring tuning or use of a feedback loop, and to simultaneously achieve a constant amplitude ac voltage or current in inversion and a constant dc output voltage or current in rectification. As switching frequencies are gradually stepping into the megahertz (MHz) region with the use of wide-bandgap (WBG) devices such as GaN and SiC, switching loss, implementing fast control loops, and current sensing become a challenge, which load-independent operation is able to address, thus allowing exploitation of the high-frequency capability of WBG devices. The traditional Class E and EF topologies are first presented, and the conditions for load-independent operation are derived mathematically; then, a thorough analytical characterization of the circuit performance is carried out in terms of voltage and current stresses and the power-output capability. From this, design contours and tables are presented to enable the rapid implementation of these converters given particular power and load requirements. Three different design examples are used to showcase the capability of these converters in typical MHz power conversion applications using the design equations and methods presented in this paper. The design examples are chosen toward enabling efficient and high-power-density MHz converters for wireless power transfer (WPT) applications and dc/dc conversion. Specifically, a 150-W 13.56-MHz Class EF inverter for WPT, a 150-W 10-MHz miniature Class E boost converter, and a lightweight wirelessly powered drone using a 20-W 13.56-MHz Class E synchronous rectifier have been designed and are presented here.**

***Index Terms*—DC-AC power converters, resonant inverters, wireless power transmission, zero voltage switching.**

I. Introduction

THE full exploitation of wide-bandgap (WBG) devices is driving the design of ever higher frequency converters extending well into the megahertz (MHz) region, but, with conventional topologies, this creates further design challenges such as high switching loss, the requirement for fast control loops, and high-bandwidth low-insertion loss current sensing. Load-independent Class E/EF converters are an effective and simple solution to these challenges, as they require no additional circuitry and are intrinsically efficient. They can be used in high-frequency conversion tasks, such as high-density dc/dc conversion, wireless power transfer (WPT), and radio-frequency (RF) amplification. These circuit topologies are particularly suited to high-frequency operation due to their use of a single low-side switch and soft switching operation. However, traditional implementations of Class E/EF topologies only achieve soft switching for a specific load and, hence, suffer a reduction in efficiency when operating with a varying load. Additionally, they are unable to operate at open-circuit or short-circuit load conditions. A load-independent solution for the Class E converter, which achieves soft switching over a wide load range [1], is known, but has limitations, particularly, that the input-to-output voltage ratio is always 1.45, and the circuit can only be designed to provide a constant output ac voltage, whereas there are some applications in which having a constant output ac current is beneficial. The recent wide availability of WBG power devices and the strong interest in applications such as wireless power warrants revisiting the load-independent Class E topology and the further investigation of load-independent implementations of the Class EF topology.

In this paper, in Sections III and IV, we present the analysis of Class E and EF inverters and rectifiers, deriving the criteria for load-independent operation, investigating component stresses as a function of load condition, and presenting design equations using a common analytical approach for all the topologies for inversion and rectification. Then, in Section V, three prototype examples are described utilizing WBG load-independent circuits, which enable efficient power conversion for applications such as MHz wireless power and dc/dc conversion. A wirelessly powered drone, operating with significant changes in the inverter load (due to changes in air gap geometry and throttle setting as the drone flies), highlights the efficient and load-independent operation of Class E and Class EF converters.

II. Background

Several approaches are available to enable zero-voltage switching (ZVS) and zero-derivative voltage switching opera-

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tion of Class E and EF inverters for a range of loads. One possibility is to actively tune the inverter as the load changes, and there have been attempts to tune the Class E inverter by using saturable reactors and varactors [2]. While these methods can increase the load range that Class E inverters can tolerate, they require a control loop and tuning elements. Furthermore, the tuning elements can limit the Class E inverter power-handling capability and efficiency.

Alternatively, it is possible to design the Class E inverter for load independence by careful choice of component values. The theoretical concept of load independence for Class E inverters was first introduced by Zulinski and Grady [1] in 1990 by showing that the Class E inverter can maintain ZVS and a constant output voltage amplitude and phase as the load varies from a finite resistance to infinite resistance without tuning or feedback control and, therefore, sustain a high efficiency. Further work was carried out in [3] and recently in [4] and [5] to extend the concept to Class EF inverters. Since it was introduced, the concept of load independence has not seen wide implementation in power conversion and amplification, since the majority of power converters operate at kilohertz frequencies using typical hard-switched topologies that are inherently load independent, and RF amplifiers are normally designed to be matched to a fixed 50-Ω load. However, emerging technologies such as WPT benefit from operating at MHz switching frequencies and require high power efficiencies [6] across a wide load range. Load-independent Class E/EF converters are ideal candidates for sustaining the required high efficiency, while also achieving a regulated output voltage or current.

Class E/EF rectifiers are well known and have been covered extensively in the literature. The majority of these rectifiers use a diode for rectification, which allows the rectifier to operate over a wide dc load range. Synchronous Class E/EF rectifiers that use a MOSFET can operate at a higher efficiency, however, at a narrow load range and at the expense of increased circuit complexity. In both cases, the output dc voltage is not regulated and ZVS is lost as the load varies from its optimum value. ON–OFF or hysteresis control methods can be used to provide output voltage regulation against variations in the load current, as shown in [7]. While ON–OFF or hysteresis control can achieve good regulation, it increases the complexity of the converter and can be difficult to implement efficiently at tens of MHz especially if isolation is required. In WPT applications, transferring the synchronization and feedback signals over the isolation barrier or the air gap may be difficult to implement. Recent work in [8] shows a design solution for implementing a practical complete WPT system for powering a television. The described system consists of five conversion stages; regulation was achieved by using a SEPIC converter preregulator with a variable dc output at the transmitting side, and a dc/dc converter postregulator on the receiving side. A 916-MHz FM radio transceiver was used to implement the feedback loop over the wireless link to provide dc output voltage regulation. By using a load-independent inverter and rectifier design solution, the WPT system will have an inherently regulated output dc voltage without having any feedback loops, making the system less complex and more efficient as multiple preregulating and postregulating dc/dc conversion stages will not be required.

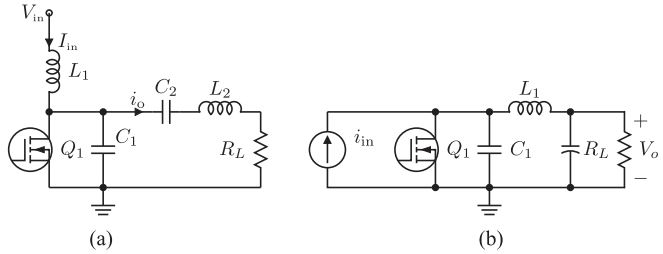

Fig. 1. Class E with the finite dc choke topology. (a) Inverter. (b) Rectifier.

III. Class E With the Finite Choke Topology

Beginning with the Class E topology, Fig. 1(a) and (b) shows the circuit diagrams of the Class E inverter and rectifier, respectively. The specific Class E topology considered in this work is the Class E topology with a finite dc choke.

A. Class E Inversion

The mathematical analysis of the Class E inverter has been widely covered in the literature [9]–[11]; therefore, only a summary of the equations that will be used to derive the load-independent conditions will be discussed and presented in this section.

The output current i_o of the inverter with a high loaded Q factor is sinusoidal and is given by

$$i_o(\omega t) = I_m \sin(\omega t + \phi) \tag{1}$$

where I_m is the output current's magnitude and ϕ is its phase. In rectification, (1) represents the input ac current. It is assumed that the switch is ON for the period $0 \leq \omega t < 2\pi D$ and OFF for the period $2\pi D \leq \omega t < 2\pi$. The equations of interest are those that describe the voltage across the switch, the load resistor R_L, and the residual reactance X in the output load network. The switch voltage normalized with respect to the input dc voltage V_{in} is given by [9], [11]

$$\frac{v_{\text{DS}}(\omega t)}{V_{\text{in}}} = \frac{I_m}{\omega C_1 V_{\text{in}}} \int_{2\pi D}^{\omega t} \frac{i_{C_1}(\tau)}{I_m} d\tau = q^2 p \beta(\omega t) \tag{2}$$

where

$$\beta(\omega t) = \int_{2\pi D}^{\omega t} \frac{i_{C_1}(\omega t)}{I_m} d\omega t \tag{3}$$

$$q = \frac{1}{\omega \sqrt{L_1 C_1}} \tag{4}$$

and

$$p = \frac{\omega L_1 I_m}{V_{\text{in}}}. \tag{5}$$

Parameter q represents the ratio of the resonant frequency of the finite choke L_1 and shunt capacitor C_1 to the switching frequency. The parameter p is considered the loading factor. It represents the ratio of the amplitude of the load current I_m

to the input dc voltage. The parameter p increases as the load resistance decreases and vice versa. Thus, p is always a positive real number.

The voltage across the load resistor and the residual reactance can be obtained by calculating the first Fourier components of the switch voltage and are given by

$$\frac{v_{R_L}}{V_{\text{in}}} = \frac{1}{\pi}\int_{2\pi D}^{2\pi} \frac{v_{\text{DS}}(\omega t)}{V_{\text{in}}} \sin(\omega t + \phi) d\omega t = \frac{q^2 p}{\pi}\int_{2\pi D}^{2\pi} \beta(\omega t)\sin(\omega t + \phi) d\omega t = \frac{q^2 p}{\pi}\psi_1 \quad (6)$$

$$\frac{v_{jX}}{V_{\text{in}}} = \frac{1}{\pi}\int_{2\pi D}^{2\pi} \frac{v_{\text{DS}}(\omega t)}{V_{\text{in}}} \cos(\omega t + \phi) d\omega t = \frac{q^2 p}{\pi}\int_{2\pi D}^{2\pi} \beta(\omega t)\cos(\omega t + \phi) d\omega t = \frac{q^2 p}{\pi}\psi_2. \quad (7)$$

The complete derivation of these equations can be found in [9].

1) Effect of Load Variation in the Classic Class E Inverter: Raab [12] has showed a detailed analysis of how the conventional Class E inverter performs as circuit parameters, mainly the load resistance, vary from their optimum values. Fig. 2 shows the effect of the load resistance varying by 25% above and below the optimum load. It can be noticed that ZVS is lost, once the load varies above or below its optimum value. For higher load resistances, the switch turns ON at a positive voltage, which discharges the capacitor C_1 through the switch resulting in a large current spike. In practice, the current spike results in energy being lost in the switch ON resistance, which then degrades the overall efficiency. It can also cause damage to the switch if its value exceeds the switch's current rating. The same occurs when the load resistance is below its optimum value. However, since a MOSFET is commonly used in such circuits, its intrinsic body diode begins to conduct once the MOSFET's drain-to-source voltage crosses 0 V and exceeds the forward bias voltage of the body diode. The current spike has a much lower magnitude here, since the diode's forward voltage is low, 0.4–2 V for Si and SiC devices and $>$ 2 V for GaN devices. Nevertheless, the overall efficiency will still degrade. Furthermore, in all cases, the output voltage across the resistor R_L will change as its value changes.

2) Load-Independent Operation Criteria: As shown above, the efficiency and performance of the conventional Class E inverter degrade as the load varies from its optimum value. The concept of load-independence allows Class E inverters and rectifiers to maintain efficient operation and maintain output voltage regulation across a wide load range by relaxing the optimum switching conditions to ZVS only. That is, the switch turns ON at zero voltage only at a positive or negative voltage derivative. In order to derive the conditions for load independence, the following criteria should be met regardless of the load value.

1) *Constant output ac voltage:* The parameter p defined in (5) was referred to as the loading parameter. Referring to (6), achieving a constant output voltage against any load variations means the parameters of the circuit, mainly the phase ϕ, should be constant for any value of p (i.e., independent of p). This criterion means that the rate of change of (6) with respect to p should be zero; this can be represented by

$$\frac{\partial}{\partial p}\left(\frac{q^2 p}{\pi}\psi_1\right) = \frac{q^2}{\pi}\frac{\partial p\psi_1}{\partial p} = 0 \text{ over range of } p. \quad (8)$$

2) *Constant switching at zero voltage:* ZVS or "high-efficiency" operation can be achieved by setting the switch voltage in (2) to zero, which produces the following equation:

$$\beta(2\pi) = 0 \text{ over } \mathbb{D}_p. \quad (9)$$

Equations (8) and (9) can now be solved for the values q and ϕ that result in load-independent ZVS and constant output voltage. Fig. 3 shows the voltage and current waveforms of the load-independent Class E inverter for different load resistances. It can be seen that ZVS and constant output voltage are maintained as the load resistance changes from 50% of its nominal value to an open-circuit condition.

Since now the independence of parameters q and ϕ on p has been established, the product of $p\psi_1$ in (6) is always constant for a given solution set of q, ϕ, and D. Hence, the output voltage is also always constant and only a function of q, ϕ, and D.

From (5) and (7), the voltage across the residual reactance X can be written as

$$\frac{v_{jX}}{V_{\text{in}}} = \frac{q^2 p}{\pi}\psi_2(q, p, \phi, D) = \frac{i_m X}{V_{\text{in}}} = p\frac{X}{\omega L_1}.$$

For a given design, the value of X will also be fixed and independent of the load. Therefore, the function ψ_2 can only be dependent on q, ϕ, and D. As a result, the residual reactance X normalized to ωL_1 for given solution set of q, ϕ, and D is

$$\frac{X(q, \phi, D)}{\omega L_1} = \frac{q^2}{\pi}\psi_2(q, \phi, D). \quad (10)$$

Table I lists the solutions for q and ϕ at different duty cycle values, in addition to the normalized values of the residual reactance and the normalized amplitude of the output ac voltage.

TABLE I
SOLUTIONS OF q AND ϕ FOR A LOAD-INDEPENDENT CLASS E INVERTER AT DIFFERENT DUTY CYCLE VALUES

D	q	ϕ	$\frac{X}{\omega L_1}$	$\frac{v_{R_L}}{V_{\text{in}}}$
0.40	1.1537	3.4557	0.5054	1.4407
0.45	1.2143	3.2987	0.3701	1.5161
0.50	1.2915	3.1416	0.2663	1.5895
0.55	1.3902	2.9845	0.1867	1.6596
0.60	1.5176	2.8274	0.1264	1.7255

B. Class E Rectification

In rectification, the equations that have been derived for inversion can be applied here. The solutions that have been found for inversion, whether for the basic operation or load-independent operation, are also applicable in rectification. The solved values of q in inversion are the same in rectification, and the solved

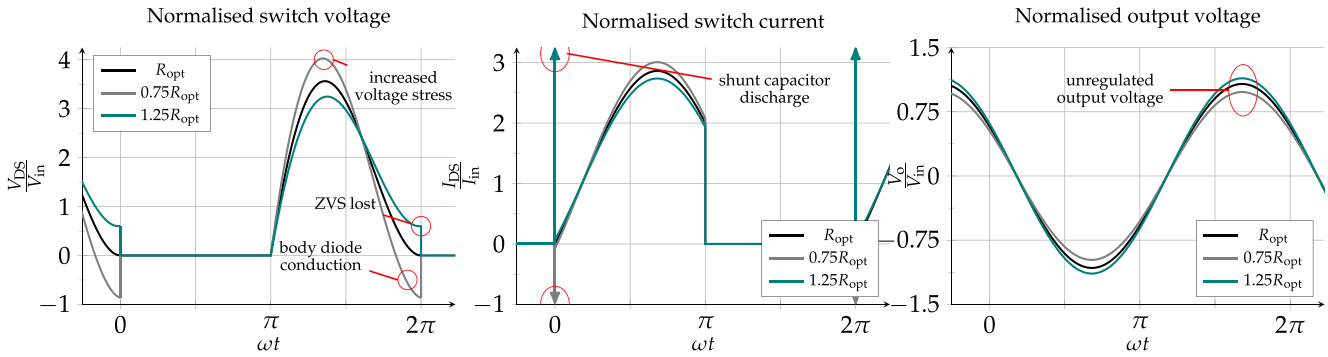

Fig. 2. Voltage and current waveforms of the conventional Class E inverter as the load changes by ± 25% from the optimum load value. ZVS is lost, discharge of the shunt capacitor occurs, and the amplitude of the output ac voltage varies.

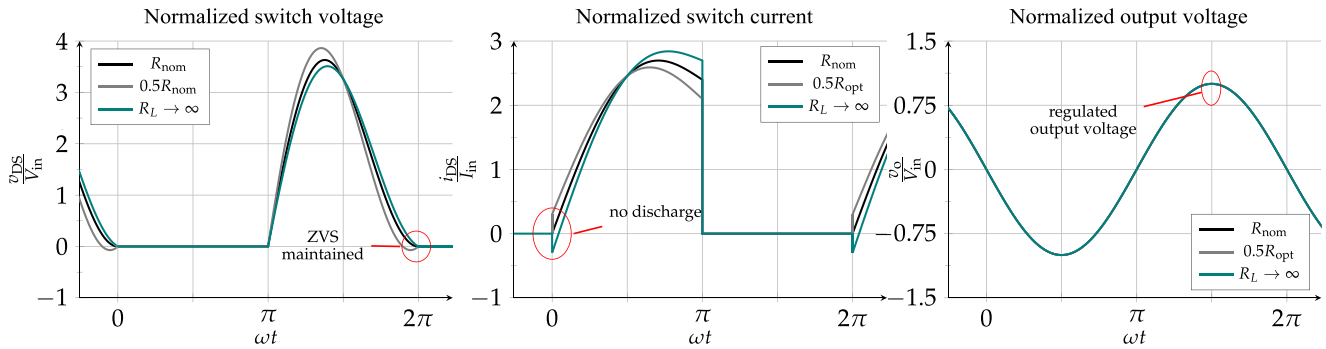

Fig. 3. Voltage and current waveforms of the load-independent Class E inverter as the load changes from open circuit to 50% of the nominal load resistance value. ZVS is maintained, no discharge of the shunt occurs, and the amplitude and phase of the output ac voltage are constant.

values of the phase ϕ for inversion need to be adjusted for rectification as follows:

$$\phi_{\rm rec} = 2\pi(1-D) - \phi_o. \tag{11}$$

It should be noted the Class E rectifier generates a output dc current if the input is a constant ac current source and generates a output dc voltage if the input is a constant ac voltage source with a series LC circuit interface, as shown in [13].

1) Effect of DC Load Variation: Fig. 4 shows how the voltage and current waveforms of the conventional Class E rectifier with a diode vary as the dc load resistance changes from 50% to 500% of its optimum value. The optimum operation for the maximum power-output capability is when the duty cycle of operation is 50%. It can be seen that the duty cycle increases for higher load resistances and decreases for lower load resistances. Additionally, the normalized amplitude and phase of the input current are also affected, which means that the rectifier's output dc voltage or current will vary with load. Similarly, Fig. 5 shows how the voltage and current waveforms are affected when an ideal switch is employed. The duty cycle is fixed at 50%. It can be seen that ZVS is lost as the load resistance changes and discharge of the shunt capacitor occurs. The normalized amplitude of the input current also changes, and consequently, the output will change. The Class E rectifier with either a diode or switch cannot cope with an open-circuit condition and does not provide output regulation.

2) Load-Independent Operation: The criteria to achieve load-independent operation for Class E rectification are the same as the Class E inversion [see (8) and (9)]. Fig. 6 shows the voltage and current waveforms of the Class E rectifier at load-independent operation. It can be noticed that the circuit maintains ZVS at all times. The input current's magnitude and phase remain constant, which means that the output voltage or current will be constant for any load; additionally, the input reactance of the rectifier will also be constant for any load. It can also be noticed that when the load resistance increases above its optimum value, the current through the switch is negative when it is turned OFF at $2\pi D$. Therefore, a switch capable of allowing positive and negative current to flow, such as a MOSFET, must be used. Diodes cannot be used here. The solutions for load-independent Class E rectification can obtained from Table I by adjusting the phase according to (11) and taking the reciprocal of the last column for the normalized output dc voltage.

3) Input Impedance: The input ac resistance of the load-independent Class E rectifier can be calculated using (5) and (6) as follows:

$$\frac{i_m R_{\rm AC}}{V_o} = \frac{q^2 \omega L_1 I_m \psi_1}{\pi V_o}. \tag{12}$$

Consequently, the normalized input ac resistance is

$$\frac{R_{\rm AC}}{\omega L_1} = \frac{q^2}{\pi}\psi_1. \tag{13}$$

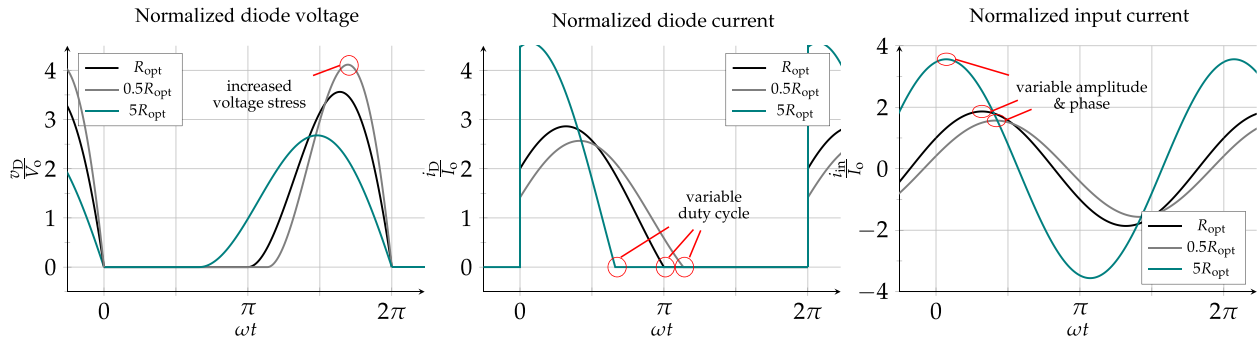

Fig. 4. Voltage and current waveforms of the conventional Class E rectifier with an ideal diode as the dc load resistance changes from 50% to 500% of its optimum value. The duty cycle deviates from its designed value of 50%, and the input current's normalized amplitude and phase vary; therefore, the dc output is not regulated.

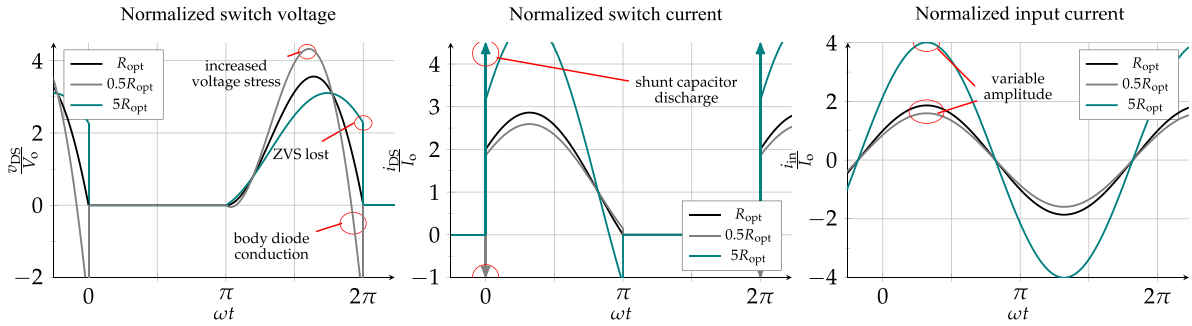

Fig. 5. Voltage and current waveforms of the conventional Class E rectifier with an ideal switch as the dc load resistance changes from 50% to 500% of its optimum value. ZVS is lost, discharge of the shunt capacitor occurs, and the input current's normalized amplitude varies; therefore, the dc output is not regulated.

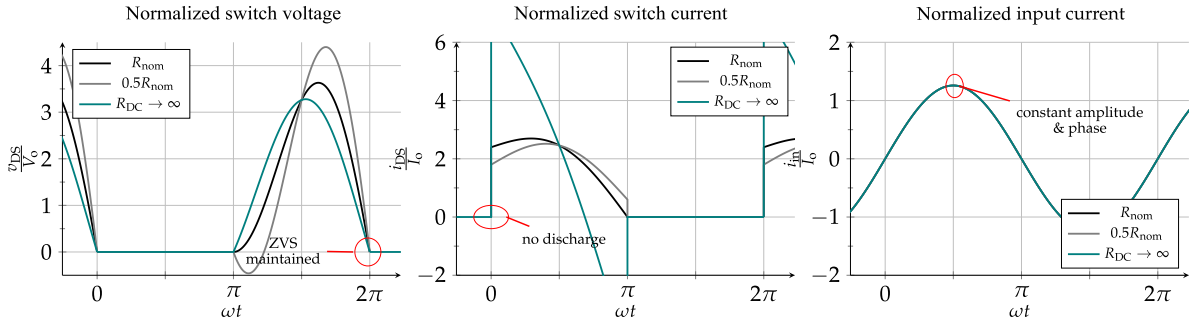

Fig. 6. Voltage and current waveforms of the load-independent Class E rectifier as the load resistance varies from 50% of its nominal value to an open-circuit condition. ZVS is maintained, no discharge occurs, and the input current's normalized amplitude and phase remain constant; therefore, the dc output is regulated.

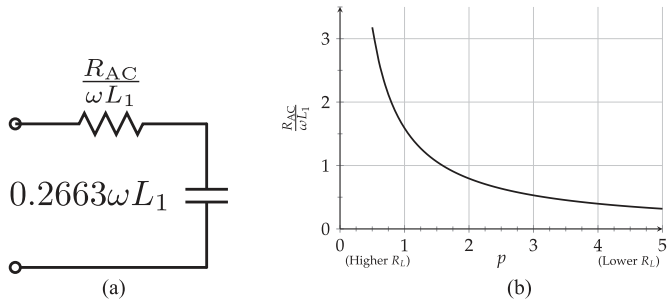

Fig. 7. Normalized input impedance of the load-independent Class E rectifier as a function of load at 50% duty cycle operation. The normalized input reactance is constant ($0.2663\omega L_1$) for all loads. (a) Equivalent circuit. (b) Normalized input ac resistance.

The input ac reactance of the load-independent Class E rectifier is equal to the residual reactance of the load-independent Class E inverter and, therefore, is constant for any dc load. The normalized input ac reactance, which will be capacitive, can be obtained from Table I. Fig. 7 shows the equivalent circuit diagram of the load-independent Class E rectifier and how the input ac resistance varies with the load when operating at a 50% duty cycle.

C. Voltage and Current Stresses

Fig. 8 shows how the peak switch voltage and current and the power-output capability vary as a function of the loading

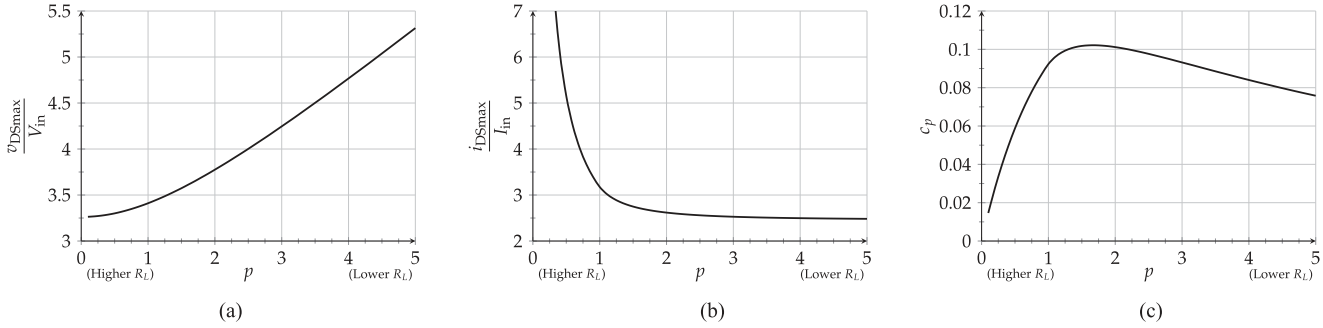

Fig. 8. Variation of voltage and current stresses of the load-independent Class E inverter/rectifier with loading at 50% cycle operation. (a) Normalized peak drain voltage. (b) Normalized peak drain current. (c) Power-output capability.

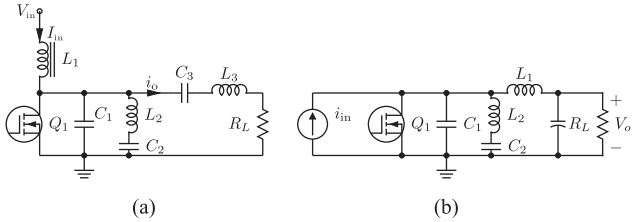

Fig. 9. Class EF topology with an infinite choke for inversion and rectification. (a) Class EF inverter. (b) Class EF rectifier.

parameter p at 50% duty cycle operation. The normalized peak switch voltage is approximately 3.25 at low values of p, which occurs at a high load resistance or open-circuit condition and rises to more than 5 as p increases when the load resistance is reduced. The normalized peak switch current is large at low values of p and decreases to approximately 2.5 as the loading increases. The power-output capability is above 0.1 for p values between 1 and 2; therefore, it is recommended that the load-independent Class E inverter and rectifier be designed to operate within this range at nominal loads.

IV. Class EF Topology

Fig. 9 shows the circuit diagrams of the Class EF inverter and the Class EF rectifier. Unlike the Class E with the finite choke topology, the Class EF topology here uses an infinite choke. Inductor L_2 and capacitor C_2 are tuned to a frequency in between the switching frequency and the second harmonic of the switching frequency. The ratio of the resonant frequency of L_2C_2 to the switching frequency is represented by parameter q_1 and is given by

$$q_1 = \frac{1}{\omega\sqrt{L_2C_2}}. \tag{14}$$

A. Class EF Inversion

In [14] and [15], a detailed analysis was performed on Class EF*n* inverters, and the general forms of the equations that describe the voltages and currents of the inverter were derived. Here, we will only present the final form of the equations that will be used to specify the conditions for load-independent operation. Referring to Fig. 9(a), similar to the Class E inverter, the output current i_o is sinusoidal and is given in (1). It is assumed that the switch is ON for the period $0 \le \omega t < 2\pi D$ and OFF for the period $2\pi D \le \omega t < 2\pi$. Beginning with the series L_2C_2 network, its current is given by

$$\frac{i_{L_2}}{I_{\text{in}}}(\omega t) = A_2\cos(q_2\omega t) + B_2\sin(q_2\omega t) - \frac{q_2^2 p}{q_2^2-1}\sin(\omega t+\phi) + \frac{1}{k+1} \tag{15}$$

where

$$k = \frac{C_1}{C_2} \tag{16}$$

$$q_2 = \frac{1}{\omega}\sqrt{\frac{C_1+C_2}{L_2C_1C_2}} = q_1\sqrt{\frac{k+1}{k}} \tag{17}$$

$$p = \frac{C_2}{C_1+C_2}\frac{I_m}{I_{\text{in}}} = \frac{1}{k+1}\frac{I_m}{I_{\text{in}}} \tag{18}$$

and the coefficients A_2 and B_2 are determined based on the equation's boundary conditions, which are the continuation of current and voltage when the circuit transition to the ON and OFF states. Similar to the Class E topology, the parameter p here is referred to as the loading parameter. The current in capacitor C_1 is given by

$$\frac{i_{C_1}}{I_{\text{in}}}(\omega t) = 1 - p(k+1)\sin(\omega t+\phi) - \frac{i_{L_2}}{I_{\text{in}}}(\omega t). \tag{19}$$

The drain voltage for the period $2\pi D \le \omega t < 2\pi$ is given by

$$\frac{v_{DS}(\omega t)}{V_{\text{in}}} = 2\pi\frac{\beta(\omega t)}{\alpha} \tag{20}$$

where

$$\beta(\omega t) = \int_{2\pi D}^{\omega t}\frac{i_{C_1}}{I_{\text{in}}}(\tau)d\tau \tag{21}$$

and

$$\alpha = \int_{2\pi D}^{2\pi}\beta(\omega t)d\omega t. \tag{22}$$

The voltage across the load resistor and the residual impedance in the output load network is given by

$$\frac{v_{R_L}}{V_{\text{in}}} = \frac{2}{\alpha}\int_{2\pi D}^{2\pi} \beta(\omega t)\sin(\omega t+\phi)d\omega t = \frac{2}{\alpha}\psi_1 \tag{23}$$

$$\frac{v_{jX}}{V_{\text{in}}} = \frac{2}{\alpha}\int_{2\pi D}^{2\pi} \beta(\omega t)\cos(\omega t+\phi)d\omega t = \frac{2}{\alpha}\psi_2. \tag{24}$$

1) Effect of Load Variation: Fig. 10 shows the effect of the load resistance varying by 25% above and below the optimum load for a Class EF_2 inverter. It can be noticed that ZVS is lost once the load varies above or below its optimum value. The same consequences and effects of load variation in the conventional Class E inverter also apply here as well. Increasing load resistances cause the switch to turn ON at a positive voltage, and decreasing load resistances result in inefficient body diode conduction. The output load current will vary as the load resistance changes.

2) Load-Independent Operation Criteria: It has been shown that the efficiency and performance of the conventional Class EF inverter degrade when the load varies from its optimum value. Similar to the load-independent operation of the Class E inverter and rectifier, load independence allows the Class EF inverter and rectifier to maintain efficient operation and maintain output current regulation across a wide the load range by relaxing the optimum switching conditions to ZVS only. The following criteria are to be met regardless of the load value.

1) *Constant output ac current:* Equation (23) can be written in the form

$$\frac{2}{\alpha(p)}\psi_1(p) = \frac{I_m R_L}{V_{\text{in}}} = \frac{I_m}{I_{\text{in}}}\frac{R_L}{R_{\text{in}}}. \tag{25}$$

Since it has been assumed that there are no losses in the circuit, all the power supplied by the input voltage is consumed in the load. The following equation can be obtained:

$$\frac{R_L}{V_{\text{in}}I_{\text{in}}} = \frac{2}{\left(\frac{I_m}{I_{\text{in}}}\right)^2}. \tag{26}$$

Substituting the above in (25) and using (18) gives

$$p\frac{\psi_1(p)}{\alpha(p)} = \frac{1}{(k+1)}. \tag{27}$$

In a similar way to the Class E topology, achieving a constant output current against any load variations means the parameters of the circuit, mainly the phase ϕ, should be constant for any value of p (i.e., independent of p). This criterion means that the rate of change of (27) with respect to p should be zero; this can be represented by

$$\frac{\partial}{\partial p}\left(p\frac{\psi_1(p)}{\alpha(p)}\right) = 0 \ \text{ over } \mathbb{D}_p. \tag{28}$$

2) *Constant switching at zero voltage:* ZVS or "high-efficiency" operation can be achieved by setting the switch voltage in (20) to zero, which produces the following equation:

$$\beta(2\pi) = 0 \ \text{ over } \mathbb{D}_p. \tag{29}$$

Equations (28) and (29) can now be solved for the values of k and ϕ that will result in load-independent ZVS and constant output current. Further details on the method used to obtain the solutions and a discussion of the solutions in addition to design equations will be provided in the following sections. Fig. 11 shows the voltage and current waveforms of the load-independent Class EF inverter at different load resistance values. It can be seen that ZVS and constant output current are maintained as the load resistance changes from its nominal value to a short-circuit condition.

The value of capacitor C_1 at a nominal load is

$$\frac{1}{\omega R_L C_1} = \frac{\pi p^2(k+1)^2}{\alpha(p)}. \tag{30}$$

For a given design, the value of the residual reactance X will also be fixed and independent of the load. Therefore, function ψ_2 can only be dependent on q_1, k, ϕ, and D. As a result, the reactance X normalized to ωC_1 for a given solution set of q_1, k, ϕ, and D is

$$\omega X C_1 = \frac{1}{\pi p(k+1)}\psi_2(q_1,k,\phi,D). \tag{31}$$

Finally, the output current for a desired p and load resistance is

$$I_m = 2\frac{\psi_1(p)}{\alpha(p)}\frac{V_{\text{in}}}{R_L}. \tag{32}$$

B. Class EF Rectification

In rectification, the equations that have been derived for the Class EF inverter can be applied here. The solutions that have been found for inversion, whether for the basic operation or load independent operation, are also applicable in rectification. The solved values of q_1 are the same as those for inversion, and the solved values of the phase ϕ for inversion need to be adjusted as follows:

$$\phi_{\text{rec}} = \pi + 2\pi(1-D) - \phi_o. \tag{33}$$

1) Effect of Load Variation: Figs. 12 and 13 show how the voltage and current waveforms vary as the load changes of the Class EF_2 rectifier employing an ideal diode and an ideal switch, respectively. The same observations and conclusion made for the Class E rectifier can be applied here as well; the dc output will change as the load varies.

2) Load-Independent Operation: The criteria to achieve load-independent operation for Class EF rectifiers are the same as those of Class EF inverters, and the solutions obtained can be applied here. Fig. 14 shows the voltage and current waveforms of the Class EF rectifier at load-independent operation. The rectifier maintains ZVS at all loads. The input current's magnitude and phased remain constant, which means that the output current can be kept constant for any load, and the input reactance of the rectifier is always constant for any load. It can also be noticed that when the load resistance increases above its optimum value, the current through the rectifying element is negative when it is turned OFF at $2\pi D$. Similar to the load-independent Class E rectifier, a switch capable of allowing positive and negative current to flow must be used.

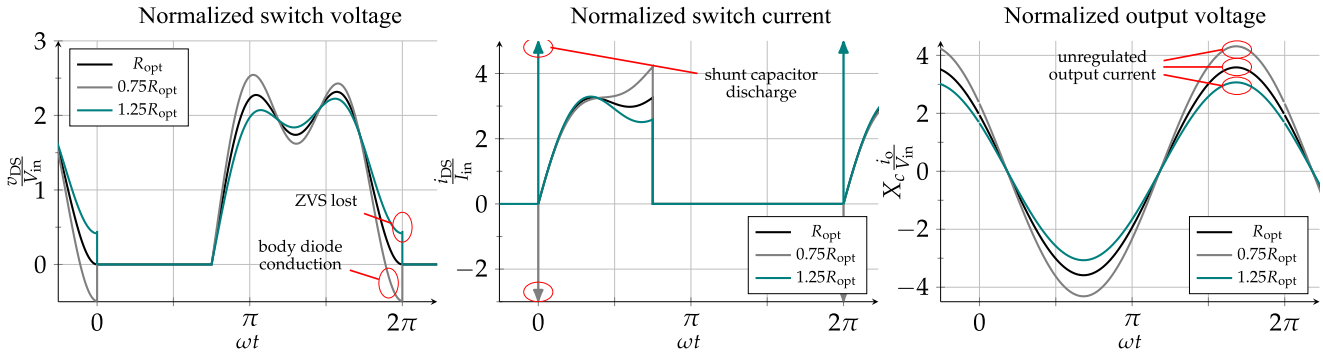

Fig. 10. Voltage and current waveforms of the Class EF_2 inverter as the load changes by $\pm$ 25% from the optimum load value. ZVS is lost, discharge of the shunt capacitor occurs, and the amplitude of the output ac current varies.

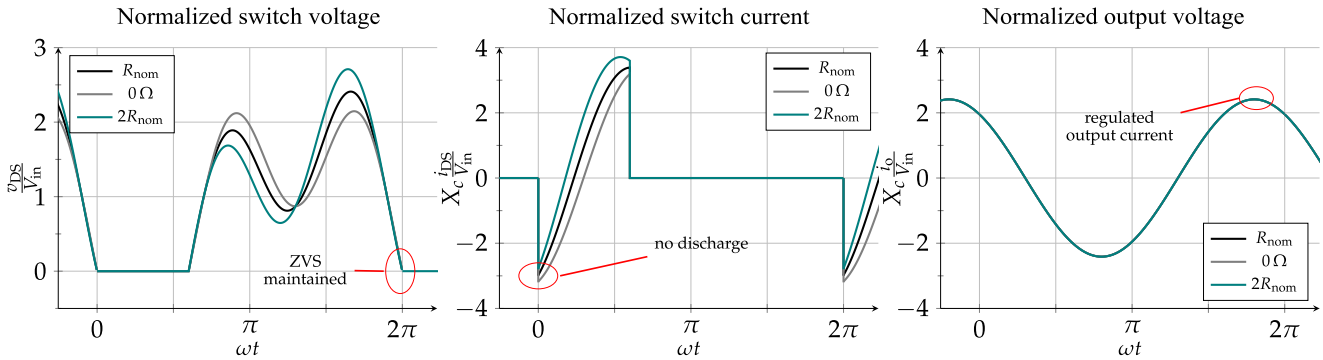

Fig. 11. Voltage and current waveforms of the load-independent Class EF inverter as the load resistance changes from 200% of its nominal value to a short-circuit condition. ZVS is maintained, no discharge of the shunt occurs, and the amplitude and phase of the output ac current are constant.

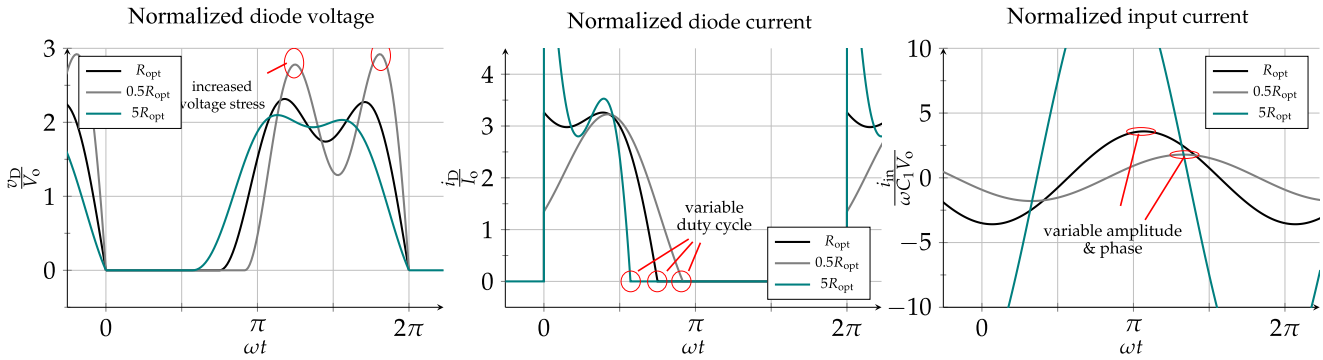

Fig. 12. Voltage and current waveforms of the Class EF_2 rectifier with an ideal diode as the dc load resistance changes from 50% to 500% of its optimum value. The duty cycle deviates from its designed value of 50% and the input current's normalized amplitude and phase vary; therefore, the dc output is not regulated.

3) Input Impedance: The equivalent circuit of the load-independent Class EF rectifier is the same as that of the load-independent Class E rectifier in Fig. 7(a). The input ac resistance normalized to ωC_1 can be obtained by taking the reciprocal of (30). The input reactance, which is capacitive and constant for all loads, can be obtained by taking the reciprocal of (31).

C. Performance Evaluation and Practical Considerations

The design process begins by setting choosing a value of q_1 and duty cycle and then solving (28) and (29) for k and ϕ. A value is then set for p that will correspond to the maximum load resistance requirement. Using (22)–(24), the parameters α, ψ_1, and ψ_2 are then calculated, from which the values of the components can then be worked out from (16), (30), and (31). Finally, the required input voltage for a particular output load current is calculated from (32).

Solving (28) and (29) results in an infinite set of solutions for load-independent operation. However, not all of these solutions are practical. It is, therefore, necessary to investigate the performance of the inverter for each solution. The performance will be judged depending on the waveform of the drain voltage, the peak

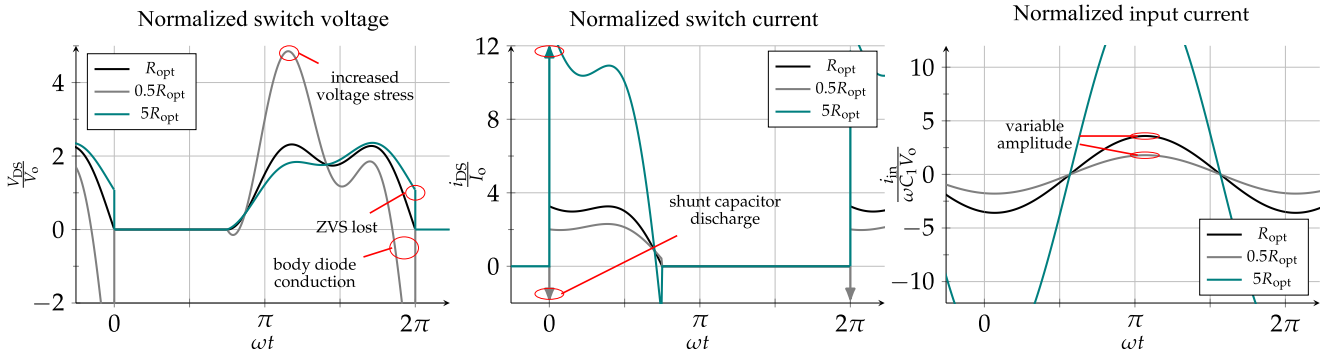

Fig. 13. Voltage and current waveforms of the Class EF_2 rectifier with an ideal switch as the dc load resistance changes from 50% to 500% of its optimum value. ZVS is lost, discharge of the shunt capacitor occurs, and the input current's normalized amplitude varies; therefore, the dc output is not regulated.

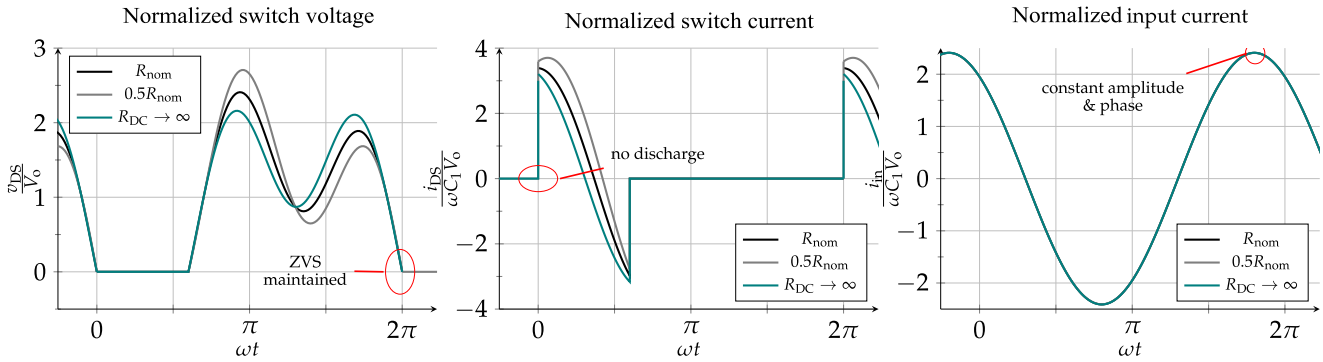

Fig. 14. Voltage and current waveforms for the load-independent Class EF rectifier as the load resistance varies from 50% of its nominal value to an open-circuit condition. ZVS is maintained, no discharge occurs, and the input current's normalized amplitude and phase remain constant; therefore, the dc output is regulated.

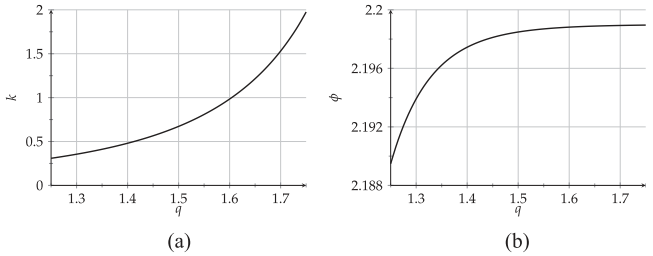

Fig. 15. Variation of k and ϕ with q_1 for the load-independent Class EF inverter. (a) k. (b) ϕ.

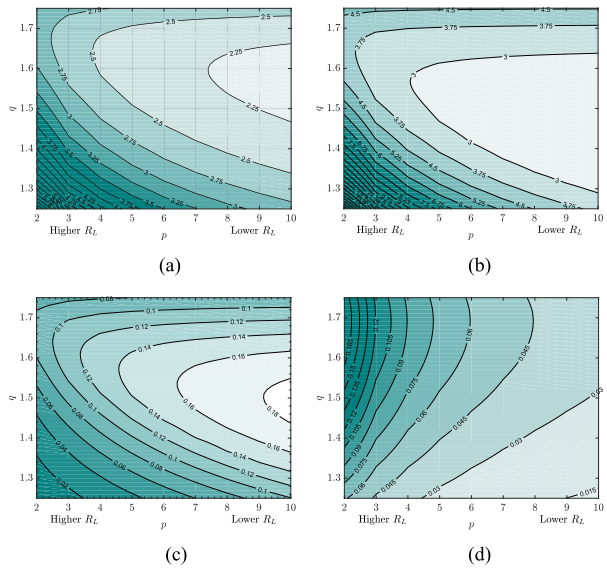

Fig. 16. Load-independent Class EF performance as a function of q_1 and p at 30% duty cycle operation. (a) Maximum drain voltage. (b) Maximum drain current. (c) Power-output capability. (d) Normalized shunt capacitance $\omega R_L C_1$.

drain voltage, and the peak drain current. For the remainder of this section, the duty cycle will be set 30% and the inverter's performance will be investigated for a q_1 ranging from 1.30 to 1.70.

Fig. 15 shows the variation of k and ϕ versus q_1. The change in the phase of the output current is relatively low for q_1 below 1.5 and approaches a fixed value for q_1 values above 1.5. Fig. 16 shows the normalized peak voltage and the normalized peak current of the switch as a function of q_1 and p. In Fig. 16(a), it can be noticed that the peak switch voltage is approximately 2.25 times the input voltage as p increases, i.e., as the load resistance approaches 0 Ω. The peak switch voltage begins to rise as p decreases, i.e., as the load resistance increases. The rate at which the normalized peak voltage increases is higher for q_1 values below 1.5, where the normalized peak voltage approaches approximately 6 at a q_1 of 1.3, and the increase rate is lower for q_1 values above 1.5, where the normalized peak voltage approaches approximately 3. In Fig. 16(b), it can be noticed that the peak

TABLE II
LOAD-INDEPENDENT CLASS EF INVERTER EQUATIONS' SHUNT CAPACITANCE, OUTPUT CURRENT, AND POWER-OUTPUT CAPABILITY FOR SELECTED VALUES OF q_1 AND p AT 30% DUTY CYCLE OPERATION

General Cases

	$q_1 = 1.3,\ k = 0.3553$					$q_1 = 1.4,\ k = 0.4802$					$q_1 = 1.5,\ k = 0.6722$				
p	$\omega R_L C_1$	$\omega X C_1$	$\frac{I_m R_L}{V_{\text{in}}}$	$P_o \frac{R_L}{V_{\text{in}}^2}$	c_p	$\omega R_L C_1$	$\omega X C_1$	$\frac{I_m R_L}{V_{\text{in}}}$	$P_o \frac{R_L}{V_{\text{in}}^2}$	c_p	$\omega R_L C_1$	$\omega X C_1$	$\frac{I_m R_L}{V_{\text{in}}}$	$P_o \frac{R_L}{V_{\text{in}}^2}$	c_p
2	0.0791	0.1204	0.7625	0.2907	0.0123	0.1127	0.1801	0.6823	0.2328	0.0274	0.1443	0.2478	0.6001	0.1801	0.0510
3	0.0537	0.1217	0.4999	0.1250	0.0245	0.0755	0.1806	0.4528	0.1025	0.0501	0.0964	0.2480	0.3995	0.0798	0.0854
4	0.0406	0.1224	0.3721	0.0692	0.0384	0.0568	0.1809	0.3388	0.0574	0.0741	0.0723	0.2482	0.2994	0.0448	0.1155
5	0.0327	0.1227	0.2965	0.0440	0.0535	0.0455	0.1810	0.2707	0.0366	0.0978	0.0579	0.2482	0.2394	0.0287	0.1388
6	0.0273	0.1230	0.2465	0.0304	0.0693	0.0379	0.1811	0.2254	0.0254	0.1200	0.0483	0.2483	0.1994	0.0199	0.1536
7	0.0235	0.1232	0.2110	0.0223	0.0853	0.0325	0.1812	0.1931	0.0187	0.1395	0.0414	0.2483	0.1709	0.0146	0.1639
8	0.0206	0.1233	0.1845	0.0170	0.1014	0.0285	0.1813	0.1689	0.0143	0.1524	0.0362	0.2484	0.1495	0.0112	0.1722

	$q_1 = 1.6,\ k = 0.9837$					$q_1 = 1.7,\ k = 1.5301$					$q_1 = 1.8,\ k = 2.6515$				
p	$\omega R_L C_1$	$\omega X C_1$	$\frac{I_m R_L}{V_{\text{in}}}$	$P_o \frac{R_L}{V_{\text{in}}^2}$	c_p	$\omega R_L C_1$	$\omega X C_1$	$\frac{I_m R_L}{V_{\text{in}}}$	$P_o \frac{R_L}{V_{\text{in}}^2}$	c_p	$\omega R_L C_1$	$\omega X C_1$	$\frac{I_m R_L}{V_{\text{in}}}$	$P_o \frac{R_L}{V_{\text{in}}^2}$	c_p
2	0.1691	0.3144	0.5049	0.1274	0.0798	0.1784	0.3404	0.3955	0.0782	0.0846	0.1613	0.1384	0.2739	0.0375	0.0437
3	0.1128	0.3145	0.3364	0.0566	0.1126	0.1190	0.3405	0.2636	0.0347	0.0981	0.1076	0.1384	0.1826	0.0167	0.0458
4	0.0846	0.3146	0.2522	0.0318	0.1319	0.0892	0.3406	0.1977	0.0195	0.1047	0.0807	0.1385	0.1369	0.0094	0.0468
5	0.0677	0.3146	0.2017	0.0203	0.1428	0.0714	0.3406	0.1581	0.0125	0.1085	0.0646	0.1385	0.1095	0.0060	0.0474
6	0.0564	0.3147	0.1681	0.0141	0.1501	0.0595	0.3406	0.1318	0.0087	0.1111	0.0538	0.1385	0.0913	0.0042	0.0478
7	0.0484	0.3147	0.1441	0.0104	0.1557	0.0510	0.3406	0.1129	0.0064	0.1130	0.0461	0.1385	0.0782	0.0031	0.0481
8	0.0423	0.3147	0.1260	0.0079	0.1600	0.0446	0.3406	0.0988	0.0049	0.1144	0.0404	0.1385	0.0685	0.0023	0.0483

Special Cases

	Max throughput ($P_o \times c_p$) $q_1 = 1.58,\ k = 0.9078$					Max c_p $q_1 = 1.66,\ k = 1.2706$					Max frequency $q_1 = 1.69,\ k = 1.4590$				
p	$\omega R_L C_1$	$\omega X C_1$	$\frac{I_m R_L}{V_{\text{in}}}$	$P_o \frac{R_L}{V_{\text{in}}^2}$	c_p	$\omega R_L C_1$	$\omega X C_1$	$\frac{I_m R_L}{V_{\text{in}}}$	$P_o \frac{R_L}{V_{\text{in}}^2}$	c_p	$\omega R_L C_1$	$\omega X C_1$	$\frac{I_m R_L}{V_{\text{in}}}$	$P_o \frac{R_L}{V_{\text{in}}^2}$	c_p
2	0.1651	0.3023	0.5250	0.1378	0.0746	0.1772	0.3402	0.4409	0.0972	0.0882	0.1784	0.3421	0.4071	0.0829	0.0862
3	0.1101	0.3024	0.3498	0.0612	0.1097	0.1182	0.3403	0.2938	0.0432	0.1096	0.1190	0.3422	0.2713	0.0368	0.1015
4	0.0826	0.3025	0.2622	0.0344	0.1322	0.0887	0.3404	0.2203	0.0243	0.1203	0.0893	0.3423	0.2034	0.0207	0.1090
5	0.0661	0.3026	0.2098	0.0220	0.1453	0.0709	0.3404	0.1762	0.0155	0.1265	0.0714	0.3424	0.1627	0.0132	0.1134
6	0.0551	0.3026	0.1748	0.0153	0.1537	0.0591	0.3404	0.1468	0.0108	0.1307	0.0595	0.3424	0.1356	0.0092	0.1163
7	0.0472	0.3026	0.1498	0.0112	0.1602	0.0507	0.3404	0.1258	0.0079	0.1338	0.0510	0.3424	0.1162	0.0068	0.1185
8	0.0413	0.3026	0.1311	0.0086	0.1652	0.0443	0.3405	0.1101	0.0061	0.1362	0.0447	0.3424	0.1017	0.0052	0.1201

Note: R_L corresponds to the maximum load resistance

switch current is approximately 2.25 times the input current as p increases. Similar to what occurs with the peak switch voltage, the peak switch current begins to increase as p decreases. However, the rate of increase is higher for q_1 values below 1.5, where the normalized peak switch current approaches approximately 12, and the rate of increase is lower for q_1 values above 1.5, where the normalized peak switch current approaches 4.5.

Based on the above discussion and Fig. 16, the practical operation range of the load-independent Class EF inverter and rectifier is at values of q_1 between 1.3 and 1.7 and at values of p between 2 and 8. It is, therefore, recommended to design within these ranges to achieve a certain output power with reasonable voltage and current stresses across the entire load range.

D. Design Equations

1) General Equations: Table II lists the design equations to determine the shunt capacitance C_1, the residual reactance X, and the output current along the power-output capability for a selected value of q_1 and a selected value of p that will correspond to the maximum load resistance. A designer can use these equations to determine the required the component values to achieve a certain required output ac current and power for a given load, frequency, and input dc voltage.

2) Special Cases: If there is no restriction on the input dc voltage to be used and the load value, then the design could be optimized to operate at three certain special cases, which are operating at either maximum power-output capability, maximum switching frequency, or at maximum power throughput, i.e., maximum product of output power and power-output capability. The design equations for these special cases are listed in Table II.

V. Application Examples and Experimental Verification

In this section, three design examples will be given to show the design process for load-independent Class E/EF inverters and rectifiers. Validation of load-independent operation for Class E inverters has been shown in [4], and initial validation of the load-independent operation of the Class EF inverter has been presented in our previous work [5]. The first design example will show the design and implementation of a load-independent Class EF inverter for WPT applications. The inverter will operate at 13.56 MHz and will generate a constant amplitude current of 7 A over a load range from 0 to 150 W. The second example will show the design and implementation of a high-power-density miniature Class E boost converter implemented on an aluminum-core printed circuit board (PCB). The third design example will show the design of a lightweight load-independent synchronous Class E rectifier for a wirelessly powered drone operating at 13.56 MHz and 20 W.

A. 150-W 13.56-MHz 7-A Load-Independent Class EF Inverter

This application example shows an improved design of the load-independent Class EF inverter first presented in our initial work in [5] for MHz WPT. Here, we will provide the complete design process, extensive experimental results, and power loss analysis in addition to a PCB construction technique for improved thermal performance. The requirement here is to build an inverter for WPT applications that is capable of providing up to 150 W of power at 13.56 MHz. The total load resistance in the output network, which includes the equivalent series resistance (ESR) of the transmitting coil and the reflected resistance of the secondary coil circuit, varies from 0 to 6Ω depending on the position of the receiving coil and its load resistance. The reflected resistance increases when the coupling between the transmitting and receiving coils is increased, which occurs when the two coils are brought closer to each other, or when the load at the receiving coil increases. The reflected resistance decreases when the coupling between the transmitting and receiving coils is decreased, which occurs when the two coils further from each other, or when the load at the receiving coil decreases. The ESR of the transmitting coil remains constant.

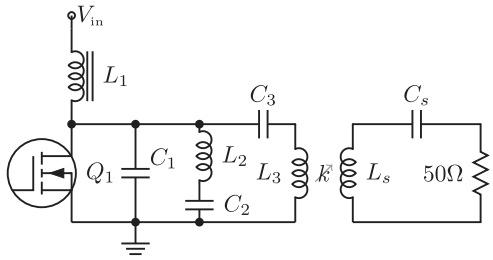

Fig. 17. Circuit diagram of setup for evaluating the MHz load-independent Class EF inverter.

1) Design: We begin the design by choosing to operate at the maximum power-output capability case ($q_1 = 1.66$). The amplitude of the output current in the transmitting coil or in the output network of the inverter, at 150 W for a 6-Ω load is 7.07 A. Next, we select a value for p for operation at the maximum load resistance. Setting a large value for p may result in small values of the required shunt capacitance, which could be lower than the output capacitance of currently available devices, whereas setting a very low value for p will cause the inverter to operate at very low c_p, which will result in low efficiencies at the maximum load resistance. Therefore, the value of p should be set to ensure a good power-output capability operation with a practical value of the required shunt capacitance. We find a value of 2 to be suitable. From Table II, we find the values of C_1, C_2, L_2, and X_{res} to be 347 pF, 273 pF, 183 nH, and 135 nF, respectively, and the required dc input voltage is 96 V. Based on the value of the input dc voltage and the voltage and current stresses, we select the device suitable for these requirements. The GS66508B (650 V/30 A) GaN FET from GaN Systems is selected. This GaN FET has an ON resistance of 50 m Ω and an input capacitance of 260 pF. Its output capacitance at 96 V is approximately 150 pF, which is lower than the designed C_1 capacitance value.

2) Implementation and Experimental Results: The transmitting coil that will be attached to the inverter consists of two spiral turns on an FR4 PCB. The outer diameter is 22 cm, the inner diameter is 20 cm, and the track width is 1 cm. Its inductance and Q factor measured at 13.56 MHz are approximately 1.14 μH and 400, respectively. Based on the parameters of the transmitting coil and the required residual inductance, the value of $C_3 = 1/\big((2\pi \times 13.56\ \text{M})^2 \times (1.14\ \mu - 135\ \text{n})\big) = 137$ pF. Fig. 17 shows the circuit diagram of the setup. Inductor L_3 represents the inductance of the primary coil of the WPT system. The secondary coil was constructed using two turns of 7-AWG wire with a diameter of 16 cm. A series capacitor (C_s) was connected to the secondary to achieve resonance. This was done in order to reflect a resistive impedance to the Class EF inverter. A fixed 50-Ω resistor was used to load the secondary coil.

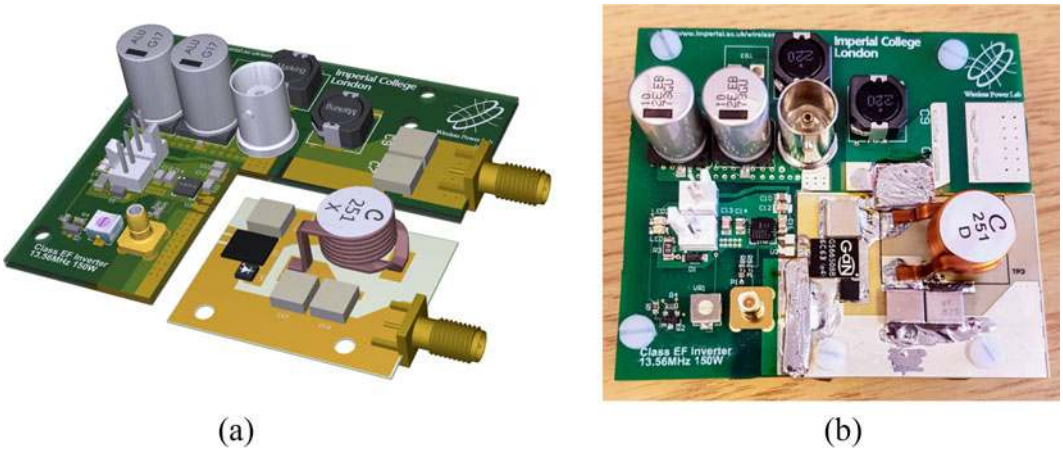

Fig. 18. Photograph of the implemented 13.56-MHz load-independent Class EF inverter. The low-power components, input connectors, electrolytic capacitors, chokes, and a gate driver are mounted on a four-layer FR4 PCB. The GaN FET and components C_1, C_2, and L_2 are mounted on a single-layer aluminum-core PCB. The two boards are then soldered to each other. (a) Illustration. (b) Implementation.

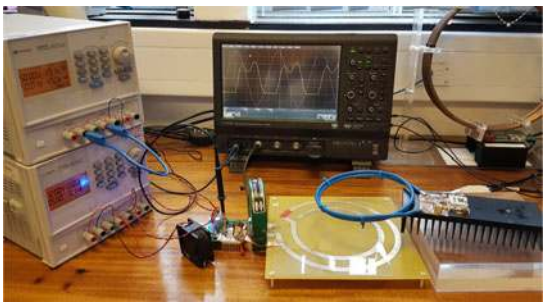

Fig. 19. Photograph of the load-independent Class EF inverter setup.

Fig. 18 shows a photograph of the inverter, which consists of two circuit boards. The first board is a four-layer FR4 PCB, which contains the low-power components, input connectors, electrolytic capacitors, chokes, and a gate driver. The second board is a single-layer aluminum-core PCB, which contains the GaN FET and components C_1, C_2, and L_2. Aluminum-core PCBs have improved thermal performance compared to FR4 and, therefore, will allow the inverter to operate at high power levels and at lower component temperatures. This design also allows for modularity where different transistors and circuit configurations could be implemented and tested without having to redesign the entire PCB. Table IV lists the implemented the component values. The implemented values of C_1 and C_2 are lower than their designed values due to the GaN FET's output capacitance and the higher parasitic capacitance of the aluminum-core PCB.

The testing of the load-independent operation of the Class EF inverter was achieved by varying the distance between the primary and secondary coils of the WPT system, which causes the reflected load to change. The secondary is series tuned at the operating frequency; therefore, it will always reflect a real impedance regardless of the coupling factor. Since the Class EF inverter generates a constant output current, the power delivered to the load increases as the coupling between the coils is increased. Fig. 19 shows a photograph of the setup.

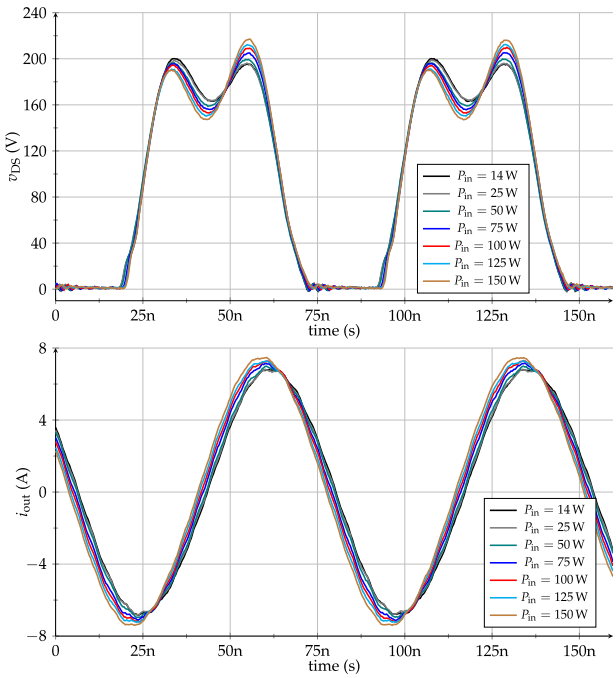

Fig. 20. Experimental voltage and current waveforms for the implemented load-independent Class EF inverter over the entire load range.

Fig. 20 shows a set of experimental voltage and current waveforms for different input powers. These waveforms were obtained without any tuning or changing of components. At an input power of 14 W, the coils were completely separated from each other; most of the input power was dissipated in the ESR of the transmitting coil. The input power to the inverter increases as the coils were brought closer to each other until the input power reached 150 W. From the drain waveforms, it can be seen that ZVS is maintained over the entire load range. The output current waveforms also show near constant amplitude and phase with minimal deviations as predicted by the analysis. The measured amplitude and phase deviation are plotted in Fig. 21.

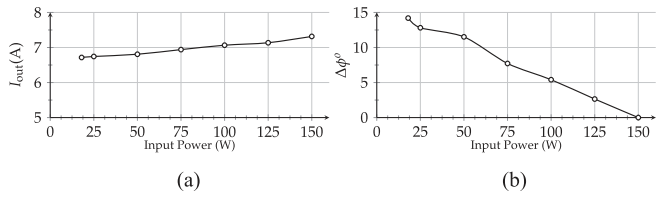

Fig. 21. Measured output current's amplitude and phase of the load-independent Class EF inverter. The phase reference is at 150-W input power. (a) Amplitude. (b) Phase deviation.

Fig. 22. Thermal steady-state image of the load-independent Class EF inverter at the 150-W input power.

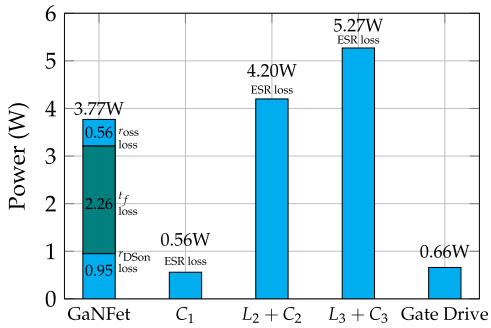

Fig. 23. Power loss breakdown for the 13.56-MHz load-independent Class EF inverter at the 150-W input power.

Fig. 22 shows a thermal steady-state image of the inverter operating at 150 W at a room temperature with 10-cfm airflow. The temperature of the GaN FET did not exceed 57°, which confirms the effectiveness of using an aluminum-core PCB for improved thermals. Higher power levels above 200 W can be achieved with this design. As a comparison, the temperature of the GaN FET on a FR4 PCB board in our initial work [5] under the same operating conditions and stresses exceeded 80°, which limited the power levels to 100 W. Fig. 23 shows the expected power loss breakdown at 150-W input power. Losses in the GaN FET consist of conduction loss associated with r_{DSon}, turn OFF loss due to its 5.2 ns current fall time that was calculated using the formula $\omega t_f P_o/12$ [10], and loss associated with the ESR (r_{oss}) of its output capacitance that is assumed to be 50 mΩ. Losses in all other passive components are due to their ESRs. All losses were obtained by first calculating the theoretical RMS

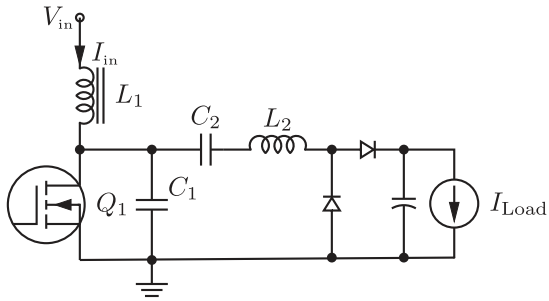

Fig. 24. Circuit diagram of the load-independent Class E dc/dc converter.

current in each component. Gate drive losses at a gate voltage of 6 V were measured to be 0.66 W. The expected efficiency of the inverter, excluding losses in the output network, is 94%.

B. 150-W 10-MHz Class E DC/DC Boost Converter With Inherent Output Voltage Regulation

This design example will show the use of the presented load-independent topologies for dc/dc conversion. Here, we will use the load-independent constant output voltage Class E inverter to develop a miniature 150-W 48-V-to-150-V dc/dc boost converter. The aim is to use only air-core coils and ceramic capacitors only; consequently, the switching frequency needs to be in the MHz range.

1) Design: Fig. 24 shows the circuit diagram of the converter. The inverter section consists of the load-independent constant output voltage Class E inverter operating at a duty cycle of 50% (see Table I) and at a switching frequency of 10 MHz and a Class D voltage-driven rectifier.

Beginning with the voltage conversion ratio, according to Table I, the load-independent Class E inverter has a voltage gain of 1.5895 at 50% duty cycle operation. The Class D rectifier has a voltage gain of 1.5710; consequently, the dc/dc voltage conversion ratio is 2.4970. Initial experimental result showed that the voltage conversion ratio is approximately 3.1. This is due to the nonlinearity of the MOSFET's output capacitance, which causes the MOSFET's peak drain voltage to increase, as discussed in [16].

The converter will be set to operate at the maximum power-output capability at the 150-W load power. From Fig. 8, this corresponds to a loading factor p equal to 1.5. At the 150-W load power and assuming a 90% power efficiency, the amplitude of the current I_m is $2 \times 150/(0.9 \times 48 \times 1.5895) = 4.3689$ A. Using (5), the finite choke inductor L_1 is 262 nH, and consequently, from Table I, the shunt capacitor C_1 and the residual inductance can be calculated and are equal to 579 pF and 70 nH, respectively. Selecting the values of L_2 and C_2 depends on the required loaded Q factor of the output network. Setting the loaded Q factor to large will result in optimal performance according to theory and potentially lower electromagnetic interference at the expense of efficiency, whereas setting the load Q factor too low may lead to loss of ZVS according to initial experimental results. Here, we will set the loaded Q factor at the maximum load to be 2.5. At the 150-W load power, the

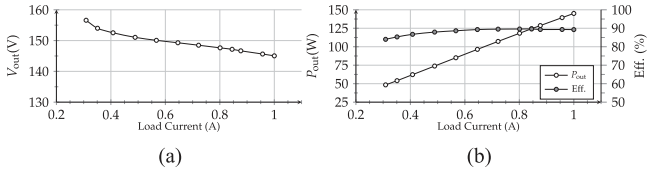

Fig. 25. Class E dc/dc converter experimental results. (a) Output voltage. (b) Output power and efficiency.

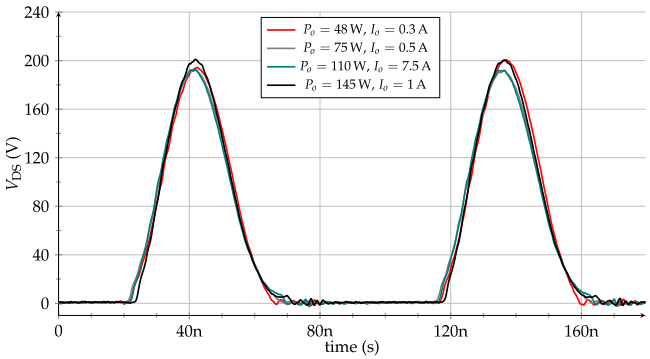

Fig. 26. Load-independent Class E dc/dc converter experimental waveforms.

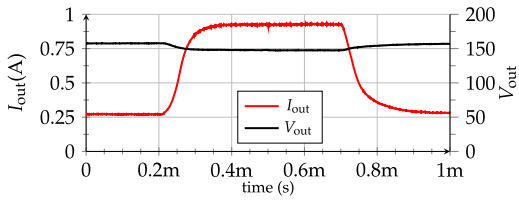

Fig. 27. Measured load-independent Class E dc/dc converter response to a step change in the load current.

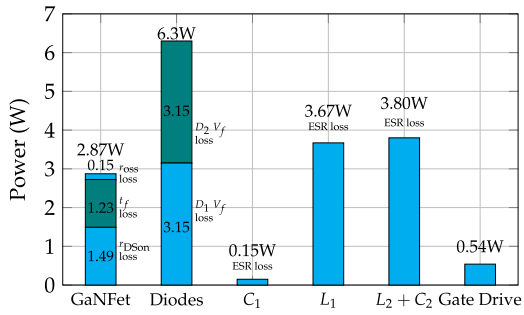

Fig. 28. Power loss breakdown for the 10-MHz dc/dc converter at the 145-W load.

ac load resistance is approximately 19.4Ω; consequently, the values of L_2 is $2.5 \times 19.4/(2\pi \times 10^7) = 772\,nH$ and C_2 is $1/\big((2\pi \times 10^7)^2 \times (772\text{n} - 70\text{n})\big) = 361\,\text{pF}$.

2) Implementation and Results: Table IV lists the implemented component values. The implemented values of C_1 and C_2 are lower than their designed values due to the GaN FET's output capacitance and the higher parasitic capacitance of the aluminum-core PCB. The GaN FET used is the GS66508B GaN FET from GaN Systems, and the diodes are the C3D1P7060Q SiC diodes from Wolfspeed. An electronic load was used to evaluate the converter. Fig. 25 shows the measured output voltage, power, and efficiency over the load current range from 0.3 to 1.0 A. Measurements at load currents below 0.3 A could not be obtained accurately due to the low control bandwidth of the electronic load, which lead to oscillations in the output voltage. All measurements were obtained without any adjustments to the switching frequency, duty cycle, and to the components. The output dc voltage is approximately 145 V at a load current of 1 A and increases to approximately 155 V at the minimum load current. The efficiency remains fairly constant at approximately 90% at load currents from 0.5 to 1 A. Fig. 26 shows the drain waveform at various loads; it can be seen the ZVS is maintained over almost the entire load range. Fig. 27 shows the measured step response of the converter.

Fig. 28 shows the expected power loss breakdown when operating at the 145-W load. The SiC diodes have a total loss of 6.3 W due to their relatively higher forward voltage drop. Replacing the diodes with synchronous switches will reduce losses and improve efficiency, as will be shown in the next design example. Gate drive losses at a gate voltage of 6 V were measured to be 0.54 W.

TABLE III
REVIEW OF RECENT MHZ DC/DC CONVERTERS

Reference	Frequency	Power	Topology	Voltages	Efficiency
This work	**10 MHz**	**150 W**	**Class E**	**48 to 150 V**	**90%**
2017 [7]	10 MHz	18 W	Class ϕ_2	24-V input	85.5%
2017 [17]	5.17 MHz	10 W	Class E	7.5 to 5 V	-
2017 [18]	20 MHz	10 W	Class E	5-V output	81.5%
2016 [19]	30 MHz	14 W	SEPIC	15 to 28 V	80%
2015 [20]	21 MHz	30 W	SEPIC	10.7 to 12 V	87%
2015 [21]	27.12 MHz	320 W	Class ϕ_2	170 to 28 V	73.6%
2015 [21]	13.56 MHz	400 W	Class ϕ_2	200 to 28 V	84%
2014 [22]	120 MHz	9 W	interleaved Class E	9 to 20 V	89%
2014 [23]	5 MHz	30 W	Flyback	48 to 12 V	87%
2009 [24]	30 MHz	900 W	Four-phase class ϕ_2	300 to 50 V	80%

The Class E dc/dc converter was not implemented with a feedback control loop. Improved output regulation can be achieved using ON–OFF control, which has been the common control method applied in recent MHz converters [7], [17]–[19], however at the expense of increased circuit complexity. Table III compares the results of the developed converter with recent work in MHz dc/dc conversion. The efficiency and power density figures in this work exceed what has been reported recently in the literature. Fig. 29 shows a photograph of the Class E dc/dc converter, which was implemented entirely on a 49 mm × 35 mm × 1.5 mm aluminum-core PCB. No heatsink was used. At power levels above 100 W, a sub-1-W fan providing 10 cfm was used. Fig. 30 shows a steady-state thermal image at the 150-W load power. At 150 W, the power density including volume of all components is approximately $500\,\text{W}/\text{in}^3$.

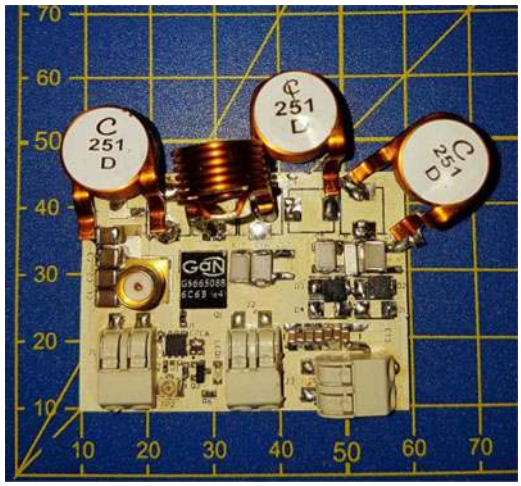

Fig. 29. Photograph of the implemented 150-W 10-MHz load-independent Class E dc/dc boost converter. The converter was built entirely on a single-layer aluminum-core PCB. The power density including the inductors and excluding the power connectors is approximately 500 $\mathrm{W/in^3}$.

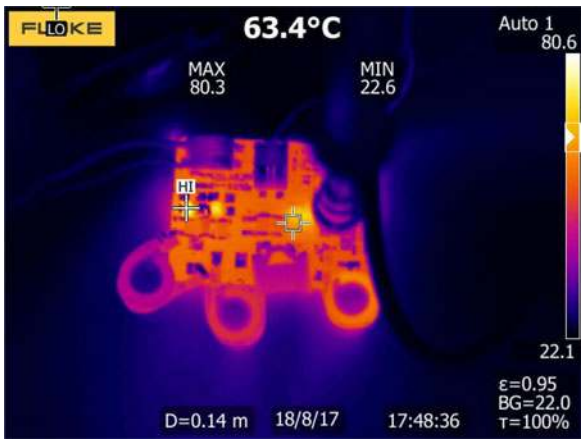

Fig. 30. Thermal image of the load-independent Class E dc/dc converter operating at 150 W. The temperature of the GaN FET is approximately 70°, and the SiC diodes are at approximately 80 °C.

To the authors' knowledge, this is highest power density figure presented for a Class-E-based dc/dc converter.

C. 20-W 13.56-MHz Synchronous Class E Rectifier in Wireless Powering of Drones

In [25], we showed how a small 15-W drone could be powered entirely wirelessly. The setup, as shown in Fig. 31(a), consisted of a load-independent Class EF inverter delivering 6 A at 13.56 MHz to a two-turn transmitting coil. The receiving coil was formed by copper plating the propeller guard of the drone forming a single-turn 330-nH coil. The rectifier on-board the drone was a hybrid Class E rectifier introduced in [26]. Thermal imaging showed that when the drone was at its furthest point away from the transmitting coil, the diodes were contributing to the majority of the losses in the rectifier, since the rectifier operates at a low-voltage high-current regime. Consequently, replacing the diode with a synchronous switch will reduce losses and

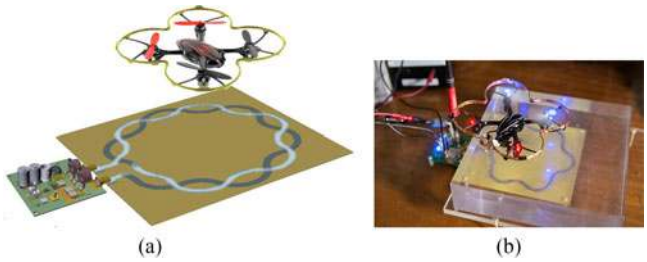

Fig. 31. Setup and implementation of the wirelessly powered drone. (a) Setup. (b) Demonstration.

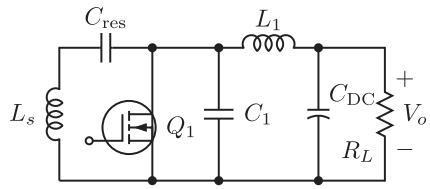

Fig. 32. Circuit diagram of the load-independent synchronous Class E rectifier in the WPT system. The induced ac voltage is in inductor L_s.

improve the overall system efficiency especially when operating at large separation distances or at lower coupling coefficients.

This design example follows on our previous work in [25] for wireless powering of drones. Here, we will design a 20-W load-independent Class E rectifier with a synchronous switch to convert the induced 13.56-MHz ac voltage at the receiving coil on-board a drone to a dc voltage. The rectifier will also provide a good degree of output regulation with variations in loading only.

1) Design: Fig. 32 shows the circuit diagram of the load-independent Class E rectifier connected to a WPT receiving coil (L_s). The receiving coil has an inductance of 330 nH, and the series capacitor C_s is 417 pF and is used to resonate the receiving coil at 13.56 MHz, hence creating a current-output source to drive the rectifier. The coupling coefficient between the transmitting coil and the receiving on-board the drone varies from 20%, when the drone is stationary above the transmitting coil, to 4%, when the drone hovers at the furthest point above the transmitting coil. Simulation results and initial measurements indicate that the induced EMF range at the receiving coil will be 29 V at 4% coupling to 90 V at 20% coupling.

The rectifier will be designed at the lowest coupling coefficient point for the maximum overall efficiency, since it will be operate at a low-voltage high-current regime. At an induced ac voltage of 29 V, the current supplied by the receiving coil to a 20-W load is 1.379 A. The rectified dc voltage, according to Table I, is $29/1.5895 = 18.2$ V. Using (5) and assuming operation at $p = 1$, the value of inductor L_1 is $1 \times 18.2/(2\pi \times 13.56 \times 10^6 \times 1.379) = 154.9$ nH. The nearest commercially available inductor is the 146-nH 1010VS series air-core inductor from the Coilcraft. Consequently, the value of C_1 is 565.7 pF.

2) Initial Implementation and Results: The load-independent Class E rectifier was initially implemented on the evaluation board EPC9052 from EPC Corp., which uses the EPC2012C GaN FET. Fig. 33 shows a photograph of the

Fig. 33. Photograph of the load-independent synchronous Class E rectifier setup.

TABLE IV
IMPLEMENTED COMPONENT VALUES FOR ALL THE DESIGN EXAMPLES

Component	13.56 MHz Class EF	10 MHz Class E DC/DC	13.56 MHz Sync. Class E
L_1 (μH)	88	0.257	0.146
L_2 (nH)	176	771	–
L_3 (μH)	1.14	–	–
C_1 (pF)	124 + C_{oos}	200 + C_{oos}	540 + C_{oos}
C_2 (pF)	138	257	–
C_3 (pF)	136	–	–
$V_{\text{in}/o}$ (V)	100	48	20

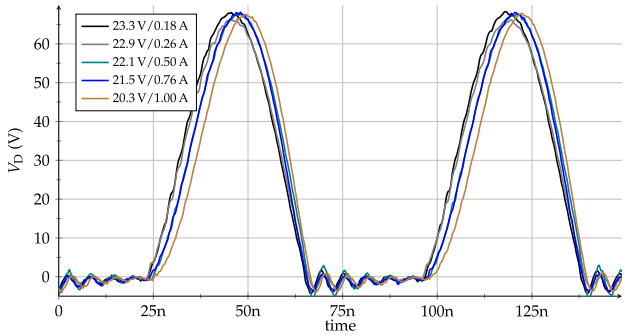

Fig. 34. Experimental waveforms of the load-independent synchronous Class E rectifier for different loads.

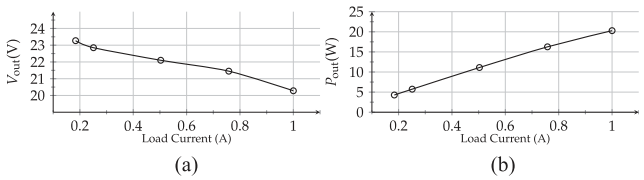

Fig. 35. Measured output voltage and power of the load-independent synchronous Class E rectifier from no load to maximum load. (a) Output voltage. (b) Load power.

test setup. Table IV lists the implemented component values. For evaluation purposes, the switching signals for the load-independent Class EF inverter and the Class E rectifier were provided from a function generator with a phase difference of 120°. Fig. 34 shows the drain waveforms for different dc loads. It can be seen that the synchronous FET operates at ZVS over the entire load range. The measured rectified output dc voltage and load power are plotted in Fig. 35. The rectified output voltage varies from 23 V at a low dc load current and drops to

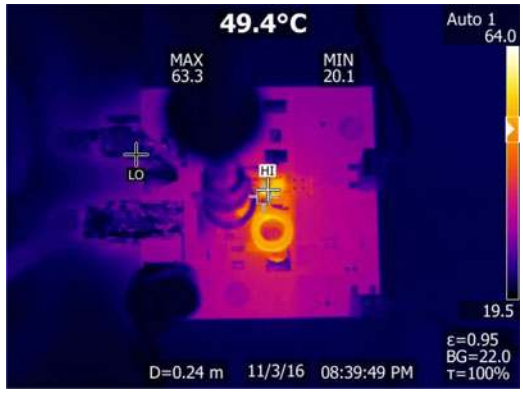

Fig. 36. Thermal steady-state image of the load-independent synchronous Class E rectifier at the 20-W load.

20 V at a dc load current of 1 A; this corresponds to a voltage regulation of 14.7%. The difference between the designed rectified dc voltage and the measured dc voltage is due to the nonlinearity of the GaN FET's output capacitance. It should be noted that the rectifier was operating continuously, and no adjustments were made to the frequency, duty cycle, phase, or modification of the components, while the load was swept. This confirms that the rectifier achieved load-independent operation.

Fig. 36 shows a thermal steady-state image of the board at a 20-W load. Measuring the rectifier's efficiency can be challenging here, since using current probes will not be accurate and will disturb the circuit. However, the rectification efficiency can be estimated from the thermal image. The GaN device's temperate is 63°; from the manufacturer's datasheet, this temperature rise at 20° ambient corresponds to a power dissipation of approximately 500 mW. The estimated power loss in the inductor according to SPICE simulations is 780 mW. Consequently, the rectification efficiency at the 20-W load is expected to be up to 94%.

The design of the load-independent synchronous Class E rectifier is only valid at a rectified dc voltage range 18–25 V, i.e., at a coupling coefficient around 4%, since the design takes into account the average value of the FET's output capacitance at that dc voltage range. The rectifier will not provide full load-independent operation at higher rectified dc voltages or higher coupling coefficients since FET's output capacitance will vary. Consequently, at higher coupling coefficients, passive rectification is only enabled, since it is efficient, whereas synchronous rectification is enabled at lower coupling coefficients.

3) Second Implementation: After verifying the operation of the synchronous Class E rectifier using the EPC9052 evaluation board, the rectifier was then implemented on a miniaturized PCB that can be placed inside the drone, as shown in Fig. 37. The GS66504B GaN FET from GaN Systems was used to obtain better thermal performance. A feedback circuit was designed to derive the switching signals to drive the synchronous FET from its drain waveform. A comparator first detects when the drain voltage crosses a certain voltage threshold and outputs a pulse, which triggers a monostable circuit. The monostable circuit then generates a 30-ns pulse to the FET driver. A linear voltage regulator powered from the dc output of the recti-

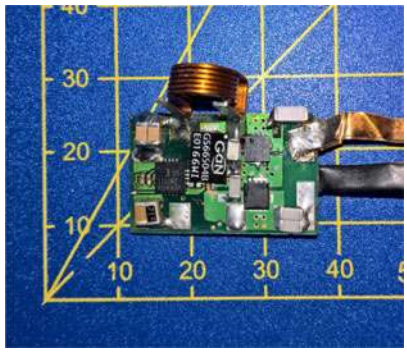

Fig. 37. Photograph of the miniaturized load-independent synchronous Class E rectifier. The feedback and control circuitry are on the bottom layer.

fier is used to generate the low-voltage logic supply and gate drive voltage. The selected drone and its motors operate from a 3.7-V supply. The dc/dc buck converter module LMZ36002 was installed after the rectifier to provide a regulated 3.7-V supply. Further information and details and a video demo can be seen at https://youtu.be/GyOoOeNrbfM.

VI. Conclusion

This paper presented the concept of load-independent operation for Class E and Class EF inverters and rectifiers. ZVS is maintained across a wide load range with inherent output regulation without requiring tuning, control, or feedback loops. As switching frequencies are rising toward MHz frequencies with the use of WBG devices, load-independent operation becomes increasingly important to achieve high efficiency, high performance, and robustness. The combination of load-independent topologies with WBG devices can significantly improve the performance in current applications and also enables new applications and technologies to be developed such as MHz WPT and high-power-density coreless power converters. Three design examples were provided to show the significant advantages of this combination. The following general conclusions can be made.

1) Traditional Class E/EF inverters and rectifiers can only operate efficiently at a fixed or narrow load range. Efficiency is degraded and output regulation is lost as the load varies from its optimal value. They also cannot operate at open-circuit or short-circuit conditions.
2) Load-independent Class E inverters with a finite choke maintain ZVS and a constant output ac voltage with varying load. The practical load resistance can range from a maximum infinite resistance to a minimum finite value at which the inverter is designed for. The inverter is, therefore, tolerant to open-circuit load conditions only, similar to traditional switch-mode conversion topologies.
3) Load-independent Class EF inverters with a dc choke maintain ZVS and a constant output ac current with varying load. The practical load resistance can range from a minimum 0-Ω resistance to a maximum finite value at which the inverter is designed for. The inverter is, therefore, tolerant to short-circuit load conditions only.
4) Load-independent Class E and EF rectifiers with a synchronous switch maintain ZVS and a regulated dc output voltage or current. They can tolerate either open- or short-circuit load conditions and have a constant input reactance regardless of the load.
5) Class E/EF inverters and rectifiers are the dual of each other; this means the solutions for load-independent operation are the same for inversion and rectification.
6) When used in applications such as MHz WPT, load-independent operation enables a WPT system to operate efficiently and reliably as the system geometry and loading changes without the need for tuning or a feedback loop, thus enabling mobile WPT.

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