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Load Modulation of Harmonically Tuned Amplifiers and Application to Outphasing Systems

Paolo Enrico de Falco, Student Member, IEEE, Prathamesh Pednekar, Student Member, IEEE, Konstantinos Mimis, Souheil Ben Smida, Member, IEEE, Gavin Watkins, Member, IEEE, Kevin Morris, Member, IEEE, and Taylor Barton, Member, IEEE

Abstract-Modulation of load impedance is an effective way to maintain efficient power amplifier (PA) operation over high dynamic range modulated signals. For high efficiency, a load modulation approach can be applied to inherently efficient classes of PAs such as those with harmonic tuning: class J, class F, and inverse class F. This paper presents an analysis of harmonically tuned amplifiers operating under load modulation conditions, deriving the optimal loading trajectories for these multiple classes of operation. Because these load trajectories are complex, it is then shown - through a series of analysis, simulations and measurements - that harmonically tuned amplifiers are better suited for outphasing systems, than conventional amplifiers such as class B. A design methodology is proposed and validated through design and measurement of a 900 MHz outphasing system, comprising of two Gallium Nitride (GaN) class J branch PAs, delivering 44.6 dBm with 75% PAE at saturation, while mantaining PAE above 60% over a 7 dB output power back-off.

Index Terms-outphasing, continuous modes of operation

I. INTRODUCTION

W IRELESS communication is predicted to grow significantly in the next decade thanks to the introduction of smart technologies in wearable, healthcare and vehicular applications. To achieve the necessary increase in capacity, a higher density of base stations is required. This in turn results in greater energy consumption, which efficient amplifiers can help to offset. Single-transistor amplifiers cannot operate with sufficient efficiency and linearity when driven by variable time-domain envelope signals with large peak-to average power ratio (PAPR). Instead, efficiency enhancement techniques are preferred, such as Doherty [1]–[12], outphasing [13]–[39] or other related techniques [40]–[43] in which load modulation is used to increase efficiency over a large output back-off (OBO).

Outphasing is a particularly attractive technique, as the branch PAs are driven with a constant envelope, phasemodulated signal. As a result, the PAs can theoretically operate in deep saturation and hence with high efficiency without a degradation in the linearity of the transmitted signal.

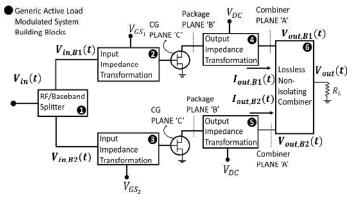


Fig. 1. Block diagram of a generic, actively load modulated system, highlighting the different planes of analysis.

Amplitude modulation of the original signal is reconstructed by vectorial summation of the output of each branch in the combiner. Because of this advantage, outphasing has received renewed interest in recent years [20], [21], [29], [36]–[39]. Nevertheless, the reactive loading which each PA branch is presented with, during non-isolating outphasing operation is a significant obstacle to its implementation [13].

Branch amplifiers experience a complex load modulation during outphasing operation due to the phase shift applied to their input signals, which causes the in-phase and quadrature voltage and current components to vary over the output power dynamic range. Both analysis and measurements have shown this effect on the branch PAs of an outphasing system [14], [15]. In conventional PAs, this reactive loading degrades efficiency by de-tuning the phase relationship between the voltage and current waveforms at the current generator (CG) of the device. Reactance compensation techniques place the load modulation trajectories as close as possible to the real axis, cancelling out the reactance, at a given point in the dynamic range [16]. However, in conventional Chireix outphasing this compensation can only be achieved for a maximum of two output power levels. Proposed techniques to mitigate the reactive loading problem involve either isolating the two PA branches [17], [18] or compensating for the reactive loading through the design of the combiner itself [13], [16]. Both approaches have limitations. By using an isolating power combiner the efficiency enhancement mechanism of active load pull is lost, therefore limiting the theoretical efficiency of the approach [18]. Alternatively, combiner re-design to com-

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P. E. de Falco, S. Smida, and K. Morris are with the Department of Electrical and Electronic Engineering, University of Bristol, Bristol, UK.

P. Pednekar and T. Barton are with the Department of Electrical, Computer, and Energy Engineering, University of Colorado Boulder, Boulder, CO, USA.

K. Mimis and G. Watkins are with Toshiba Research Europe Limited, Bristol, UK.

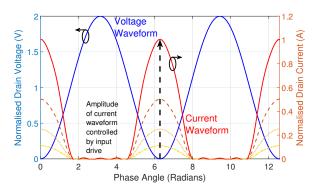


Fig. 2. Theoretical I/V waveforms of Doherty and DLM systems with input drive and load variation (Load Modulation Mechanism 1).

pensate for reactive loading, such as in four-way outphasing, greatly complicates both the design of the system and the input signal generation [13], [19].

In outphasing systems employing Chireix reactive compensating techniques, the branch amplifiers are typically designed as class E [20]–[26], F [27], F^{-1} [28], [29] power amplifiers or as saturated class B amplifiers [30], [31]. Recently in [21], continuous class E theory was utilised in the design of a wideband outphasing system showing promising results. However class E operation, where the active device is operated as a switch, can represent a limitation in terms of both frequency and power [44].

Studies on ideal drain current and voltage waveforms have determined, through the analysis of their Fourier components (for both a finite and infinite number of harmonics), the optimal fundamental and harmonic load impedances required to achieve maximum efficiency and output power for a given device [45]–[49]. Based on these studies, continuous modes introduced in [50] have shown that PA performance can be maintained under reactive loads if the appropriate harmonic terminations are presented. From the mode B/J this formulation has been expanded to modes F, F^{-1} [51]–[54] and is widely used in the design of broadband or multi-band power amplifiers [55], [56]. The theory initially applied only to amplifiers where the active device operates as a voltage controlled current source, i.e. in small levels of compression, has since been expanded to consider overdriven operation, where the device is approximated as a switch [57]. A continuum of waveforms meeting the zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS) class E requirements, has been recognized with the modes E, EF2 and E/F2 as subsets of the continuous design space [57].

Continuous modes of operation theory has also been exploited for dynamic load modulated (DLM) [40] and Doherty systems [1], [2]. When applied to load modulated systems, it has been shown in our previous work [39], [41], [42] that it can be beneficial to use Harmonically Tuned (HT) amplifier modes in DLM and outphasing systems, as it is possible to move across the continuous design space, when complex load modulation is applied. Particularly, the complex fundamental optimal load trajectory of HT amplifiers makes them well-suited to outphasing systems, in which a complex loading is

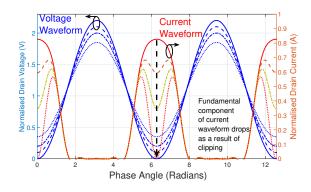


Fig. 3. Theoretical I/V waveforms of outphasing system with load variation but fixed input drive (Load Modulation Mechanism 2).

inherently presented to the branch PAs – even if reactance compensation techniques are implemented [39].

This paper presents an analysis of HT amplifiers operating under load modulation conditions, and their application to load modulated systems. From the insights deriving from analysis, simulations and load-pull measurements, a methodology is proposed for the design of outphasing systems. A comparison in simulations with existing techniques for the design of outphasing amplifiers shows the advantage of the method and a hardware demonstration using class J amplifiers is presented, exhibiting state-of-the-art performance.

In Section II a review of the two main mechanisms used to control output power in active load modulated systems is provided. In Section III the optimal load modulation trajectories for harmonically tuned PAs are defined in closed form for modes B/J, continuous F and continuous F^{-1} and are experimentally validated through load-pull measurements for mode B/J only. The optimal fundamental load modulation trajectories for continuous E mode of operation, considering the fundamental and second harmonic termination only, is computed numerically in Section III. From the ideal waveform formulations, the optimal load modulation trajectories of continuous modes B/J, F and F^{-1} are investigated in simulation in Section IV, demonstrating the impact of the second harmonic termination on the back-off efficiency of heavily saturated HT amplifiers. Based on these findings, a design method is proposed in Section V to exploit the complex load modulation trajectories of HT amplifiers. The comparison between an outphasing system using Class J PAs and one using conventional Class F amplifiers is described in Section VI. Section VII reports the experimental results of the fabricated prototype and a comparison with state-of-the-art load-modulated systems.

II. LOAD MODULATION MECHANISMS

Load impedance modulation of RF amplifiers for output power control is one of the most widely used techniques to achieve efficient amplification of variable envelope signals [58]. Variable loading can be achieved through active loadpull by allowing multiple amplifiers to interact through a lossless combiner, as in outphasing, Doherty or other active load modulation techniques. A generalized block diagram for an active load modulated system is shown in Fig. 1, for which the various techniques are differentiated by the implementation of the functions in blocks 1 and 6. Considering a generic amplitude- and phase-modulated signal as the input of the amplification system in Fig. 1:

$$V_{in}(t) = E(t)\exp(j\omega t + \phi(t)) \tag{1}$$

where E(t) is the time-varying envelope and $\phi(t)$ is the original phase modulation. The outputs of block 1 driving the branch amplifiers can be written as:

$$V_{in,B1}(t) = A_1(V_{in}) \exp(j\omega t + \phi(t) + \psi_1(V_{in}))$$
(2)

$$V_{in,B2}(t) = A_2(V_{in})\exp(j\omega t + \phi(t) + \psi_2(V_{in}))$$
(3)

with $A_{1,2}$ and $\psi_{1,2}$ functions of the original time-varying input signal $V_{in}(t)$. With the design of the splitter (block 1), the combiner (block 6) and choice of gate source biases (V_{GS_1} , V_{GS_2}), these functions can be controlled. The combiner is designed to ensure the output of the load modulated system is a linear amplified replica of its input, represented as:

$$V_{out}(t) = \mathcal{F}(A_{1,2}, \psi_{1,2})$$
(4)

$$= G(E(t)\exp(j\omega t + \phi(t)))$$
(5)

where G is the gain of the amplification system.

If $\psi_{1,2}$ are constant (0 or a fixed offset) and the envelope variation $A_{1,2}$ is a function of E(t), the active load modulation results in a Doherty-like load modulation (Load Modulation Mechanism 1), where maximum voltage swing is maintained for a range of input drive levels, as can be seen from Fig. 2. For this type of technique power is modulated by both the variation of the instantaneous loading on each PA and the envelope variation of the branch input signals ($V_{in,B1}$, $V_{in,B2}$). The amount of gain compression (or knee interaction) tolerated throughout the load modulation is determined by whether efficiency, output power or a compromise of both needs to be maximised in the design [3]–[5].

On the other hand when $A_{1,2}$ are constant and the envelope is reconstructed through the variation of $\psi_{1,2}$ the branch amplifiers will be subject to an outphasing-like load modulation (Load Modulation Mechanism 2). Output power is controlled, by reducing the fundamental component of the current waveform as a result of the clipping action while, the voltage waveform remains nearly constant, as shown in Fig. 3 [59]. In conventional outphasing systems, the level of gain compression of the transistors is directly proportional to the output power back-off as the envelope of the branch amplifier's input signal ($V_{in,B1}$, $V_{in,B2}$) is not varied throughout the back-off range. Mixed-mode operation techniques offer additional efficiency benefits [29], [30].

III. OPTIMAL FUNDAMENTAL LOAD MODULATION OF HT PAS

In this section the optimal load modulation trajectories of HT PAs are analysed for the idealised cases where no clipping or knee interaction occurs (III-A), and where they can be approximated as ideal switching devices (III-B). The limitations of this idealised approach are identified and discussed (III-C).

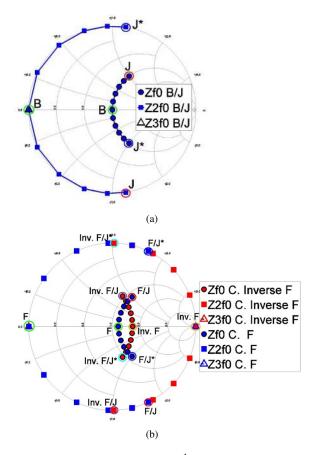


Fig. 4. Continuous Class B/J, F and F^{-1} design spaces in the impedance domain.

A. Theory applied to current source active devices

As previously shown in [50], reactive fundamental impedances can be tolerated at the intrinsic drain of a transistor when compensated for with an appropriate reactive second harmonic impedance termination. The harmonic impedances for this B/J mode are shown in Fig. 4(a). A critical aspect of operation is that these waveforms assume no interaction with the knee voltage. By decreasing the value of the resistive part of the fundamental load impedance from its optimum value, it was shown [60] that it is possible to further relax the constraints on the second harmonic impedance termination.

Considering the Class B half-wave rectified current wave $i_{HWR}(\theta)$ with conduction angle θ and drive level $\gamma \in [0, 1]$, the Class B/J continuous waveforms can be written as:

$$i_{HWR}(\theta) = \begin{cases} \gamma I_{max} \cos(\theta) & \text{ for } |\theta| < \frac{\pi}{2} \\ 0 & \text{ Otherwise} \end{cases}$$
(6)

$$v_{B/J} = (1 - \cos\theta)(1 - \delta\sin\theta) \tag{7}$$

where the design space $\delta \in [-1, 1]$. Eq. (7) can be expanded in its Fourier series:

$$i_{HWR} = \frac{I_{max}\gamma}{\pi} + \frac{I_{max}\gamma}{2}\cos\theta + \frac{2I_{max}\gamma}{3\pi}\cos2\theta...$$
(8)

with I_{max} denoting the maximum drain current for a given device. The optimal resistance which maximises voltage swing

for a Class B PA ($\delta = 0$) at the CG plane can be defined as a function of input drive level or output power back-off:

$$R_{opt} = \frac{2\left(V_{DC} - V_{knee}\right)}{I_{Max}\gamma} = \frac{R_L}{\gamma} = R_L 10^{\frac{|\beta|}{10}} \tag{9}$$

Here, V_{DC} is the drain supply voltage, V_{knee} is the knee voltage and β is the OBO in dB from maximum output power $(V_{DC}I_{max})/4$. In order to maintain the appropriate Class B/J waveform relationships when $\delta \neq 0$, not only the fundamental, but also the second harmonic impedance becomes a function of the back-off level:

$$Z_{B/J,f0} = \frac{R_L}{\gamma} + j\frac{R_L\delta}{\gamma} = R_{opt} + jR_{opt}\delta \qquad (10)$$

$$Z_{B/J,2f0} = -j\frac{3\pi}{8\gamma}\delta R_L = -j\frac{3\pi}{8}\delta R_{opt}$$
(11)

For the load modulation trajectory to maintain the same mode of operation (and with the same value of δ) throughout the back-off region, both fundamental and second harmonic impedance load modulation is theoretically required [39], [41], [42]. In [39] it was noted that by moving across the design space with a fixed second harmonic termination, it is possible to determine in closed form a fundamental optimal load modulation trajectory with waveforms still maintaining the same B/J relationship. To find the value for the design space of the optimal fundamental impedance, the second harmonic termination for back-off in (11) can be equated to the second harmonic impedance for peak power:

$$Z_{B/J,2f0,\beta=0} = Z_{B/J,2f0,\text{back-off}}$$
(12)

and a design space parameter α can be introduced so that for an initial value of δ , determining the optimal second harmonic for peak power, (13) holds throughout the back-off range:

$$-j\frac{3\pi}{8}\delta R_{opt} = -j\frac{3\pi}{8}\alpha R_L \tag{13}$$

resulting in:

$$\alpha = \delta \gamma \tag{14}$$

The fundamental optimal load modulation trajectory for a fixed second harmonic now becomes:

$$Z_{B/J,f0,opt} = R_{opt} + jR_{opt}\alpha \tag{15}$$

The same principle can be applied to continuous class F mode of operation with the voltage waveform up to the third harmonic [53]:

$$v_{Cont.F} = \left(1 - \frac{2}{\sqrt{3}}\cos\theta + \frac{1}{3\sqrt{3}}\cos3\theta\right)\left(1 - \delta\sin\theta\right) \quad (16)$$

The resulting fundamental and harmonic impedance design space is shown in Fig. 4(b). When δ takes a value of 0, the second harmonic is a short, the fundamental load is purely real and the conventional class F mode is realised. The corner cases, where $\delta = 1$ and $\delta = -1$, are here referred to as F/J and F/J* modes. It can be shown that the optimal fundamental impedance trajectory as a function of back-off for a fixed second and third harmonic termination (17) and (18):

$$Z_{Cont.F,2f0} = -j\frac{7\sqrt{3\pi}}{24}R_L\delta \tag{17}$$

$$Z_{Cont,F,3f0} = \infty \tag{18}$$

is determined by (19):

$$Z_{Cont.F,f0,opt} = \frac{2}{\sqrt{3}}R_{opt} + jR_{opt}\alpha$$
(19)

with α as defined in (14). For the continuous Class F⁻¹ mode of operation, the current formulation in (20) is used [54]:

$$i_{Cont.F^{-1}} = \gamma (I_{DC} - I_1 \cos \theta + I_2 \cos 2\theta + I_3 \cos 3\theta) \times (1 - \xi \sin \theta) \quad (20)$$

where $I_{DC} = 0.37$, $I_1 = 0.43$, $I_2 = 0$, $I_3 = 0.06$, and the voltage waveform is assumed to remain a constant half-wave rectified cosine wave. This design space is shown in Fig. 4(b) where modes F^{-1} , F^{-1}/J and F^{-1}/J^* are labeled for values of ξ of 0, -1 and 1 respectively.

The optimal admittances as a function of back-off are written as:

$$Y_{Cont.F^{-1},f0} = G_{opt}\sqrt{2}I_1 + jG_{opt}\sqrt{2}I_{DC}\xi \qquad (21)$$

$$Y_{Cont.F^{-1},2f0} = -j2G_{opt}(I_1 + I_3)\xi$$
(22)

$$Y_{Cont.F^{-1},3f0} = \infty \tag{23}$$

while $G_{opt} = \frac{1}{R_{opt}}$. It can be noted that the design space parameter δ was substituted by ξ to be consistent with the original formulation in the literature [51]. In order to find the value of the new design space which allows the PA to operate within the same continuous F^{-1} mode, it is possible to equate the second harmonic admittance for maximum power to the second harmonic admittance for back-off:

$$Y_{Cont.F^{-1},2f0,\beta=0} = Y_{Cont.F^{-1},2f0,\text{back-off}}$$
(24)

introducing again the design space parameter α :

$$-j2G_{opt}(I_1 + I_3)\xi = -j2G_L(I_1 + I_3)\alpha$$
(25)

where $G_L = \frac{1}{R_L}$. In order for (25) to hold throughout the back-off range:

 α

$$\xi = \xi \gamma$$
 (26)

and the continuous F^{-1} optimal fundamental admittance trajectory for a fixed second harmonic defined by (27):

$$Y_{Cont.F^{-1},f0} = G_{opt}\sqrt{2}I_1 + jG_{opt}\sqrt{2}I_{DC}\alpha \qquad (27)$$

From (14) and (26) it can be seen that the value of the design parameter α is inversely proportional to the back-off level. For continuous modes B/J and F this means that the ratio of the reactance of the optimal fundamental load to its resistance decreases with back-off. The impedance load modulation trajectories for different design space values of the class B/J mode will be later shown graphically in Section III-D and Section IV-B and compared to measured and simulated load-pull results.

As opposed to modes B/J and F it can be observed that in continuous mode F^{-1} , it is the ratio of the susceptance of the optimal fundamental admittance to its conductance that decreases with back-off. This finding confirms the experimental results presented in [61] which considers the optimal load modulation trajectories of continuous F^{-1} amplifiers.

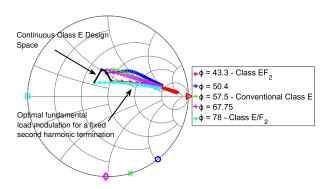


Fig. 5. Continuous Class E design space and optimal load modulation trajectories for a fixed second harmonic impedance termination.

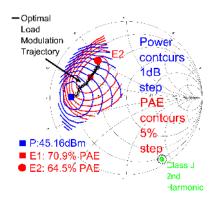


Fig. 6. Load pull power and efficiency contours (package plane) for the Wolfspeed GaN HEMT CGH40025, with a Class J second harmonic termination.

As shown in [39] a value of $|\delta| = 1$ for continuous modes B/J and F will maximise the available design space in backoff, exploiting the large reactance of the second harmonic termination to move across the design space, as back-off increases. On the other hand a median value for $|\xi| < 0.2$ for continuous Class F⁻¹ mode will maximise the available design space as the reactance of the second harmonic termination this time is inversely proportional to the back-off level.

The efficiency for the continuous modes B/J, F and F^{-1} is determined as:

$$P_{RF} = \frac{1}{2} \mathcal{R}(-V_1 I_1^*) \tag{28}$$

$$P_{DC} = I_{DC} V_{DC} \tag{29}$$

$$\eta = \frac{P_{RF}}{P_{DC}} \tag{30}$$

Where V_1 and I_1 are the fundamental components of the voltage and current waveforms respectively. A theoretical constant efficiency of 78.5%, 90.7% and 81.5% can be obtained for the Class B/J, F and F⁻¹ modes based on the waveforms in Eq. (6), (7), (16) and (20), when the knee voltage V_{knee} is assumed to be 0. When the optimal load modulation trajectories are followed, a constant efficiency is theoretically maintained throughout back-off. In practice, a non-zero knee voltage will reduce the maximum efficiency achievable if the active device is solely operated within its linear region.

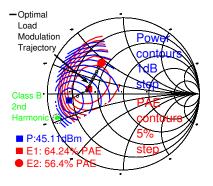


Fig. 7. Load pull power and efficiency contours (package plane) for the Wolfspeed GaN HEMT CGH40025, with a Class B second harmonic termination.

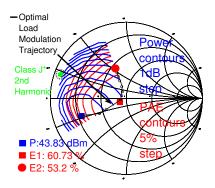


Fig. 8. Load pull power and efficiency contours (package plane) for the Wolfspeed GaN HEMT CGH40025, with a Class J^* second harmonic termination.

B. Theory applied to switched active devices

In order to overcome the limitations posed by the knee voltage, the active device can alternatively be operated as a switch. In this analysis, the single-ended switch mode power amplifier (SMPA) is modeled as a lossless switch ($R_{ON} = 0$ and 50% duty cycle) with a shunt capacitance terminated in a generic load network and the supply applied via an inductive RF choke. Following Raab's analysis on the transitioning between modes F, E and F^{-1} in PAs defined by second and third harmonics only [47], Ozen in [57] has shown analytically that a continuity in these waveform solutions can be found, and that for an arbitrary second harmonic switch impedance Z_2^S , the ZVS and ZVDS class E conditions can be satisfied.

When this analysis is extended to consider load modulation of the fundamental and second harmonic impedances, it is possible to obtain the optimal fundamental load modulation trajectories for a fixed second harmonic across the continuous design space. For modes EF_2 and E/F^{-1} where the second harmonic is a short and open, the optimal trajectories correspond to the constant Q trajectories shown in [21] as the optimal second harmonic does not move in the back-off. For other cases in the design space where Z_2^S is not a short or open, the optimal combination of fundamental and second harmonic can be obtained moving across the continuous design space as shown in Fig 5. If no losses are considered theoretical efficiency for this continuous mode is 100% as zero voltage

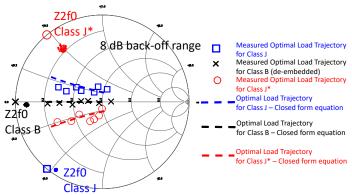


Fig. 9. Fundamental optimal load modulation impedance trajectories deembedded to the CG plane (markers) and theoretical equations (dashed).

and current overlap occurs. Losses and efficiency degradation due to non-ideal switching operation can be calculated as shown in [62].

C. Limitations of ideal waveform analysis

The analyses in Section III-A and III-B don't consider the effect that knee interaction has on the current and voltage waveform shaping. In practice, the optimal impedance trajectories for HT amplifiers depend on the amount of gain compression they are subject to throughout the load modulation process, which is determined by this interaction [59]. High efficiencies can be achieved by allowing the voltage waveform to swing deep into the knee region, increasing the available fundamental voltage swing [8], [63], and also exploiting the harmonics generated by the clipping of the current waveform to shape the voltage wave [58]. By allowing the voltage waveform to interact with the knee, the harmonic components in the current waveform will change as a function of overdrive (and back-off level), as the current bifurcation becomes more pronounced. Most nobably, the second harmonic component of the current waveform will decrease at a higher rate than its fundamental component, becoming negative as high levels of compression are reached (> 3dB), as described in [64]. It is outside of the scope of this paper to consider this phenomenon analytically, as it is strongly dependent on the clipping current waveform assumed. Rather, we focus on its implications for the design of efficient load modulated systems.

For the case of B/J PAs with a value of design space δ equal to zero which determines a shorted second harmonic, the reduction in the value of the fundamental Fourier component of the clipped waveform will result in an increase in the optimal fundamental load for efficiency, as recently shown in [59]. For HT PA modes of operation the reduction, or suppression, of the second harmonic Fourier component in the current waveform as a function of overdrive must also be considered. This reduction is particularly significant when analysing the optimal load modulation trajectories of saturated HT PAs. For HT amplifiers, a larger reactance is required in the fundamental load impedance in order to maintain the appropriate waveform shaping, as the back-off (and the

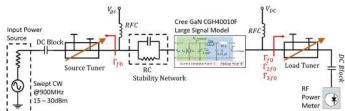


Fig. 10. Simulated test-bench with source and load tuners where V_{gs} and V_{DC} are the gate and drain supply respectively, and RFC is an RF choke.

amount of compression) is increased. Different load modulation trajectories can be determined for a given amount of gain compression by replacing the current formulation used to derive the closed form equations in (6) with other formulations such as the ones proposed in [59], [64].

D. Validation through load pull measurements

The closed form equations for the optimal load modulation trajectories for continuous mode B/J are compared to loadpull characterisation measurements on a 25W GaN Highelectron-mobility transistor (HEMT) device manufactured by Wolfspeed (CGH40025) previously presented in [42]. The measurements are carried out using Toshiba's Research Development Centre's passive harmonic load/source-pull measurement system in Kawasaki, Japan. The device is characterised at 900 MHz and biased in class B ($Ids_q = 0$ mA) with a drain-source voltage of 28 V. Only up to the second harmonic terminations were considered, with the third harmonic set to 50 Ω throughout the measurements. A variable input drive was used to keep the device at a fixed gain compression level (P_{1dB}) throughout the fundamental load-pull. Measurements were carried out for different second harmonic impedance terminations, corresponding to different values of δ in the continuous Class B/J space. Power and efficiency contours at the package plane of the device for a J, B and J* second harmonic impedance, are shown in Fig. 6, 7 and 8 respectively, highlighting the optimal fundamental load modulation trajectories. The measured optimal fundamental load trajectories are plotted in Fig. 9 after de-embedding to the CG plane using the large-signal model provided by the manufacturer. For comparison, the theoretical equations for the class B/J optimal load modulation trajectories with a fixed second harmonic Eq. (15) are plotted for different values of δ [-1, 0, 1], using $R_{opt} = 14\Omega$. The fundamental impedance points resulting in the highest measured PAE are plotted for the three modes over a 7 dB output power dynamic range. A back-off PAE greater than 50% was measured over the 7 dB output dynamic range for all cases of second harmonic terminations, with the Class J exhibiting the highest performance with 65% PAE over a 7 dB output dynamic range. The difference in measured performance can be attributed to the device's nonlinear shunt drain-source capacitance which favors capacitive reactive second harmonic impedance terminations. By enabling better waveform shaping, higher efficiency is achieved in modes with an inductive fundamental impedance, such as Class J. Additionally, the third harmonic is terminated at 50 ohms in

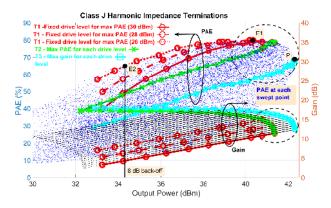


Fig. 11. Class J simulated load trajectories for: maximum efficiency with maximum input drive (red), peak efficiency with swept input power (green) and maximum gain (cyan).

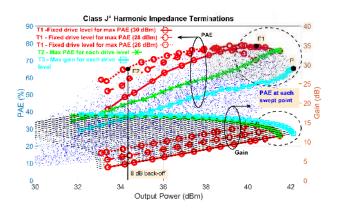


Fig. 12. Class J* simulated load trajectories for: maximum efficiency with maximum input drive (red), peak efficiency with swept input power (green) and maximum gain (cyan).

all cases, and higher harmonics are not controlled, which can contribute to the differences in measured performance among the different modes. A good agreement between the proposed formulation in Eq. (15) and the measurements verifies this analysis as a good approximation for the load modulation trajectories of PAs operated at small levels of gain compression.

IV. HT PAS LOAD MODULATION TRAJECTORIES: INVESTIGATION IN SIMULATION

A. Simulated test setup

A simulated test-bench is set up in AWR Microwave Office as shown in Fig. 10 to investigate the load modulation trajectories of HT PAs operated at different compression levels. The Wolfspeed CGH40010 GaN HEMT is used for all simulations at a target frequency of 900 MHz. The device is biased with $V_{DC} = 28$ V, $I_{ds_q} = 13$ mA and stabilised at the input with a parallel resistor-capacitor pair (5 pF || 39 Ω) in series with the gate. Simulated fundamental load pull is carried out for different harmonic impedance terminations corresponding to three values of design space (δ, ξ) for each of the continuous modes considered in Section III-A. First the Class B load-line resistance R_L is found through observation of the IV-curves and confirmed through simulated load-pull with the second

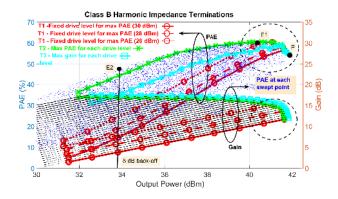


Fig. 13. Class B simulated load trajectories for: maximum efficiency with maximum input drive (red), peak efficiency with swept input power (green) and maximum gain (cyan).

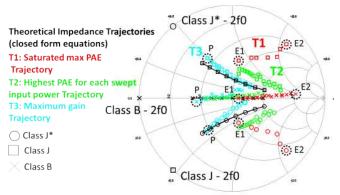


Fig. 14. CG plane impedance trajectories for: maximum efficiency with overdriven input drive (red), peak efficiency with swept input power (green) and maximum gain (cyan).

and third harmonics shorted at the CG plane. From equations (10)-(11), (17)-(19) and (21)-(22), the fundamental and second harmonic impedance terminations at the CG plane for peak power ($\beta = 0$) are calculated for continuous modes B/J, F and F^{-1} , for values of $\delta = [1, 0, -1]$ and $\xi = [0.2, 0, -0.2]$. These impedances are then transformed from the CG plane to the package plane, utilising an equivalent-circuit model for this device previously shown in [54]. The resulting fundamental and harmonic impedances normalised to 50 Ω are shown in Table I. The input was matched (at the fundamental frequency only) to the large-signal optimal impedance for maximum efficiency. Using ideal tuners, fundamental load pull was then carried out at the output, sweeping input power from 15 dBm to 30 dBm, for each harmonic termination condition. The load pull data was then de-embedded to the CG plane, using the intrinsic waveforms provided by the transistor nonlinear model.

B. Simulated load modulation trajectories comparison

Fig. 11–13 show a performance comparison for different load modulation trajectories for modes J, B and J* while Fig. 14 is presenting the resulting CG plane impedances for each trajectory compared to the equations in Section III-A. Both

TABLE I Second and Third harmonic impedances presented at Plane B and C normalised to 50 Ω

Mode:	В/Ј			Continuous F		Continuous Inverse F				
	$\delta = 1$	$\delta = 0$	$\delta = -1$	$\delta = 1$	$\delta = 0$	$\delta = -1$	$\xi = 0.2$	$\xi = 0$	$\xi = -0.2$	
$Z_{\rm f0, `C'}$	0.5 + j0.5	0.5	0.5 - j0.5	0.578 + j0.5	0.578	0.578 - j0.5	0.8 - j0.14	0.82	0.8 + j0.14	
$Z_{2\mathrm{f0},\mathrm{`C'}}$	-j0.589	0	j0.589	-j0.79	0	j0.79	j2.55	∞	-j2.55	
$Z_{3f0,'C'}$	0	0	0	∞	∞	∞	0	0	0	
$Z_{\rm f0, `B'}$	0.32 + j0.39	0.48 + j0.03	0.8 - j0.5	0.36 + j0.41	0.55 + j0.06	0.9 - j0.43	0.8 + j0.09	0.72 + j0.2	0.63 + j0.28	
$Z_{2f0,'B'}$	-j1.67	-j0.1751	-j0.23	-j3.93	-j0.1751	-j0.309	j0.618	j0.9371	j1.688	
$Z_{3f0'B'}$	-j0.278	-j0.278	-j0.278	-j0.544	-j0.544	-j0.544	-j0.278	-j0.278	-j0.278	

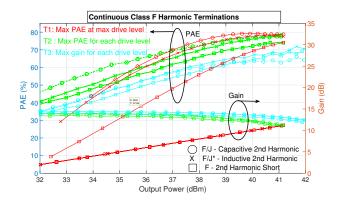


Fig. 15. Continuous F simulated load trajectories for: maximum efficiency with overdriven input drive (red), peak efficiency with swept input power (green) and maximum gain (cyan).

PAE and gain are plotted for each of the selected trajectories to assess the efficiency and the corresponding gain compression for each case.

The different load trajectories are selected as follows:

- Trajectory 1 (red) : Maximise PAE at a fixed input drive level throughout the OBO. This represents the target trajectory for outphasing systems. Three different input drive levels are considered: 30 dBm, 28 dBm and 26 dBm.
- Trajectory 2 (green) : Maximise PAE at each swept input power level from 15 dBm to 30 dBm with 0.5 dB step size. This represents the target trajectory for Doherty/DLM systems optimised for efficiency.
- Trajectory 3 (cyan) : Maximise gain at each swept input power level. This represents the target trajectory for Doherty/DLM systems optimised for constant gain/linearity.

The three different trajectories have been selected to investigate the different performance trade-offs available for load modulated system using HT PAs with reactive harmonic impedance terminations. Points P, E1 and E2 have been annotated to define the maximum power point, the maximum efficiency point and the maximum efficiency point at 8 dB back-off, respectively. First, it can be noted that for each harmonic termination a comparable maximum output power and efficiency is achieved from saturation throughout the back-off range. As expected, the optimal load modulation trajectories of PAs with $\delta = 0$ result in a purely resistive optimal load modulation, while for PAs with a reactive second harmonic impedance the optimal load trajectories are complex.

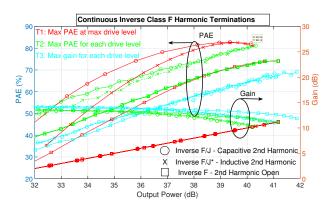


Fig. 16. Continuous F^{-1} simulated load trajectories for: maximum efficiency with overdriven input drive (red), peak efficiency with swept input power (green) and maximum gain (cyan).

Fig. 14 indicates a close match between the predicted optimal load modulation trajectories from (15) and Trajectory 3. The predicted movement across design space is found for Trajectory 2 where small levels of gain compression are tolerated. The performance of Trajectory 2 is higher than Trajectory 3 throughout the back-off range, confirming the advantage that small levels of compression or clipping have on the efficiency even when input drive is varied. For Trajectory 1 where output power back-off is equal to gain compression (irrespective of the input drive level), the optimal fundamental load trajectory follows a different profile compared to Trajectory 2 and 3. The reactance in the fundamental load necessary to compensate for the reactive second harmonic is observed to increase with back-off, confirming the observations in Section III-C.

Figs. 15 and 16 show a comparison of PAE versus output power for the load modulation Trajectories 1, 2 and 3 for continuous modes F and F⁻¹. Similar peak efficiency and back-off performance is shown for both continuous modes for all design space cases. As with the previous simulations, the efficiency of Trajectory 1 is maximised when a reactive second harmonic termination is provided. On the other hand for cases where $\xi = 0$ and $\delta = 0$, corresponding to the conventional Class F and F⁻¹ modes, a combination of input power and load variation (Trajectory 2) result in the highest performance. The optimal impedance trajectories for continuous class F mode follow the same profile of the B/J trajectories shown in Fig. 14. For the continuous class F⁻¹ the fundamental load trajectories are seen to follow the optimal trajectories reported in [61].

C. Discussion and application to outphasing systems

From the results of these simulations, it is shown that modes of operation with a shorted second harmonic termination ($\delta = 0, \xi = 0$), perform best when the Dohertylike load modulation mechanism 1 is applied, with output power modulated through both load and input power variation (Trajectory 2). This makes these modes not suitable as branch amplifiers for outphasing systems. Harmonically tuned PAs with a reactive second harmonic impedance have manifested the highest efficiency when driven deep into compression (Trajectory 1). The analysis furthermore confirms that at large values of back-off it is advantageous to modulate both input drive and the load impedance to maintain gain (and PAE), i.e., it is advantageous to use mixed-mode outphasing [30]. The optimal load modulation profiles for Trajectory 1 follow a convex curve in modes where $\delta = 1, \xi = -1$. A concave curve is followed instead when $\delta = -1$ and $\xi = 1$. In [39] it was proposed that this symmetry could be exploited in an outphasing system by utilising conjugate modes of operation for the upper and lower branch amplifiers. However, using different lower and upper amplifier branches could cause additional challenges in the design. Gain and phase imbalance between amplifier branches has been shown to be crucial for the linearity of outphasing systems [35]. Additionally, Class J amplifiers, widely investigated in the literature [56], [58], [63], have also demonstrated excellent efficiency and bandwidth performance. In the next section a design methodology is proposed to utilise HT PAs as branch amplifiers for outphasing systems ($\delta = 1$). A comparison is then drawn with outphasing system using PAs operating in conventional high efficiency modes ($\delta = 0$).

V. OUTPHASING AMPLIFIER DESIGN METHODOLOGY

A. Conventional outphasing theory

In an outphasing system with simple lossless quarterwaveform combining, the reactive loading at the combiner plane A in Fig. 1 is defined in [14] for the upper and lower branch amplifiers as:

$$Y_{1,2}(\psi) = R_{load} \frac{2\cos^2 \psi}{Z_0^2} \pm j R_{load} \frac{\sin 2\psi}{Z_0^2}$$
(31)

where ψ is the outphasing angle, related to the OBO by $\beta = 20 \log_{10} (\cos^2 \psi)$, Z_0 and R_{load} are the characteristic impedance of the $\frac{\lambda}{4}$ line and the load impedance respectively. Output power is therefore controlled through the variation of ψ . It has often been assumed in previous literature that the efficiency of outphasing systems is proportional to the power factor of the combiner [13], [14], [16] defined as:

$$k_p = \frac{Re(Y_1) + Re(Y_2)}{|Y_1| + |Y_2|}$$
(32)

In order to maximise the power factor, the reactive loading can be compensated in the combiner through a series or shunt reactance X_c . For the case of a two-way outphasing system the reactive loading can be canceled at two points only in the outphasing output power dynamic range. For a given output power back-off level β_{comp} where perfect reactive cancellation is desired it is possible to define the normalised powers P_1 and P_2 as in [29] so that:

$$\beta_{comp} = 10 \log 10(\frac{P_1}{P_2})$$
 (33)

$$P_1 + P_2 = 1 \tag{34}$$

The instantaneous outphasing angles ψ_1 and ψ_2 where the reactance is zeroed can be calculated from (35) and (36):

$$P_1 = \frac{2V_L^2 \cos \psi_1^2}{R_{load}^2}$$
(35)

$$P_2 = \frac{2V_L^2 \cos \psi_2^2}{R_{load}^2}$$
(36)

where V_L is the maximum voltage swing at the load, and R_{load} is the load resistance. This approach leads to a value for the series compensating reactance X_c given by (37):

$$X_c = \frac{R_{load}}{\frac{\sin\psi_1}{\sin\psi_2}} \tag{37}$$

and an instantaneous loading on the PA branches:

$$Y_{1,2}(\psi) = \frac{2}{R_{load}} (\sin \psi^2 \pm j (\cos \psi \sin \psi - \frac{R_{load}}{X_c})) \quad (38)$$

However, due to the package parasitics and the drain source capacitance of real devices, the load pull contours shift away from the real axis and therefore a black box approach is often followed in the design of outphasing PAs. This consists in the optimisation of the output matching networks of each branch and combiner, based on load pull data obtained through simulations or measurements [36]. The harmonics are either shorted or load pulled at saturation for peak power and efficiency, potentially leading to sub-optimal solutions in the back-off. As the second harmonic impedance termination is shown to have a significant impact on the back-off efficiency of outphasing amplifiers, the approach proposed in this paper is to design branch amplifiers with HT PAs such as Class J PAs, which favour the complex outphasing loading trajectories determined by (31). The Chireix combiner will not be used to cancel the reactance at a given point but rather to provide the appropriate phase shift in each branch so that the optimal load modulation trajectory at the CG plane, shown in Fig. 14, is followed as closely as possible throughout the outphasing operation for both PA branches.

B. New method

As shown in Section IV, multiple fundamental and harmonic impedance solutions exist which achieve comparable high efficiency at the maximum rated power for a given device. However as it was previously seen for each of these solutions, both back-off performance and optimal load modulation trajectory profiles differ. For this reason, a methodology is proposed to maximise the back-off efficiency and output power dynamic range through the appropriate selection of the amplifier's mode of operation and design of the output matching and combiner networks. The methodology aims not only to achieve high efficiency over a wide back-off range but also to exploit the maximum output power capabilities of a given device.

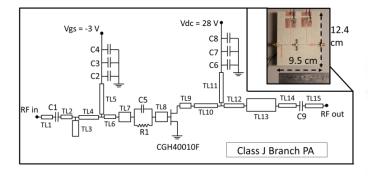


Fig. 17. Schematic of fabricated Class J PA. Dimensions of the transmission lines follow as widths mm /lengths mm: TL1 = 1.7/2, TL2 = 1.7/1 TL3 = 3.9/26.8, TL4 = 1.7/17.8, TL5 = 1/51.8, TL6 = 1.7/2.4, TL7 = 4.1/4.6, TL8 = 4.1/4.6, TL9 = 2.5/2.7, TL10 = 1.1/16.5, TL11 = 1/51.8, TL12 = 1.7/4.9, TL13 = 5.9/13.8, TL14 = 1.7/5, TL15 = 1.7/5. Component values are: C1, C2, C6, C9 = 100pF, C3, C7 = 1nF, C4, C9 = 10nF, C5 = 5pF, R1 = 39 Ohms.

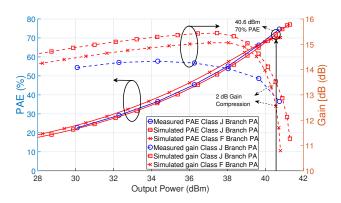


Fig. 18. PAE, gain versus output power of single-ended Class J (measurement and simulations) and Class F amplifiers when loaded with 50 Ω .

Step 1: Determine the desired maximum output power of the outphasing system (P_{max}) and the frequency of operation (f_c) . This will determine the choice of technology and required size for the devices.

Step 2: Estimate a value for C_{ds} and package parasitics. To ensure that the appropriate harmonic impedances are presented at the CG plane of each transistor, it is necessary to estimate the drain-source capacitance and main parasitics. If the nonlinear model of the device used provides access to the current and voltage intrinsic waveforms, the fundamental components of these waveforms can also be used to determine the impedance at the CG plane.

Step 3: Estimate the optimal class B fundamental resistance R_L at the CG plane of the device. An initial guess can be taken observing the I-V curves and using (9). For a more accurate estimation a simulated test set-up as in Fig. 10 should be used. After stabilising the device, the transistor should be matched at the input to the complex conjugate of its large signal input impedance. While ensuring a short is presented at the second and third harmonic at the CG plane, the fundamental load impedance should be swept for maximum power. This process should be repeated for multiple input power levels as the choice of input drive will impact the gain compression and PAE of the amplifier at the peak power point. A compromise

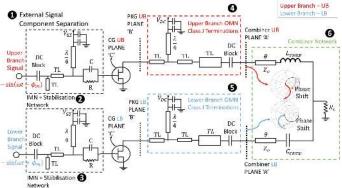


Fig. 19. Block Diagram of proposed J-J outphasing system exploting the reactive harmonic terminations to improve back-off efficiency.

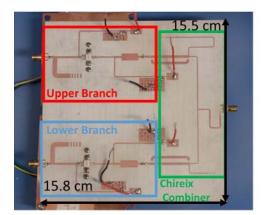


Fig. 20. Photograph of the fabricated J-J outphasing amplifier.

should be chosen depending on the gain requirements of the system at peak power.

Step 4: Select the continuous mode of operation, design space value (δ, ξ) and determine the value of the required second harmonic impedance terminations for the upper and lower branch amplifiers. The continuous mode of operation will determine the placement of the third harmonic and the shape of the optimal load trajectory for efficiency. As shown in Figs. 11-16, when driven hard into saturation all continuous modes considered (B/J, F and F^{-1}) can present high values of efficiency throughout a large back-off range. The choice of continuous mode of operation therefore does not represent a critical factor in the design of outphasing systems. On the other hand, the choice of the design space is critical: for values of $|\delta| > 0.8$ and $|\xi| < 0.2$ a large second harmonic impedance is present, which can compensate for the outphasing reactive loading. It should be also noted that convex and concave optimal load trajectories are observed for conjugate modes of operation such as J and J*. An advantage can be found if different values of design space (δ, ξ) are applied in the design of the upper and lower branch amplifiers which will then present different harmonic terminations. Once the values of the design space are found, the second harmonic termination can be calculated using (11), (17) and (22).

Step 5: Select the bias level of the upper and lower branch amplifiers. The bias can be selected once the mode of oper-

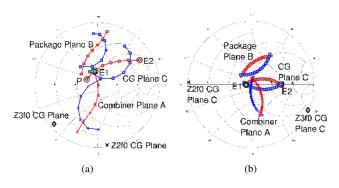


Fig. 21. Impedances at combiner (plane A), package (plane B) and current generator plane (plane C) for the outphasing systems designed with: (a) – class J amplifiers, and (b) – class F amplifiers.

ation is chosen: while for B/J modes the transistor is biased at pinch-off to reduce the third harmonic component from the current waveform, class AB biasing is preferred in class F and a biasing closer to class A for F^{-1} modes as the harmonics in the current waveform are more suitable for the required shaping of the waveform at these biasing levels. Note that the choice of the design space value within a particular continuous mode will not affect the choice of biasing (δ , ξ).

Step 6: Find points P, E1 and E2 for the chosen continuous mode by load pulling the device at the overdriven input power level selected while presenting at the CG plane the second and third harmonic terminations previously calculated [*Step* 4]. If different values of (δ, ξ) were selected for the lower and upper branches, the points P, E1 and E2 will be different for the two branches. Transform the required impedances to the package plane of the amplifier to find points P_{PKG} E1_{PKG} and E2_{PKG}.

Step 7: Design the branch amplifiers' output matching networks so that the input impedance of each network corresponds to point P_{PKG} [Step 6] at the fundamental frequency and at the second and third harmonics to the values found in [Step 4].

Step 8: Design an ideal Chireix combiner so that the CG plane trajectories of the lower and upper outphasing branches intersect at points P and E2, passing through the high efficiency point E1. If the same value of δ or ξ is used for both branches, it will not be possible to simultaneously meet this condition for both branches. It will be later shown that the degradation in performance, due to deviation from the ideal trajectory, is not significant.

Step 9: Transform the ideal combiner into a realizable lumped or distributed circuit using optimisation techniques or, one of the design techniques shown in [29]. It should be noted that to additionally reduce size and losses in the output network, [*Step 7*] and [*Step 8*] can be combined utilising analytical techniques [65].

VI. DESIGN EXAMPLE

A comparison is carried out in simulation between two outphasing systems designed following the method proposed in Section V-B. In one system, Class J amplifiers ($\delta = 1$) are selected as the outphasing PA branches; in the other case

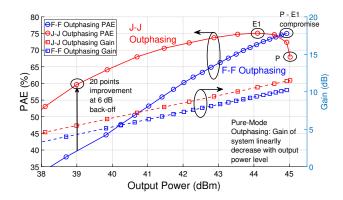


Fig. 22. Simulated comparison between PAE and gain of outphasing system when implemented with Class F and Class J PAs.

conventional Class F PAs ($\delta = 0$) are used. In order to support a direct comparison, the amplifier branches of both outphasing systems are designed for comparable efficiency and output power when driven into saturation at their P_{2dB} compression point.

A. Outphasing branch amplifier design [Steps 1 - 7]

For the design example and proof of concept a target maximum output power of 25 Watts is set (P_{max}) at a centre frequency of 900 MHz (f_c) [Step 1]. The Wolfspeed CGH40010F 10-W GaN HEMT is selected based on the results in Section IV-A, which show the device is capable of delivering up to 15 Watts output power at the frequency of interest. Additionally, the nonlinear device model provided by the manufacturer allows direct access to the intrinsic CG current and voltage waveforms. The simulation results presented in Section IV-A are now used as an aid in the design of the outphasing system. A model for the package parasitics and drain-source capacitance ($C_{ds} = 1.2 \text{ pF}$) previously published [54] is used to find the impedance terminations required at the package of the transistor to achieve a second and third harmonic short. The CG harmonic impedances are also verified using the intrinsic current and voltage waveforms from the nonlinear model [Step 2]. The amplifier is stabilised at the input and matched to the large-signal optimal impedance for efficiency which was found through simulated source-pull. With a short presented at both harmonics, a fundamental load-pull is carried out (shown in Fig. 13) and $R_L = 25\Omega$ can be estimated at a $P_{in} = 30$ dBm [Step 3]. The B/J continuous mode has been chosen for this example and a value of design space $\delta = 1$ (Class J) was selected for both upper and lower branch PAs. The motivation for this choice is led by the simplicity of the Class J circuit design approach and the scalability of the method at higher frequencies of operation. The second harmonic impedance termination can then be calculated at the CG plane $Z_{2f0,CG} = -j14.7\Omega$ and transformed to the package $Z_{2f0,PKG} = -j41.25\Omega$, approximating the device's output parasitics as a two port newtork. The same applies to the third harmonic, short at the CG plane, but resulting in $Z_{3f0,PKG} = -j6.9\Omega$ at the package [Step 4]. Biasing is set at pinch off with $V_{GS} = -3.05$ V, throughout the simulations

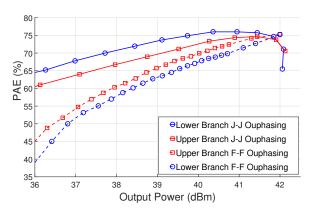


Fig. 23. Simulated lower and upper branch amplifier efficiencies for F-F and JJ outphasing systems.

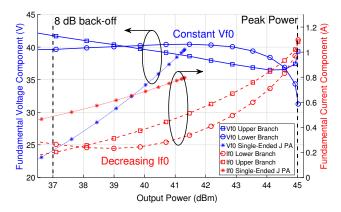


Fig. 24. Simulated lower and upper branch amplifier voltage and current fundamental components for J-J outphasing system and single-ended Class J PA.

on the Class J single branch PA [Step 5].

The simulated load pull and resulting optimal load trajectory for a fixed drive level (T1) in Fig. 11 and Fig. 14 are used to find the target impedances for the design of the output matching network of the J-J outphasing system's branch amplifier. As upper and lower branch amplifiers are designed with the same value of design space, it will not be possible to present at the CG plane of both their optimal load trajectory throughout the outphasing complex load modulation. The matching network of the Class J PA is designed so that a compromise impedance, between points E1 and P (Fig. 14), for maximum power and efficiency respectively, is presented at the CG plane of the device [Step 6]. The matching topology implemented consists of an open stub and stepped impedance transformer to control the fundamental and second harmonic impedance terminations [55]. The layout is optimised in NI AWR Axiem and ADS Momentum electromagnetic simulators to minimise the insertion loss of the matching network in the desired frequency band. The schematic and a photograph of the Class J PA is shown in Fig. 17.

For the amplifier operating in a conventional mode with $\delta = 0$, a Class F PA is implemented as inherently more efficient than a Class B, when operated in deep saturation [48]. A similar matching topology is implemented for the Class F

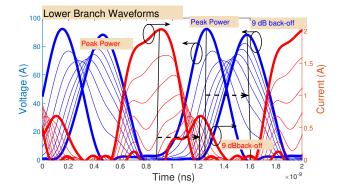


Fig. 25. Current and voltage waveforms at the device's CG plane for the J-J outphasing Lower Branch, for different outphasing angles and back-off levels.

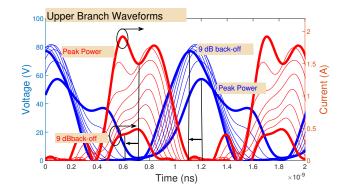


Fig. 26. Current and voltage waveforms at the device's CG plane for the J-J outphasing Upper Branch, for different outphasing angles and back-off levels.

PA using an additional double balanced open stub to control the third harmonic termination. Fig. 18 presents the simulated PAE and gain for the Class F and Class J branch amplifiers designed, demonstrating very close performance both in terms of efficiency and gain. In order to verify the simulated results, the Class J PA circuit was fabricated on Rogers 4350 substrate (0.762 mm thickness) with $\epsilon_r = 3.48$ and $\tan \delta = 0.0037$. Its measured performance for 50 Ω loading is compared to the simulations of both PAs in Fig. 18, finding close agreement. The Class J PA achieves over 14.5 dB small-signal gain and delivers in excess of 40.5 dBm with 70% PAE at its P_{2dB} compression point [*Step 7*]. A small difference between the measured and simulated gain for the Class J PA is observed although it does not impact the PAE predictions.

B. Outphasing system integration [Steps 8 - 9]

Once the single-ended Class J and F PAs have been designed and their performance compared, the next step is to integrate the branches into the outphasing system. A block diagram and picture of the J-J outphasing system can be seen in Figs. 19 and 20 where the building blocks of a generic active loadmodulated system, previously defined (Sec. II, Fig. 1), are also annotated. A description of the design of blocks 2-5 is given in the previous section while the signal component generation and separation (block 1) is assumed to be external to the outphasing system. Block 6 in Fig. 19 shows the ideal implementation used for the design of the Chireix outphasing

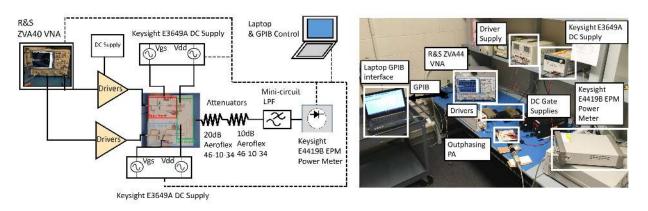


Fig. 27. Block Diagram and photograph of measurement set-up utilised to test the proposed J-J outphasing system.

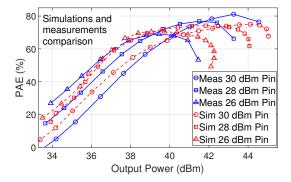


Fig. 28. Measurement and simulated comparison of J-J outphasing system at 900 MHz.

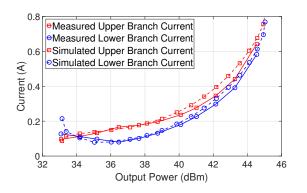


Fig. 29. Simulated and measured DC currents for upper and lower branch PAs in the J-J outphasing system.

combiner. By controlling the electrical lengths of the series transmission lines as well as the values of the capacitor C_{comp} and the inductor L_{comp} it is possible to control the values of the reactances presented to each of the PA branches as well as the phase shift between them. Considering the branch amplifiers have been designed to operate in a 50 Ω load, the aim of the combiner network is to present to each branch an impedance close to 50 Ω when the outphasing angle between the two branches is 0° corresponding to in-phase (or peak power) combining. Additionally the network should introduce the appropriate phase shift between the two PA branches so that the load seen by the amplifers, dynamically varying with

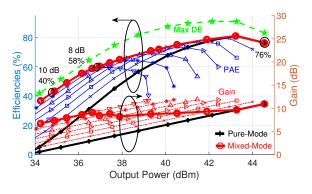


Fig. 30. Measured PAE and gain at 900 MHz of J-J outphasing system for pure-mode and mixed mode outphasing for a swept angle of 74° .

outphasing angle, follows the wanted high efficiency trajectory (Fig. 14) throughout the back-off. The conventional analysis in Section V-A, which assumes the power factor of the Chireix combiner is proportional to the system's efficiency, can be used only for the design of the conventional F-F outphasing system $(\delta = 0)$. In the design of the J-J system the compensating elements have been empirically tuned to obtain the closest possible match with the wanted load trajectory for both the lower and upper amplifier branches [Step 8]. Once the values of the ideal compensating elements are found they can be transformed to real distributed elements as shown in [65] and [29]. The lumped elements were transformed to distributed transmission lines using open circuit stubs in both branches for the J-J and F-F outphasing systems, to minimise the effect of the parasitics and tolerances of the components on the final performance [Step 9].

C. J - J and F - F outphasing system comparison

After EM optimisation of the layouts of the combining networks for the J-J and F-F outphasing systems, the resulting impedance trajectories at planes A, B and C for the two cases are shown in Fig. 21. This plot shows the impedance trajectories that designers working at the CG plane, package plane or with pre-matched amplifiers would target when implementing an outphasing system, for two different harmonic termination conditions. As derived analytically in Section III and demonstrated on a single-ended PA with passive load tuning in Section IV, the trajectories resulting from the design of an outphasing system for cases (a) and (b) differ significantly. Focusing on the CG plane, the trajectories of the F-F system resemble the conventional outphasing curves with the upper and lower branch PAs experiencing a complex inductive and capacitive load modulation respectively. On the other hand the J-J CG plane trajectories for both amplifier branches remain in the inductive side of the smithchart over the entire back-off range considered, and are also not centered around the real axis. A simulated PAE/gain vs output power comparison between the two outphasing systems is shown in Fig. 22. As expected, the outphasing systems present comparable performance at saturation both in terms of efficiency and output power. However in the back-off, the efficiency of the J-J outphasing system shows a significant improvement when compared to the F-F system. This can be attributed to the effect that a reactive second harmonic termination has, shaping the current and voltage waveforms (as compared to a second harmonic short), when high voltage knee interaction occurs. In Fig. 23 the efficiencies of the upper and lower branch amplifiers for both J-J and F-F outphasing systems can also be observed. The efficiencies of the two branches follow similar profiles in both systems with the J-J branches perfoming better than the F-F in the back-off, as expected. For the J-J outphasing case the efficiency of the lower branch is higher than the upper branch throughout the back-off, due to the convex class J optimal load trajectory close match with the convex outphasing lower branch loading. The behaviour of the J-J system can be analysed through Figs. 24-26, which show the lower and upper branch PAs' CG plane current/voltage fundamental components and time-domain waveforms, over a 9 dB output power back-off. Fig. 24 demonstrates the principle of operation of the outphasing system. As the outphasing angle is increased and output power decreases, the voltage fundamental component can be seen to remains (almost) constant, while the current fundamental component decreases. The increase in the fundamental component of the voltage waveforms at small levels of back-off can be attributed to a transition from a class J to an increasingly switched mode reduced harmonic class E PA, once the PA is heavily overdriven. This corresponds to the transistion of the instantaneous loading from the high power point P to the high efficiency point E1. The fundamental V and I components of the single-ended class J branch PA operating in a 50 Ω load versus output power, have also been included, highlighting the different operating principles. As opposed to the outphasing system, in the single-ended case both the fundamental voltage and current components increase proportionally with input drive, controlling in this way the output power delivered to the load. From the time-domain waveforms it can be observed that as the outphasing angle is increased, the current waveform drops and shifts in time due to the reactive instantaneous loading. The reactive loading does not cause additional power dissipation due to the compensation of the second harmonic termination.

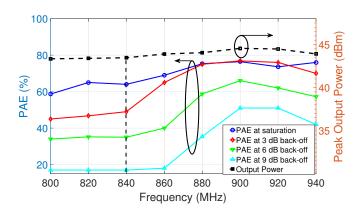


Fig. 31. Measured peak output power and PAE at different back-off levels of J-J outphasing system over frequency.

VII. SYSTEM IMPLEMENTATION AND EXPERIMENTAL VALIDATION

A. Realisation and experimental setup

A J-J outphasing amplifier demonstrator was built to experimentally validate the simulated results. The outphasing amplifier is realised on Rogers 4350 substrate and mounted on a brass fixture. A photograph of the manufactured outphasing PA is shown in Fig. 20.

The PA is tested using two RF phase coherent sources generated by a R&S ZVA40 VNA. The VNA is controlled via GPIB, through a Matlab script running on a host laptop. The outputs from the two ports of the VNA are amplified by two Mini-circuit ZHL-1000 linear drivers and fed into the outphasing PA. A digital Keysight DC supply measures the currents drawn by the two branch amplifiers. Output power is measured after an attenuator and low-pass filter using a Keysight power meter E4419B EPM. A photograph and a block diagram of the setup is shown in Fig. 27.

B. CW system performance

Continuous Wave (CW) measurements are carried out by varying both the amplitude and relative phases of the two CW branch PA inputs. Both PA branches are supplied with 28 V and $Ids_q = 13$ mA. Fig. 28 shows a comparison of simulated and measured PAE vs. output power at the nominal 900 MHz operating frequency. It can be seen that the compression characteristics at the upper 4 dB of operation do not exactly match between the model and measured result, but overall there is agreement between measurement and simulation. Similarly, the measured and simulated drain currents vs. output power, shown in Fig. 29, present good agreement. The lower branch PA has been measured to be more efficient throughout the outphasing range, confirming the theoretical assumptions and the findings in simulations.

Fig. 30 shows CW 900 MHz measurements in which the input power is stepped from 24.5 to 30.5 dBm and the outphasing angle is swept from $-14 \deg$ to 70 deg. A PAE of 76% is measured at saturation, while the outphasing system delivers 44.6 dBm with the branch PAs driven with 30.5 dBm. Using pure-mode outphasing, over 55% PAE is achieved for 6

	Technology	Arch.	f _o (GHz)	P_{peak} (W)	$\substack{\eta @P_{peak} \\ (\%)}$	η @ 6dB OPBO (%)	η @ 8dB OPBO (%)
[32]	GaN	Asymmetrical Multi-Level Outphasing	1.95	18	57	56	55
[34]	GaN	4-Way Outphasing	2.14	60	69	55	50
[30]	GaN	Conventional Chireix	2.14	>63	60	58	52
[23]	GaN	Chireix using Load Insensitive SMPA Branches	2.25	>54	65	50	60
[21]	65 nm CMOS-GaN	Chireix using Cont. Class E Branches	0.9	>24	79	81	70
[20]	GaN	Doherty Outphasing Power Amplifier	2.14	112	66	58	60
[38]	LDMOS	RF-input Doherty Outphasing	2.17	138	>55	>55	50
[7]	GaN	3-Way Doherty	2.14	100	70	>60	>55
[9]	GaN	4-Way Doherty	2.14	100	77	>60	60
[29]	GaN	4-Way Outphasing	2.14	105	72	>60	55
[10]	GaN	Asymmetric Doherty	2	15	71	>50	60
[24]	GaN	Chireix with Class E Branches	2.3	70.6	81	>60	>60
[22]	CMOS GaN	Chireix with Class E Branches	1.95	19	>70	>60	>60
[11]	GaN	Symmetrical Doherty	3.5	28	>70	>65	>60
[12]	GaN	Symmetrical Doherty	1.95	25	>60	62	60
This work	GaN	J-J Chireix	0.9	28.18	83	81	65

 TABLE II

 COMPARISON PERFORMANCE WITH STATE-OF-THE-ART LOAD MODULATED SYSTEMS

dB back-off. With mixed mode outphasing, PAE can be further improved and kept greater than 60% for an output power back off range of 8 dB. The measured results are compared with the state of the art in Table II. The higher absolute efficiency performance recorded by the J-J system can be attributed to the lower frequency and power level utilised in this work compared to most of the load modulated systems in Table II. Among the works considered, [21] is the closest comparison in terms of performance, frequency, output power level and design approach exploiting the continuous class E method (which also presents a reactive second harmonic termination). The benefits of the methodology in V-B and the advantage of using PA modes with a reactive harmonic termination in outphasing is therefore clearly demonstrated. As the shape of the optimal load modulation profile of the Class J PA matches the outphasing loading trajectories, constant drain efficiency can be obtained throughout a wide output power dynamic range, without having to sacrifice performance at saturation, power utilisation and output power dynamic range.

C. Bandwidth investigation

The combiner implementation in this work was not designed for wideband operation. However it was noted that the Class J PAs designed in Section VI-A exhibit constant output power and efficiency over a 200 MHz bandwidth (800 MHz - 1 GHz), due to their appropriate fundamental and second harmonic impedance movements in the band. Therefore, the bandwidth of the outphasing system has been characterized and the results for a sweep of 140 MHz are shown in Fig. 31. A drain efficiency of more than 50% at 6 dB back-off was recorded for 140 MHz bandwidth, leading to an estimated fractional bandwidth of 13%. Exploring HT modes of operation for wideband outphasing is a topic of interest for future work.

VIII. CONCLUSIONS

Closed form equations for the optimal load modulation of various families of PA continuous modes have been derived. The predicted optimal load trajectory formulation for the continuous B/J mode has been verified with load-pull measurements. The importance of the second harmonic termination has been stressed in systems operating under complex load modulation trajectories, and a methodology for the design of outphasing PAs exploiting a reactive second harmonic is proposed. The methodology is verified through the design and measurement of a J-J outphasing amplifier showing results that compare favorably to the state of the art with PAE >60% over 7dB output power back-off.

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REFERENCES

- V. Carrubba, E. Ture, S. Maroldt, M. Mußer, F. Van by, R. Quay, and O. Ambacher, "A dual-band UMTS/LTE highly power-efficient class-ABJ Doherty gan pa," in *Eur. Microw. Conf.*, 2015, pp. 1164–1167.
- [2] N. Tuffy and L. Pattison, "A linearized, high efficiency 2.7 GHz wideband Doherty power amplifier with class-J based performance enhancement," in *Eur. Microw. Conf.*, 2015, pp. 215–218.
- [3] J. Moon *et al.*, "Efficiency enhancement of Doherty amplifier through mitigation of the knee voltage effect," *IEEE Trans. Microw. Theory and Techn.*, vol. 59, no. 1, pp. 143–152, 2011.
- [4] P. Colantonio et al., "Increasing Doherty amplifier average efficiency exploiting device knee voltage behavior," *IEEE Trans. Microw. Theory* and Techn., vol. 59, no. 9, pp. 2295–2305, 2011.
- [5] W. Hallberg *et al.*, "A Doherty power amplifier design method for improved efficiency and linearity," *IEEE Trans. on Microw. Theory and Techn.*, vol. 64, no. 12, pp. 4491–4504, Dec 2016.
- [6] W. H. Doherty, "A new high efficiency power amplifier for modulated waves," *Proc. of the Inst. of Radio Eng.*, vol. 24, no. 9, pp. 1163–1182, 1936.
- [7] M. J. Pelk et al., "A high-efficiency 100-W GaN three-way Doherty amplifier for base-station applications," *IEEE Trans. Microw. Theory* and Techn., vol. 56, no. 7, pp. 1582–1591, 2008.
- [8] J. Kim et al., "A saturated Doherty power amplifier based on saturated amplifier," *IEEE Microw. and Wireless Compon. Lett.*, vol. 20, no. 2, pp. 109–111, 2010.

- [9] A. Grebennikov, "A high-efficiency 100-W four-stage Doherty GaN HEMT power amplifier module for WCDMA systems," in *IEEE MTT-S Int. Microw. Symp. Dig.* IEEE, 2011, pp. 1–4.
- [10] H. Jang, P. Roblin, and C. Quindroit, "Adjustable load-modulation asymmetric Doherty amplifier design using nonlinear embedding," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2014, pp. 1–4.
- [11] M. Özen and C. Fager, "Symmetrical Doherty amplifier with high efficiency over large output power dynamic range," in *IEEE MTT-S Int. Microw. Symp. Dig.*, June 2014, pp. 1–4.
- [12] M. Ozen, K. Andersson, and C. Fager, "Symmetrical doherty power amplifier with extended efficiency range," *IEEE Trans. on Microw. Theory and Techn.*, vol. 64, no. 4, pp. 1273–1284, April 2016.
- [13] D. J. Perreault, "A new power combining and outphasing modulation system for high-efficiency power amplification," *IEEE Trans. on Circuits* and Syst. I: Reg. Papers, vol. 58, no. 8, pp. 1713–1726, 2011.
- [14] F. Raab, "Efficiency of outphasing RF power-amplifier systems," *IEEE Trans. Commun.*, vol. 33, no. 10, pp. 1094–1099, 1985.
- [15] M. Litchfield, T. Reveyrand, and Z. Popović, "Load modulation measurements of X-band outphasing power amplifiers," *IEEE Trans. Microw. Theory and Techn.*, vol. 63, no. 12, pp. 4119–4129, 2015.
- [16] H. Chireix, "High power outphasing modulation," Proc. of the Inst. of Radio Eng., vol. 23, no. 11, pp. 1370–1392, 1935.
- [17] A. F. Aref *et al.*, "Efficient amplification of signals with high PAPR using a novel multilevel LINC transmitter architecture," in *Eur. Microw. Conf.*, 2012, pp. 1035–1038.
- [18] P. A. Godoy *et al.*, "A 2.4-GHz, 27-dBm asymmetric multilevel outphasing power amplifier in 65-nm CMOS," *IEEE J. of Solid-State Circuits*, vol. 47, no. 10, pp. 2372–2384, 2012.
- [19] T. W. Barton and D. J. Perreault, "Theory and implementation of RFinput outphasing power amplification," *IEEE Trans. Microw. Theory and Techn.*, vol. 63, no. 12, pp. 4273–4283, 2015.
- [20] A. R. Qureshi et al., "A 112W GaN dual input Doherty-Outphasing power amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2016, pp. 1–4.
- [21] M. Özen et al., "A generalized combiner synthesis technique for Class-E outphasing transmitters," *IEEE Trans. on Circuits and Syst. I: Reg. Papers*, 2017.
- [22] M. P. van der Heijden et al., "A 19W high-efficiency wide-band CMOS-GaN class-E Chireix RF outphasing power amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2011, pp. 1–4.
- [23] D. A. Calvillo-Cortes *et al.*, "A package-integrated Chireix outphasing RF switch-mode high-power amplifier," *IEEE Trans. Microw. Theory and Techn.*, vol. 61, no. 10, pp. 3721–3732, 2013.
- [24] D. A. Calvillo-Cortes, M. P. van der Heijden, and L. C. de Vreede, "A 70W package-integrated class-E Chireix outphasing RF power amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2013, pp. 1–3.
- [25] M. P. van der Heijden and M. Acar, "A radio-frequency reconfigurable CMOS-GaN class-E chireix power amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2014, pp. 1–4.
- [26] R. Zhang et al., "Generalized Semi-Analytical Design Methodology of Class-E Outphasing Power Amplifier," *IEEE Trans. on Circuits and Syst.* I: Reg. Papers, vol. 61, no. 10, pp. 2951–2960, Oct 2014.
- [27] M. Litchfield and Z. Popovic, "Multi-level Chireix Outphasing GaN MMIC PA," in 2015 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), Oct 2015, pp. 1–4.
- [28] W. Gerhard and R. Knoechel, "Differentially coupled outphasing WCDMA transmitter with inverse class F power amplifiers," in *Proc. IEEE Topical Conf. Power Amplif. Wireless Radio Appl.*, Jan 2006, pp. 355–358.
- [29] T. W. Barton, A. S. Jurkov, P. H. Pednekar, and D. J. Perreault, "Multi-way lossless outphasing system based on an all-transmissionline combiner," *IEEE Trans. Microw. Theory and Techn.*, vol. 64, no. 4, pp. 1313–1326, 2016.
- [30] J. H. Qureshi *et al.*, "A 90-W peak power GaN outphasing amplifier with optimum input signal conditioning," *IEEE Trans. Microw. Theory and Techn.*, vol. 57, no. 8, pp. 1925–1935, 2009.
- [31] I. Hakala et al., "A 2.14-GHz Chireix outphasing transmitter," IEEE Trans. on Microw. Theory and Techn., vol. 53, no. 6, pp. 2129–2138, June 2005.
- [32] P. A. Godoy *et al.*, "A highly efficient 1.95-GHz, 18-W asymmetric multilevel outphasing transmitter for wideband applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2011, pp. 1–4.
- [33] A. Ravi et al., "A 2.4-GHz 20–40-MHz channel WLAN digital outphasing transmitter utilizing a delay-based wideband phase modulator in 32-nm CMOS," *IEEE J. of Solid-State Circuits*, vol. 47, no. 12, pp. 3184–3196, 2012.

- [34] T. W. Barton, J. L. Dawson, and D. J. Perreault, "Experimental validation of a four-way outphasing combiner for microwave power amplification," *IEEE Microw. and Wireless Components Letters*, vol. 23, no. 1, pp. 28– 30, 2013.
- [35] T. M. Hone et al., "Gain/phase compensation for outphasing transmitters targeting LTE applications," in Proc. IEEE Topical Conf. Power Amplif. Wireless Radio Appl. IEEE, 2014, pp. 40–42.
- [36] M. Pampín-González et al., "Outphasing combiner synthesis from transistor load pull data," in *IEEE MTT-S Int. Microw. Symp. Dig.* IEEE, 2015, pp. 1–4.
- [37] T. Hwang et al., "Nonlinearity modeling of a Chireix outphasing power amplifier," *IEEE Trans. on Circuits and Syst. I: Reg. Papers*, vol. 62, no. 12, pp. 2898–2907, 2015.
- [38] H. Jang et al., "RF-input self-outphasing Doherty–Chireix combined amplifier," *IEEE Trans. Microw. Theory and Techn.*, vol. 64, no. 12, pp. 4518–4534, 2016.
- [39] P. E. de Falco et al., "Asymmetrical outphasing: Exploiting conjugate continuous modes of operation," in Proc. IEEE Topical Conf. Power Amplif. Wireless Radio Appl., 2017, pp. 18–21.
- [40] C. M. Andersson *et al.*, "Theory and design of class-J power amplifiers with dynamic load modulation," *IEEE Trans. Microw. Theory and Techn.*, vol. 60, no. 12, pp. 3778–3786, 2012.
- [41] K. Mimis and G. T. Watkins, "Design method for harmonically-tuned, dynamic load-modulated power amplifiers," in 2015 German Microw. Conf., March 2015, pp. 1–4.
- [42] K. Mimis *et al.*, "Output harmonic optimisation of dynamically load modulated power amplifiers," in *Eur. Microw. Conf.*, 2016, pp. 1071– 1074.
- [43] D. J. Shepphard, J. Powell, and S. C. Cripps, "An efficient broadband reconfigurable power amplifier using active load modulation," *IEEE Microw. and Wireless Compon. Lett.*, vol. 26, no. 6, pp. 443–445, 2016.
- [44] S. D. Kee et al., "The class-E/F family of ZVS switching amplifiers," IEEE Trans. Microw. Theory and Techn., vol. 51, no. 6, pp. 1677–1690, June 2003.
- [45] F. H. Raab, "Class-F power amplifiers with maximally flat waveforms," *IEEE Trans. Microw. Theory and Techn.*, vol. 45, no. 11, pp. 2007–2012, Nov 1997.
- [46] —, "Maximum efficiency and output of class-F power amplifiers," *IEEE Trans. Microw. Theory and Techn.*, vol. 49, no. 6, pp. 1162–1166, Jun 2001.
- [47] —, "Class-E, class-C, and class-F power amplifiers based upon a finite number of harmonics," *IEEE Trans. Microw. Theory and Techn.*, vol. 49, no. 8, pp. 1462–1468, Aug 2001.
- [48] D. M. Snider, "A theoretical analysis and experimental confirmation of the optimally loaded and overdriven RF power amplifier," *IEEE Trans.* on Electron Devices, vol. 14, no. 12, pp. 851–857, 1967.
- [49] J. D. Rhodes, "Output universality in maximum efficiency linear power amplifiers," *International Journal of Circuit Theory and Applications*, vol. 31, no. 4, pp. 385–405, 2003. [Online]. Available: http://dx.doi.org/10.1002/cta.239
- [50] S. C. Cripps et al., "On the continuity of high efficiency modes in linear RF power amplifiers," *IEEE Microw. and Wireless Compon. Lett.*, vol. 19, no. 10, pp. 665–667, 2009.
- [51] V. Carrubba et al., "Exploring the design space for broadband PAs using the novel continuous inverse class-F mode," in *Eur. Microw. Conf.*, 2011, pp. 333–336.
- [52] —, "On the extension of the continuous class-F mode power amplifier," *IEEE Trans. Microw. Theory and Techn.*, vol. 59, no. 5, pp. 1294–1303, 2011.
- [53] —, "The continuous class-F mode power amplifier," in *Eur. Microw. Conf.*, 2010, pp. 1674–1677.
- [54] K. Chen and D. Peroulis, "Design of broadband highly efficient harmonic-tuned power amplifier using in-band continuous Class-F-1 F mode transferring," *IEEE Trans. Microw. Theory and Techn.*, vol. 60, no. 12, pp. 4107–4116, 2012.
- [55] K. Mimis *et al.*, "Multichannel and wideband power amplifier design methodology for 4G communication systems based on hybrid class-J operation," *IEEE Trans. Microw. Theory and Techn.*, vol. 60, no. 8, pp. 2562–2570, 2012.
- [56] P. Wright *et al.*, "A methodology for realizing high efficiency class-J in a linear and broadband PA," *IEEE Trans. Microw. Theory and Techn.*, vol. 57, no. 12, pp. 3196–3204, 2009.
- [57] M. Ozen, R. Jos, and C. Fager, "Continuous class-E power amplifier modes," *IEEE Trans. on Circuits and Syst. II: Express Briefs*, vol. 59, no. 11, pp. 731–735, Nov 2012.
- [58] S. Cripps, RF power amplifiers for wireless communications. Artech House, 2006.

- [59] R. Quaglia, D. J. Shepphard, and S. Cripps, "A reappraisal of optimum output matching conditions in microwave power transistors," *IEEE Trans. Microw. Theory and Techn.*, 2016.
- [60] T. Canning, P. J. Tasker, and S. C. Cripps, "Continuous mode power amplifier design using harmonic clipping contours: Theory and practice," *IEEE Trans. Microw. Theory and Techn.*, vol. 62, no. 1, pp. 100–110, 2014.
- [61] L. Xiang, M. Helaoui, and F. Ghannouchi, "Optimal fundamental load modulation for harmonically tuned switch mode power amplifier," *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 60, no. 12, pp. 4107–4116, 2016.
 [62] F. H. Raab and N. O. Sokal, "Transistor power losses in the class E
- [62] F. H. Raab and N. O. Sokal, "Transistor power losses in the class E tuned power amplifier," *IEEE Journal of Solid-State Circuits*, vol. 13, no. 6, pp. 912–914, Dec 1978.
- [63] J. Moon, J. Kim, and B. Kim, "Investigation of a Class-J power amplifier with a nonlinear Cds for optimized operation," *IEEE Trans. Microw. Theory and Techn.*, vol. 58, no. 11, pp. 2800–2811, 2010.
- [64] J. Moon et al., "Behaviors of Class-F and Class-F and Class F-1 amplifiers," *IEEE Trans. Microw. Theory and Techn.*, vol. 60, no. 6, pp. 1937–1951, 2012.
- [65] M. Ozen, K. Andersson, and C. Fager, "Symmetrical Doherty power amplifier with extended efficiency range," *IEEE Trans. on Microw. Theory and Techn.*, vol. 64, no. 4, pp. 1273–1284, April 2016.



Paolo Enrico de Falco Paolo received his B.E. in Electronic Engineering from the University of Portsmouth in 2013, where he developed a strong interest in telecommunications. He then went on to start a PhD at the Centre for Doctoral Training in Communications at the University of Bristol. His research interests include broadband RF amplifiers and efficiency enhancement techniques for wireless communication applications. During his time at the University of Bristol Paolo has won first place in the International Microwave Symposium (2016 IMS)

High Efficiency Power Amplifier Student Design Competition as well as in the 2016 European Microwave Week Student Challenge.



Prathamesh Pednekar received his B.E. degree in Electronics and Telecommunication Engineering at The University of Mumbai in 2012. Prior to joining UT Dallas in 2014, he worked as a Research Scientist at Society for Applied Microwave Electronic Engineering and Research, Mumbai. He completed his M.S. degree in Electrical Engineering in August 2016, and is now pursuing a PhD at the University of Colorado Boulder. His research interests are Efficiency enhancement techniques for Power amplifiers, Passive Microwave components

and Phased array RADAR architectures.



Souheil Ben Smida (M07) received the M.Sc. degree in electronics and instrumentation from the University of Pierre and Marie Curie Paris 6, Paris, France, in 2000, and the Ph.D. degree in electronics and communications from the Ecole Nationale Suprieure des Telecommunications, Paris, France, in 2005. He was a Post-Doctoral Fellow with the iRadio Laboratory, University of Calgary, Calgary, AB, Canada, from 2006 to 2008. He is currently a Lecturer of electrical and electronic engineering with the University of Bristol, Bristol, U.K. His

current research interests include nonlinear characterization and linearization of power amplifiers for mobile and satellite applications and microwave instrumentation.



Kevin Morris received the B.Eng. and Ph.D. degrees in electronics and communications engineering from the University of Bristol, Bristol, U.K., in 1995 and 2000, respectively. He is currently a Reader of RF engineering and Head of the Department of Electrical and Electronic Engineering, University of Bristol. He has authored or coauthored over 70 academic papers. He holds five patents. His research interests principally concern looking at methods of reducing power consumption in communications systems including the area of RF hardware design

with a specific interest in the design of efficient linear broadband power amplifiers for use within future communications systems. Dr. Morris is currently involved with a number of the Engineering and Physical Sciences Research Council (EPSRC) and Industry funded research programs within the U.K.



Gavin Watkins is a member of both the Institute of Engineering Technology and the European Microwave Association. He received the MEng degree in Electrical and Electronic Engineering in 2000 from the University of Bristol and a PhD from the same institution in 2003 on the topic of Wideband Feedforward Amplifiers for Software defined Radios. From 2003 to 2004, he was a technical consultant for Detica Information Intelligence before joining the University of Bristol as a research associate. Since 2008 he has been with Toshiba Research

Europe Limited where he is currently a Research Fellow and responsible for supervising a number of RF related projects. He is an executive committed member of the IETs RF and Microwave Technical and Professional Network. In 2016 he received a Toshiba Innovation award for his contribution to a new range of high efficiency FM radio transmitters. He also won the International Journal of Microwave and Wireless Technologies Best Paper Award in 2015 for his work on envelope tracking RF power amplifiers.



Konstantinos Mimis received the M.Sc. and Ph.D. degrees from the University of Bristol, Bristol, U.K., in 2008 and 2013, respectively. Since 2012 he has been with Toshiba Research Europe Limited, Bristol, UK where he currently is a member of the RF team as a Senior Research Engineer. His main research interests include high efficiency, broadband power amplifier design, amplifier linearization, efficiency enhancement techniques and RF/MW instrumentation.



Taylor Wallis Barton Taylor W. Barton (S'07, M'12) received the Sc. B., M.Eng., E.E., and Sc.D degrees from the Massachusetts Institute of Technology, Cambridge, MA. In 2016 she joined the Department of Electrical, Computer, and Energy Engineering at the University of Colorado Boulder, where she is currently an Assistant Professor. Prior to joining CU Boulder, she was a Postdoctoral Associate in the MIT Microsystems Technology Laboratories and then an Assistant Professor at the University of Texas at Dallas. Her research interests

include high-efficiency RF, power, and analog circuit design.