Hindawi Publishing Corporation
Journal of Nanomaterials
Volume 2013, Article ID 831252, 5 pages
http://dx.doi.org/10.1155/2013/831252

Research Article

Long Channel Carbon Nanotube as an Alternative to Nanoscale Silicon Channels in Scaled MOSFETs

Michael Loong Peng Tan

Faculty of Electrical Engineering, Universiti Teknologi Malaysia (UTM), 81310 Skudai, Johor, Malaysia

Correspondence should be addressed to Michael Loong Peng Tan; michael@fke.utm.my

Received 11 July 2013; Accepted 26 November 2013

Academic Editor: Chunyi Zhi

Copyright © 2013 Michael Loong Peng Tan. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Long channel carbon nanotube transistor (CNT) can be used to overcome the high electric field effects in nanoscale length silicon channel. When maximum electric field is reduced, the gate of a field-effect transistor (FET) is able to gain control of the channel at varying drain bias. The device performance of a zigzag CNTFET with the same unit area as a nanoscale silicon metal-oxide semiconductor field-effect transistor (MOSFET) channel is assessed qualitatively. The drain characteristic of CNTFET and MOSFET device models as well as fabricated CNTFET device are explored over a wide range of drain and gate biases. The results obtained show that long channel nanotubes can significantly reduce the drain-induced barrier lowering (DIBL) effects in silicon MOSFET while sustaining the same unit area at higher current density.

1. Introduction

Carbon nanotubes (CNTs) are gaining momentum in the current silicon technology as a complementary nanostructure that could reform the device architecture. CNT modeling has been rigorously studied and examined [1–5] to assess the performance of the device at the circuit level. Advancement of the nanotechnology devices modeling is vital for the foreseeable future of carbon nanotube as switching device, interconnect and memory in integrated circuits (ICs). An in situ growth single-walled carbon nanotube (SWCNT), which integrates long channel 600 nm CNT channel, thin Al_2O_3 top gate contact, and Palladium (Pd) metal source/drain contacts, has been demonstrated [6].

In addition, we report the potential of long channel 65 nm CNT as substitute to 45 nm silicon metal-oxide semiconductor field-effect transistor (Si MOSFET) from the perspective of modeling for future CNT-logic applications. We observe good agreement between CNTFET and Si MOSFET respectively, when simulating two-terminal drain current–voltage (I_d-V_d) characteristic. The projection has shed light on the reduction of DIBL and high field effects [7] as well as reduction in long channel CNT which is a widespread phenomenon in nanoscale Si MOSFET [8, 9]. We also demonstrate the effects of the channel area restructuring on the maximum electric field as well as density of states (DOS) in the conductance of CNT. Unlike MOSFET, it is revealed that the performance of CNT is enhanced when the source and drain width is minimized rather than the length, primarily due to the gate-to-source-drain parasitic fringe capacitances [10]. MOSFET scaling in accordance with Moore's Law will reach its fundamental limitation as a result of process controllability in the next 10 years. Consequently, it is necessary to ensure that novel material is studied to provide alternatives to the current technologies and challenges in the new era of nanotechnology.

2. Carbon Nanotube and MOSFET Modeling

The layout of a CNTFET device is depicted in Figure 1. The area of the channel is given by the multiplication of the width, W, of the source and drain contact and the length, L, of the nanotube [6]. Details of the quasiballistic MOSFET device modeling can be found in previous work in [11, 12].

The carbon nanotube model [13] is a unified nanostructure model based on quantum transport theory established by Datta [14]. This work extended the universal DOS spectral

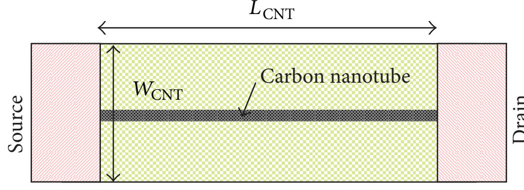


Figure 1: The unit area size of CNT channel with source and drain.

function [15] into the numerical calculation for CNT conduction subbands. We have included multiband density of states to account for multimode transport [16]. For an accurate simulation, the input parameters shown in Table 1 for MOSFET and CNTFET are extracted from TSMC [17] and Javey et al. [18], respectively. The 60 nm nanotube device model incorporate quasiballistic transport scattering as confirmed by [18]. At 60 nm length, the carriers travelling on the CNT surface have smaller mean free path than acoustic phonon which occurred at 300 nm.

The typical width of a high-tech CNTFET device is reported [10] to be 1 μm. The width of the CNT is calculated to be $W_{CNT} = A_{MOS}/L_C$, when both CNT and MOSFET devices are having identical channel area ($A_{MOS} = A_{CNT}$). In a case when both devices can provide same level of current, channel area becomes $A = (kL)^2$ when given the scaling factor; k and both parameter $W = L$. CNT channel with length, $2\,kL_{CNT}$, can provide the same current with $W_{CNT} = 0.5\,L_{CNT}$. Even when the physical widths of the CNT channel, $W \leq 0.5\,kL_{CNT}$, there is no area drawback provided $L \geq 2\,kL_{CNT}$. As nanotube channel length increases, maximum electric field in CNT, E_{mCNT} reduces tremendously [19, 20]. As for CNT with $L = 60$ nm, the maximum electric field is found to be $E_m = (3/4)E_{mSi}$.

In the I_d-V_d simulation of CNTFET, Landauer-Buttiker formalism is utilized [21]. The drain current, I_d is given as

$$\begin{aligned} I_d(V_G, V_d, V_s) &= G_{ON}\frac{k_BT}{q}\left[\log\left(1+\exp\left(q\frac{(E_F - V_{sc}(V_G, V_d, V_s))}{k_BT}\right)\right)\right] \\ &\quad - G_{ON}\frac{k_BT}{q} \\ &\quad \times\left[\log\left(1+\exp\left(q\frac{(E_F - V_{sc}(V_G, V_d, V_s) - V_d - V_s)}{k_BT}\right)\right)\right], \end{aligned} \tag{1}$$

where G_{ON} is the ON-conductance, V_{sc} is the channel potential, E_F is the Fermi energy, k_B is the Boltzmann Constant, T is the temperature, q is the charge of an electron, V_G is the gate voltage, V_d is the drain voltage, and V_s is the source voltage.

The quantum conductance limit of a ballistic SWCNT is $G_{ON} = 4q^2/h$. The theoretical framework of (1) derivation can be found in [19, 20]. The quasi-one-dimensional (Q1D) density of state function of CNT [22] is given by

Table 1: Device model input and output parameter at $V_G = 1$ V.

Parameter	CNT	MOSFET
Type	Zigzag	NMOS
Structure	Q1D	Q2D
Gate insulator thickness, t_{ox}	1.1 nm	1.1 nm
Channel length, L	60 nm	45 nm
Channel width, W	67.5 nm	90 nm
Channel area, A	4.05×10^{-15} m^2	4.05×10^{-15} m^2
Tube diameter, d	1.5437 nm	—
Chiral vector (n, m)	(20, 0)	—
Maximum electric field, E_m	0.75 E_{mSi}	E_{mSi}
Maximum current, $I_{d\max}$	59.43 μA	65.2 μA
Carrier density, $I_{d\max}/(d$ or $W)$	42.8 μA/nm	0.8 μA/nm
DIBL	39.41 mV/V	56.23 mV/V
Subthreshold swing, SS	74.44 mV/dec	32.37 mV/dec
On-off ratio	9.2×10^3	3.8×10^3

$$D(E) = \frac{2g_v g_s}{3\pi a_{cc} t}\sum_i \frac{E}{\sqrt{E^2 - (E_G/2)^2}}, \tag{2}$$

where $a_{cc} = 1.42$Å and $t = 3$ eV is the carbon-to-carbon (C–C) bonding energy, E_G is the bandgap energy, g_s is the spin degeneracy, and g_v is the valley degeneracy. On the other hand, the I_d-V_d characteristics for a short channel MOSFET can be expressed as

$$I_d = \frac{C_G \mu_{ef} W_{MOS}}{L}\frac{((V_G - V_T) - (1/2)V_d)V_d}{1 + V_d/V_c}, \quad 0 \leq V_d \leq V_{d\,sat}, \tag{3}$$

where C_G is the gate capacitance, μ_{ef} is the gate-field dependent mobility, $V_{d\,sat}$ is the saturation voltage at the point of current saturation, V_c is the critical voltage, and V_T is the threshold voltage. At current saturation, (3) becomes

$$I_{d\,sat} = \alpha C_G (V_G - V_T - V_{d\,sat}) W v_{sat}, \quad V_d \geq V_{d\,sat}, \tag{4}$$

where $\alpha = v_D/v_{sat}$ is ratio of drift velocity, v_D with saturation velocity and v_{sat} at the drain [11, 23].

3. Results and Discussion

Figure 2 shows the density of states for Q1D of [20, 0] zigzag CNT with three van Hove singularities. As the energy span widens, more electrons are capable of occupying the singularities pinned between source and drain Fermi levels.

In the I_d-V_d simulation, the source Fermi energy is set to be at 0.22 eV below the conduction band. Our simulation results in Figure 3 which comes from (1) indicate that the CNT is able to offer drain current performance comparable to a 45 nm Si MOSFET. Remarkably, the effective current per

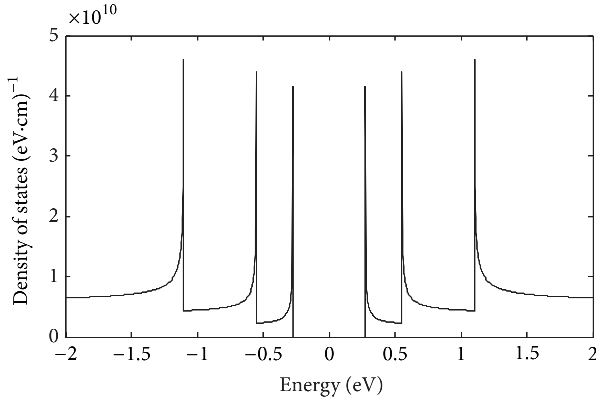


Figure 2: Electronic density of states calculated for [20, 0] zigzag nanotubes.

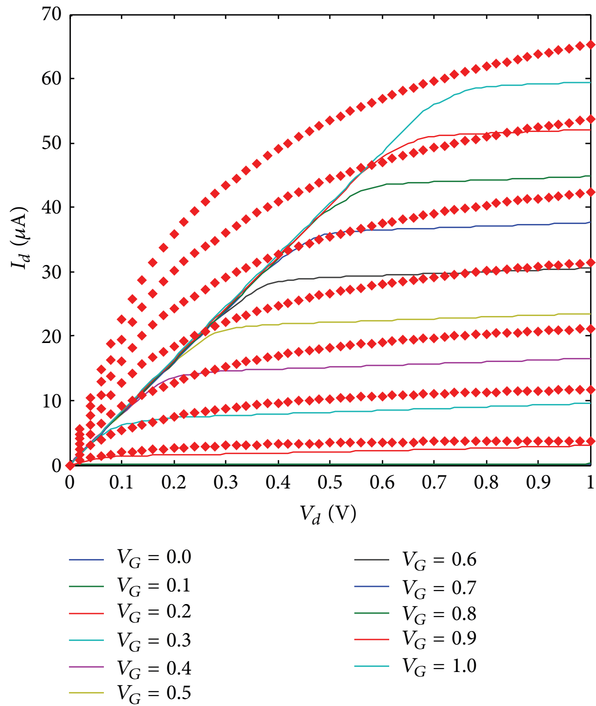


Figure 3: Drain characteristic of 60 nm single-walled carbon nanotube (colour solid lines) and 45 nm MOSFET (diamonds) with 0.1 V gate increment. Initial V_G for MOSFET is 0.4 V (bottom).

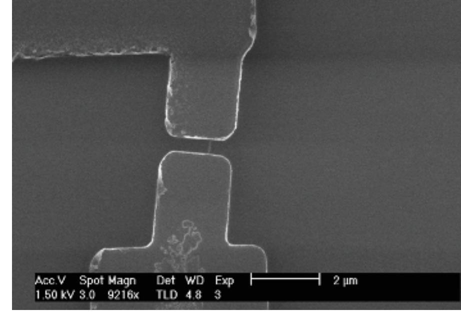


Figure 4: Plan view of SWCNT formed between Palladium source and drain contact.

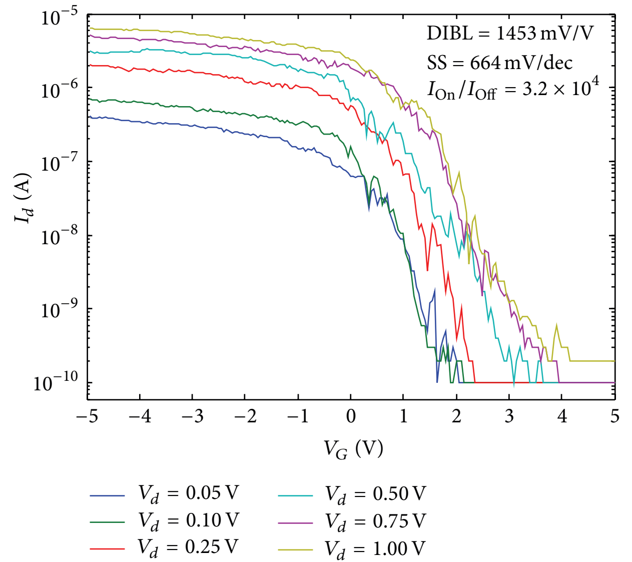


Figure 5: Gate characteristics measurement of a 600 nm CNT from V_d = 0.05 to V_d = 1.0 V.

unit dimension yielded 53.5 times more of Si channel because of the small diameter tube.

The DIBL effects is suppressed fairly well for both devices with a slight advantage to CNT. Silicon demonstrated a superior subthreshold swing at 32.37 mV/dec, a value half of CNT. Although CNT has a lower on current, it sustains a high on-off ratio in 4 orders of magnitude. In addition to the device simulation, a SWCNT with a channel length of 600 nm is fabricated and shown in Figure 4. The Paladium contacts are made by electron beam lithography on SWCNT grown by thermal CVD from catalyst islands.

The I_d-V_G measurement was carried out on a back gate geometry ≈200 nm SiO_2 depicted in Figure 5. From Figure 3, the gate characteristic, I_d-V_G, can be generated for the 60 nm CNT model and it is illustrated in Figure 6. The DIBL for the experimental data is at 1453 mV/V, while SS is estimated to be 664 mV/dec. Nevertheless, the 600 nm fabricated CNT is compensated by a high off-on ratio at 3.2×10^4. It is found that DIBL can be lowered by at least one order of magnitude by doping the source end region of the channel [24] or the whole CNT [25, 26].

4. Conclusion

It is revealed that long channel CNT can deliver drain current comparable to a MOSFET. The carrier density along the CNTFET is at least 50 times that of the Si MOSFET. In the same channel area, CNT has better control of short channel effect (SCE) than Si as it has lower E_m. This brings an enormous advantage since lower E_m has a smaller DIBL. A double gate or a cylindrical gate structure has the best control

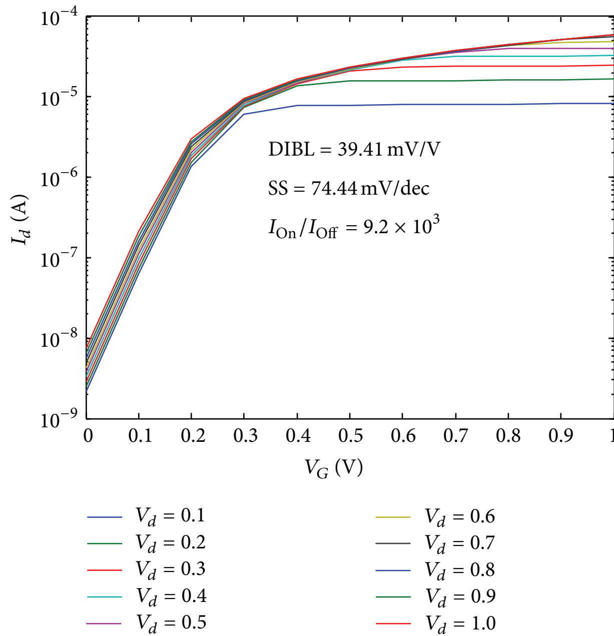


Figure 6: Gate characteristics of a 60 nm CNT model from $V_d = 0.1$ to $V_d = 1.0$ V in 0.1 V increment.

to suppress DIBL [27]. Based on this, we could have lower off-current in the transistor. As a result, a CNT uses less power consumption as a switching device when operating at the same frequency as a MOSFET.

Acknowledgments

MLPT thanks the Ministry of Higher Education Malaysia and the Universiti Teknologi Malaysia (UTM) for the award of advanced study fellowship leading to a Ph.D. degree at the University of Cambridge. This work is partially supported by UTM Research University Grant vot no. Q.J130000.2623.09J21 and Fundamental Research Grant Scheme (FRGS/2/2013/SG02/UTM/02/2). MLPT is also immensely grateful to Aun Shih Teh for providing the experimental data of SWCNT. The author also thanks the Research Management Centre (RMC) of UTM and Centre for Advanced Photonics and Electronics (CAPE), Cambridge, UK, for providing an excellent research environment to complete this work.

References

[1] J. Deng and H.-S. P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application. Part I: model of the intrinsic channel region," *IEEE Transactions on Electron Devices*, vol. 54, no. 12, pp. 3186–3194, 2007.

[2] J. Deng and H.-S. P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application. Part II: full device model and circuit performance benchmarking," *IEEE Transactions on Electron Devices*, vol. 54, no. 12, pp. 3195–3205, 2007.

[3] J. Guo, S. Datta, M. Lundstrom et al., "Assessment of silicon MOS and carbon nanotube FET performance limits using a general theory of ballistic transistors," in *Proceedings of the IEEE International Devices Meeting (IEDM)*, pp. 711–714, December 2002.

[4] J. M. Marulanda, A. Srivastava, and A. K. Sharma, "Transfer characteristics and high frequency modeling of logic gates using carbon nanotube field effect transistors (CNT-FETs)," in *Proceedings of the 20th Symposium on Integrated Circuits and System Design*, pp. 202–206, Rio de Janeiro, Brazil, September 2007.

[5] K. Natori, Y. Kimura, and T. Shimizu, "Characteristics of a carbon nanotube field-effect transistor analyzed as a ballistic nanowire field-effect transistor," *Journal of Applied Physics*, vol. 97, no. 3, Article ID 034306, 2005.

[6] G. A. J. Amaratunga, A. S. Teh, S. N. Cha et al., "Nanotube and nanowire transistors," in *Proceedings of the Interational Semiconductor Conference (CAS '05)*, vol. 1, pp. 3–8, October 2005.

[7] V. K. Arora and M. L. P. Tan, "High-field transport in graphene and carbon nanotubes," in *Proceedings of the IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC '13)*, pp. 1–2, 2013.

[8] M. T. Ahmadi, R. Ismail, M. L. P. Tan, and V. K. Arora, "The ultimate ballistic drift velocity in carbon nanotubes," *Journal of Nanomaterials*, vol. 2008, Article ID 769250, 8 pages, 2008.

[9] R. Vidhi, M. L. P. Tan, T. Saxena, A. M. Hashim, and V. K. Arora, "The drift response to a high-electric-field in carbon nanotubes," *Current Nanoscience*, vol. 6, no. 5, pp. 492–495, 2010.

[10] B. C. Paul, S. Fujita, M. Okajima, and T. Lee, "Modeling and analysis of circuit performance of ballistic CNFET," in *Proceedings of the 43rd Design Automation Conference*, pp. 717–722, 2006.

[11] V. K. Arora, M. L. P. Tan, I. Saad, and R. Ismail, "Ballistic quantum transport in a nanoscale metal-oxide-semiconductor field effect transistor," *Applied Physics Letters*, vol. 91, no. 10, Article ID 103510, 2007.

[12] M. L. P. Tan, R. Ismail, R. Muniandy, and V. K. Wong, "Velocity saturation dependence on temperature, substrate doping concentration and longitudinal electric field in nanoscale MOSFET," in *Proceedings of the IEEE National Symposium on Microelectronics*, 2005.

[13] A. Rahman, J. Guo, S. Datta, and M. S. Lundstrom, "Theory of ballistic nanotransistors," *IEEE Transactions on Electron Devices*, vol. 50, no. 9, pp. 1853–1864, 2003.

[14] S. Datta, *Electronic Transport in Mesoscopic Systems*, Cambridge University Press, Cmabridge, UK, 1994.

[15] J. W. Mintmire and C. T. White, "Universal density of states for carbon nanotubes," *Physical Review Letters*, vol. 81, no. 12, pp. 2506–2509, 1998.

[16] J. Appenzeller, J. Knoch, M. Radosavljević, and P. Avouris, "Multimode transport in schottky-barrier carbon-nanotube field-effect transistors," *Physical Review Letters*, vol. 92, no. 22, Article ID 226802, 2004.

[17] Z. Dawei, Z. Hao, Y. Zhiping, and T. Lilin, "A unified charge model comprising both 2D quantum mechanical effects in channels and in poly-silicon gates of MOSFETs," *Solid-State Electronics*, vol. 49, no. 10, pp. 1581–1588, 2005.

[18] A. Javey, J. Guo, M. Paulsson et al., "High-field quasiballistic transport in short carbon nanotubes," *Physical Review Letters*, vol. 92, no. 10, Article ID 106804, 2004.

[19] M. L. P. Tan and G. A. J. Amaratunga, "Performance prediction of graphene nanoribbon and carbon nanotube transistors," in *Proceedings of the AIP Conference Proceedings,*, vol. 1341, pp. 365–369, 2011.

[20] M. L. P. Tan, G. Lentaris, and G. A. Amaratunga, "Device and circuit-level performance of carbon nanotube field-effect transistor with benchmarking against a nano-MOSFET," *Nanoscale Research Letters*, vol. 7, article 467, 2012.

[21] Y. Imry and R. Landauer, "Conductance viewed as transmission," *Reviews of Modern Physics*, vol. 71, no. 2, pp. S306–S312, 1999.

[22] D. C. Y. Chek, M. L. P. Tan, M. T. Ahmadi, R. Ismail, and V. K. Arora, "Analytical modeling of high performance single-walled carbon nanotube field-effect-transistor," *Microelectronics Journal*, vol. 41, no. 9, pp. 579–584, 2010.

[23] M. L. P. Tan, V. K. Arora, I. Saad, M. Taghi Ahmadi, and R. Ismail, "The drain velocity overshoot in an 80 nm metal-oxide-semiconductor field-effect transistor," *Journal of Applied Physics*, vol. 105, no. 7, Article ID 074503, 2009.

[24] Z. Arefinia and A. A. Orouji, "Novel attributes in the performance and scaling effects of carbon nanotube field-effect transistors with halo doping," *Superlattices and Microstructures*, vol. 45, no. 6, pp. 535–546, 2009.

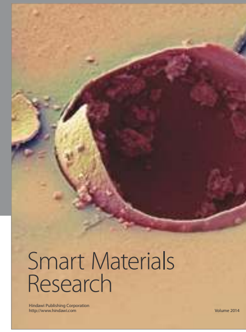
[25] J. Chen, C. Klinke, A. Afzali, and P. Avouris, "Self-aligned carbon nanotube transistors with charge transfer doping," *Applied Physics Letters*, vol. 86, no. 12, Article ID 123108, pp. 1–3, 2005.

[26] K. Alam and R. Lake, "Role of doping in carbon nanotube transistors with source/drain underlaps," *IEEE Transactions on Nanotechnology*, vol. 6, no. 6, pp. 652–659, 2007.

[27] N. Bahador, M. L. P. Tan, M. T. Ahmadi, and R. Ismail, "A unified drain-current model of silicon nanowire field-effect transistor (SiNWFET) for performance metric evaluation," *Science of Advanced Material*, vol. 6, pp. 354–360, 2014.

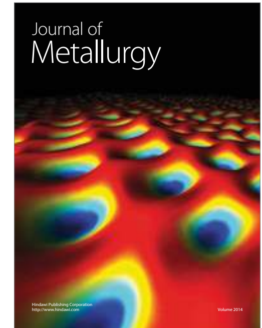
Journal of
Nanotechnology

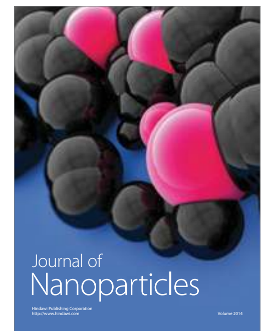
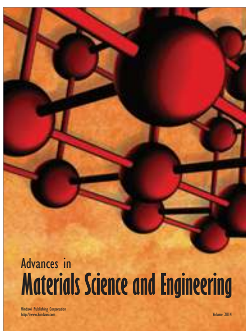
International Journal of
Corrosion

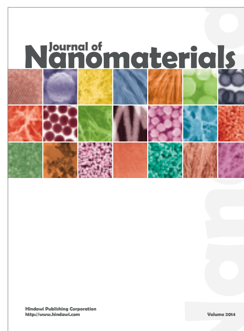
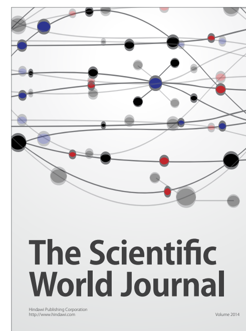
International Journal of
Polymer Science

Smart Materials
Research

Journal of
Composites

BioMed
Research International

Hindawi
Submit your manuscripts at
http://www.hindawi.com

Journal of
Metallurgy

Journal of
Materials

Journal of
Nanoparticles

Advances in
Materials Science and Engineering

Scientifica

Journal of
Nanomaterials

The Scientific
World Journal

International Journal of
Biomaterials

Journal of
Nanoscience

Journal of
Coatings

Journal of
Crystallography

Journal of
Ceramics

Journal of
Textiles