








Long-Haul Coupled 4-Core Fiber Transmission Over 7,200 Km With Real-Time MIMO DSP

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Abstract—In this work, we present an experimental demonstration of real-time transoceanic space-division multiplexed transmission with coupled-core multicore fibers. To compensate for modal coupling in the coupled-core multicore fibers, we implement real-time multiple-input multiple-output (MIMO) digital signal processing based on field programmable gate array circuits. Using optical receivers with a real-time MIMO, we demonstrate 16-channel wavelength-division multiplexed coupled four-core fiber transmission over 7200 km. The results show the feasibility of real-time coupled-core multicore fiber transmission.

Index Terms—Long-haul transmission, mode-division multiplexing, real-time digital signal processing.

I. INTRODUCTION

IN OPTICAL submarine cable systems, as a part of the global communication infrastructure, the total cable capacity must be continuously enlarged to meet the vast future traffic demands. Because the available power supply from cable landing stations to optical amplifiers is limited practically [1], the average optical power in optical submarine cable systems is strongly constrained. Under the average optical power constraint, massive space division multiplexing (SDM) operating at reduced capacity per SDM channel is effective for increasing the total capacity [1]–[2] because increasing the number of spatial paths

is a more power-efficient approach than increasing the channel power and spectral efficiency. The straightforward approach is based on optical cables containing fiber pairs (FPs), in which many conventional single mode fibers are packed together and employed as SDM channels. To date, 16-fiber-pair cables have become commercially available [3]. However, as the number of FPs increases, the cross-sectional area of the fiber cable that can accommodate optical fibers inevitably increases [4]. This suggests that the approach of increasing FPs will reach space limitations unless the current cable designs are changed. However, it is challenging to develop new cable designs considering optical characteristics, mechanical reliability, manufacturing cost, lifetime, water pressure resistance and so on.

Multicore fibers (MCFs) are a promising candidate to increase the number of SDM channels under space limitations in current cable designs. The MCFs have many cores [5]–[6] in a fiber, and the cores are utilized as SDM channels. Even with the same cladding diameter as a conventional single mode fiber, MCFs can have 4–5 cores. Moreover, conventional digital signal processing (DSP) for standard single mode fibers can be utilized for signal reception because the crosstalk between cores is sufficiently suppressed. Recently, long-haul transmission experiments with MCFs have been demonstrated [7]–[10]. Thus, MCFs seem to be a reasonable approach to increasing cable capacity by a factor related to the number of cores in an MCF.

To further increase the number of SDM channels in optical cables, mode division multiplexing (MDM) techniques based on few-mode fibers (FMFs) and coupled-core multicore fibers (CC-MCFs) are more advantageous than the MCF approach. In FMFs, parallel SDM channels (i.e., linear polarized modes) share the cross-section of the fiber, resulting in a large number of multiplexed modes. In CC-MCFs, crosstalk between cores is allowed to increase the number of cores. Because spatial mode couplings are inevitable during FMF and CC-MCF propagation, which should be compensated by introducing multiple-input multiple-output (MIMO) DSP in optical receivers. The most challenging issue is clarifying how many modes can be processed with a practical MIMO DSP.

The complexity of the MIMO DSP strongly depends on the mode count and spatial modal dispersion (SMD). Because the mode number determines the numbers of rows and columns in the MIMO matrix, the DSP complexity is proportional to the

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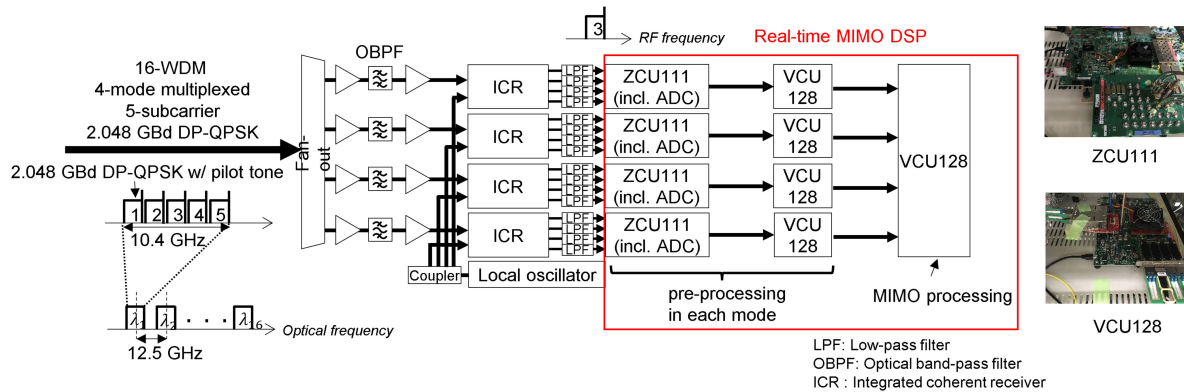


Fig. 1. Configuration of a real-time MIMO coherent receiver.

square of the mode count. The SMD is defined by the group velocity difference between multiplexed modes, and it affects the arrival time of the propagating modes. To compensate for the SMD, the entries of the MIMO matrix are not scalar values but finite impulse response (FIR) filters. The greater the SMD accumulates as the signal propagates, the longer the tap number of the FIR filters becomes. Therefore, the DSP complexity is proportional to the accumulated SMD. The coupled core structure of CC-MCFs is the best way to reduce SMD because it introduces strong random mode coupling that can suppress the accumulation of SMD [11]. It is also advantageous due to its high spatial density and low propagation loss [12]–[13]. Long-haul transmission over 12100-km CC-MCFs with seven cores was demonstrated [12], although MIMO processing was performed offline. For practical deployment of CC-MCF transmission systems, MIMO processing should be performed in real time.

To evaluate resource requirements and the real-time transmission performance, real-time DSP implementation based on field-programmable gate array (FPGA) circuits is commonly employed prior to implementing application-specific integrated circuits (ASICs). Real-time MDM transmission experiments over CC-MCFs have been recently reported with real-time FPGA-implemented MIMO DSP for mode equalization [14]–[15]. Although the transmission distances of the demonstrations have been limited to single span transmission with a length of approximately 60 km, it is expected that CC-MCF has the potential for application in long-haul submarine cable systems.

In this work, we demonstrate real-time long-haul MDM transmission with the CC-MCF and real-time MIMO DSP. We implement a real-time MIMO DSP to equalize four modes with dual polarization using FPGA boards. With the real-time MIMO DSP in optical coherent receivers, we conduct $16 \times$ wavelength-division multiplexed (WDM) $4 \times$ MDM dual-polarization (DP) quadrature phase shift keying (QPSK) transmission over a 7200-km coupled four-core fiber. This paper extends our previous work [16] by providing the following additional contributions.

- The tolerance of adaptive MIMO to frequency offset and laser phase noise in different QAM formats was evaluated in experiments.
- The number of FIR taps considering the SMD of the coupled four-core fiber and the resource requirement of the FPGA implementation of MIMO processing are described.

II. REAL-TIME MIMO COHERENT RECEIVER FOR FOUR SPATIAL MODES

A. Configuration of the Real-Time MIMO Coherent Receiver

We designed and fabricated a real-time MIMO DSP to equalize four spatial modes with two polarizations. Fig. 1 shows the configuration of parallel coherent receivers with real-time MIMO DSP, receiving $4 \times$ MDM optical signals with a signal bandwidth of 10.4 GHz. The signals were modulated with a five-subcarrier multiplexed DP-QPSK format. The length of a data frame is 32768 symbols. The baudrate of one subcarrier was 2.048 GBd. By demultiplexing one subcarrier, we can reduce the required sampling rate of the following analog-to-digital converters (ADCs). Each subcarrier is accompanied by a frequency pilot tone, which is used to estimate the frequency offset in intradyne coherent detection. The power ratio of the pilot tone to the signal power was -10 dB. The received signals after coupled four-core fiber transmission were spatially demultiplexed and coupled into four single mode fibers by a fan-out (FO) device based on free space optics. After amplification with optical bandpass filtering, the four mode-demultiplexed signals were simultaneously received by four integrated coherent receivers (ICRs), where a tunable external cavity laser with a linewidth of 5 kHz was used as a local oscillator (LO). By tuning the LO frequency, only the desired subcarrier was converted to the baseband. The received electrical signals passed through low-pass filters (LPFs) with cutoff frequencies of 1.2 GHz to suppress the sampling aliases, and they were then sent to the real-time MIMO DSP for mode equalization.

The DSP was implemented with four Xilinx Zynq UltraScale+ RFSoc ZCU111 evaluation boards and five Xilinx Virtex UltraScale+ FPGA boards (VCU128). The 16 streams of detected electrical signals with 2.048 GBd were digitized using 12-bit ADCs embedded on the ZCU111 boards. The sampling rate was 4.096 GSa/s, which corresponds to two samples/symbol. The four ZCU111 boards were used for analog-to-digital conversion and front-end imperfection compensation, and four of the VCU128 boards were used for filtering and frequency offset compensation. The MIMO equalization was implemented in the last VCU128 board. The appearance of the FPGA boards is also shown in Fig. 1. The flow of real-time digital signal processing is described in the next section.

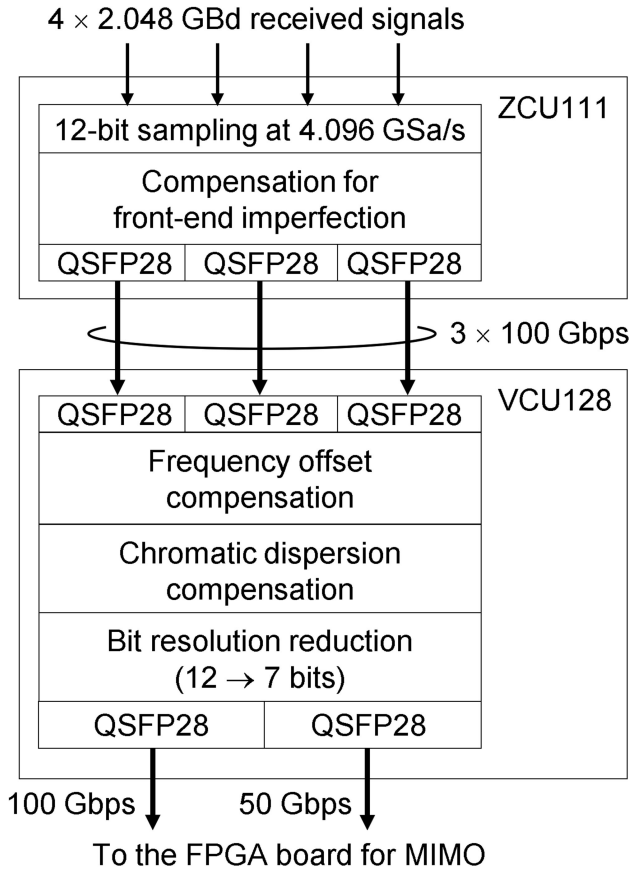


Fig. 2. DSP procedure before MIMO implemented in the former FPGA boards.

B. Real-Time DSP Before MIMO

The detected mode-demultiplexed signal containing four electrical streams independently underwent DSP before MIMO, which was implemented in the ZCU111 and VCU128 boards, as shown in Fig. 2. The four sets of the two FPGA boards were used for the four demultiplexed modes. After sampling at 4.096 GSa/s, front-end imperfection in the ICRs was compensated for by an FIR filter with 25 taps in the first FPGA board (ZCU111). The processed data were sent to the next FPGA board (VCU128) by three 100-Gbps QSFP28 active optical cables. In the VCU128 boards, high accuracy frequency offset compensation based on pilot tone detection was performed [17]. After the bit resolution was reduced from 12 to 7 bits, the data were transferred to the last FPGA board through two QSFP28 optical transceivers at 100 Gbps and 50 Gbps. For all four demultiplexed modes, the total transfer speed between the second FPGA board and the last FPGA board was 600 Gbps, which is sufficiently large for the required data speed of 458 Gbps ($= 4.096 \text{ GSa/s} \times 7 \text{ bits} \times \text{I and Q} \times \text{dual pol.} \times 4 \text{ modes}$).

In our frequency offset compensation, the frequency offset value was estimated by detecting the pilot tone transmitted with the signals in the frequency domain. The frequency detection error is determined by the frequency resolution of the fast Fourier transform (FFT). Because the FFT size is approximately 1000 in practical real-time DSP, the resolution is limited to approximately 1/1000 of the sampling rate. The detection error due to such poor resolution becomes critical for stable operation of the following MIMO equalization. Fig. 3(a) shows the

principle of our proposed high accuracy frequency offset compensation based on dual-stage frequency offset estimation. In the first stage, the pilot tone component is roughly extracted and frequency-shifted to the baseband based on the FFT with block size M_1 . The frequency of the downshifted pilot tone remains due to the poor resolution determined by M_1 . In the second stage, the roughly downshifted pilot tone is downsampled by a factor of K , and the remainder of the frequency of the pilot tone is detected based on an FFT. Even if we use the FFT with size M_2 , the frequency resolution improves by a factor of K thanks to prior downsampling. In our dual-stage method, it is easy to achieve a frequency resolution less than 1/10000 of the sampling rate.

Fig. 3(b) shows our DSP of the high accuracy frequency offset compensation, which was implemented based on an overlapped FFT (OL-FFT) with a block size of 1024, an FFT with a block size of 256 [18], and downsampling by 1/256, namely, $M_1 = 1024$, $M_2 = 256$, and $K = 256$. In the first stage, the input data underwent the OL-FFT with a block size of 1024. The peak frequency of the intensity spectrum, f_1 , was detected as the pilot frequency, and the complex-value spectral data were then shifted by $-f_1$. The signal spectrum and the pilot tone component were separated by rectangular-shaped filtering, and the extracted pilot tone was spectrally shifted to the baseband around the DC. The signal spectrum also underwent chromatic dispersion compensation. By inverse FFT and removing overlapping samples, the signal and downshifted pilot tone were recovered in the time domain. Although the frequency offset was roughly compensated after the first stage, the frequencies of the signal and pilot tone were still uncertain due to the limited FFT resolution of 4 MHz ($= 4.096 \text{ GHz}/1024$). In the second stage, the samples of the downshifted pilot tone were downsampled by 1/256, and an FFT with a block size of 256 was performed. Because the frequency resolution was approximately 63 kHz ($= 4.096 \text{ GHz}/256/256$), the residual frequency offset can be precisely estimated by detecting the peak frequency f_2 of the downshifted pilot tone. According to the detected frequency f_2 , complex field samples with $-f_2$, namely, $\exp(-j2\pi f_2 k \Delta t)$, where k and Δt are the discrete index and the sampling interval, respectively, were generated by the coordinate rotational digital computing (CORDIC) algorithm [19]. By multiplying the signal with the inverse rotation field sample, the residual frequency offset of the signals was compensated for.

C. Real-Time MIMO Equalization

In the last FPGA board (VCU128), we implemented half-symbol-spaced [20] real-value 16×4 MIMO equalization [15], where a single DP-QPSK signal of one mode was equalized from 16 input streams (I and Q \times dual pol. \times four modes). The entries of MIMO consisted of FIR filters with 25 tap coefficients, which were updated by the improved least mean square (LMS) algorithm [21]. In the training mode, the tap coefficients were updated using a training sequence and then switched to decision-directed mode after the update error sufficiently converged. Compared with our previous work [15], the real-time MIMO component was improved. The dual polarization output could be handled by increasing the MIMO matrix size from 16×2 to 16×4 . The MIMO was operated at 2 samples/symbol [20], reducing the performance degradation observed in the previous

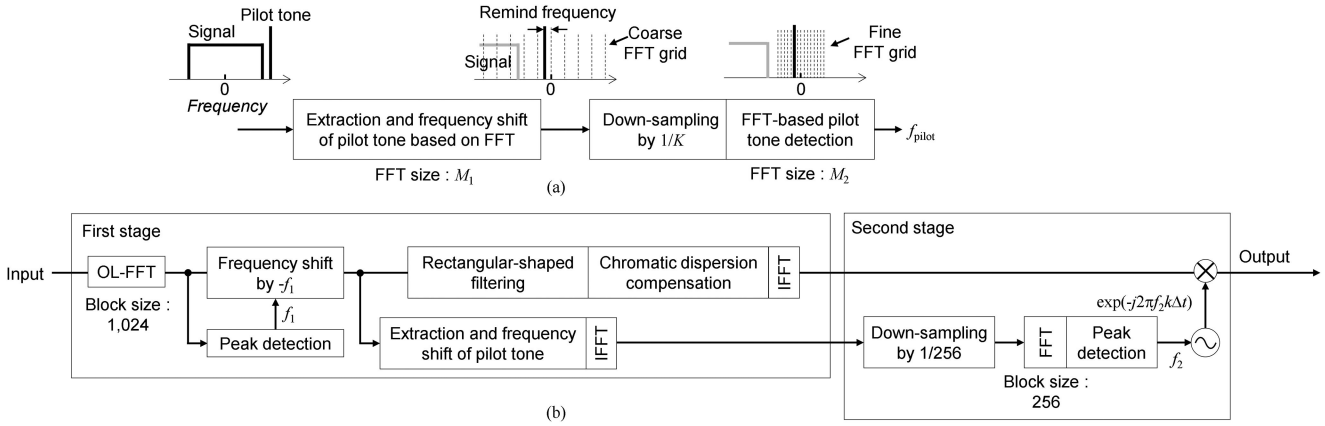


Fig. 3. (a) Principle. (b) DSP procedure of high accuracy frequency offset compensation.

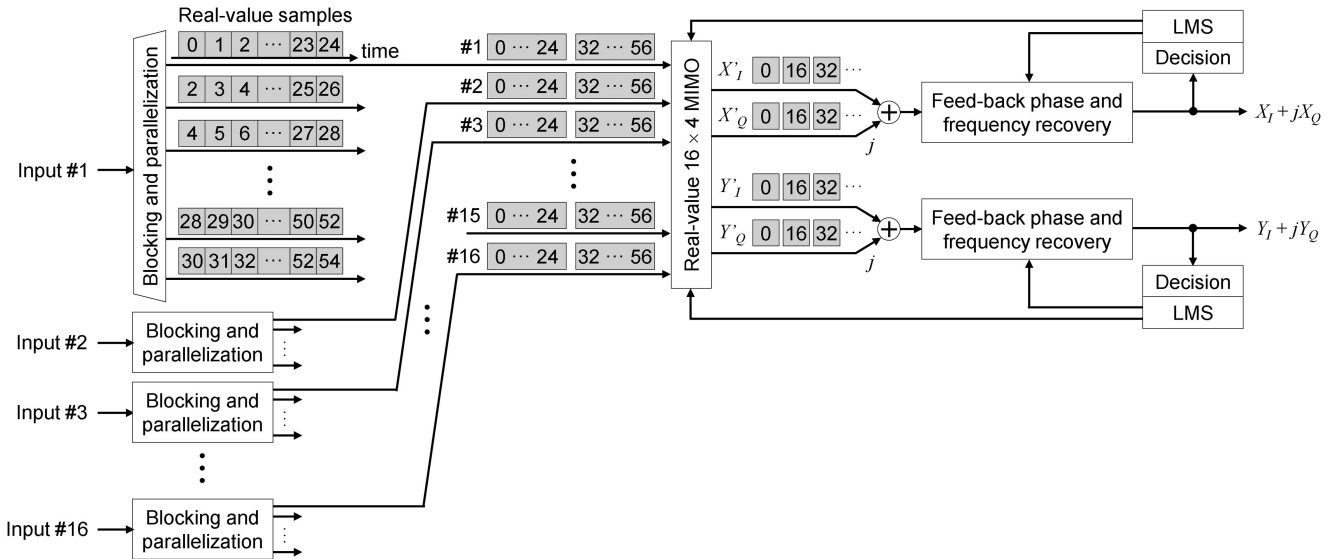


Fig. 4. Configuration of real-value 16x4 MIMO equalization.

1-symbol/sample MIMO. In our implementation, one tributary was demodulated. In principle, all parallel tributaries can be demodulated using additional FPGA boards to equalize different parallel tributaries.

Fig. 4 shows the configuration of our implemented MIMO. The input samples transferred from the previous FPGA boards were blocked into multiple registers with 25 samples the same as the MIMO tap size, and the registers were parallelized into 16 tributaries because the clock rate of the FPGA board was 128 MHz. The parallelized tributaries of the 16 input channels underwent real-value 16×4 MIMO, and the four real-value samples corresponding to I and Q on dual polarization were equalized. These samples were converted into complex-value samples, and carrier phase and frequency recovery based on a single complex-value tap that was independently performed for the two polarization tributaries. The tap coefficients of the FIR filters and carrier phase and frequency recoveries were simultaneously updated based on the improved LMS algorithm [21]. In real-time DSP, calculation delay is inevitable within the feedback loop, and the speed of the tracking is reduced. In our

implementation, the delays were 45, 5, and 5 clocks for FIR filters and phase and frequency updates, respectively. The speed of phase and frequency tracking will be discussed in Section III.

After the MIMO equalization, bit error rates (BERs) or Q^2 values of equalized symbols were measured. In a recirculating loop experiment, a trigger signal is fed to the FPGAs, which has a synchronized timing with the rising edge of a gating signal that controls optical SWs in the recirculating loop system. This trigger signal informs the FPGAs of the start of the timing (i.e., 1st loop) of the recirculating loop transmission. After the trigger signal was detected, the FPGAs waiting for the propagation delay corresponded to a desired transmission distance. Then, the FPGAs initialize the MIMO equalizer coefficients and initiate the real-time signal processing. During signal processing, the results (e.g., the number of error bits) are continuously written in an internal memory embedded on the VCU128 FPGA board for MIMO equalization. The maximum amount of time DSP can be executed continuously is limited to the time required to propagate over one loop. The time corresponds to the length of 75 data frames. Here, the length of the sequence that is

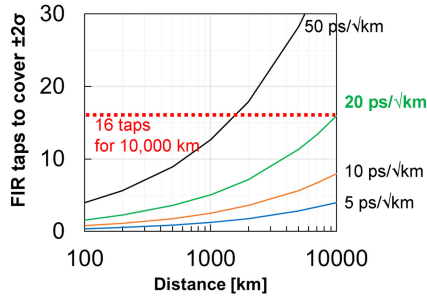


Fig. 5. The FIR tap number to cover a $\pm 2\sigma$ interval as a function of SMD coefficient, assuming a 2 Gbd signal with half-symbol-spaced equalizer.

used to train the LMS-based MIMO equalizer is 20 frames ($= 20 \times 32768$ symbols). Therefore, the maximum length of the blind sequence, which is used for BER counting, is 55 frames (55×32768 symbols). The length of 55 frames corresponds to 0.88 ms. Additionally, considering that only one of the 16 parallel time tributaries is being demodulated, the maximum number of symbols that can be used for BER counting is $(1/16) \times (55 \times 32768) = 112640$ symbols. The length of BER counting is sufficiently large to measure Q^2 lower than 10 dB. After finishing the transmission experiment, the MIMO equalizer coefficients used at the end of the blind sequence and the accumulated BER over the blind sequence are read by a PC.

D. DSP Resource Requirements for MIMO

As the SMD coefficients of CC-MCF increase, the required number of MIMO FIR taps increases. Fig. 5 shows the numerical dependence of the tap number on the SMD coefficient of CC-MCF, assuming a signal baudrate of 2 Gbd with a half-symbol-spaced equalizer. To roughly estimate how many taps should be implemented, with the tap number being determined by the two standard deviations of the impulse response ($\pm 2\sigma_I$). The tap number is calculated as follows [11]. An accumulated SMD, which is defined as the standard deviation σ_R of the differential group delay (DGD) distribution after L -km transmission, was calculated by the product of the SMD coefficient [$s/km^{1/2}$] and $L^{1/2}$ [$km^{1/2}$]. σ_R is twice the standard deviation σ_I of the impulse response, namely, $\sigma_R = \pm 2\sigma_I$. Thus, the tap number covering $\pm 2\sigma_I$ was obtained by $2\sigma_R / (T/2)$, where T is the symbol period. We found that 16 taps were required for a 10000-km transmission for an SMD coefficient less than $20 \text{ ps}/km^{1/2}$, as shown in Fig. 5. CC-MCFs with such low SMD coefficients can be fabricated. For example, it has been reported that the measured SMD coefficient σ_R of our fabricated coupled four-core fiber including FI and FO devices was $18 \text{ ps}/km^{1/2}$ [22]. Using the low-SMD CC-MCF, the MIMO FIR tap number is reduced to 16 even for long-haul transmission.

As mentioned in the previous subsection, we implemented FIR filters with 25 taps applicable for long-haul transmission over low-SMD CC-MCFs. Table I shows the number of utilized DSP slices for FIR filters, carrier phase and frequency recoveries, LMS update calculations, and other circuits of our implemented MIMO equalization in the FPGA board (VCU128). The DSP usage was 47% of the total number of DSP slices, and

TABLE I
REQUIRED DSP RESOURCES OF OUR IMPLEMENTED MIMO IN THE FPGA BOARD (VCU128)

Function	Number of DSP slices
FIR filters	1,600
Carrier phase recovery	520
Carrier frequency recovery	16
LMS update	1,600
Others (e.g. scaling)	512
Total of used DSP slices	4,248 (47.1%)

we found that FIR filtering and the update calculations predominantly consumed DSP slices. Although more DSP slices can be consumed to increase the number of FIR taps and decoding parallels, it would make the circuit design more difficult.

III. CHARACTERIZATION OF THE REAL-TIME MIMO COHERENT RECEIVER

A. Performance Evaluation for Frequency Offset and Phase Noise

We evaluated the tolerance of the real-time MIMO DSP to the frequency offset and phase noise. In this experiment, we emulated received signals impaired with a frequency offset and phase noise due to intradyne detection, and the samples were stored in the FPGA board (ZCU111) instead of sampling analog electrical signals. The experimental setup is shown in Fig. 6. The QAM signal with a length of 32768 symbols was generated. The signal was upsampled to two samples/symbol, and the pilot tone used for frequency offset compensation was inserted. The samples suffered from AWGN, whose signal-to-noise ratios, including the pilot tone power, were 11, 18, and 25 dB for QPSK, 16QAM and 64QAM, respectively. After the FFT, the samples were circularly shifted with a specific frequency offset. In our experiment, the frequency offset was varied from 62.5 kHz to 4 MHz. After the IFFT, the data samples were then impaired with phase noise from a laser. The former half of the phase noise sequence was generated based the Wiener process [23], and the latter half was folded to remain continuous in the periodic waveforms of the samples, as shown in Fig. 6, although it would slightly deviate from a true Wiener process. For dual polarization input, the samples delayed by 87 ns for decorrelation were used for another polarization tributary. The two sets of samples were stored on the FPGA board (ZCU111) as the input samples. Instead of sampling received electrical signals, they were repeatedly generated and launched into our implemented DSP on the boards. Finally, the bit error ratios (BERs) in each polarization after MIMO equalization over more than 20 data frames were counted and averaged over the polarizations.

We measured the dependence of the BERs on the frequency offset without phase noise when the DSP for frequency offset compensation was turned off. The black, blue, and orange dots in Fig. 7(a) indicate the measured BERs in the QPSK, 16QAM and 64QAM cases, respectively. The frequency offset was normalized by an FPGA clock frequency of 128 MHz. We found that

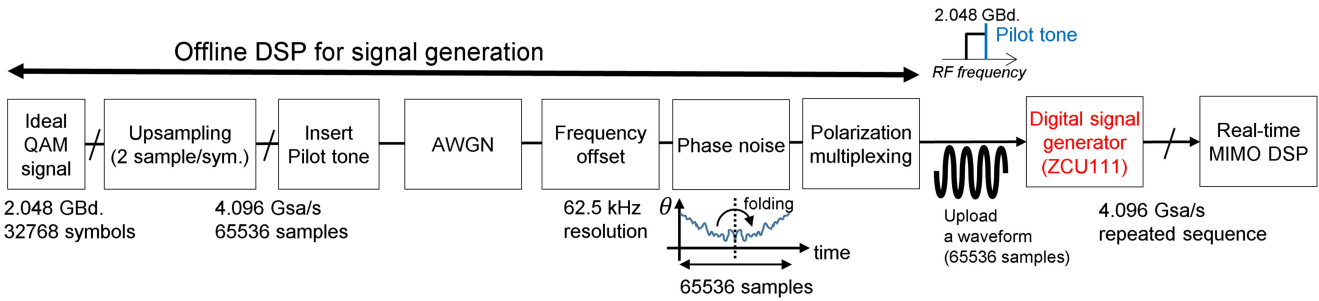


Fig. 6. Experimental setup of frequency offset and phase noise tolerance evaluation.

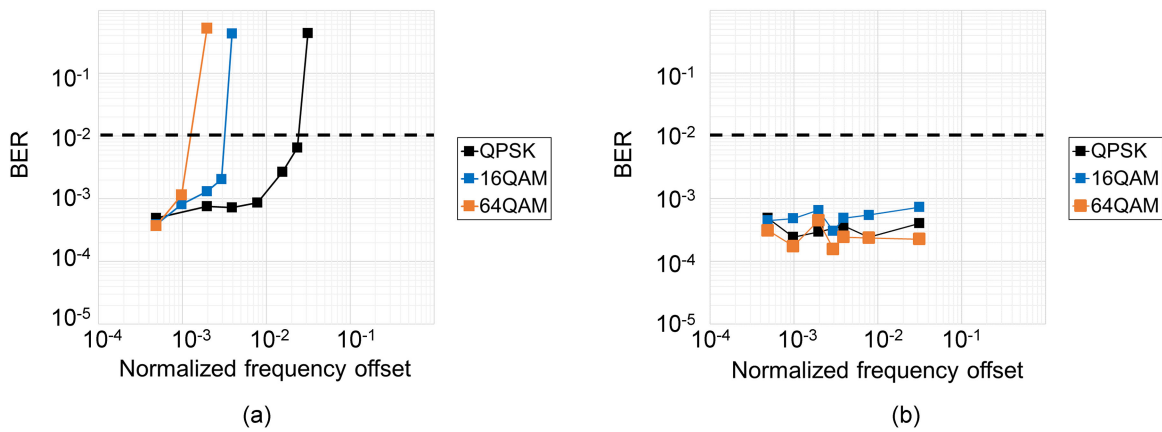


Fig. 7. Frequency offset tolerance of the real-time MIMO DSP (a) without or (b) with two-stage FOE.

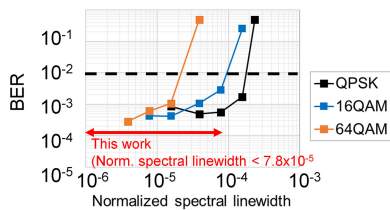


Fig. 8. Phase noise tolerance of the real-time MIMO DSP.

BERs below 1×10^{-2} were maintained for frequency offsets less than 2.3×10^{-2} (3 MHz), 2.9×10^{-3} (375 kHz), and 9.8×10^{-4} (125 kHz) for QPSK, 16QAM, and 64QAM, respectively. When our two-stage frequency offset compensation turned on, we measured the BERs on the frequency offset. The results are illustrated in Fig. 7(b). The marker definition is the same as those in Fig. 7(a). We found that the BER penalty due to the frequency offset was negligible even in the 64-QAM case. This is because the error of the frequency offset compensation could be suppressed below 63 kHz, which was the frequency resolution in the second stage of the frequency offset compensation. These results suggest that our high-resolution frequency offset compensation is effective in suppressing the degradation of BER performance in the following MIMO.

We also measured the BERs when the QAM signals were impaired with phase noise without the frequency offset. Fig. 8

shows the measured dependence of the BER on the spectral linewidth of the phase noise. The spectral linewidth was normalized to an FPGA clock frequency of 128 MHz. A BER of less than 1×10^{-2} was achieved when the linewidth was approximately 1.7×10^{-4} (22 kHz), 9.4×10^{-5} (12 kHz), and 2.3×10^{-5} (3 kHz) for QPSK, 16QAM and 64QAM, respectively. In our later explained long-haul transmission experiment, we used external cavity lasers with linewidths of less than 5 kHz for signal generation and LO. The linewidth of the phase noise was expected to be approximately 7.8×10^{-5} (10 kHz). The BER penalty due to the phase noise was suppressed for the QPSK signals, and it would not be avoidable for the 16QAM and 64QAM cases, as shown in Fig. 8. The poor phase noise tolerance predominantly originated from the calculation delay of the feedback configuration of the carrier phase and frequency estimation [23], [24]. A challenging issue is to further improve the phase noise tolerance of our implemented MIMO DSP for high-order QAM formats. Feedforward carrier phase recovery [23], [25] with MIMO is a promising candidate that has been widely applied to real-time DSP for polarization division multiplexed transmission systems.

B. Real-Time Performance Evaluation of an Optical Receiver With Real-Time MIMO DSP in a Single-Mode Case

Using optical coherent receivers with our implemented MIMO DSP, we measured the BER performance of single-mode

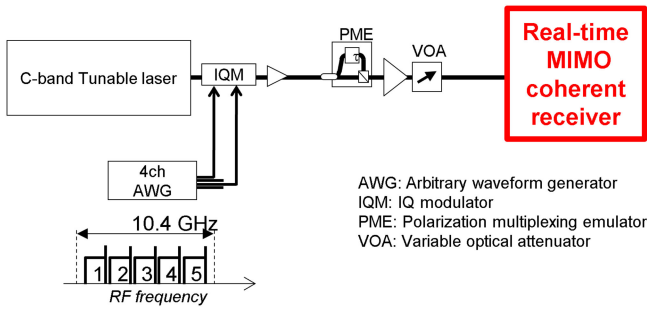


Fig. 9. Experimental setup in back-to-back configuration.

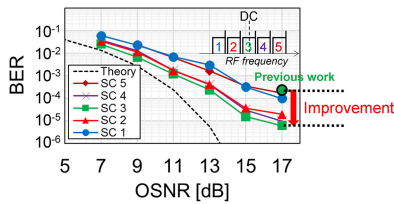


Fig. 10. Measured BER versus OSNR of each subcarrier back-to-back.

subcarrier-modulated DP-QPSK signals without any mode multiplexing in the back-to-back configuration. Fig. 9 shows the experimental setup. A CW light generated from a tunable external cavity laser was modulated using an optical IQ modulator (IQM), which was driven with electrical QPSK signals with five subcarriers at 2.048 Gbd generated from a four-channel arbitrary waveform generator (AWG). The signal was polarization multiplexed by a polarization multiplexing emulator (PME) with a delay of 87 ns. After the optical signal-to-noise ratio (OSNR) adjustment by a variable optical attenuator (VOA), the optical DP-QPSK signals were received using the optical receivers with our implemented MIMO DSP, as shown in Fig. 1.

Fig. 10 shows the BER of each subcarrier versus OSNR. The BER was averaged over the polarizations. The theoretical OSNR-BER curve was also plotted. We determined the subcarrier dependence caused by the bandwidth limitation of the AWG. We observed that the BER was independent of the sampling phase of the ADCs because the MIMO was operated at two samples/symbol and accurate digital sampling phase recovery was achieved [20]. The BER of the center subcarrier was also improved from 2.2×10^{-4} in our previous 1-symbol/sample-based MIMO [15] to 6.1×10^{-6} at an OSNR of 17 dB. We confirmed the performance improvement of the real-time MIMO DSP in this work.

IV. REAL-TIME 7200-KM COUPLED FOUR CORE FIBER TRANSMISSION

A. Experimental Setup

With real-time MIMO DSP, we demonstrated a 7200-km coupled four-core fiber transmission with a recirculating loop. Fig. 11 shows the experimental setup. In the transmitter, a 12.5 GHz-spaced 16-channel WDM five-subcarrier-multiplexed 2.048-Gbaud Nyquist-shaped QPSK signal at approximately

1550 nm was generated by an even/odd decorrelation method utilizing a four-channel AWG and two IQMs, followed by a PME with a delay of 87 ns. The WDM signal was split into four paths with a relative delay of 200 ns between subsequent paths for decorrelation and fed into a recirculating loop system. Here, the delays of 87 and 200 ns for the decorrelation were sufficiently larger than the time window of the MIMO equalizer (6.1 ns). The transmission line consisted of four spans of 60.2-km coupled-core four-core fiber [26] with a FIFO device, conventional C-band EDFAs, variable optical delay lines (VODLs), and two 2-channel C-band wavelength-selective switches (WSSs) for gain equalization. The four cores arranged in a square lattice of the coupled MCF had almost the same refractive index profile as an ultralow-loss pure-silica-core single-mode fiber used for long-haul transmission. The core-averaged transmission loss, effective area, core pitch and SMD for the coupled MCF at 1550 nm were approximately 0.155 dB/km, $113 \mu\text{m}^2$, $20.2 \mu\text{m}$, and $7.1 \text{ ps}/\sqrt{\text{km}}$, respectively. The averaged total span losses were 11.8 dB, including FIFO devices and VODLs. The detailed characteristics of the CC-MCF recirculating loop system have been reported in our previous work [27]. The transmitted WDM signal was received by the real-time MIMO coherent receiver and demodulated in real time.

B. Results

We measured the Q^2 averaged among four cores and dual polarizations at the center subcarrier as a function of the power per channel at a 3120-km transmission distance to determine the optimum fiber launch power, as shown in Fig. 12(a). Here, the launch power means the total launch power of subcarriers and polarizations per wavelength and core. The highest Q^2 values were obtained at $-5 \text{ dBm}/\text{ch}$. Fig. 12(b) shows Q^2 as a function of the transmission distance with the optimum fiber launch power. After a 7200-km transmission, the Q^2 at the center subcarrier exceeds an assumed forward error correction (FEC) threshold of 4.95 dB [28]. Finally, we measured Q^2 for all cores and subcarriers of WDM channels at 7200-km transmissions, as shown in Fig. 13(a). To save time on the experiment, only five of the sixteen WDM channels around the center channel were evaluated. The Q^2 deviation between spatial tributaries was observed, which would come from mode-dependent loss [27]. The temporal Q^2 fluctuation caused by state of mode change would occur over time-scales of minutes as long as CC-MCFs were in stable environments [29]. Because the maximum time for continuous BER counting is limited to 0.88 ms, as we mentioned in Section II-C, it is hard to evaluate the slow Q^2 fluctuation. The evaluation of fast Q^2 fluctuation caused by state of mode change under unstable environments is a future task. A higher Q^2 than FEC threshold for all cores and subcarriers was achieved. Fig. 13(b) shows the measured 16×4 impulse responses at the center channel after the 7200-km transmission. All elements in the 16×4 MIMO matrix with 25 taps were plotted. The tap length was 25 in the implemented MIMO, which was sufficient for compensation of accumulated SMD even after the 7200-km transmission. Thus, real-time transoceanic distance MDM transmission using real-time MIMO-DSP was achieved.

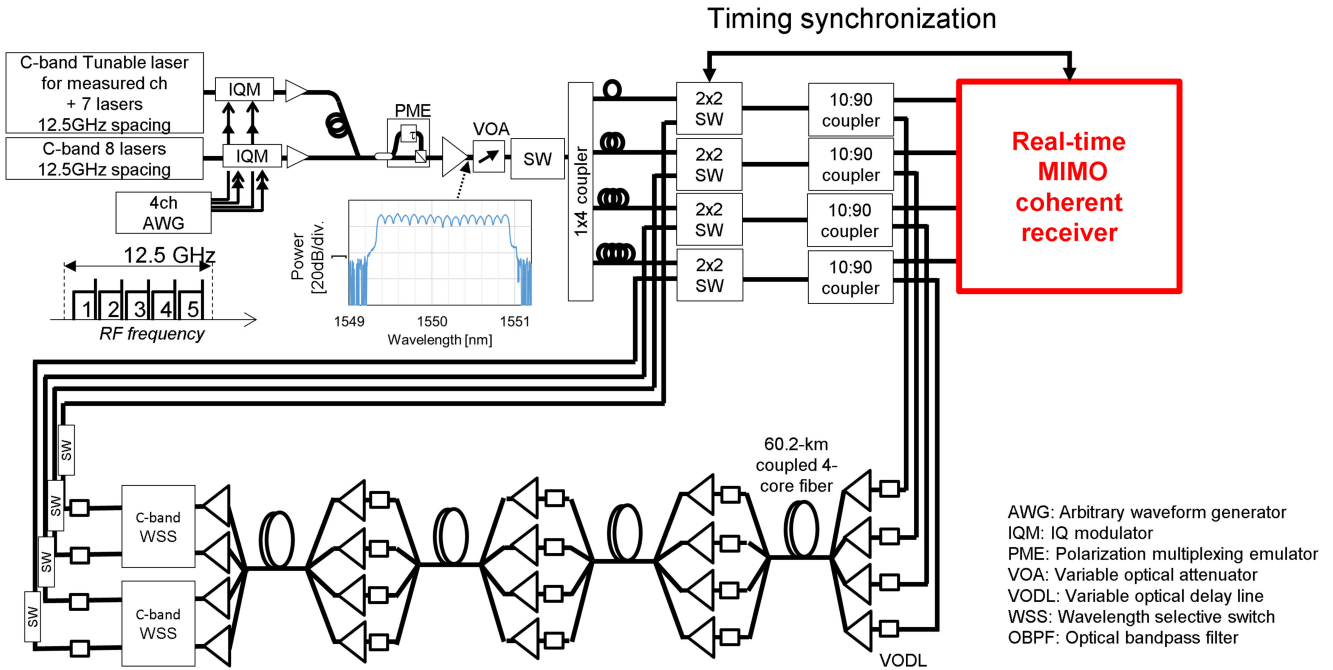


Fig. 11. Experimental setup for a long-haul coupled four-core fiber transmission.

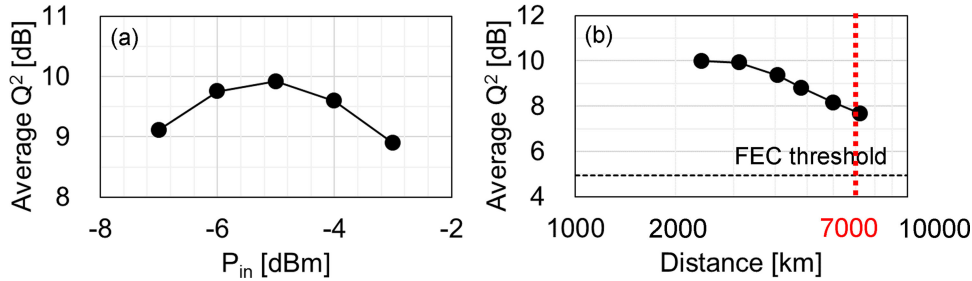


Fig. 12. (a) Measured average Q^2 as a function of the fiber launch power at a 3120-km transmission distance. (b) Measured average Q^2 as a function of the transmission distance.

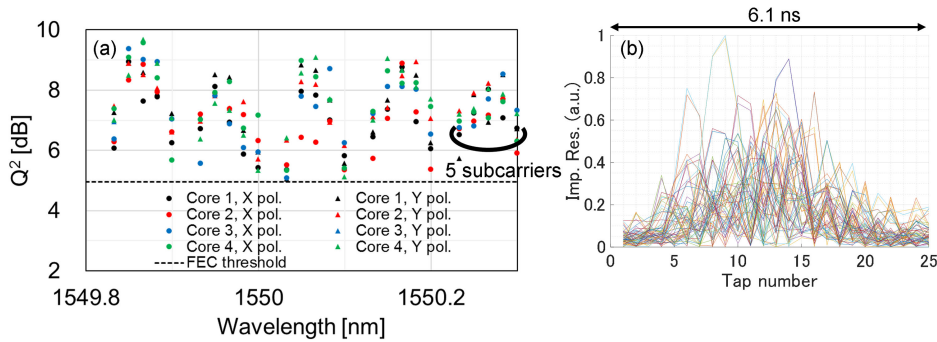


Fig. 13. (a) Measured Q^2 of all cores and subcarriers after 7200-km coupled four-core fiber at the five WDM channels around the center channel. (b) 16×4 MIMO impulse responses at the center channel after the 7200-km transmission.

V. CONCLUSION

We implemented a real-time MIMO DSP to equalize four spatial modes with dual polarizations in the presence of accumulated spatial mode dispersion. The tolerances to frequency offset and phase noise of the real-time MIMO DSP were evaluated, and

the applicability to QAM signals was discussed. With the MIMO DSP, we demonstrated real-time transoceanic distance MDM transmission. The WDM DP-QPSK signals were transmitted and demodulated in real time over 7200-km coupled 4-core fibers. The feasibility of real-time ultralong-haul coupled-core multicore fiber transmission was confirmed.

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