

Long Lifetime DC-Link Voltage Stabilization Module for Smart Grid Application

Huai Wang^{*}, Henry Chung[†], Wenchao Liu[†], Frede Blaabjerg^{*}

^{*} Center of Reliable Power Electronics (CORPE), Department of Energy Technology, Aalborg University, Denmark.

[†] Centre for Smart Energy Conversion and Utilization Research (CSCR), City University of Hong Kong, Hong Kong.

hwa@et.aau.dk; eesch@cityu.edu.hk; wenchao.liu@cityu.edu.hk; fbl@et.aau.dk

ABSTRACT

Power converters enable efficient and flexible control and conversion of electric energy among different smart grid players (i.e. producers, energy storage systems, and loads). One of the expected features of smart grid is that it will be more reliable compared to conventional grid. However, power converters are one kind of the lifetime limiting components applied in smart grid. One of the major causes is the malfunction of electrolytic capacitors (E-Caps) which are widely used for stabilizing the dc-link voltage in various types of power converters applied in smart grid. A dc-link module is therefore proposed in this paper with a reduced value of dc-link capacitor and a series voltage compensator. It allows the replacement of the popularly used E-Caps with alternatives of longer lifetime, like power film capacitors. The basic concept, implementation and operation principle of the dc-link module are given. The theoretical analysis is verified by simulation and experimental results.

1. INTRODUCTION

The smart grid is characterized by a two-way flow of energy and information, which creates an automated, widely distributed energy generation and delivery network [1]. Fig. 1 gives a possible scenario of the future power system based on smart grid technologies [2]. Power electronic building blocks (PEBBs) and mechanical building blocks (MEBBs) are the intelligent energy conversion nodes interconnecting the producers, energy storage systems and loads. PEBBs composed of power converters enable efficient and flexible control and conversion of electric energy. However, the reliability issue of PEBBs as discussed in [3] is a challenge in smart grid applications.

PEBBs have various architectures, of which the ones shown in Fig. 2 are dominant for power generation, transmission, and consumption in the smart grid. They are widely applied in lighting application, telecom power supplies, photovoltaic (PV) systems, wind turbine systems and so on. Multiple power converters are interconnected by a dc link. The dc-link voltage is supported by a capacitor bank for

absorbing instantaneous power difference between the input source and output load, minimizing voltage variation on the dc link, and providing sufficient energy during the hold-up time of the system.

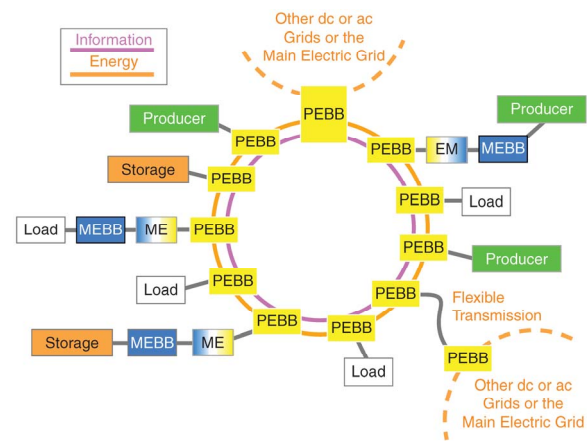


Fig. 1. A possible scenario of the future power system based on smart grid technologies (PEBB- power electronic building block, MEBB- mechanical building block, ME- mechanical electrical interface) [2].

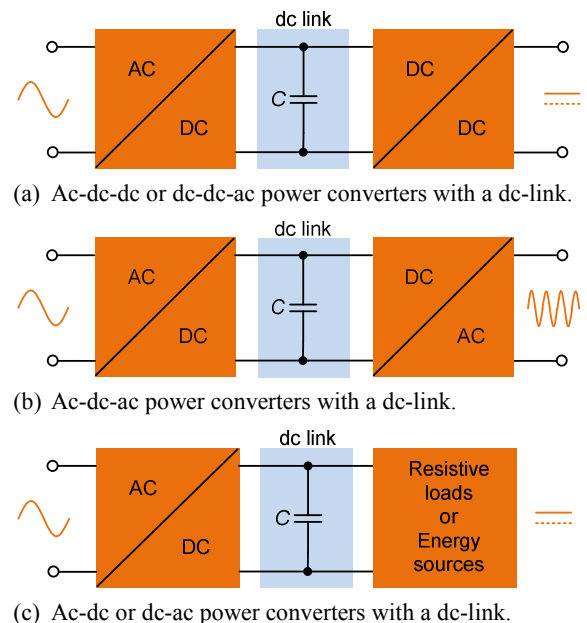


Fig. 2. Typical power electronic building blocks used in the smart grid (power flow from left-to-right, right-to-left, or bi-directional).

Table I. Comparisons between aluminum electrolytic capacitors and power film capacitors.

	Aluminum electrolytic capacitors	Power film capacitors
volumetric efficiency	high	relatively low
voltage ratings	from low voltage to 700 V	from low voltage to 100 kV
capacitance tolerance	typical $\pm 20\%$	typical $\pm 5\%$, $\pm 10\%$
ripple current	typical 20 mA/ μF	typical 1 A/ μF
ESR**	high	Low
lifetime	typical 2,000 to 10,000 hours *	typical 100, 000 hours*
cost	low	relatively high

*Under rated conditions. ** Equivalent series resistance.

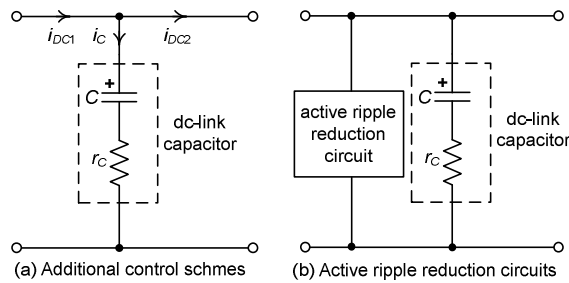


Fig. 3. Prior-art concepts for reducing dc-link capacitors.

Among different types of capacitor, aluminum electrolytic capacitors (E-Caps) are the most popular choice for the dc-link application because of their high volumetric efficiency and low cost, however, suffering from short lifetime. Power film capacitors outperform E-Caps in terms of power loss, self-healing capability, life expectancy, dc-blocking capability, ripple current capability, reliability, and environmental performance. The challenge is that the volume and cost of power film capacitors are 5-10 times of those of E-Caps with same voltage rating and capacitance. Table I gives the comparisons between these two types of capacitors.

To lessen the dependency of the dc-link capacitance, there are several prior-art methods for reducing the required energy storage as shown in Fig. 3. One is by adopting control methods to render the current i_{DC1} to i_{DC2} as shown in Fig. 3(a) [4]-[9]. The performance of the controllers is highly dependent on the accuracy of the calculations and affected by time delays. Moreover, it is not suitable for power factor corrector (PFC) front-end with constant load power applications. The other concept is to add an active ripple reduction circuit in parallel with dc-link capacitors as shown in Fig. 3(b) [10]-[12]. The common challenge of all these methods is that the components used in the auxiliary circuit are under a high voltage stress, which could be as high as the dc-

link voltage. In [13], a third port circuit is introduced for power balancing. It requires that the additional port has a power rating the same as that of the main conversion system.

This paper proposes a module that can reduce the required dc-link capacitance for voltage stabilization. Its operating principle is based on connecting a series voltage compensator between the dc-link capacitor and the load. The energy storage in the dc link is reduced, making it possible to replace the high-value E-Caps with low-value high-performance (e.g., lifetime) capacitors. The voltage compensator is of low voltage and low power rating, as it only produces low voltage and handles reactive power. Its implementation only requires low-voltage switching devices and low-voltage capacitors of long lifetime. The developed module could be integrated into different type of PEBBs that are suitable for smart grid applications. The basic concept, implementation, operation principle, simulation and experimental verifications are presented in the following sections.

2. CONCEPT OF THE PROPOSED MODULE

Fig. 4 depicts the basic concept of the module for reducing the dc-link capacitance. The dc-link capacitor is connected to the output of the first power converter. The capacitor voltage v_C is composed of dc component V_C and ripple voltage Δv_C . The peak-to-peak value of Δv_C is $2|\Delta v_C|$. A voltage source v_{ab} is connected in series between the dc-link capacitor C and output v_d . It generates a voltage counteracting Δv_C with its dc component equal to zero (i.e., $v_{ab} = \Delta v_C$). Thus, v_d has the same dc value as that across C , but with a zero ripple voltage in the ideal situation. Such architecture allows a high voltage ripple on C , implying that the value of C can be made smaller, but at the expense of increasing the magnitude of v_{ab} .

From energy storage perspective, the dc-link module has energy storage in both the dc-link capacitor C and the voltage compensator. Fig. 5 shows the energy storage E and instantaneous power p of the dc-link capacitor. The dc component of energy E_1 maintains a certain level of dc-link voltage. Only the ac component of E requires the power p for balancing the input and output power of the entire system. Therefore, with the proposed dc-link module, the energy storage elements are divided into two parts: one is stored in the reduced dc-link capacitor and the other one is stored in the voltage compensator. The theoretical minimum energy storage required is E_{\min} . In the practical design, the overall energy storage of the dc-link module is reduced to a certain level between E_1 and E_{\min} , for example E_2 as illustrated in Fig. 5.

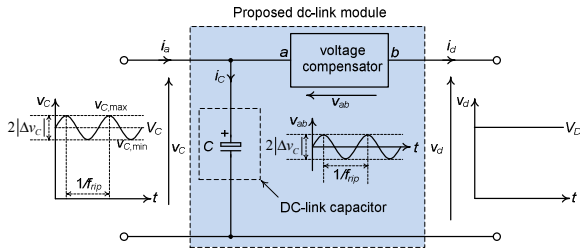


Fig. 4. Basic concept of the proposed dc-link module.

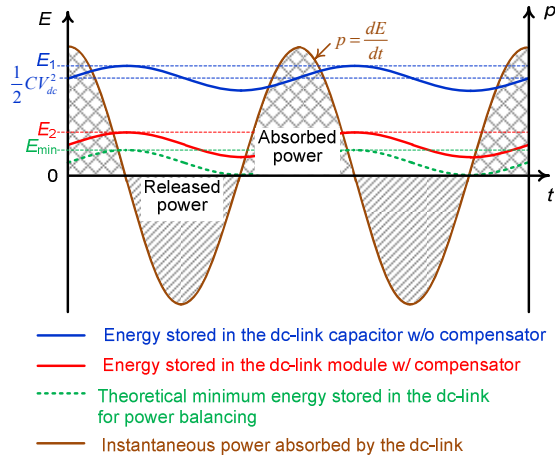


Fig. 5. Energy stored and instantaneous power handled by the dc-link capacitor bank.

3. IMPLEMENTATION OF THE MODULE

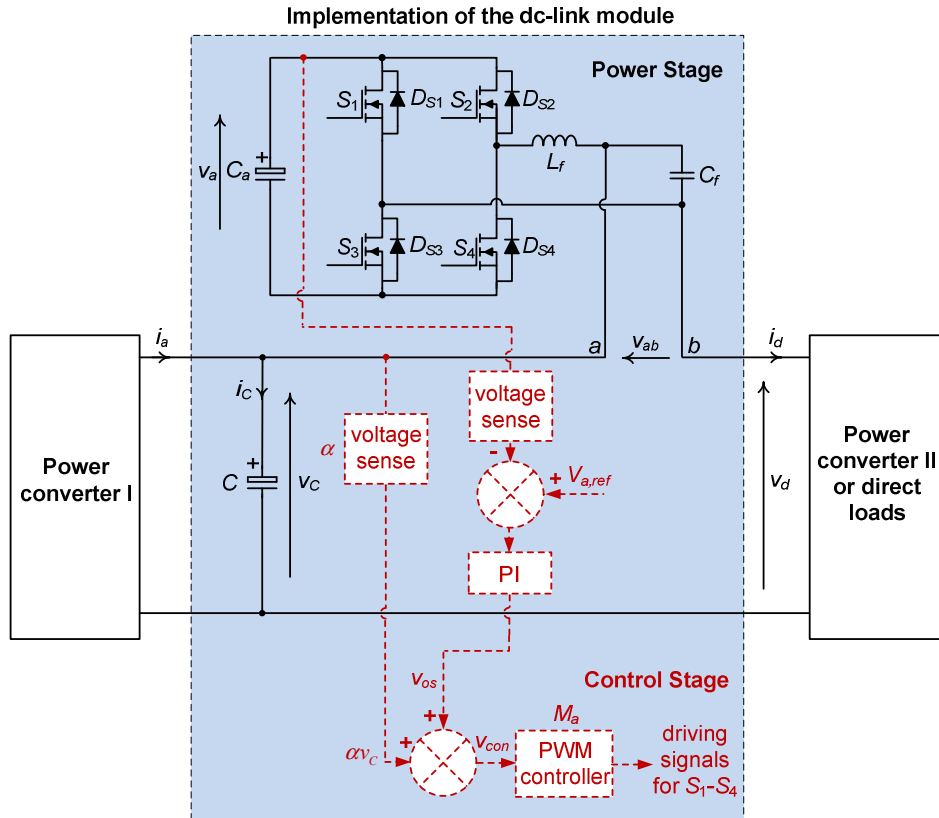


Fig. 6. One kind of implementation of the proposed dc-link module.

Fig. 6 shows one kind of the implementation of v_{ab} and its corresponding control method. v_{ab} is generated by a dc-ac converter consisting of a full-bridge (FB) and an output filter formed by the inductor L_f and capacitor C_f . Its dc side is connected to an energy storage device such as a capacitor. The gate signals for the switches S_1-S_4 in the FB are generated by a PWM modulator. It is noted that a half-bridge circuit can also be used if the current i_d is unidirectional. v_a is regulated at the reference $V_{a,ref}$ by a feedback loop. The difference between $V_{a,ref}$ and v_a is averaged by a low-pass filter and processed by a PI controller to give an offset voltage v_{os} . v_{con} is derived by combining the scaled-down dc link voltage αV_C with v_{os} .

The design of the dc-link capacitance value C in the proposed dc-link module is a compromise among the allowable voltage level of v_a , and the stress on the capacitor C_a and the MOSFETs S_1-S_4 . A smaller value of C requires higher voltage ratings of C_a and S_1-S_4 . The capacitor C_a withstands a low voltage stress. There are several choices in practical implementation. One choice is to use low voltage E-Caps with high ripple current and long lifetime. Unlike the ones with high voltage ratings, they are available and cost-effective. Another choice is to use ceramic capacitor tank or low-voltage film capacitors. The detailed selection of these two capacitors is discussed in [14].

4. OPERATION PRINCIPLE OF THE VOLTAGE COMPENSATOR

Figs. 7(a) and (b) present the operation modes of the voltage compensator. When S_2 and S_3 are on, the capacitor C_a is charged by the load current i_d and when S_1 and S_4 are on, the capacitor C_a is discharged. Fig. 7(c) shows the waveforms of the dc-link capacitor voltage v_C , modulating signal v_{con} , carrier signal v_{tri} , and the voltage across C_a , v_a . It should be noted that the feedback signal αv_C may contain multiple frequency components as it is obtained by scaling down v_C . t_0 and t_1 in Fig. 7(c) are defined as the two time instants when Δv_C is across zero within one period. During t_0-t_1 , the capacitor C_a is being charged by the load current and its voltage increases from minimum to maximum. During t_1-t_2 , the capacitor C_a is being discharged by the load current from maximum to minimum. Based on Fig. 7 and the SPWM principle discussed in [15], the output of the voltage compensator v_{ab} is in phase with the modulating signal v_{con} , thus, in phase with voltage ripple across the dc-link capacitor. The detailed derivations of the operation of the proposed dc-link module are presented in [14]. It can be derived that the voltage compensator processes only reactive power except for a special case when the ac components of i_a and i_d are of same frequency and in phase. For the special case concerned, the dc-link capacitance can be reduced by the synchronization control of the two phases as applied in [7].

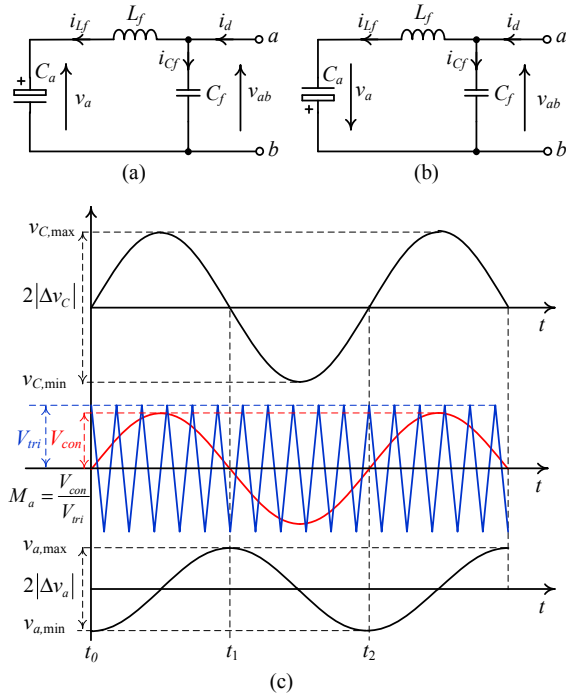
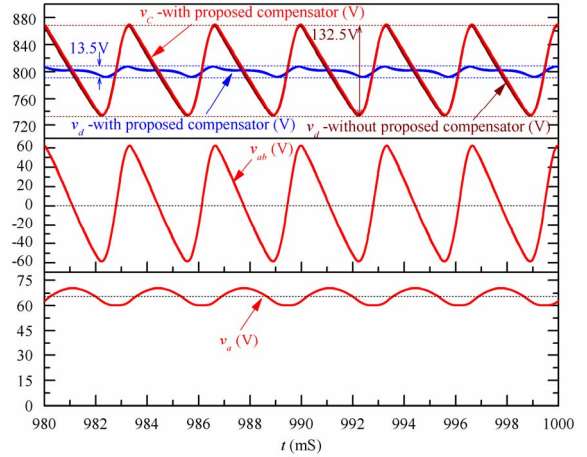
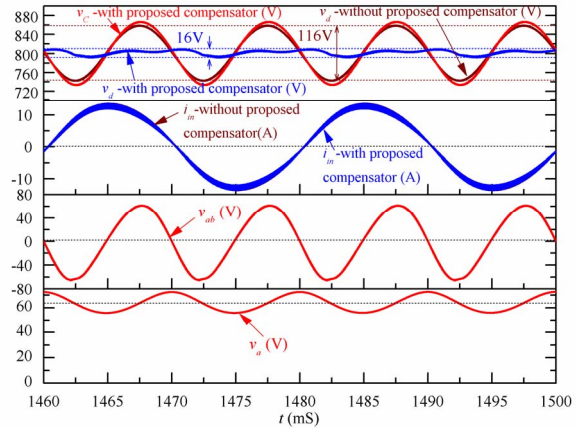


Fig. 7. Operation modes of the voltage compensator: (a) operation mode when S_2 and S_3 are on, (b) operation mode when S_1 and S_4 are on and (c) SPWM and the voltage across C_a .

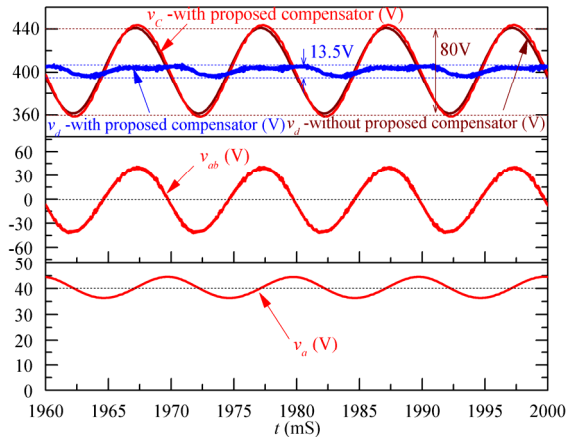
5. SIMULATIONS ON THREE PEBBS



(a) Three-phase uncontrolled diode bridge rectifier with 800 V dc-link voltage and direct resistive load ($P_o = 2$ kW, C : 900 V/40 μ F, C_a : 100 V/220 μ F).



(b) Single phase full-bridge PWM rectifier with 800 V dc-link voltage and direct resistive load ($P_o = 2$ kW, C : 900 V/50 μ F, C_a : 100 V/470 μ F).



(c) Power factor corrector with 400 V dc-link voltage and single phase full-bridge dc-dc converter switching load ($P_o = 1$ kW, C : 450 V/100 μ F, C_a : 50 V/1000 μ F).

Fig. 8. Simulation results of three different PEBBs.

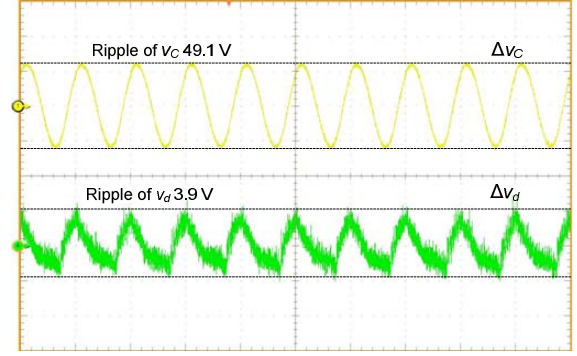
Fig. 8 shows the simulation results on three different PEBBs to verify the feasibility of the proposed dc-link module for dc-link voltage stabilization with reduced dc-link capacitance and long lifetime power film capacitors.

6. EXPERIMENTAL VERIFICATIONS

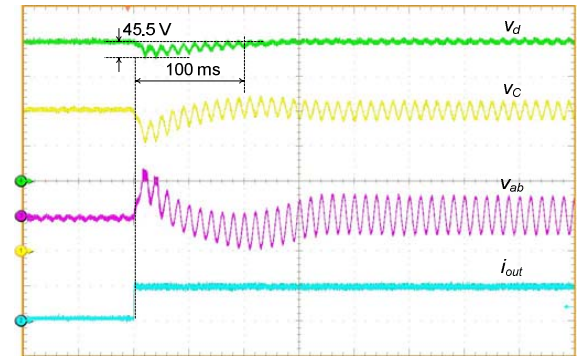
For illustration, an experimental study case has been investigated for the PEBB shown in Fig. 2(a). A test bed is built and constructed by connecting a 3 kW PFC (i.e. power converter I) to a 600 W phase-shifted full-bridge dc-dc converter (i.e. power converter II). The PFC is supplied by an ac power source with voltage of 220 V and frequency of 50 Hz. The output of the dc-dc converter is connected to an electronic load and its output voltage is 12 V.

With conventional solution, the dc-link capacitor bank C is implemented by connecting two 330 μF , 450 V E-Caps in parallel. According to the manufacturer's datasheet, the lifetime of the capacitors is 3,000 hours at 105°C (12,000 hours estimated at 85°C under rated ripple current and rated voltage stress). The measured dc-link voltage ripple is 10.8 V and the setting time from 10% load to full load transition is 100 ms. After a line dropout (i.e. the input 220 V /50 Hz ac source is turned off), the energy stored in the dc-link capacitor bank solely delivers power to the load. The measured hold-up time is 24.6 ms.

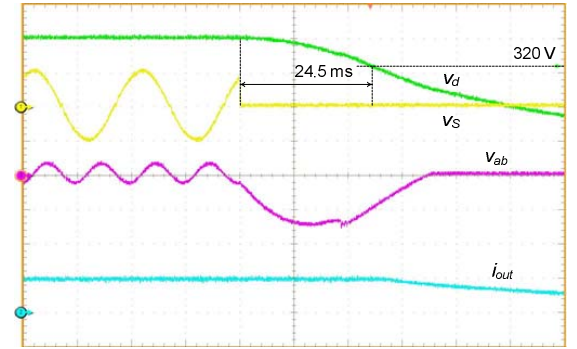
With the proposed dc-link module, a 120 μF (82% capacitance reduction) film capacitor with the lifetime of 100,000 hours at 85°C under rated voltage stress is used to replace the capacitor bank. A 1000 μF / 63 V low-voltage E-Cap with the lifetime of 8,000 hours at 125°C (128,000 hours estimated at 85°C under rated ripple current and rated voltage stress, which is comparable with the lifetime of the film capacitor) is used for the voltage compensator, i.e. C_a . The voltage across C_a is designed to be 50 V. Fig. 9(a) shows the steady-state waveforms of the capacitor ripple voltage Δv_C and module output ripple voltage Δv_d , when the output is at full load. Their peak-to-peak ripple voltages are 49.1 V and 3.9 V, respectively. Fig. 9(b) shows the transient waveforms of v_d , v_C , module output voltage v_{ab} and dc-dc converter output current i_{out} , when the output is suddenly changed from 10% load to full load. v_d is momentarily reduced by 45.5 V and its settling time is 100 ms. For the applications with hold-up time requirement, the dc-link capacitance is increased from 120 μF to 450 μF , which is 32% capacitance reduction and 28% overall energy storage reduction compared to the E-Caps solution. The hold-up time is measured with 24.5 ms as shown in Fig. 9(c), which is similar as that of the E-Caps solution.



(a) Steady-state waveforms of v_C and v_d under the full-load condition (Δv_C : 20 V/div, Δv_d : 2 V/div, Timebase: 10 ms/div).



(b) Transient waveforms when the output is changed from 10% load to full load (v_d : 100 V/div, v_C : 100 V/div, v_{ab} : 40 V/div, i_{out} : 50 A/div, Timebase: 50 ms/div).



(c) Transient waveforms after a sudden supply outage under the full-load condition (v_d : 100 V/div, v_s : 300 V/div, v_{ab} : 20 V/div, i_{out} : 50 A/div, Timebase: 10 ms/div).

Fig. 9. Experimental waveforms with the proposed dc-link module applied in the ac-dc-dc PEBB prototype.

The experimental results reveal that the proposed dc-link module can reduce the required capacitance value for the dc-link capacitor without sacrificing the transient and steady-state responses of the power converters. The resulting effect will extend the life expectancy of the entire PEBB from the perspective of reducing the chance of failure due to ageing of the dc link capacitor bank. The proposed method has an additional distinct advantage for high-voltage

applications in the smart grid, due to the fact that the voltage rating of power film capacitors is usually higher than that of E-Caps. With the proposed module, the dc-link capacitance can be reduced and a fewer number of high-voltage power film capacitors are used to replace the E-Caps which are connected in series to withstand the high voltage.

7. CONCLUSIONS

An active dc-link module with a series voltage compensator is proposed for dc-link voltage stabilization of PEBBs which are widely used in the smart grid. The overall energy storage and dc-link capacitance requirement is reduced compared to the conventional E-Caps solution, allowing a cost-effective replacement of the short lifetime E-Caps by long lifetime high performance power film capacitors. The implementation of the voltage compensator requires low-voltage devices, because it handles ripple voltage on the dc-link and reactive power only. Simulation and experimental results are in well agreement with the theoretical analysis.

As a critical component, the developed module could be integrated into different type of power converters suitable for smart grid applications. It enables new opportunity to enhance reliability of the smart grid from the component level.

8. REFERENCES

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