

Losses and CMV Evaluation in Transformerless Grid-Connected PV Topologies

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Abstract.—Controlling the thermal losses in the semiconductors as well as the Common Mode Voltage (CMV), are important issues in the design of power electronics converters for photovoltaic applications. At present time there are several topologies that offer a good performance regarding losses and CMV. In this paper an evaluation of three of these converters topologies: H5, HERIC and NPC transformerless for single phase PV systems will be carried out by means of simulations performed with PSIM 7.05. This software permits to estimate accurately the switching and conduction losses, thanks to its Thermal Module. This analysis together with the CMV study for each case will permit to establish the pros and cons of each topology.

I. INTRODUCTION

Grid-connected PV-Systems consist of three main blocks: the DC bus (PV panels), the power converter and the electrical network. The power converter acts as an interface between the DC voltage, and the grid, injecting power into the electrical network. The DC/AC conversion performed in this power converter implies the appearance of some power losses such as switching losses, conduction losses and losses in reactive elements. The typical weighted conversion efficiency, also known as “European Efficiency” for PV power converters is in the range of 95% to 98%.

For grid-connected PV-systems there are several topologies based on basic single-phase full-bridge inverters. These topologies can be classified in two different groups: one that collects the topologies with galvanic isolation and another that include all those without isolation. In the first case the galvanic isolation can be achieved by means of a high frequency (HF) transformer located on the DC side or a big-bulky transformer on the AC side. The galvanic isolation provides good safety features, but in both cases, there are more than two stages in the converter, this implies a lot of semiconductors something that increases the cost. In addition, as the number of semiconductors grows the losses increase as well, reducing finally the efficiency of the whole system. On the other hand, in second case where the transformer is omitted the efficiency can be increased around an extra 1-2%. The most important advantages of the transformerless PV inverters leads in the smaller size and weight of the converter and its higher efficiency. In addition, the lack of transformer, and the fact that

less semiconductors are needed, contributes to reduce the cost of the product.

On the contrary, the main problem with transformerless PV inverters is the leakage ground current. This leakage ground current can be a safety problem in an industrial application, due this, being necessary then to eliminate it. In general there are some solutions to minimize the leakage ground current, an issue that has been previously treated in many papers, like: [1-5].

In this paper some transformerless single-phase PV topologies will be analyzed using PSIM 7.05 (H5, HERIC and NPC topology). The idea is to know the distribution losses using the Thermal Module from PSIM, in this sense an IGBT real model will be used and in addition, the CMV will be analyzed.

II. THERMAL MODULE FROM PSIM

The Thermal Module is an add-on module to the basic PSIM program. This module allows estimating the losses of semiconductor devices (Diode, IGBT and MOSFET). The model is constructed by introducing a database from the manufacturer datasheet. This device model is used in the simulation. In the simulation the model takes into account the static characteristics of the device such as conduction voltage drop, on-state resistance, etc. The dynamic characteristics such as turn-on and turn-off transients are taken into account. Using the voltages and the currents calculated during the simulation, PSIM accesses the device database and then calculate the switching losses and conduction losses. At this point it is necessary to take into account that these losses calculations are only an approximation and its accuracy depends on the data device accuracy. Moreover this Thermal Module allows estimating the thermal behaviour according with the losses.

In the simulation processes there is a parameter *Frequency* under which the losses are calculated. If switching frequency is 10kHz and switching parameter is equal to 10kHz, then the losses will be the value for one switching period. However if parameter frequency is set to 50Hz, then the losses will be the values for a period of 50Hz.

A. Diode losses

The diode losses are calculated as follow:

- 1) *Conduction losses*: The diode conduction losses is calculated using equation (1)

$$P_{cond_cal} = V_d \cdot I_F \quad (1)$$

Where V_d is the diode voltage drop at the diode, I_F is the diode forward current and D is the duty cycle.

- 2) *Switching losses*: When calculating the switching losses, the diode turn-on losses are neglected. The diode turn-off losses due to the reverse recovery is calculated as:

$$P_{sw_off} = E_{rr} \cdot f \quad (2)$$

or

$$P_{sw_off} = \frac{1}{4} \cdot Q_{rr} \cdot V_R \cdot f \quad (3)$$

Where E_{rr} is the reverse recovery energy losses, Q_{rr} is the reverse recovery charge, V_R is the reverse blocking voltage, and f is the frequency as defined in the input parameter *Frequency*. The reverse recovery charge Q_{rr} is defined as:

$$Q_{rr} = \frac{1}{2} \cdot t_{rr} \cdot I_{rr} \quad (4)$$

Whenever E_{rr} is given in the device database, the losses will be calculated based on E_{rr} , if E_{rr} is not given, the losses will be calculated based on Q_{rr} , if Q_{rr} is not given, the losses will be calculated based on t_{rr} and I_{rr} , if both are not given, then the losses will be considered as zero.

B. IGBT losses

Also in the case of the IGBT losses there is a parameter *Frequency* which works in the same way that in the diode.

The IGBT losses are calculated as follow:

- 1) *Conduction losses*: The IGBT conduction losses is calculated using equation (5)

$$P_{cond_cal_Q} = V_{ce(sat)} \cdot I_C \quad (5)$$

Where $V_{ce(sat)}$ is the transistor collector-emitter saturation voltage, and I_C is the collect current.

- 2) *Switching losses*: The transistor switching losses during the Turn-on processes is calculated using (6).

$$P_{turn_on} = E_{on} \cdot f \quad (6)$$

Where E_{on} is the transistor turn-on energy losses and f is the frequency as defined in the input parameter *Frequency*.

On the other hand, the transistor turn-off energy losses are calculated with equation (7).

$$P_{turn_off} = E_{off} \cdot f \quad (7)$$

Where E_{off} is the transistor turn-off energy losses and f is the frequency as defined in the input parameter *Frequency*.

The loss calculation for the anti-parallel diode or free wheeling diode is the same as is described above. A complete explanation about how losses are calculated is available in [6].

III. H5 TOPOLOGY

In transformerless PV inverters which generate varying common mode voltages, leakage currents can flow from the PV panels to the ground through stray capacitance. H5 topology [7] is a solution to eliminate the dangerous leakage currents (common-mode currents) problem in transformerless PV inverters. This topology provides a disconnection from the DC side in order to get a zero leakage ground current. The disconnection is necessary because when no transformer exists between the grid and the inverter a galvanic connection can appear, therefore resonant circuits can turn up in the system. The H5 topology structure is given in Fig. 1.

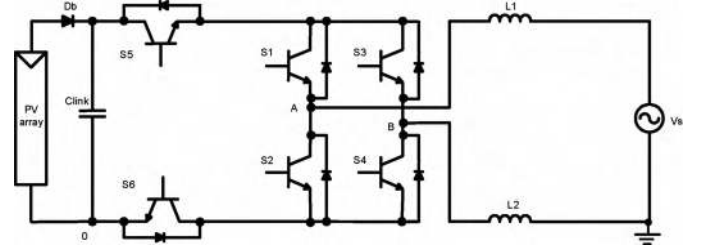


Fig. 1. H5 topology from SMA technologies.

The system works as follow: During the positive half cycle, S5 and S6 commute at switching frequency whereas S1 and S4 are ON in order to modulate the input voltage. On the other hand, when negative half cycle is present, S5 and S6 commute at switching frequency whereas S3 and S2 are ON.

A simulation with PSIM was done using discrete components in order to know the losses exact localization. The simulation results are shown in Fig. 2.

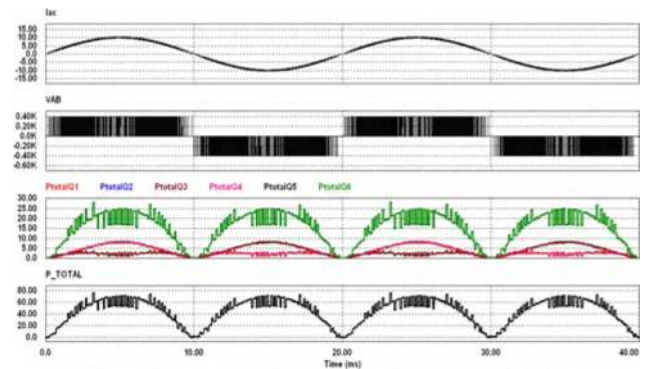


Fig. 2. H5 Losses distribution using PSIM Thermal Module.

As shown in Fig. 2, Thermal module allows seeing the distribution losses when discrete components are used.

According with this simulation, it is possible to obtain table 1 as shown below.

TABLE 1
LOSSES DISTRIBUTION FOR H5 TOPOLOGY

	S1	S2	S3	S4	S5	S6	Total	
H5	3.45	3.44	3.45	3.45	15.21	15.22	44.23	W

As it can be seen in Table 1, S1, S2, S3 and S4 have almost the same power losses while S5 and S6 have the major power dissipation (around 68.68%). These simulation results can be used in order to do a good thermal design. Furthermore an efficiency estimation can be performed. The simulation was done using a simple hysteresis current control.

Regarding to the CMV using this modulation technique, the result can be seen in Fig. 3

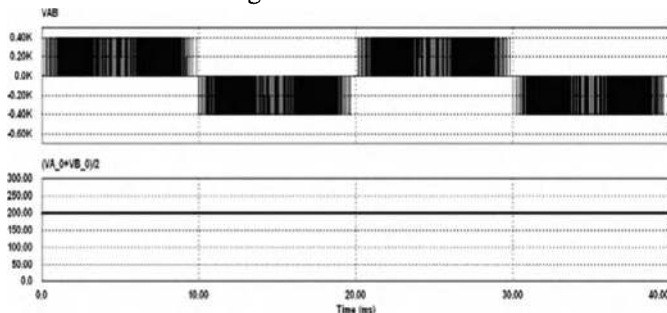


Fig. 3. Common mode Voltage in H5 topology.

Fig. 3 shows that there is no a fluctuating potential on the DC side. This means that this single-phase PV inverter can fulfill with security standard regarding to leakage ground current (VDE 0126).

IV. HERIC TOPOLOGY

The HERIC (Highly Efficient and Reliable Inverter Concept) topology is another structure that avoids a fluctuating potential on the DC terminals of the PV generators by means of disconnecting the converter from the load (utility grid). In this case the zero voltage level is obtained using a bidirectional switch during freewheeling periods [8]. This topology is shown in Fig. 4.

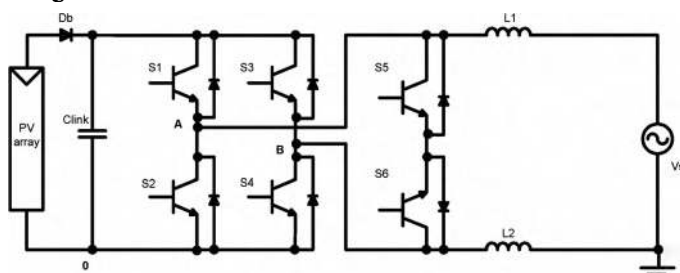


Fig. 4. High Efficient and Reliable Inverter Concept (HERIC) topology.

Topology works as follow: during the positive half cycle S6 remains connected, whereas S1 and S4 commutate at switching frequency in order to generate both active and zero vectors. When an active vector is present (S1 and S4 are ON), current

flows from the PV panels to the load (grid), when a zero vector occurs, S1 and S4 are switched OFF and then, the current flows through S6 and D1, this is the freewheeling situation. On the other hand, when the negative cycle is coming, S6 goes OFF and S5 goes ON, whereas S3 and S2 commutate at switching frequency. It means that an active vector is present when S3 and S2 are ON, therefore the current flows from the PV panel towards the load, thus when S3 and S2 turn off, a zero voltage vector is present in the load, then current flows through S5 and D2. This kind of modulation allows having a freewheeling situation with no connected load (utility grid).

Fig. 5 shows a simulation performed with PSIM using discrete IGBT in the same way that H5.

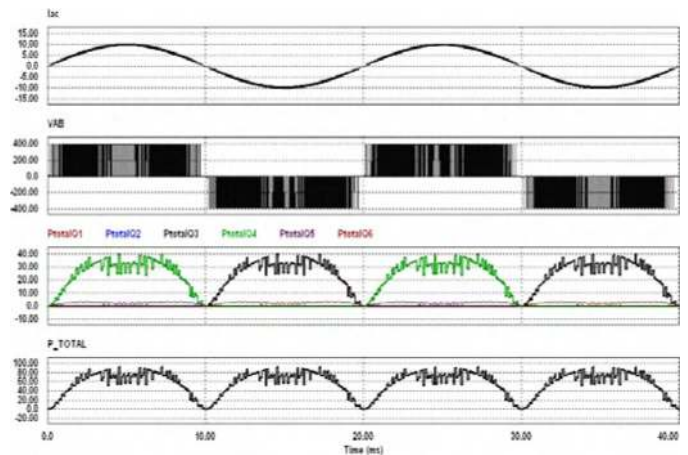


Fig. 5. HERIC topology simulation wave forms.

Fig. 5 shows the losses distribution among all six transistors. As it can be seen, high losses percentage is on S1 to S4 (basic full bridge) due to the high switching frequency, the other two switches have a very low losses percentage (they are switching at grid frequency). An average losses value for each switch is shown in table 2.

TABLE 2
LOSSES DISTRIBUTION FOR HERIC TOPOLOGY

	S1	S2	S3	S4	S5	S6	Total	
HERIC	13.26	13.29	13.25	13.27	1.101	1.101	61.31	W

The common mode voltage obtained for this topology is shown in Fig. 6.

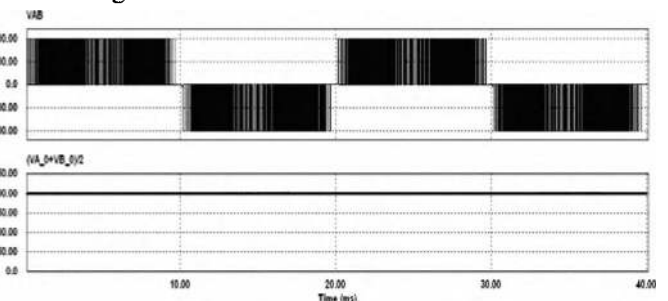


Fig. 6. Common mode voltage in HERIC topology.

Fig. 6 shows that there is no a fluctuating potential on the DC side, this means that the DC voltage remains constant through all grid period. This way the leakage current through the parasitic capacitance would be very small.

V. NPC TOPOLOGY

The NPC is another single phase interesting topology in transformerless PV systems. This topology has a good performance regarding the voltage fluctuations present on the DC bus, due to the fact that in this case the middle point of the input capacitors is connected to neutral; this situation avoids capacitive earth current and their negative influence on the electromagnetic compatibility of the circuit. In order to allow power transfer into the grid the DC bus voltages have to be always higher than the grid voltage amplitude, due this, take into account that the output voltage of PV modules is around 24 V, it is necessary to use a large number of modules or in other case, it is possible to use an input converter in order to boost the input voltage. Fig. 7 shows the NPC topology scheme [9].

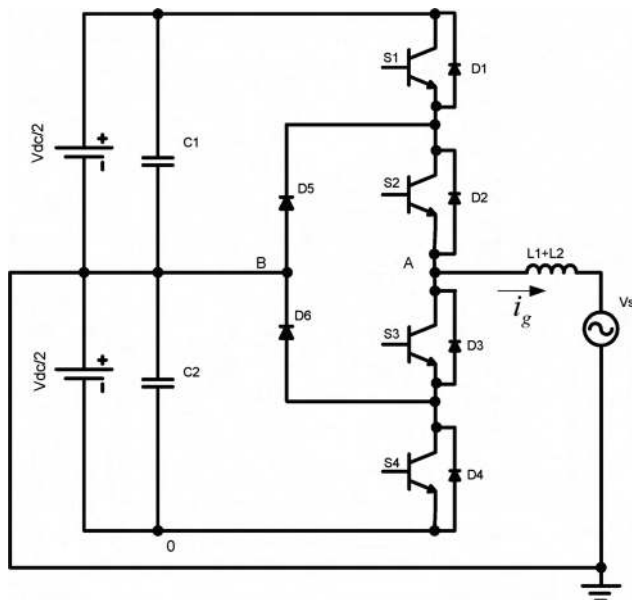


Fig. 7. NPC (Neutral Point Clamped) topology.

The operation of this topology is as follow: During the positive half cycle, S2 remains ON, S1 commutate at switching frequency and S3 and S4 are OFF. When S1 is ON, and active vector is applied to the load and the current flows through S1 and S2 toward the load (current increasing), also when S1 is OFF, a zero voltage vector is applied to the load, in this case, the current flows through D5 and S2 (current decreasing). On the other hand, during the negative half cycle, S3 remains ON, whereas S4 commutate at switching frequency and S1 and S2 are OFF. When S4 is ON an active vector is applied to the load and current flows through S3 and S4 toward the load (current increasing), also when S4 is OFF, a zero voltage vector is

applied to the load, in this case, current flows through S3 and D6 (current decreasing).

With this PWM pattern modulation it is possible to get a three voltage level in the output voltage.

A simulation was performed using this PWM pattern and with a simple hysteresis control system. Simulation results are shown in Fig. 8.

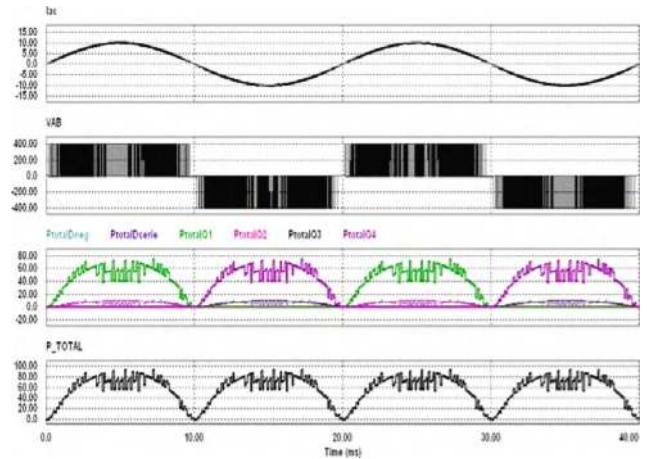


Fig. 8. Losses distribution for NPC topology.

Fig. 8 shows the losses distribution among all semiconductor devices in the circuit. In this case the losses are located mainly in switches S1 and S4 due to its high switching frequency. In the case of the other switches the losses are very low due to the low switching frequency (grid frequency). The table 3 shown an average losses value over each semiconductor device.

TABLE 3
LOSSES DISTRIBUTION FOR NPC TOPOLOGY

	S1	S2	S3	S4	D5	D6	Total	
NPC	22.59	3.25	3.25	22.59	2.98	2.98	57.66	W

The common mode voltage regarding this topology is shown in Fig. 9.

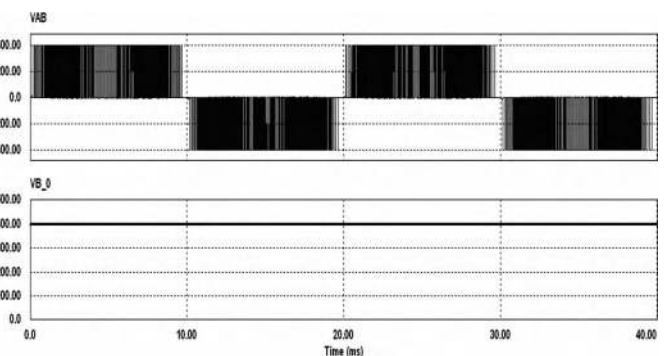


Fig. 9. Common mode voltage in NPC topology.

Fig. 9, shows that there is not voltage variations on the DC bus, this means that there is not leakage current flowing

through the parasitic capacitance between PV module and earth.

All simulations were performed using a real model. The IGBT is an IPM (Intelligent Power Module) from Mitsubishi PM75DSA120. The DC bus was of 400V (H5 and HERIC), whereas for NPC was of 800V. The load was a grid with $L=4$ mH, $V_s= 325$ V and $f=50$ Hz. The parasitic capacitance was choosing with a typical value of 100n [10].

VI. CONCLUSIONS

Nowadays PV systems are widely used in the electricity market. Security and Efficiency are two very important issues in these systems. Moreover, another target in the design is to reduce the cost. In this sense, a good thermal design is required. With Thermal Module from PSIM a real device model can be used, therefore the losses simulation results can be a very good approximation to real experimental results. Using discrete devices it is possible to know where losses are exactly located; with this premise a good thermal design can be done.

The analyzed topologies are the more widely used in transformerless PV systems. Based in the previously comparative simulations results it can be concluded that in the case of H5 topology losses are concentrated in S5 and S6. In case of HERIC topology losses are located among S1, S2, S3 and S4. Finally in NPC single phase topology, losses are located in S1 and S4. These results mean that in each case, the losses distribution is not the same and a different thermal design should be done. In addition it can be concluded that the total losses are higher in HERIC and NPC topologies than H5 topology.

On the other hand, take into account the common mode voltage results, it can be conclude that with the disconnection system (from the grid or DC side) it is possible to avoid voltage variations on the DC side, as a consequence no leakage currents appear. In the same way in the case of NPC topology no leakage ground currents appear because of the connection of neutral terminal with the midpoint of the capacitors.

ACKNOWLEDGMENT

This research work was supported by the project ENE2008-0841-C02-01/ALT from the Spanish Ministry of Science and Technology (MCYT).

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