Lossless Operation of an 8 × 8 SiPh/InP Hybrid Optical Switch

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***Abstract*— We design a lossless 8 × 8 Silicon Photonics (SiPh)/Indium Phosphide (InP) hybrid optical switch. The design consists of an 8-channel InP gain block for coupling to an 8 × 8 thermally tuned Mach-Zehnder interferometer-based Banyan switch in a passive SiPh platform. The gain block is an array of eight 1300 μm-long semiconductor optical amplifiers (SOAs). We experimentally verified the InP gain block while the SiPh chip is accounted by replacing it with a loss component. The SOA in line with the optical signal path provides a net gain larger than 25 dB to compensate for the inherently large insertion loss of the 8 × 8 SiPh optical switch. The total energy consumption of the hybrid optical switch in lossless operation mode is 10.44 pJ/bit at 12.5 Gb/s.**

***Index Terms*— Optical interconnections, silicon photonics, indium phosphide, semiconductor optical amplifiers, hybrid integrated circuits, energy efficiency.**

I. Introduction

THE ever-growing internet traffic asks for the increase in the capacity and energy efficiency of the next generation data centers [1]. Electronic switches, currently used in the data centers, may have problems meeting such requirements due to their relatively high power consumption and large latency. Alternatively, optical switches promise higher capacity and lower latency, while, potentially consuming less power [2]. Even though optical switching for data centers still is in exploratory stage, various technologies in different material platforms have already demonstrated a high-capacity switching with superior figure of merit [3], [4].

Advanced data center applications demand high radix switches to connect the servers at different network levels. This requires cascaded multiple input—multiple output port optical switch architecture, which, inevitably leads to significant insertion loss. Therefore, reduction or, ideally, elimination of the insertion loss is an enabling condition for any practical use of the optical switches [5].

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Silicon photonics (SiPh) is a technology particularly suitable for scalable optical switches. Its compatibility with the ubiquitous CMOS process leads to low fabrication cost, large wafer size, and high level of integration [4]. However, optical switches in SiPh incur substantial insertion loss, while not providing any practical mechanism for its compensation, by virtue of an indirect bandgap semiconductor inherently incapable of inter-band gain. The required gain could be provided off chip by hybrid integration to an external gain block, e.g., in Indium Phosphide (InP)—a direct bandgap semiconductor featuring strong inter-band gain in the spectral range of interest for most optical switch applications [6]–[8]. In a SiPh/InP hybrid optical switch, routing the optical signal from an input port to the desired output port is on the SiPh chip, while the InP gain block provides amplification required for compensation of the insertion loss.

In this paper, we demonstrate the feasibility of a lossless operation of an 8 × 8 SiPh Mach-Zehnder interferometer (MZI)-based Banyan optical switch with thermal phase shifters coupled to an 8-channel InP gain block. We experimentally verified the InP gain block. Alternatively, the SiPh chip is accounted by replacing it with a loss component. The InP semiconductor optical amplifier (SOA) provided gain exceeds 25 dB, 10 dB more than in earlier reported 4 × 4 SiPh/InP hybrid integrated optical switch [6]. Further to [8], this paper presents an evaluation of the noise figure (NF), the optical signal-to-noise ratio (OSNR) degradation in the gain block, and the switch energy consumption. The OSNR at the output of the gain block is sufficient for a distortion-free 12.5 Gb/s optical data transmission.

II. Hybrid Switch Optical Power Budget

The proposed design for the SiPh/InP hybrid switch consists of an 8 × 8 SiPh switch edge-coupled to an InP gain block as shown in Fig. 1 (a). The SiPh switch employs a 4 × 3 matrix of 2 × 2 symmetric MZIs as the switching elements in a 3-stage multistage Banyan architecture. The switch is designed for an application in which the latency controller accounts for the blocking scenarios [9]. This flexibility allows us to use Banyan architecture that offers simple structure, lower number of switching MZIs, fewer waveguide crossings, and accordingly lower fiber-to-fiber loss. However, one can implement the same design idea using other non-blocking switching architecture such as Beneš or dilated Beneš according to the application. The InP gain block is an array of eight SOAs. The input light to the SiPh chip and the output from the InP gain block are edge-coupled.

TABLE I
LOSS AND GAIN OPTICAL POWER BUDGETED VALUES

Loss/gain of active/passive elements	Value
SiPh switch: input coupling loss	-3.3 dB
SiPh switch: on-chip loss	-8.4 dB
SiPh switch to InP gain block: inter-chip coupling loss	-7.0 dB
InP gain block: on-chip loss	-2.9 dB
SOA/InP net gain	+24.6 dB
InP gain block: output coupling loss	-3.0 dB

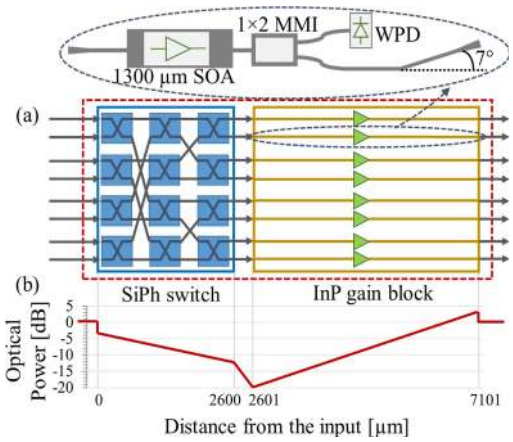

Fig. 1. (a) Schematic view of the SiPh/InP hybrid switch. (b) Normalized optical power relative to the positions (not to the scale) indicated in part (a).

Table I summarizes the loss and gain of the active and passive elements used in the proposed hybrid optical switch. Based on these values, Fig. 1 (b) shows the normalized optical power of the optical signal passing through the hybrid switch. The SiPh design is for fabrication on a 220 nm thick Silicon on Insulator (SOI) wafer through Applied Nanotools [10]. Design and fabrication of the SiPh part is based on the designs of SOI-MZI thermo-optic switches previously designed and validated by our research group [11]. The 200 nm thick Ti-W metal heaters modify the phase of optical propagating payload signals in the MZI arms. The SiPh input and output ports use spot-size converters with trident waveguides. The input optical fiber mode field diameter (MFD) of 10.4 μm reduces to 3.0 μm at its lensed output before propagating the SiPh waveguides with a width of 0.5 μm. The MFD of the fundamental TE mode in this SiPh waveguide is approximately 220 nm in the chip's plane and 130 nm perpendicular to the chip's plane. The trident waveguide at the output of the SiPh chip leads to an MFD of 2.8 μm in the chip's plane and 0.96 μm perpendicular to the chip's plane. This achieved MFD optimizes the mode overlap at the input of the InP chip with the tapered waveguides with the MFD of 2.8 μm in the chip's plane, and 0.96 μm perpendicular to the chip's plane. The minimum coupling loss for this spot size converter is 2.3 dB increasing to 3.3 dB for an offset of $\pm$0.9 μm [12]. We consider the other design values for SiPh on-chip loss based on the building block features reported by Applied Nanotools. The SiPh on-chip loss accounts for 5.4 dB insertion loss for the three MZIs in each path and 1.3 dB waveguide propagation and crossing loss. We budget 1.7 dB of unforeseen loss to the SiPh for a conservative budget.

The InP gain block is fabricated through SMART Photonics [13]. The front and back facets of the input and output ports are coated to reduce the reflectivity to below -30 dB. To minimize the residual Fabry-Perot effects, the output ports of the InP gain block are tilted at seven degrees. We estimate the inter-chip coupling loss between the SiPh and InP chips to be 2.7 dB at the optimum position. This coupling loss accounts for the SiPh output trident SSC and the loss of the InP input tapered waveguide. The coupling loss between a similar trident SSC waveguide design and an InP laser diode with a similar spot size of approximately 3 μm is reported to be 2.3 dB [12]. This value is sensitive to the alignment precision in the packaging step. The worst-case misalignment using solder-aligned photonic flip-chip assembly technique is reported to be 0.26 μm in the vertical direction or 0.58 μm in the horizontal direction [14]. According to the tolerance curves reported by SMART, the aforementioned misalignment translates into 1 dB and 3.3 dB of additional inter-chip coupling loss in the horizontal and vertical axis, respectively. Therefore, the maximum coupling loss between the two chips is budgeted at 7 dB (2.7 dB + 1 dB + 3.3 dB).

The InP on-chip loss of 2.9 dB and output coupling loss of 3.0 dB are based on process design kit (PDK) guaranteed values reported by SMART Photonics. Considering all the losses, for a minimum net gain of 24.6 dB per channel, the hybrid optical switch can perform lossless operation. Each channel of the InP gain block comprises a booster SOA coupled to a 1×2 multimode interference (MMI) splitter 85:15) and a waveguide photodetector (WPD) for on-chip optical power measurement.

III. GAIN BLOCK EXPERIMENTAL VALIDATION

In SiPh/InP hybrid integrated optical switches, a major source of OSNR degradation is the amplified spontaneous emission (ASE) generated in the gain block. Thus, measuring the OSNR degradation of the gain block provides an assessment for the performance of the SiPh/InP hybrid integrated optical switch. ASE noise generated by the SOAs limits the SOA cascadability towards switch scalability [15].

A set of experimental measurements investigates the lossless operation of the 8×8 SiPh/InP hybrid optical switch by measuring the gain provided by the InP gain block. As illustrated in the inset of Fig. 2, a tunable C-band laser generates a continuous wave (CW) optical signal at 1550 nm wavelength. A polarization controller (PC) sets the state of polarization of the optical signal to a quasi-TE optical mode. This optical signal is edge-coupled to the InP gain block through an array of lensed fibers positioned by a six-axis nano-positioning stage. The optical power at the output of the InP gain block is monitored using the on-chip WPDs. We estimate the fiber-to-fiber loss of the SiPh/InP hybrid optical switch based on the measured optical gain of the SOA gain block and the loss values reported in Table 1. As reported in Fig. 2, the estimated fiber-to-fiber loss decreases with SOA bias current. Due to the SOA optical gain saturation, the fiber-to-fiber loss increases with input optical power. For an input optical power below 1.5 dBm, lossless operation of the hybrid switch requires an SOA bias current of 75 mA or higher. We measured a variation in the gain of less than 1 dB between different gain block channels. Figure 2 presents the results for the channel providing the lowest gain. We test the chip at the room temperature without using a temperature controller. All-channel simultaneous operation would be also possible with an appropriate test bed.

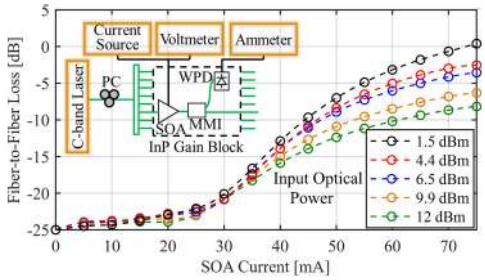

Fig. 2. Estimated fiber-to fiber loss as a function of SOA current. Inset: experimental setup for the CW test.

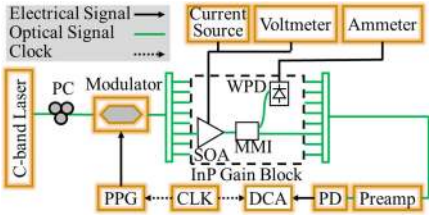

Fig. 3. Experimental setup for 12.5 Gb/sec payload transmission. One channel of the InP gain block is tested at a time.

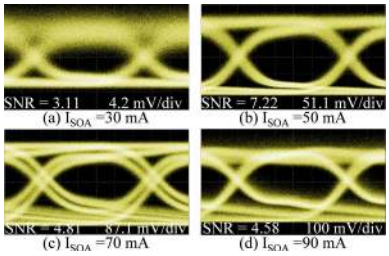

Fig. 4. Eye diagrams for 12.5 Gb/s payload transmission over a single channel of the InP gain block for different bias current values.

The experimental setup in Fig. 3 assesses the impact of ASE noise on the gain block performance at high bias current when the noise figure becomes important. A pulse pattern generator (PPG) generates a 12.5 Gb/s nonreturn-to-zero (NRZ) PRBS-31 signal. The quasi-TE polarized modulated optical signal is edge-coupled to the InP chip. A current source provides the electrical biased current to the SOAs. An erbium-doped fiber amplifiers (EDFA) based preamplifier compensates for the additional losses to meet the photodetector (PD) sensitivity of −18 dBm at 12.5 Gb/s. A 20 GHz clock synthesizer (CLK) provides the external clock to the PPG and triggers the digital communication analyzer (DCA) for recording eye diagrams.

The 12.5 Gb/s eye diagrams (Fig. 4) are recorded for the payload data transmission over one single channel of the gain block. The input optical power of the signal to the InP chip is set to −17.5 dBm representing the weakened signal from propagating through the SiPh chip. Considering the power budget (Table I) and Fig. 1 (b), −17.5 dBm of input power to the InP chip corresponds to an input power of approximately +1.2 dBm to the SiPh switch. Lossless operation of the hybrid switch is viable at this input power (Fig. 2). As observed in Fig. 4, for small SOA bias current (i.e., 30 mA), the eye diagram is degraded by a low SNR. At this level of bias, the SOA gain is insufficient to compensate for the coupling losses and even contributes to the total loss. As SOA bias current reaches 50 mA, owing to sufficient SOA gain, wide-open eye diagrams are observed, demonstrating distortion-free high-speed payload transmission. The optical gain starts to

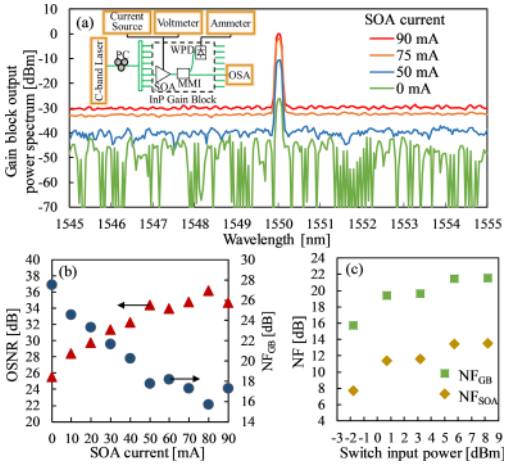

Fig. 5. (a) Measured output spectra of the gain block, inset: experimental setup for the NF test. (b) OSNR and NF of gain block versus SOA current. c) NF_{SOA} and NF_{GB} as functions of hybrid switch input power.

saturate when the bias current increases to 70 mA. Consequently, when the SOAs are biased close to the threshold of the saturation region, the sequences of payload bits with more binary ones experiences less gain than the sequences of bits with more binary zeros. This operation region leads to pattern dependency and the double edge seen. For a bias current above 90 mA toward deep gain saturation region, the SOAs saturate regardless of the optical binary sequence type passed through them. Despite this phenomena, the eye remains open even for SOA bias current as large as 90 mA. The distortion observed in the eye diagrams presented in Fig. 4 (c, d) increases the power penalty of the optical switch.

To quantitatively estimate the degradation of the signal-to-noise ratio, we measured the OSNR at the output of the gain block and the NF by an optical spectrum analyzer (OSA). Figure 5 (a) shows the spectra at the gain block output, when the input to the InP gain block is a CW optical signal at 1550 nm wavelength. As in the previous measurements, the optical power of the signal to the InP chip is set to −17.5 dBm. From this power spectrum, we extract the OSNR at the output of the gain block. Fig. 5 (b) shows the OSNR as a function of the SOA bias current. The OSNR increases with the SOA bias current, then saturates and slightly decreases as the SOA reaches the gain saturation region. The OSNR remains larger than 30 dB for the SOA current bias above 30 mA.

We calculated the noise factor (F) and NF of the gain block using the source subtraction technique [16]. This technique solves the problem of separating the source spontaneous emission (SSE) from the SOA generated ASE by characterizing the SSE when the gain blocked is bypassed. As the SSE spectral density is time invariant, we can subtract it from the total noise at the gain block output to obtain the ASE generated by the gain block. We express the noise factor of the gain block, F_{GB}:

$$F_{GB} = \frac{2\rho_{total}}{G_{GB}h\upsilon} + \frac{1}{G_{GB}} - \frac{2\rho_{SSE}}{h\upsilon} \tag{1}$$

where, ρ_{total} is the ASE power spectrum density measured at the output of the gain block, G_{GB} is the gain of the gain block, ρ_{SSE} is the ASE power spectrum density at the gain block input, h is the Planck constant, and $\boldsymbol{\upsilon}$ is the frequency of light. The first and second terms in eq. (1) represent the signal-spontaneous beat noise factor and shot noise factor of the gain block, respectively. The third term is the subtracted source

spontaneous emission. The NF of the gain block (NF_{GB}) is the noise factor expressed in decibels. NF_{GB} versus SOA bias current is shown in Fig. 5 (b). A minimum NF_{GB} of 17.56 dB is achieved at 80 mA bias current. The NF_{GB} is comparable but slightly higher than the *NF* of 16.6 dB recently reported for 4×4 SOA integrated SiPh switch [6]. This higher than expected *NF* is mainly due to the extra coupling loss at the input of gain block. The gain block consists of two passive coupling losses at the input and output facets and one active SOA, all cascaded. To extract the NF of the SOA (NF_{SOA}) from the NF_{GB} we use the Friis formula that expresses the total noise factor of multiple cascaded stages:

$$F_{GB} = F_{input} + (F_{SOA} - 1)L_{input} + \frac{(F_{output} - 1)L_{output}}{G_{SOA}} \tag{2}$$

where, F_{input}, F_{SOA}, and F_{output} are the noise factors of the input coupling, the SOA, and the output coupling, respectively. G_{SOA} is the net gain of the SOA. L_{input} and L_{output} are the input and output coupling losses, respectively. The noise factor of a passive lossy device is identical to its loss (in a linear ratio) [15], hence, F_{input} and F_{input} in eq. (2) are replaced by L_{input} and L_{output}. Since, G_{SOA} is large, especially at lossless operation of the switch, the last term of eq. (2) is negligible. Simplifying eq. (2) one obtains:

$$NF_{GB} = 10log_{10}L_{input} + NF_{SOA}. \tag{3}$$

Figure 5 (c) presents the NF_{GB} and NF_{SOA} versus input power to the SiPh/InP hybrid switch. NF_{GB} and NF_{SOA} are measured at 80 mA bias current. The minimum value of measured NF_{SOA} is 7.7 dB which is in agreement with the fabrication foundry value (7 dB). The extracted NF_{SOA} is smaller than the *NF* of 10 dB reported for the hybrid switch with smaller port count [6]. We showed in this study that in spite of the 25 dB of gain provided by the SOAs, the OSNR remains large enough even at large values of SOA bias current (Fig. 5). Along with the clear eye diagrams presented in Fig. 4, these results reveal that the gain block is capable of low noise data transmission.

In a SiPh/InP hybrid switch, the unused SOAs that are not in the active optical signal paths are switched off. This reduces the crosstalk by absorbing the leaked signal in the SiPh block to the unused ports, and reduces the system level crosstalk between the active channel and the idle channels. To further suppress the crosstalk, one can exploit low crosstalk SiPh switch fabrics [17]. The power dissipation in the SiPh 8×8 switch mainly consists of the power dissipated in the thermo-optic MZIs. We consider an average of 10 mW power dissipation per MZI, thus, 120 mW in total [18]. For lossless operation of the switch, the SOAs in line with the signal are biased at 75 mA current, corresponding to 1.54 V voltage, consuming 115.5 mW power. Therefore, the energy consumption of the presented hybrid switch at zero fiber-to-fiber loss while all ports are active is 10.44 pJ/bit. This is 17% lower compared with the lowest energy consumption so far reported for a lossless 8×8 switch on InP platform (12.6 pJ/bit in a similar bit rate [19]).

IV. Conclusion

The lossless operation of an 8×8 SiPh/InP hybrid optical switch is experimentally demonstrated. The proposed device consists of an 8×8 MZI-based thermo-optic Banyan switch in the SiPh platform edge-coupled to the 8-channel gain block in InP. Zero fiber-to-fiber optical loss is achieved for a net gain of approximately 25 dB, provided by 1300 μm long SOAs biased at 75 mA to 90 mA. Wide open eye diagrams for 12.5 Gb/s NRZ PRBS-31 payload transmission and OSNR greater than 30 dB are demonstrated. These results confirm the suitability of hybrid integrated lossless switch for the distortion-free high-speed optical payload data transmission. The total energy consumption of the hybrid switch while operating at lossless mode and data rate of 12.5 Gb/s is 10.44 pJ/bit.

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