Lossy Power Distribution Networks with Thin Dielectric Layers and/or Thin Conductive Layers

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Abstract

Through their inherent skin losses, conductive planes around sufficiently thin dielectric layers may provide good suppression of plane resonances in printed-circuit-board power distribution networks. When combined with thin conductive layers, a resistor-like flat self-impedance and low-pass transfer-impedance profiles can be created. A lossy transmission-line grid model is used to simulate power-ground plane pairs with thin dielectric and thin conductive layers. Some of the modeling errors of the analytical plane-impedance expressions and lossy transmission-line grid plane models are compared. Simulated and measured impedances are compared on test structures with plane separation of 40 and 8 microns (1.6, and 0.3 mils).

I. Introduction

With increasing clock speeds and decreasing supply voltages in computing devices, the correct design and measurement verification of power-distribution networks (PDN) become more challenging. In some systems the required target impedance may reach the sub milliohm range, while the bandwidth of transients moves into the GHz range [1]. At the same time, systems may have large printed-circuit boards (PCB) with board dimensions in excess of 0.5 meters. It is also typical that the DC sources are located on the same PCB in the form of DC-DC converters. The power is then distributed on one or more power/ground planes of the PCB. These conductive planes form the basis of the PDN. The wideband low impedance is achieved by the combination of properly designed DC-DC converters, bulk capacitors, medium- and high-frequency signal-integrity (SI) capacitors. The power-ground planes of PCB interconnect these elements, but because the PCB size is not negligible compared to the wavelength of the highest frequency of interest,

the transmission-line effects of the planes must also be considered, and eventually the planes become an integral part of the PDN.

At the low end of the spectrum, the PDN in high-end systems must carry large currents, sometimes exceeding one hundred Amperes. The DC resistance of a square of a 35-micron (one-ounce) copper plane is approximately 0.7 milliohms. To achieve sufficiently low DC drop, several conductive planes in parallel may be required. An often overlooked requirement of PCB PDNs is that isolation is also required among the electronic subsystems attached to the PCB. With physically separate subsystems, such as plug-in cards, the isolation partly comes from the connectors and wires. At high frequencies, the equivalent characteristic impedance of connectors and wires is usually much higher than the impedance of the power-distribution network, and therefore these can be considered as decoupling inductances. On the printed-circuit boards, however, we may need closely spaced power/ground planes to achieve the low impedance at high frequencies. Combined with the typical epoxi-resin-fiberglass (e.g., FR4) dielectric materials, the power-ground planes form a two-dimensional transmission line with fairly low attenuations up to a couple of GHz.

If not designed properly, the power/ground planes in the PDN may exhibit resonances in the frequency domain [2], and at specific resonance frequencies the transfer impedance at remote points may be even higher than the self-impedance at the location of the noise source. To avoid the resonances in the PDN, there are several options. In conventional designs, many bypass capacitors may be attached to the PDN planes. These capacitors eventually create a capacitively loaded transmission structure, and it can suppress plane resonances while creating low-pass function as well. The limitation of this approach stems from the difference between the mounted inductance of bypass capacitors and the equivalent inductance of power-ground planes. The mounted inductance of regular, two-terminal bypass capacitors is several hundred pH, see e.g., [3]), whereas the equivalent inductance of closely-spaced power/ground planes is few times ten pH.

Another possibility for suppressing plane resonances is to increase the losses of the dielectric material between the power/ground planes. A lossy conductive layer in the dielectric material is suggested in [4]. This technique requires an extra step in PCB manufacturing, and we have to make sure that the signal vias are not effected by the losses. Resistive termination at the plane edges can also be used [5], [6]. The resistive termination reduces the resonance peaks in the impedance and radiation profile, but it does not, in itself, provide a low-pass transfer function. As it is shown in this paper, yet another possibility to reduce plane resonances, and at the same time to provide low-pass filter transfer function is to rely on the inherent conductive losses of the PCB planes. This is of particular interest in light of recent efforts to embed bypass capacitors into the PCB ([13], [14]).

Using any methodology to design the PDN, the accurate and efficient simulation of the two-dimensional transmission-line planes becomes a necessity. This paper summarizes some accuracy considerations for two of the simulation approaches: the transmission-line grid method and the analytical plane-impedance method. The measurement methodology suitable for very low impedances over a wide frequency band was described in [7], [8].

II. Effect of inherent transmission losses in PDN power-ground plane pairs

In this section, three possible loss mechanisms, all inherent to PCB PDNs are considered:

- effect of conductive losses of regular-weight conductive layers around thin dielectrics
- effect of conductive losses of thin conductive layers around regular or thin dielectrics, and
- effect of dielectric losses.

II.1. Lossy transmission-line grid model

To consider the time-of-flight and resonance effects of planes, a grid of transmission lines was used (see e.g., [11] and [12]). Figure 1 shows the transmission-line grid model used for the simulations in this paper. The equivalent circuit has a grid of sub circuits, each of which contains a loss less transmission line, a DC and AC resistance separately for the upper and lower conductive planes, and a parallel resistor describing the dielectric losses. The AC series resistance is scaled with the square root of frequency, while the parallel loss scales linearly with frequency. The input parameters and the derived HSPICE parameters for the sub

circuits are shown in Figure 2. Note that Figure 1 contains two different sub circuits: T_line_g is the lossy transmission line sub circuit for all of the internal paths of the grid, whereas T-Line_e is the sub circuit only for the edges. The T-Line_e parameters are adjusted by a factor of two, to take into account the fact that they have no neighboring planes. Note that in this grid representation the grid cells correspond to squares on the planes, and if the x and y dimensions of the planes are not the same, the number of cells along the two axes will reflect the different dimensions. Note also that the grid is 'floating', the reference side of the Tlines are not hardwired to SPICE node0, thus allowing – if necessary - a combination of various grid layers.

II. 2. Effect of dielectric thickness on the plane impedance with regular copper thickness

It is known that the series conductor losses of a transmission line increase the attenuation, which under matched conditions can be expressed as:

$$A^{dB} = 4.35\left(\frac{R_s}{Z_o} + G_d Z_o\right)$$

where

A is the attenuation of the matched-terminated trace in dB,

Rs is the series attenuation at the required frequency

Gd is the parallel conductance of the dielectrics at the required frequency

Zo is the characteristic impedance of trace

Rs is the total series resistance of the conductor at the frequency of interest, determined by the cross section of conductor. At higher frequencies, the resistance of conductor increases, because current tends to flow on the surface, leaving for current conduction only an effective channel of depth, which is proportional to the inverse square root of frequency. This effective depth is called the skin depth, and at a first approximation is expressed as:

$$\delta = \sqrt{\frac{1}{\pi f \sigma \mu}}$$

where

δ is the skin depth

f is the frequency of interest

σ is the conductivity of conductor

μ is the permeability of conductor

The above expressions suggest that the same series resistance produces higher attenuation if the characteristic impedance is lower. This also suggests that in case of parallel conductive planes, if the planes are put sufficiently close (in order to reduce the equivalent characteristic impedance of the planes), without any change in the material properties, the series AC resistance eventually may provide enough attenuation to suppress plane resonances.

The lossy grid model of Figures 1 and 2 was applied to simulate a pair of 25cm by 25cm parallel planes with 35 micron (one ounce) copper on either side, but with variable thickness of dielectric separation. The dielectric constant was assumed to be 4. The grid size was 20x20, providing at least 1GHz of useful upper limit for the model.

Figure 3 shows the magnitude and phase of self impedance, measured between the upper and lower planes at the center. As the dielectric thickness is reduced, the impedance profile becomes more smooth at high frequencies. There is another obvious advantage: the low-frequency impedance is also reduced inversely proportional to the dielectric thickness due to the increase of static capacitance. This helps to reduce the need for low-frequency bulk capacitors, but the real advantage is the complete suppression of plane resonances whenever the dielectric thickness is below about 8 microns (0.3 mils). It is also shown on the phase figures: with thin dielectrics, the phase of the self impedance becomes more resistive. Note also the slant of the self-impedance magnitude at high frequencies: this is due to the increase of skin resistance with the square root of frequency. Figure 4 proves our assumption that increasing series losses create a low-pass transfer function. While dielectric thickness above about 25 microns (one mil) yields a transfer function with noticeable peaks at high frequencies, a thickness of 2.5 microns (0.1 mils) creates a flat response, and even thinner dielectric separation provides a monotonic low-pass function. The series losses also increase

the upper frequency limit of the simulation model by reducing the reflections, and effectively creating a resistor rather then transmission line grid at high frequencies.

II. 3. Effect of dielectric thickness on the plane impedance with thin conductors

While the advantages of thin dielectrics are clear from the simulations results of Figures 3 and 4, it is unfortunately not practical to manufacture and handle a dielectric layer of a few micrometer or less thickness with the usual several micrometer or more copper layers. With a 0.25 microns (0.01 mil) dielectric layer the conductor layers may be about hundred times thicker.

To look at the other possible extreme, Figures 5 and 6 show the same structure under the same assumptions as Figures 3 and 4, except the conductive layer on both sides is assumed to be 0.25 microns (0.01 mils) copper. Note that the skin depth in copper at 1GHz is approximately 2 microns (0.08 mils), which is about eight times higher than the selected copper thickness. Hence the series loss resistance is less dependent on frequency. By comparing Figures 3-5 and Figures 4-6, we can see that the series losses of the 0.25-micron conductive layers still leave considerable peaking in the impedance profile with thick (>25 micron) dielectric layers.

In case of thin conductive layers, the high-frequency impedance does not drop inversely proportional to the plane separation, as one would expect based on the equivalent inductance between the planes. It is because the impedance now becomes limited by the series AC loss resistance. With the 0.025-micron (0.01 mils) copper conductors, the self-impedance profile is almost totally flat as soon as at about 10MHz the impedance of the static capacitance intercepts the series resistance. The higher series resistance also creates a stronger low-pass filtering.

On the other hand, using very thin conductive layers alone is not practical either, because the copper weight may be needed to handle the large DC currents in the systems. However, by using both thin dielectric and thin conductive layers, we can provide the necessary copper weight by stacking up several of these thin layers. At the same time this will further reduce the impedance, because of the parallel connection of individual plane pairs. A typical 50 micron dielectric separation with 35 micron (one ounce) copper has a

total thickness of 120 microns. If we used the 120 micron total thickness and we stacked up 240 pairs of 0.025 microns dielectrics with 0.025 microns conductive layers, we would end up with the same total thickness, same amount of total conductor weight on either side, and (neglecting the connecting impedance between the stacked layers) an approximately 25 micro ohm flat resistive impedance in the 10-1000MHz frequency range. However, to use multiple thin conductive and dielectric layers in large-size rigid PCBs, several technological problems have to be addressed first.

It is also clear that stacking power-ground plane pairs in parallel has most of its advantages if we already reach the resistive bottom of the impedance profile with the thin dielectrics. It is illustrated in Figure 7 that in the unsaturated range of the curves it is better (results in smoother impedance profile) to use one plane pair with thinner dielectrics as opposed to stack up several of them.

II. 4. Effect of dielectric losses on the plane impedance

The typical PCB materials have been optimized for low-loss signal transmission, and because of this, they do not provide sufficient suppression of plane resonances. If used only between the power/ground planes, intentionally high dielectric losses may be used. Figure 8 contains the real part and magnitude of the simulated self impedance at the center of a pair of 25cm by 25cm planes with a dielectric separation of 50 microns (2 mils). The impedance magnitude curves are placed on a zoomed frequency scale so that individual traces can be distinguished. The impedance magnitude curve show that a dielectric loss tangent of 0.3 or higher is sufficient to suppress almost completely the plane resonances.

III. Simulation models of power/ground planes in PDNs

In this section we look into some of the accuracy considerations of two modeling approaches: analytical plane expressions, and transmission-line grid models.

III. 1 Analytical plane model

One useful alternative to the bedspring equivalent circuit is the analytical impedance expression of the power/ground planes, that was originally derived for microwave resonators and patch antennas [9]. Not limited by a fixed grid of components, the analytical expression can be solved for any set of arbitrary points on the planes. The expressions yield the self and/or transfer impedances, and the computation may be very efficient [10].

The generic impedance between any two ports on the planes (assuming negligibly small port dimensions) is

$$Z_{ij}(\omega) = j\omega\mu h \sum_{n=0}^{\infty}\sum_{m=0}^{\infty} \frac{\chi_{mn}^{2}}{w_x w_y \left(k_n^{2} - k^{2}\right)} \cos\left(\frac{2m\pi x_i}{2w_x}\right)\cos\left(\frac{2n\pi y_i}{2w_y}\right)\cos\left(\frac{2m\pi x_j}{2w_x}\right)\cos\left(\frac{2n\pi y_j}{2w_y}\right)$$

given by:

where w_x and w_y are the dimensions of planes in the x and y directions, respectively
$\omega=2\pi f$ is the angular frequency
μ is the permeability of dielectric ($\mu=\mu_0=4\pi 10^{-7}$)
c is the speed of light, and for loss less structures,

$$\chi_{mn} = 1\ for\ m=0\ and\ n=0;\ \sqrt{2}\ for\ m=0\ or\ n=0;\ 2\ for\ m\neq 0, n\neq 0$$

$$k = \omega\sqrt{\varepsilon\mu} = \omega\sqrt{\varepsilon_r\varepsilon_0\mu_0} = \sqrt{\varepsilon_r}\frac{\omega}{c}$$

$$k_n^{2} = \left(\frac{m\pi}{w_x}\right)^{2} + \left(\frac{n\pi}{w_y}\right)^{2}$$

For structures with light losses, the imaginary part of k may represent the lossy nature: $k = k' - jk''$, where $k' = k$ above.

Though not limited by finite spatial granularity, there are two fundamental limitations to consider when we apply this formula to PDNs. First, the initial assumptions limit the validity of the expression to low-loss cases. Second, the analytical expression has a double infinite series, which for practical calculations must be truncated, so that instead of being infinite, we have to use finite n_max = N, and m_max = M.

The plane-impedance expression contains a double series of second-order terms. These second-order terms accurately describe the poles (peaks) in the impedance profile, and the frequencies of the peaks do not change as we add or remove terms. The minima of the impedance profile, however, do change as more terms are added to the series. More importantly, beyond the frequency of the last pole of the truncated series, as opposed to the inductive upslope of the plane impedance at high frequencies, the truncated series yields an impedance of capacitive down slope. Also for this reason, the spreading inductance of planes can be obtained from the expression only with large summation limits.

To show these effects, a pair of 25cm by 25cm square planes with a dielectric separation of 50 micron (2-mils) was simulated. Figure 9 shows the simulated self impedance at the corner of planes with different N=M summation limits. While the simulated impedance peaks line up for all values of N=M, the frequencies of minima vary with the summation limit. The bottom graph of Figure 9 shows that the frequency of the first minimum shifts in a range of almost 2:1.

III. 2 Transmission-line grid model

The bedspring model as defined in Figures 1 and 2 was used to study the effect of number of cells. With fixed physical plane dimensions, the frequency range of validity of the plane model is improved as the number of cells increases. A practical limit to the increase of cell number is the simulation run time. It was found that with HSPICE running on an UltraSparc60 machine, the runtime is below three minutes up to a grid size of 30x30.

To see the effect of grid granularity on the simulated poles and zeros, the self impedance profile of a pair of 25cm by 25cm planes with a dielectric separation of 50 microns (2 mils) was simulated with the lossy grid model. The dielectric constant was 4, and the grid granularity was stepped from 4x4 up to 30x30. The self impedance magnitude measured at the corner of the planes is shown in Figure 10.

It was found that both with the analytical plane model and with the lossy transmission-line grid, the frequency of the first minimum showed noticeable variation, while the second and third minima had successively lower sensitivity. Note that the lossy transmission line grid model results in almost the same 2:1 frequency variation of the first minimum as what we see with the analytical plane model.

IV. Simulated and measured results of test structures

IV. 1. 40 and 8 micron (1.6, and 0.3 mils) dielectric layers with a dielectric constant of 16.

Figures 11 shows the simulated and measured self impedances of a test board with dimensions of 50cm by 25cm with a dielectric separation between adjacent power-ground planes of 40 microns. The boards had six layers, four of those were arranged as power/ground plane pairs, located approximately 200 microns (8 mils) below the PCB surface. The dielectric constant was approximately 16 ([15], [16]). To allow the measurement of self and transfer impedances in various combinations, at every inch interval, a set of vias were connected separately to each plane. The measurements were done with the instrumentation and set up described in [7] and [8].

A standalone 8-micron (0.3 mils) sheet of copper-clad dielectric layer was also measured and simulated. The size of sheet was 45cm by 25cm with one ounce copper, and the self impedance was measured and simulated at one of the plane corners. Due to the difficulties of the probe connection to the standalone sheet, the measured and simulated impedances in Figure 12 differ more at high frequencies.

IV. 2. Thin dielectric and thin conductive layer

Thin dielectric and conductive layers can be manufactured by various thin-film processes ([17], [18]). A structure assuming a 10cm by 10cm size, 35 micron (one ounce) copper base, 0.2 micron silica dielectric layer and 0.5 micron aluminum layer on top was simulated with a lossy transmission-line grid of 20x20. The simulated self and transfer impedance magnitudes as well as the phase of the self impedances are shown in Figures 13. Note that the self impedance shows a square root of frequency increase at high frequencies because of the copper base, which is much thicker than the skin depth at 1GHz. The transfer impedance has a monotonic low-pass nature.

Conclusions

It was shown that thin dielectric layers in power distribution provide good suppression of plane resonances. When combined with thin conductive layers, a resistor-like flat self-impedance and low-pass transfer-impedance profiles can be created. Analytical plane-impedance expressions have a limitation due to the necessary truncation of the double infinite summation. Lossy transmission-line grid plane models can simulate power-ground planes with heavy losses, and show acceptable agreement with measured results.

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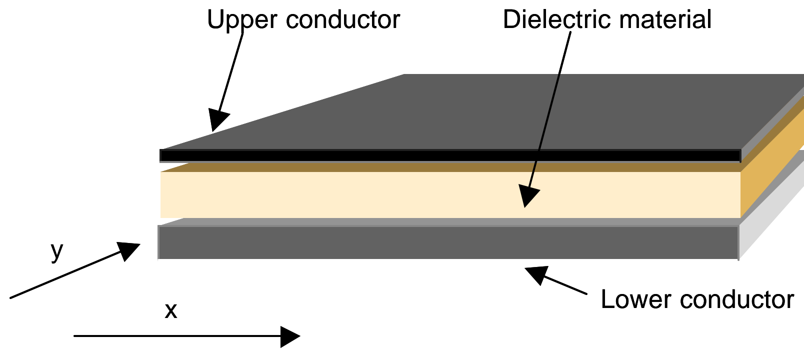
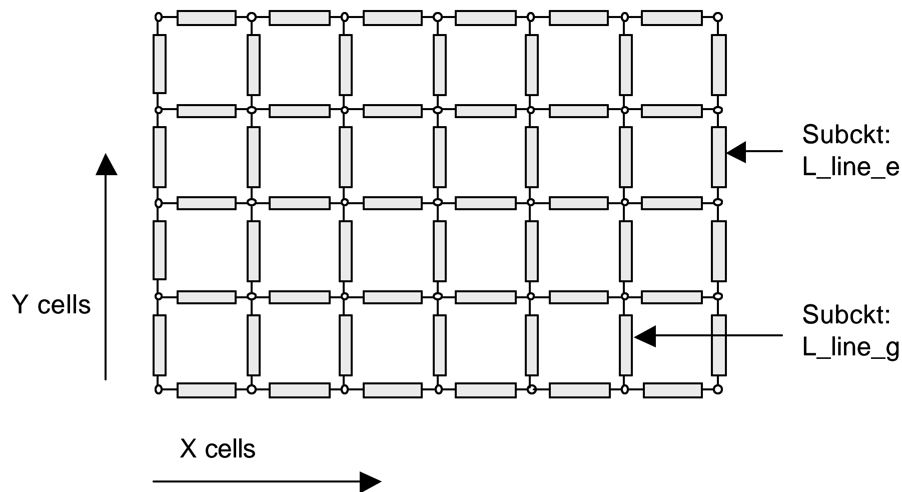
Figures:

Conductive plane pair with dielectric separation:



Grid subcircuit model:



Lossy subcircuit detail:

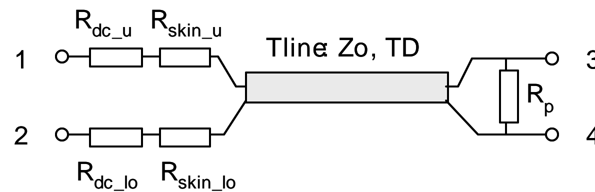


Figure 1: Lossy transmission-line grid model for power-ground plane simulations.

```
* Constants *
.param PI= 3.14159265
.param eps_nul= 0.00000000000885
.param mu_nul= '4*PI*0.0000001'


 *  Input data *
.param unit_length=0.0254 $ unit length in meters
.param x_cells=20 $ number of grid cells in x direction [-]
.param y_cells=20 $ number of grid cells in y direction [-]
.param grid_size='10/20' $ size of one grid cell [selected unit]
.param plane_sep=0.005 $ separation of planes [selected unit]
.param eps_rel=4 $ relative dielectric constant [-]
.param tan_delta=0.002 $ loss tangent of dielectrics [-]
.param u_cond_th=0.0012 $ thickness of upper conductor [selected unit]
.param u_sigma=5.8E7 $ conductivity of upper conductor [S/m]
.param lo_cond_th=0.0012 $ thickness of lower conductor [selected unit]
.param lo_sigma=5.8E7 $ conductivity of lower conductor [S/m]

 *  Derived data *
.param L_u= 'mu_nul*plane_sep*unit_length'
.param C_u= 'eps_nul*eps_rel*grid_size/plane_sep*grid_size*unit_length'
.param Zo_grid= 'sqrt(L_u/C_u)*sqrt(2)'
.param tpd_sq= 'sqrt(L_u*C_u)/sqrt(2)'
.param Rdc_u_grid = '1/(u_sigma * u_cond_th)'
.param Rs_u_grid = 'sqrt(PI*mu_nul/u_sigma)'
.param Rdc_lo_grid = '1/(lo_sigma*lo_cond_th)'
.param Rs_lo_grid = 'sqrt(PI*mu_nul/lo_sigma)'
.param cond_grid = '2*PI*tan_delta*tpd_sq/Zo_grid'

.subckt   L_line_g   1  2  3  4
   Rdc_u    1  5       Rdc_u_grid
   Rskin_u  5  6       'Rs_u_grid*sqrt(hertz)'
   Rdc_lo   2  7       Rdc_lo_grid
   Rskin_lo 7  8       'Rs_lo_grid*sqrt(hertz)'
   Tline    6  8  3  4  Z0=Zo_grid  TD=tpd_sq
   Rp_g     3  4       '1/cond_grid/hertz'
   Rdummyg  2  4       1E6
.ends    L_line_g

.subckt   L_line_e   1  2  3  4
   Rdc_u    1  5       '2*Rdc_u_grid'
   Rskin_u  5  6       '2*Rs_u_grid*sqrt(hertz)'
   Rdc_lo   2  7       '2*Rdc_lo_grid'
   Rskin_lo 7  8       '2*Rs_lo_grid*sqrt(hertz)'
   Tline    6  8  3  4  Z0='2*Zo_grid'  TD=tpd_sq
   Rp_e     3  4       '2/cond_grid/hertz'
   Rdummye  2  4       1E6
.ends    L_line_e
```

Figure 2.: User input and derived parameters for the HSPICE lossy transmission-line grid model.

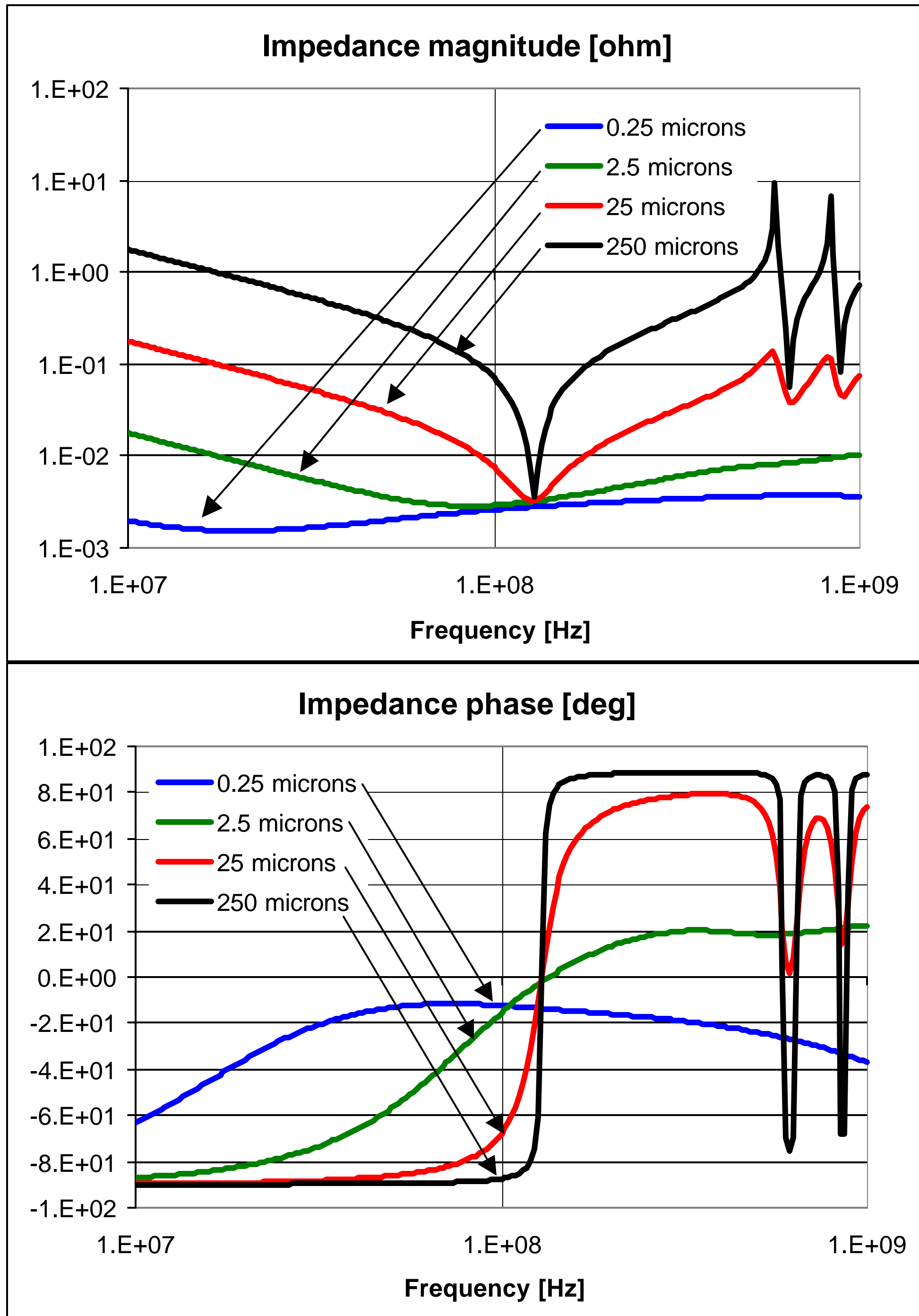


Figure 3.: Effect of dielectric thickness on the self impedance of a pair of 25cm by 25cm planes, with 35 micron copper on either side. The self impedance magnitude is measured at the center of planes.

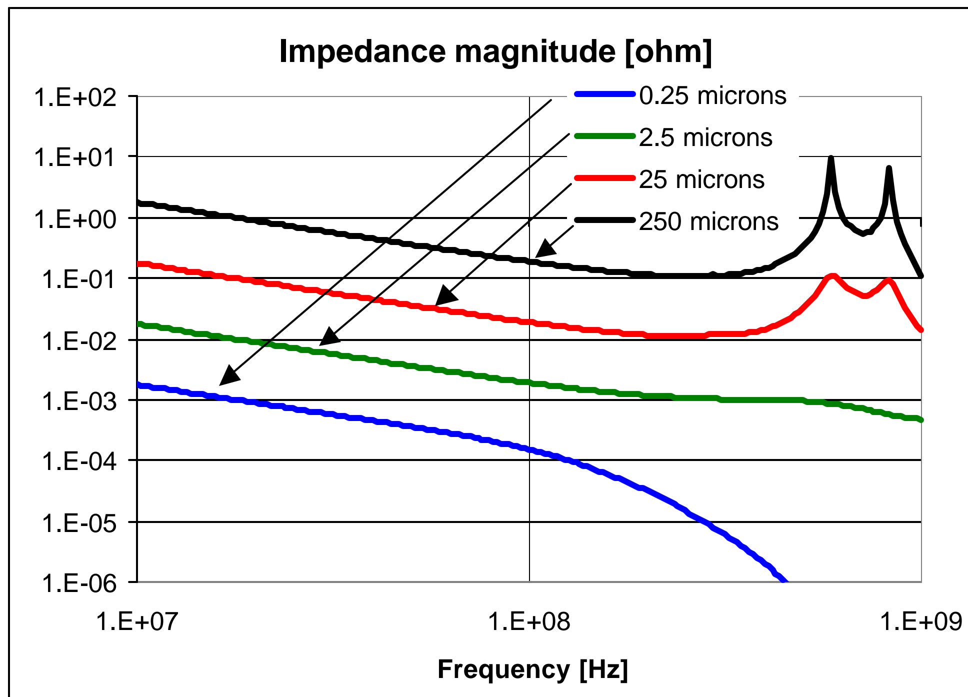


Figure 4.: Effect of dielectric thickness on the transfer impedance of a pair of 25cm by 25cm planes, with 35 micron copper on either side. The magnitude of the transfer impedance is measured between the center and one of the corners of the planes.

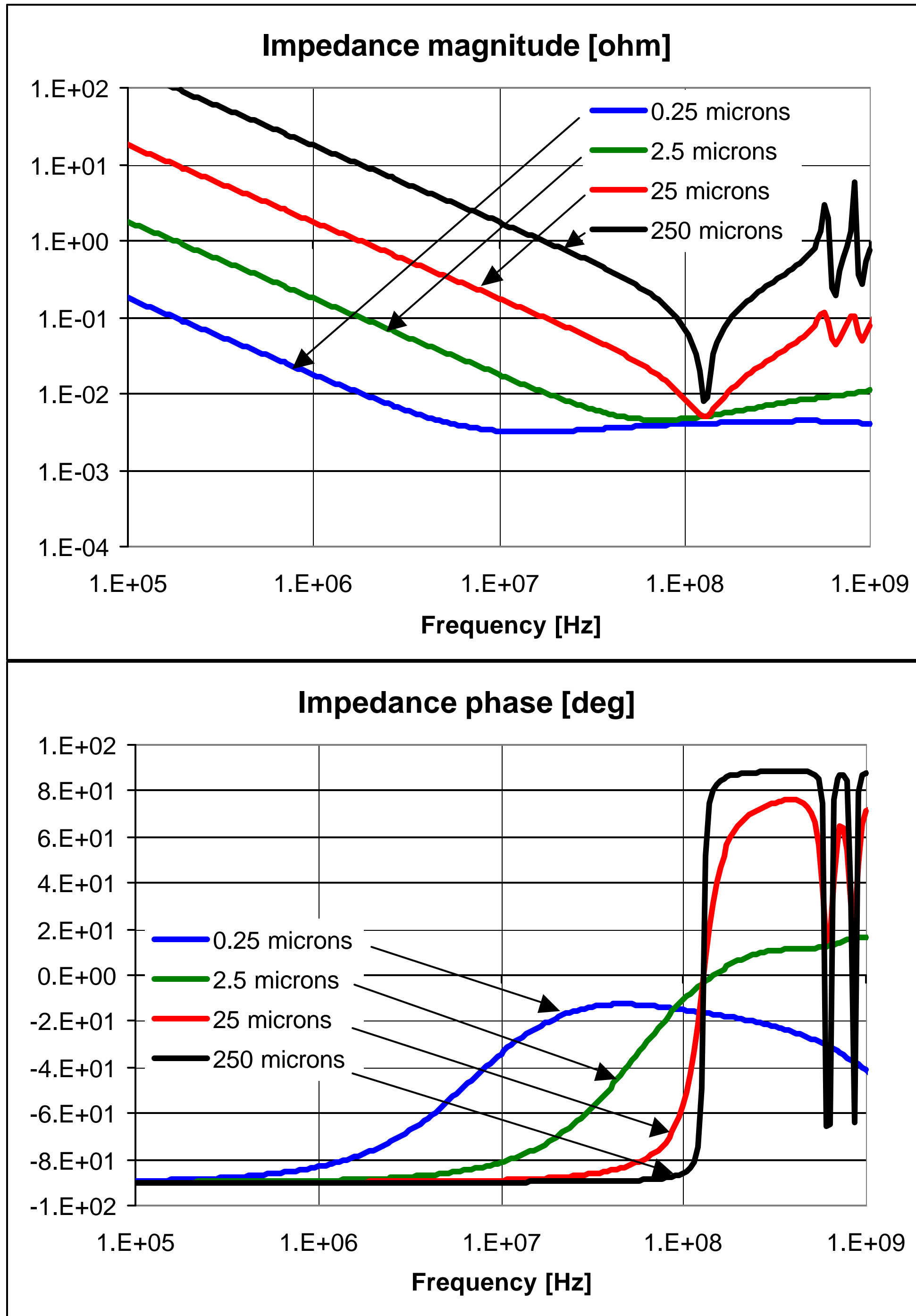


Figure 5.: Effect of dielectric thickness on the self impedance of a pair of 25cm by 25cm planes, with 0.25 micron copper on either side. The self impedance magnitude is measured at the center of planes.

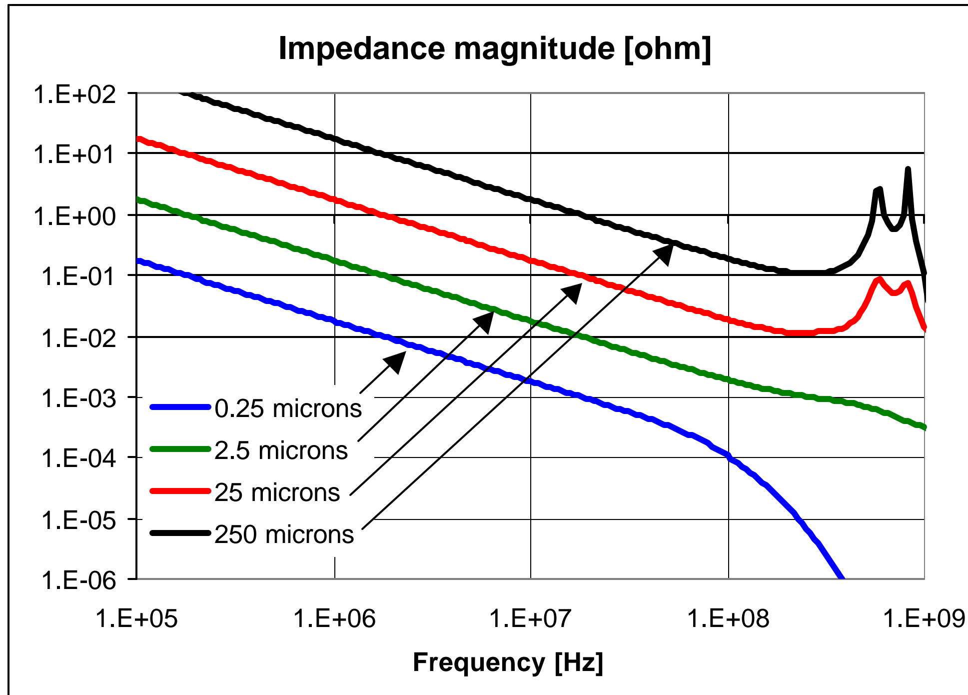


Figure 6.: Effect of dielectric thickness on the transfer impedance of a pair of 25cm by 25cm planes, with 0.25 micron copper on either side. The transfer impedance magnitude is measured between the two planes from the center to the corner.

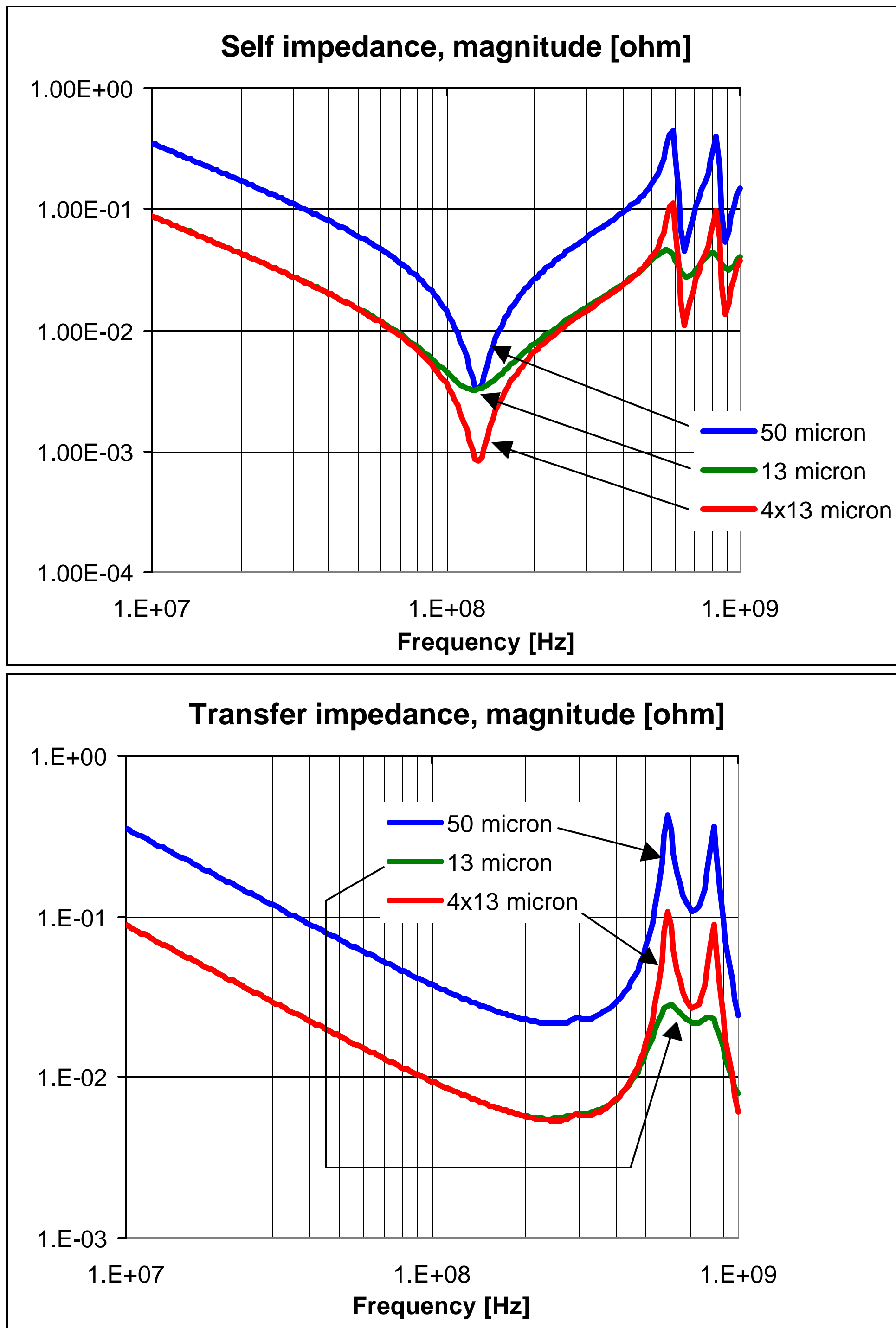


Figure 7.: Self and transfer impedance magnitude of a pair of 25cm by 25cm parallel planes with three different configurations: a) standalone pair with 50 micron dielectric separation, b) standalone pair with 13 micron dielectric separation, and c) four pairs of planes with 13 micron dielectric separation. The self impedance is measured between the planes at the center, transfer impedance is measured between the two planes from center to corner.

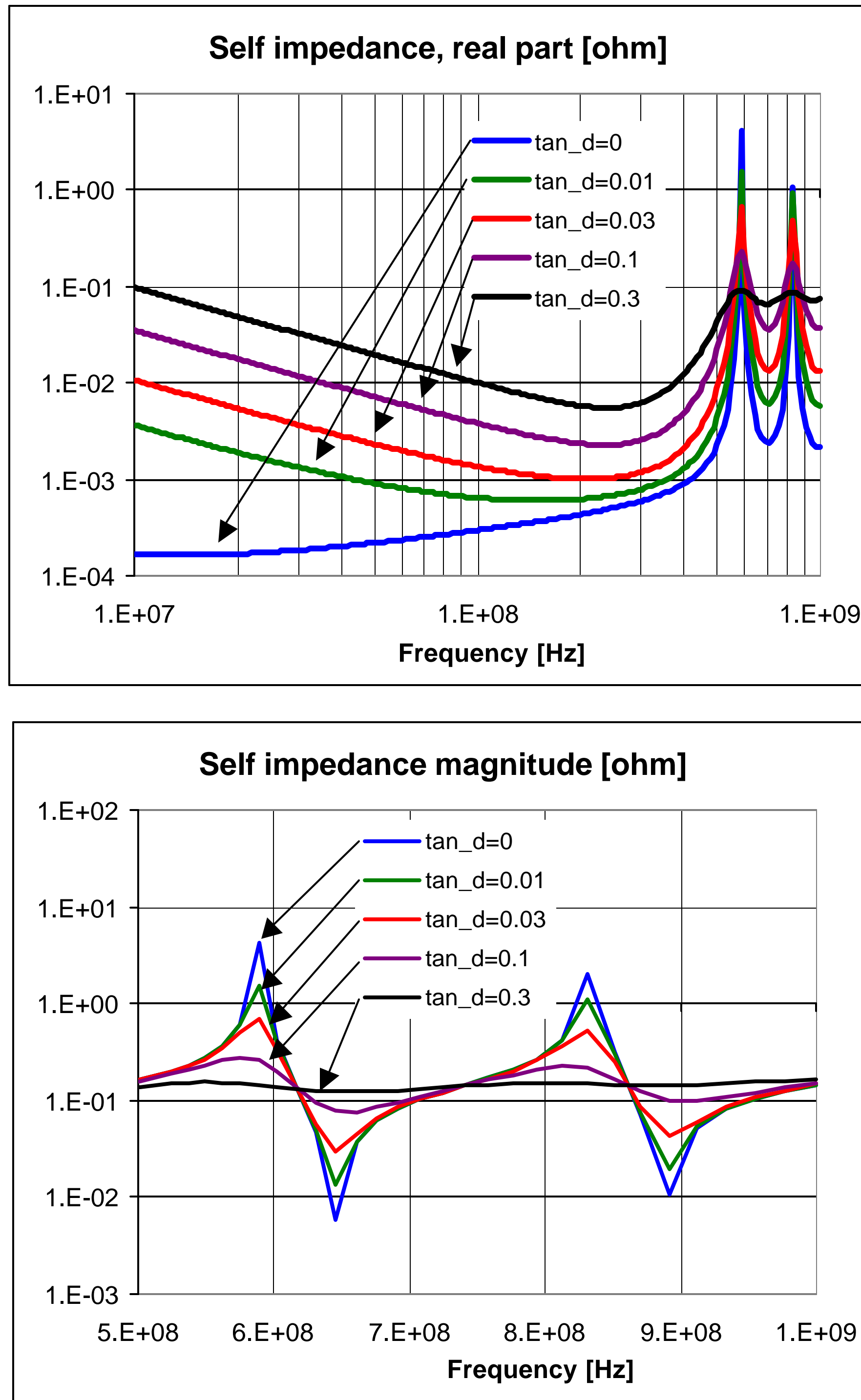


Figure 8.: Effect of dielectric losses on the real part and magnitude of self impedance measured at the center of a pair of 25cm by 25cm planes with a dielectric separation of 50 microns (2 mils), dielectric constant 4, and 35 micron (one ounce) copper .

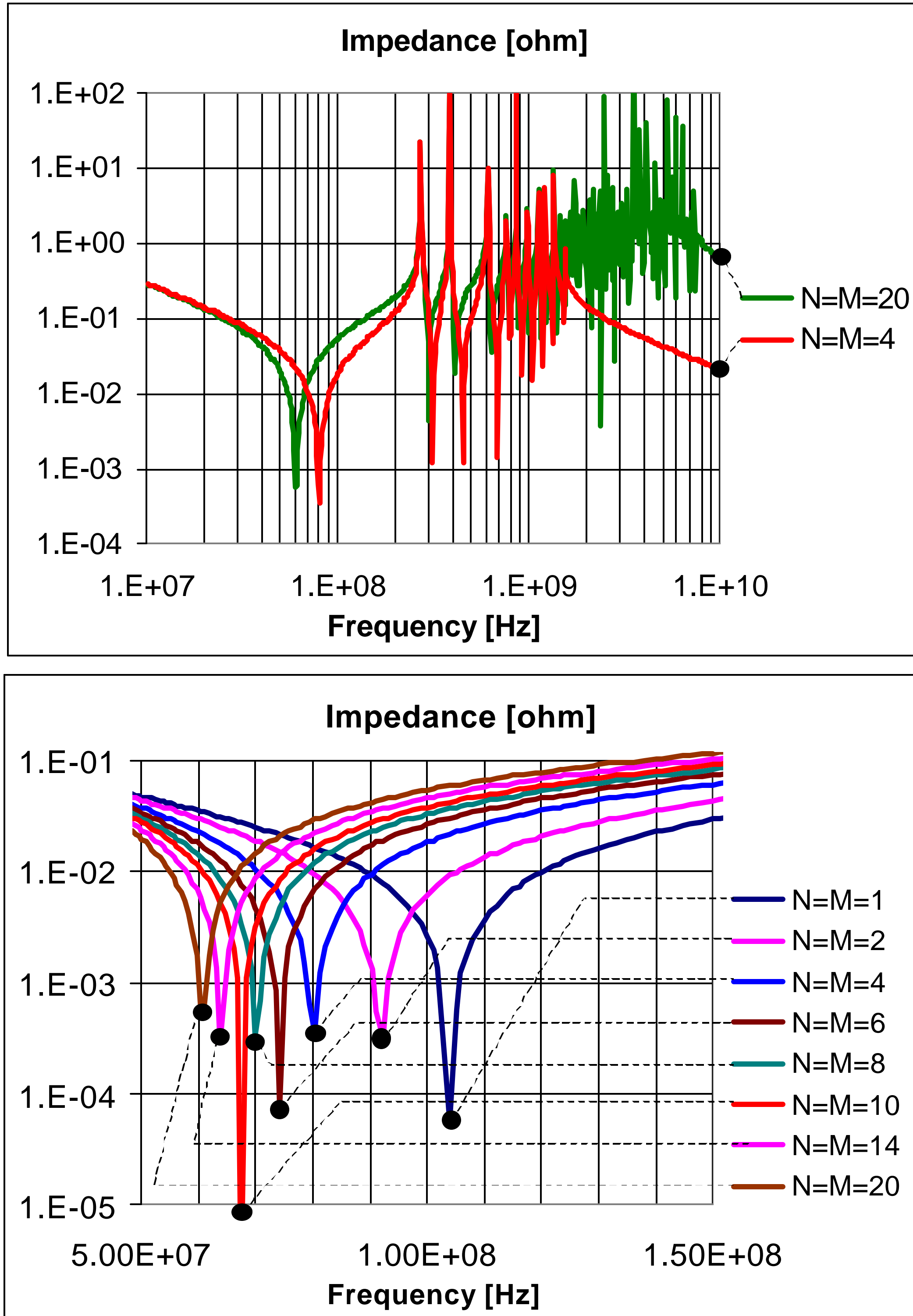


Figure 9.: Self impedance of a 25cm by 25cm pair of planes, with a dielectric separation of 50 microns (2 mils), dielectric constant of 4. Impedance is simulated by the analytical plane expression, at the corner of the planes. Top graph: full span of impedance with two different summation limits are shown, N=M=4, and N=M=20. Bottom graph: zoomed frequency scale around the first impedance minimum with multiple N=M limits.

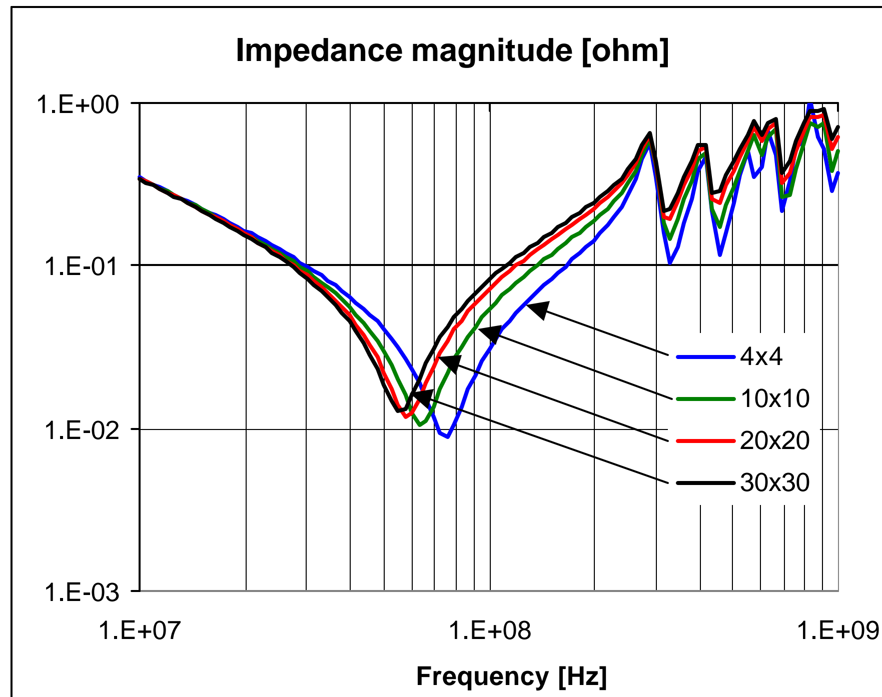


Figure 10.: Self impedance profile at the corner of a pair of 25cm by 25cm pair of planes with a dielectric separation of 50 microns (2 mils), dielectric constant of 4. The square planes were modeled by a lossy transmission line grid with 4x4, 10x10, 20x20, and 30x30 cells.

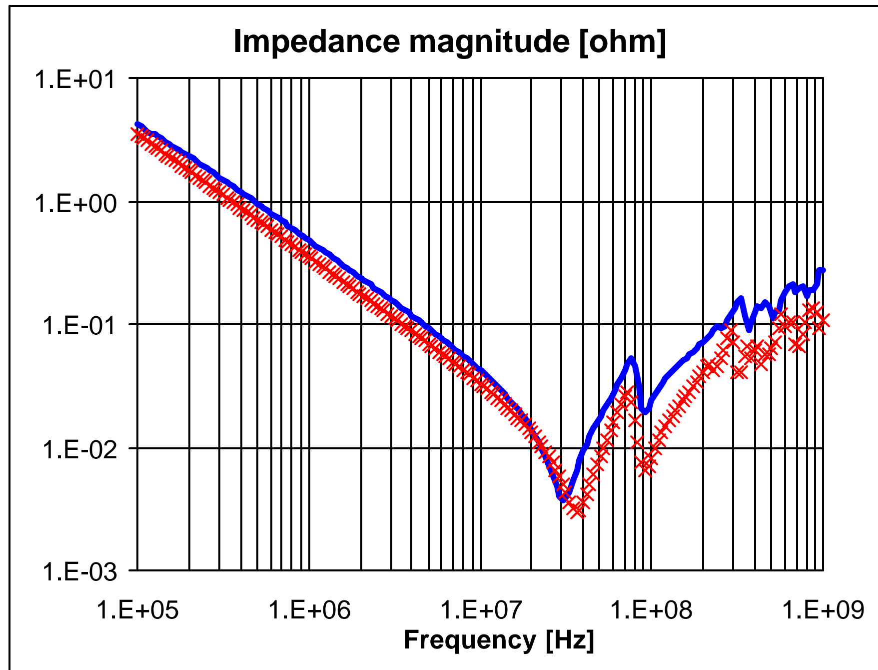


Figure 11.: Measured and simulated self impedance of a 50cm by 25cm test board with 40 micron (1.6mil) dielectrics, dielectric constant of 16. Solid line: measured, crosses: simulated. The probe point was 12.5cm in each direction from the corner of the planes.

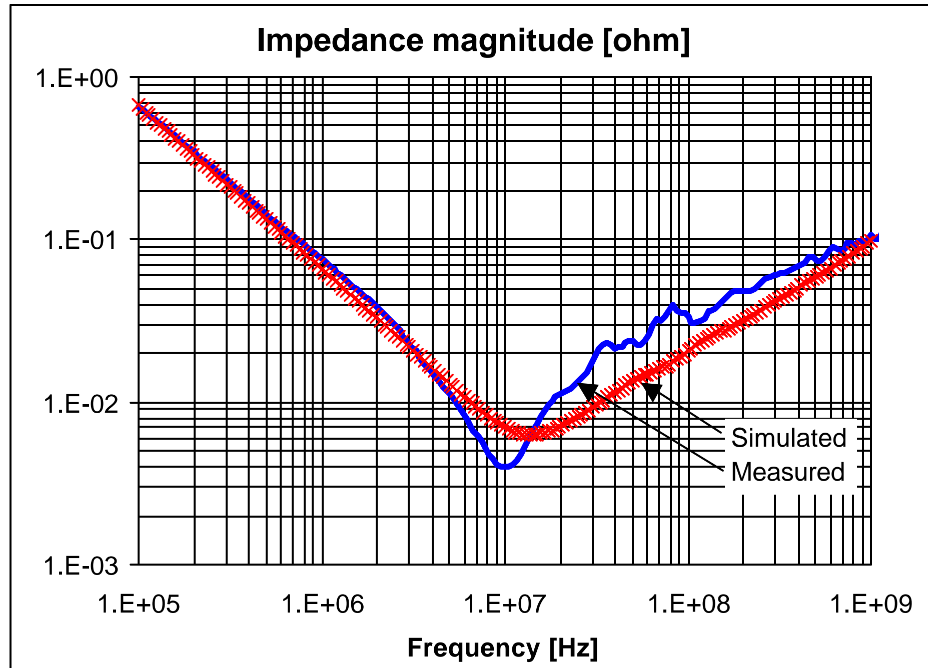


Figure 12.: Simulated and measured self impedance magnitude, measured at the corner of a 45cm by 25cm laminate with 8 micron (0.3mil) dielectric thickness and 35 micron (one ounce) copper on each side.

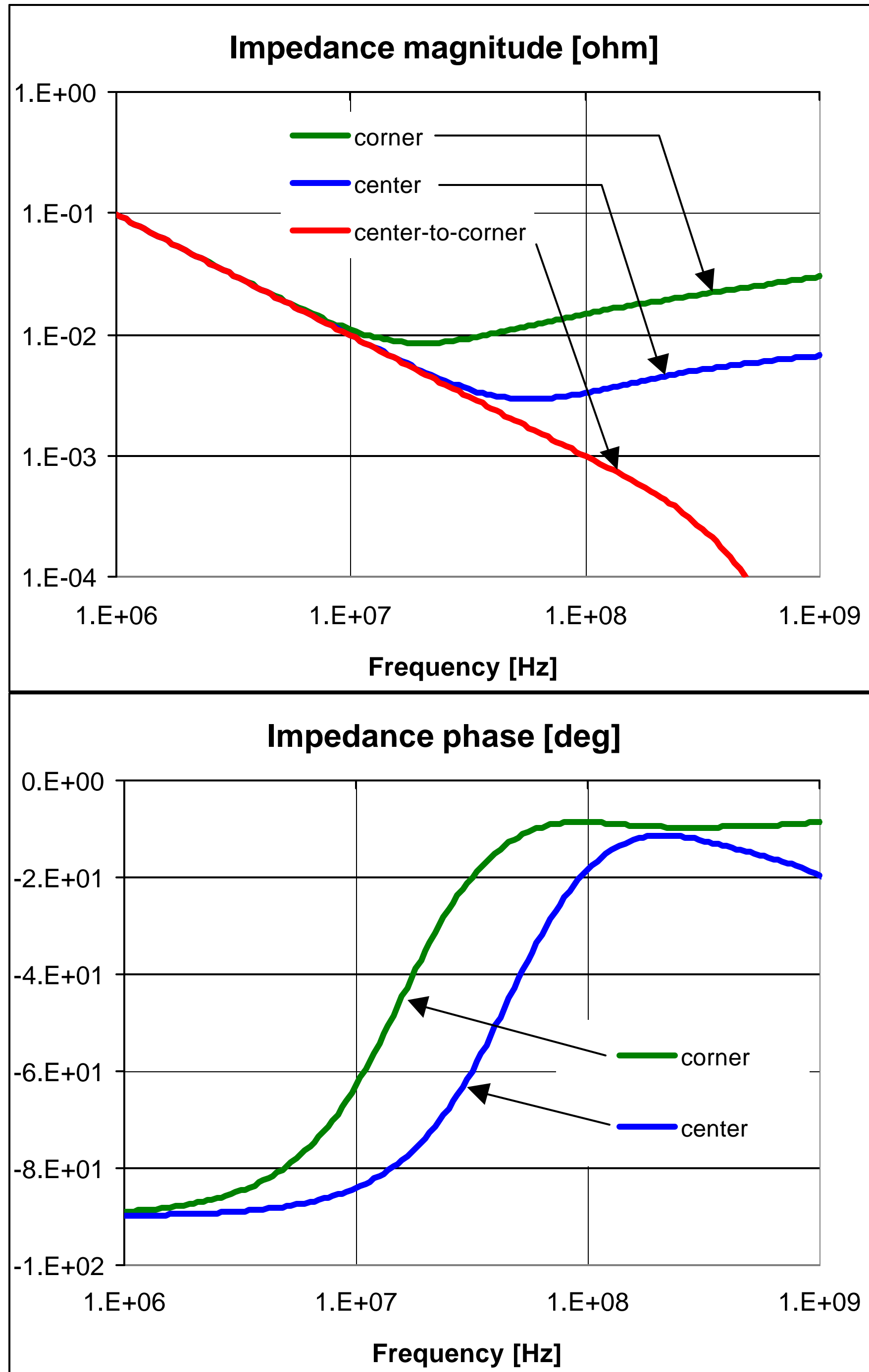


Figure 13: Simulated impedances of a 0.2 micrometer silica layer on a 35-micron copper base, with 0.5 micrometer aluminium metallisation on the top. The assumed dimensions are: 10cm by 10cm square. Three impedance magnitudes are shown: self-impedance measured at the corner, self-impedance measured at the center, and transfer impedance measured between the center and one of the corners. The phase is shown for the self impedances only.

Figure captions:

Figure 1: Lossy transmission-line grid model for power-ground plane simulations.

Figure 2.: User input and derived parameters for the HSPICE lossy transmission-line grid model.

Figure 3.: Effect of dielectric thickness on the self impedance of a pair of 25cm by 25cm planes, with 35 micron copper on either side. The self impedance magnitude is measured at the center of planes.

Figure 4.: Effect of dielectric thickness on the transfer impedance of a pair of 25cm by 25cm planes, with 35 micron copper on either side. The magnitude of the transfer impedance is measured between the center and one of the corners of the planes.

Figure 5.: Effect of dielectric thickness on the self impedance of a pair of 25cm by 25cm planes, with 0.25 micron copper on either side. The self impedance magnitude is measured at the center of planes.

Figure 6.: Effect of dielectric thickness on the transfer impedance of a pair of 25cm by 25cm planes, with 0.25 micron copper on either side. The transfer impedance magnitude is measured between the two planes from the center to the corner.

Figure 7.: Self and transfer impedance magnitude of a pair of 25cm by 25cm parallel planes with three different configurations: a) standalone pair with 50 micron dielectric separation, b) standalone pair with 13 micron dielectric separation, and c) four pairs of planes with 13 micron dielectric separation. The self impedance is measured between the planes at the center, transfer impedance is measured between the two planes from center to corner.

Figure 8.: Effect of dielectric losses on the real part and magnitude of self impedance measured at the center of a pair of 25cm by 25cm planes with a dielectric separation of 50 microns (2 mils), dielectric constant 4, and 35 micron (one ounce) copper .

Figure 9.: Self impedance of a 25cm by 25cm pair of planes, with a dielectric separation of 50 microns (2 mils), dielectric constant of 4. Impedance is simulated by the analytical plane expression, at the corner of the planes. Top graph: full span of impedance with two different summation limits are shown, N=M=4, and N=M=20. Bottom graph: zoomed frequency scale around the first impedance minimum with multiple N=M limits.

Figure 10.: Self impedance profile at the corner of a pair of 25cm by 25cm pair of planes with a dielectric separation of 50 microns (2 mils), dielectric constant of 4. The square planes were modeled by a lossy transmission line grid with 4x4, 10x10, 20x20, and 30x30 cells.

Figure 11.: Measured and simulated self impedance of a 50cm by 25cm test board with 40 micron (1.6mil) dielectrics, dielectric constant of 16. Solid line: measured, crosses: simulated. The probe point was 12.5cm in each direction from the corner of the planes.

Figure 12.: Simulated and measured self impedance magnitude, measured at the corner of a 45cm by 25cm laminate with 8 micron (0.3mil) dielectric thickness and 35 micron (one ounce) copper on each side.

Figure 13: Simulated impedances of a 0.2 micrometer silica layer on a 35-micron copper base, with 0.5 micrometer aluminium metallisation on the top. The assumed dimensions are: 10cm by 10cm square. Three impedance magnitudes are shown: self-impedance measured at the corner, self-impedance measured at the center, and transfer impedance measured between the center and one of the corners. The phase is shown for the self impedances only.

Biography:

Istvan Novak (M'83-SM'90-FM'98) received the M.SD. and D. Sci degrees in electronics engineering from the Technical University of Budapest, Budapest, Hungary, in 1976 and 1979, respectively, and Ph.D. degree from the Hungarian Acadamy of Sciences in 1989.

He was a Research Assistant from 1976 to 1978 and Assistant Lecturer from 1979 to 1983 at the Department of Microwave Telecommunications, Technical University of Budapest, Budapest, Hungary. In 1983-1984 and 1989-1991 he was a Project Engineer at Design Automation, Inc., Lexington, MA. In 1985-1989 he was Senior Lecturer, in 1992-1997 he was Associate Professor at the Department of Microwave Telecommunications, Technical University of Budapest. He is currently Signal Integrity Senior Staff Engineer at SUN Microsystems in Burlington, MA. His current activities cover signal-integrity design of high-speed serial and digital buses, as well as power distribution.
In 1998 Dr. Novak was elected to the Fellow of IEEE for his contributions to the theory and practice of radio-frequency monitoring techniques, and of measuring and simulation of high-speed digital systems.