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Low Cost and High Performance UPQC with Four-Switch Three-Phase Inverters

Quoc-Nam Trinh* and Hong-Hee Lee†

Abstract – This paper introduces a low cost, high efficiency, high performance three-phase unified power quality conditioner (UPQC) by using four-switch three-phase inverters (FSTPIs) and an extra capacitor in the shunt active power filter (APF) side of the UPQC. In the proposed UPQC, both shunt and series APFs are developed by using FSTPIs so that the number of switching devices is reduced from twelve to eight devices. In addition, by inserting an additional capacitor in series with the shunt APF, the DC-link voltage in the proposed UPQC can also be greatly reduced. As a result, the system cost and power loss of the proposed UPQC is significantly minimized thanks to the use of a smaller number of power switches with a lower rating voltage without degrading the compensation performance of the UPQC. Design of passive components for the proposed UPQC to achieve a good performance is presented in detail. In addition, comparisons on power loss, overall system efficiency, compensation performance between the proposed UPQC and the traditional one are also determined in this paper. Simulation and experimental studies are performed to verify the validity of the proposed topology.

Keywords: Unified power quality conditioner, Four-switch inverter, Low cost, Harmonic compensation

1. Introduction

The intensive use of power electronics devices and nonlinear loads such as diode rectifiers, adjustable speed motor drives, and switching power supplies leads to the injection of a large amount of harmonic currents into the power distribution systems. Harmonic currents cause various severe impacts on power systems such as voltage distortions, increasing losses and heat on networks, malfunction of electronic equipment, and degrading the power quality of networks. Due to these issues, various international standards such as IEEE 519-1992 [1] or IEC 61000-3-2 [2] have been published to restrict the amount of harmonic currents injected into distribution networks by nonlinear loads, where the total harmonic distortion (THD) of load current is regularly limited within 5% at the rated power condition. Meanwhile, the THD of the voltage harmonics in the low voltage distribution system (<1kV) is also restricted within 5% according to IEEE 519-1992 or EN 50160 standards [3]. As a consequence, to comply with those harmonic standards, installing power filters and custom devices to compensate current harmonics and improve the power quality becomes a feasible solution and mandatory requirement for both network operators and end users.

Various kinds of custom power devices have been proposed and developed in the literature: Passive filters [4], shunt active power filters (APFs) [5, 6], and hybrid APFs [7] are used to mitigate current harmonics. Meanwhile, series APFs [8] and dynamic voltage restorers [9] are used for voltage distortion and voltage sag compensation. These compensating devices are effective solutions, but most of them can only deal with one or two power quality issues. Recently, unified power quality conditioners (UPQCs) have been introduced as a powerful and advanced custom power device to simultaneously deal with various current and voltage related problems. An UPQC, composed of shunt and series APFs, is capable of compensating voltage distortions at the supply side as well as current harmonics at the load side to make the load voltage and the supply current become pure sinusoidal. Control of UPQC for harmonic compensation have been widely investigated and various kind of control techniques have been introduced such as hysteresis control [10-15], fuzzy logic control [16], artificial neural network [17, 18], particle swarm optimization-based control [19], resonant control [20], etc.

In spite of exhaust researches on UPQC control system, high cost and complexity of control system still restrict the wide application of UPQC in practice, especially in medium and high voltage systems because of some reasons: 1) A typical UPQC topology for three-phase system is composed of twelve power switches, which lead to a high cost of an UPQC system. 2) The high DC-link voltage, regularly larger than the peak-to-peak value of the supply voltage, not only causes higher power losses on the UPQC system but also requires high voltage switching devices. 3) Complex control systems with multi-stage

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control and a large number of sensors are regularly required for the conventional UPQC control system [11], [12]. In order to reduce the complexity of the UPQC control system, several novel control approaches have been developed by omitting the harmonic detectors and reducing the number of sensors in system [13-15, 20]. Even though the suggested control approaches can improve the control performance of UPQC with a simpler hardware and control system, a high DC-link voltage is still required and the high cost problem of the UPQC system cannot be solved in those methods. In [21], a modified three-phase UPQC with reduced DC-link voltage is introduced. The suggested topology has a low operating DC-link voltage, but it has several limitations: 1) Due to the use of hysteresis controllers, the control performance is not effectively improved. 2) Comparisons on power loss and system efficiency of the proposed topology with those of the conventional UPQC are not clearly investigated. 3) The number of switching devices is not reduced compared to the conventional UPQC. In order to reduce the number of switching devices in the UPQC, the four-switch three-phase inverters (FSTPIs) can be considered to replace the traditional three-phase inverters. However, in case that the FSTPI instead of the traditional three-phase inverters is applied to the UPQC system without any modification, the DC-link voltage of the UPQC will increase twice [22]. In addition, because one phase leg of FSTPI is the mid-point of two capacitors, the inherent variation of these two capacitor voltage badly affects the performance of the UPQC.

To overcome those issues, this paper introduces a new topology to apply the FSTPI to the UPQC without degrading control performance. A new topology for three-phase UPQC includes two FSTPIs and an extra capacitor in series with the shunt APF of the UPQC. The proposed topology shows remarkable advantages compared to the traditional UPQC: 1) By employing two FSTPIs for both shunt and series APFs in the UPQC, the number of switching devices is reduced from twelve to eight, which results in the cost reduction of the UPQC system. 2) By adding an extra capacitor in series with the shunt APF, the DC-link voltage using in the proposed UPQC is significantly decreased compared to that of the traditional one, which leads to the reduction of both the power losses and the voltage ratings for the power switches on UPQC. 3) A simple system with a minimum number of sensors is proposed to improve control performance of the UPQC. Design of passive components for the proposed UPQC to achieve a good performance is presented in detail. Simulation and experimental studies are performed to verify the validity of the proposed topology.

This paper is organized as follows. Section 2 depicts the hardware configuration of the conventional and proposed UPQC topologies. Section 3 describes the design of passive components for the proposed UPQC system. In Section 4, the control strategy for proposed UPQC topology is presented. Section 5 shows simulation results of both the traditional and proposed UPQCs. Section 6 corroborates the expected features of the proposed UPQC topology through experimental results. Section 7 presents the conclusions of this study.

2. Proposed UPQC Topology

2.1 Configuration of conventional three-phase UPQC

Fig. 1 shows the configuration of the traditional three-phase UPQC, which consists of two voltage source inverters connected back-to-back through a common DC-link capacitor, where one inverter is the shunt APF and another inverter is the series APF. The series APF is connected in series between the supply and the load through a series transformer. Meanwhile, the shunt APF is connected in parallel with the loads through an inductor L_{pf}. A LC (L_f,C_f) filter is connected at the ac output voltage of the series APF to eliminate high frequency switching ripples. In Fig. 1, the traditional UPQC has a large number of power switching devices, i.e., twelve devices. In addition, to ensure a proper operation of the UPQC, the voltage across the common DC-link capacitor must be higher than peak-to-peak value of supply voltage. Besides, in order to achieve the harmonic voltage and current compensation, a complex control system and a large number of sensors at v_S , i_L , v_{Sr} , i_F , and V_{dc} are generally required [8-11]. These problems result in a high system cost of UPQC and limit the application of UPQC in practice.

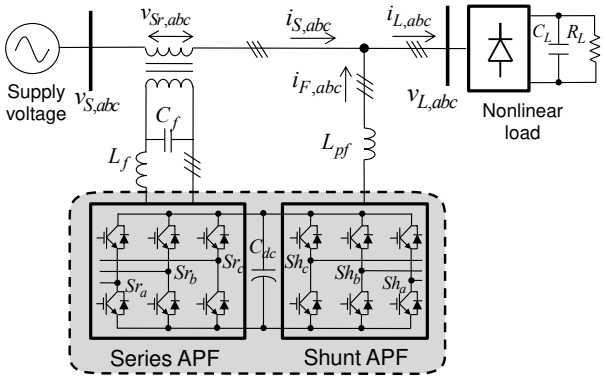

Fig. 1. Configuration of the typical three-phase UPQC.

2.2 Proposed three-phase UPQC

In order to overcome the high cost issue of the traditional three-phase UPQC, we propose three-phase UPQC by using FSTPI as shown in Fig. 2. Because the proposed UPQC is composed of two FSTPIs, the total number of switching devices is reduced from twelve in traditional topology to eight switches in the proposed system. In addition, the traditional UPQC topology is

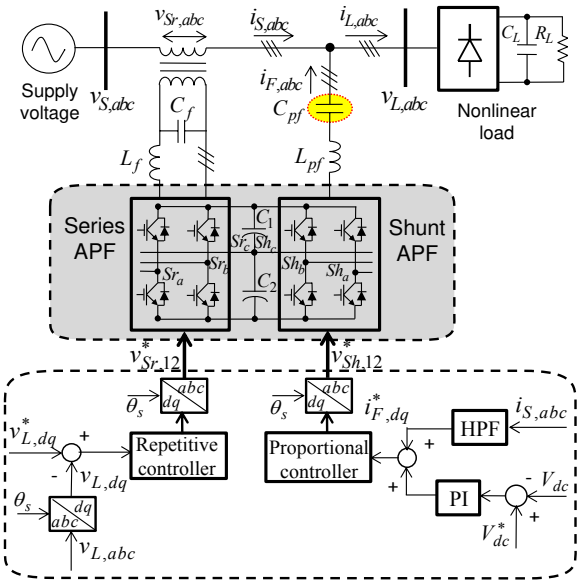

Fig. 2. Configuration of the proposed three-phase UPQC and its control strategy.

modified by adding the extra capacitor (C_{pf}) in series with the filter inductor (L_{pf}) of the shunt APF. This extra capacitor takes three major roles: 1) C_{pf} absorbs the fundamental component of the supply voltage, so that no fundamental voltage is imposed on shunt APF and the required DC-link voltage is greatly reduced. 2) C_{pf} and L_{pf} combine and operate as a passive filter to sink a specific (regularly the fifth or seventh) harmonic current. 3) C_{pf} can also supply a part of reactive power required by loads. As a consequence, the use of C_{pf} allows reducing the DC-link voltage as well as supporting the shunt APF to compensate both harmonic current and reactive power. Design of passive components in the proposed UPQC plays a vital role to achieve a good performance of the UPQC. This content will be discussed in detail in section 3. In addition, to further enhance the compensation performance of the proposed UPQC, an advanced control strategy is developed as shown in Fig. 2: The repetitive controller is employed in the voltage control scheme for the series APF and a proportional controller is adopted in the current control loop of the shunt APF. Analysis and design of the voltage and current controllers are described in detail in section 4.

3. Design of Passive Components for Proposed UPQC Topology

The passive components for UPQC include the inductor L_{pf}, the capacitor C_{pf}, the LC filter of the series APF, and the DC-link capacitor C_{dc}. They are designed as following:

3.1 Design of L_{pf} and C_{pf}

In Fig. 2, a passive filter, made of C_{pf} and L_{pf}, can eliminate the specific harmonic current generated by nonlinear loads. In this paper, C_{pf} and L_{pf} are tuned to absorb the seventh order harmonic current (n_1=7) instead of the fifth harmonic to reduce the volume and cost of C_{pf} and L_{pf} [23]. The resonant frequency of the passive filter ω_{res1} is defined as following:

$$\omega_{res1} = n_1(2\pi f_s) = \frac{1}{\sqrt{L_{pf}C_{pf}}}, \tag{1}$$

where $f_s = 50\,Hz$ denotes the fundamental frequency of system.

In addition, C_{pf} also supplies a part of reactive power required by the loads, which is calculated as

$$Q_c = (V_{l-l})^2(2\pi f_s)C_{pf}, \tag{2}$$

where $V_{l\text{-}l}$ =190V is the RMS value of the line-to-line voltage in this paper.

From (2), we can see that a higher value of C_{pf} provides a larger amount of Q_c. However, if Q_c is larger than the consumed reactive load power, overcompensation happens. In that case, the current flow into the shunt APF ($i_{F,abc}$) is significantly increased, which causes shunt APF oversized. Furthermore, a large C_{pf} makes the UPQC controller expensive and bulky. Therefore, it is important to determine the suitable value of C_{pf}. Fortunately, authors in [23] introduce the optimal C_{pf} to be 25% of the base capacitance of the system capacitance C_b which supplies the rated load power. C_b is defined as following:

$$\begin{aligned} Z_b &= \frac{(V_{l-l})^2}{P_L} \\ C_b &= \frac{1}{(2\pi f_s)Z_b} \end{aligned}, \tag{3}$$

where P_L = 5 kW is the rated load power.

$$C_f = 0.25C_b = 76.69\,\mu F \quad . \tag{4}$$

A closest commercial capacitance is chosen, i.e., C_{pf} = 75 μF.

From (1), we can obtain L_{pf} as

$$L_{pf} = 1/\omega_{res1}^2 C_{pf} = 2.756\,mH\,. \tag{5}$$

Then, a commercial inductor with the inductance value of L_{pf} = 2.8 mH is selected.

3.2 Design of LC filter (L_f and C_f)

The LC filter is used to suppress the switching noise of series APF. Since the series APF is used to compensate higher harmonic voltages than the typical inverter output

frequency, the resonant frequency of the *LC* filter should be sufficiently high not to degrade the performance of the UPQC. In this study, we assume that the highest harmonic voltage order contained in the source voltage is 13th (n_2=13), which corresponds to 650 Hz in 50 Hz system. In this case, the resonant frequency of the *LC* filter can be selected to be four times larger than the highest considering harmonic frequency [5].

$$\omega_{res2} = 4n_2(2\pi f_s) = \frac{1}{\sqrt{L_f C_f}}, \quad (6)$$

As shown in (6), there are countless options to select C_f and L_f. When the volume and cost of the filter are considered as dominant factors in design, C_f is generally selected to be less than 5% of the base value C_b for volume and cost optimization [5]. In this paper, C_f is selected as 4% of C_b:

$$C_f = 0.04C_b = 12.27\,\mu F \quad . \quad (7)$$

A closest commercial capacitance available on the market is selected, i.e., $C_f = 12\,\mu F$.

From (6), L_f is determined as

$$L_f = 1/\omega_{res1}^2 C_f = 0.48\,mH \; . \quad (8)$$

So, we choose L_f=0.5 mH.

3.3 Selection of the DC-link voltage level and DC-link capacitor

It is necessary to determine the DC-link voltage (V_{dc}) before selecting the value of DC-link capacitor C_{dc}. In order to choose V_{dc} properly, we need to know the supply voltage level. In this paper, three-phase phase voltage is selected as 110V RMS. Then, the peak-to-peak value of phase voltage becomes 311V. In case of the traditional UPQC, the DC-link voltage is higher than the peak-to-peak value of the phase voltage to ensure a proper operation of the shunt APF [24]. Hence, the reference DC-link voltage is properly selected as 350 V in the traditional UPQC.

In contrast, the DC-link voltage of the proposed UPQC becomes much lower than that of traditional topology thanks to the use of capacitor C_{pf}. In fact, the selection of DC-link voltage for the proposed UPQC is not a straightforward task because there is no lower restriction for this value. However, we have a constraint to select this value: If the DC-link voltage is low, the power losses and switching noises can be reduced, but the harmonic compensation performance is degraded at the meantime. On the other hand, if the DC-link voltage is high, the control performance is improved, but the power losses and switching noises are increased. In addition, an appropriate DC-link voltage also depends on the harmonic currents in the load current and the values of L_{pf} and C_{pf} [7]. By using the method in [7], we select the DC-link voltage to be 100V for the proposed UPQC.

Capacitance of the DC-link capacitor should be large enough to suppress the voltage fluctuation on the DC-link under the load variation. In this paper, the maximum allowable voltage variation is selected as 3% of the DC-link voltage, i.e., $\Delta V_{dc} = 0.03V_{dc}$ according to the selection guideline in [25]. If the DC-link voltage is varied with the value of ΔV_{dc} when the load is changed from 50% to full load, C_{dc} is calculated as following:

$$C_{dc} = \frac{3L_s(I_{rated}^2 - I_{rated}^2/4)}{2\Delta V_{dc}(V_{dc})^2} = 1083\,\mu F \; , \quad (9)$$

where I_{rated}=16.7A is the current rating of load.

In the proposed UPQC, two capacitors are connected in series, so the capacitance of each capacitor is twice of the determined value in (9). From (9), the closest commercial capacitance available on the market is selected, i.e., $C_1 = C_2 = 2C_{dc} = 2200\,\mu F$.

We summarize all system parameters in Table 1 including the designed parameters.

Table 1. System parameters

	Parameters	Value
Supply voltage	Fundamental voltage $V_{l\text{-}l}$ (*RMS*)	190 V
	Nominal grid frequency f_s	50 Hz
	5th harmonic voltage	7%
	7th harmonic voltage	4%
Loads	Diode rectifier load R_L	10 Ω
	Rating power P_L	5 kW
DC-link	Reference voltage for conventional UPQC V_{dc}^*	350 V
	Reference voltage for proposed UPQC V_{dc}^*	100 V
	Capacitance $C_1 = C_2 = 2C_{dc}$	2200 μF
Passive filter	Inductance value of L_{pf}	2.8 mH
	Capacitance value of C_{pf}	75 μF
Series APF	*LC* filter inductance L_f	0.5 mH
	LC filter capacitance C_f	12 μF
	Damping resistance R_f	0.2Ω
	Switching frequency f_{sw}	5 kHz

4. Control Strategy for proposed UPQC

4.1 Control of the shunt APF

The passive filter has been designed to mitigate seventh harmonic current, and the remaining harmonic currents can be sufficiently filtered by an appropriate control strategy in the shunt APF. In addition, the shunt APF also has a responsibility to maintain the common DC-link voltage in a stable condition. As a result, the control strategy includes two parts: The harmonic current compensation and the DC-link voltage regulation as shown in Fig. 3. Unlike the complex control scheme in the shunt APF of the traditional

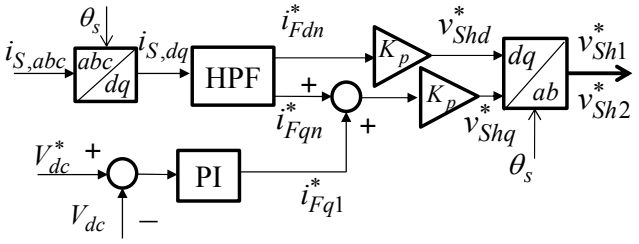

Fig. 3. Control scheme for the shunt APF.

UPQC, which requires information of load current, shunt APF current, and DC-link voltage [8], the control strategy in Fig. 3 is simpler, which demands the information of the supply current and the DC-link voltage. Therefore, only one voltage sensor and two current sensors are needed.

In Fig. 3, the DC-link voltage is regulated by using a proportional-integral (PI) controller and its output, i.e., the reference current in *q*-axis (i^*_{Fq1}). Meanwhile, in the harmonic compensation block, the three-phase supply current is measured and transformed into synchronous (*d-q*) reference frame using *abc-dq* transformation in (10).

$$\begin{bmatrix} i_{Sd} \\ i_{Sq} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta_s) & \cos(\theta_s - \frac{2\pi}{3}) & \cos(\theta_s + \frac{2\pi}{3}) \\ -\sin(\theta_s) & -\sin(\theta_s - \frac{2\pi}{3}) & -\sin(\theta_s + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} i_{Sa} \\ i_{Sb} \\ i_{Sc} \end{bmatrix}. \quad (10)$$

Then, a high-pass filter (HPF) given in (11) is applied to extract harmonic components in the supply current, which becomes the reference current i^*_{Fdn} and i^*_{Fqn} .

$$G_{HPF}(s) = \frac{s^2}{s^2 + 2\xi\omega_p s + \omega_p^2}, \quad (11)$$

where $\omega_p = 2\pi.20$ (rad/s) is the passing frequency of the HPF.

Afterward, a simple proportional controller K_p is utilized to mitigate the harmonic components in the supply current. Finally, the output control signals for the three-phase four-switch shunt APF are calculated as

$$\begin{cases} v^*_{Sh1} = v^*_{Sha} - v^*_{Shc} \\ v^*_{Sh2} = v^*_{Shb} - v^*_{Shc} \end{cases}, \quad (12)$$

where

$$\begin{bmatrix} v^*_{Sha} \\ v^*_{Shb} \\ v^*_{Shc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta_s) & -\sin(\theta_s) \\ \cos(\theta_s - \frac{2\pi}{3}) & -\sin(\theta_s - \frac{2\pi}{3}) \\ \cos(\theta_s + \frac{2\pi}{3}) & -\sin(\theta_s + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} v^*_{Shd} \\ v^*_{Shq} \end{bmatrix}.$$

In addition, since the middle point of two split capacitors is used for common phase leg of both shunt and series APFs, the instantaneous voltage on these two capacitors varies according to the filter currents, mainly the shunt APF current (i_{Fc}). In four-switch three-phase inverters, the fluctuation of capacitor voltage is unavoidable and it may badly affect the performance of both shunt and series APFs. However, it is not necessary to insert the additional controller to balance the capacitor voltage because the performance of the series and shunt APFs is not degraded if a proper voltage variation compensation scheme is employed. According to [22], if the modulation signals for two phase legs (Sh_a and Sh_b) of the shunt APF are adjusted as (13), the voltage variation on V_{C1} and V_{C2} becomes negligible, and the compensation performance of the shunt APF is not degraded.

$$\begin{cases} d_1 = \dfrac{V_{C2}}{V_{C1}+V_{C2}} + \dfrac{v^*_{Sh1}}{V_{C1}+V_{C2}} \\ d_2 = \dfrac{V_{C2}}{V_{C1}+V_{C2}} + \dfrac{v^*_{Sh2}}{V_{C1}+V_{C2}} \end{cases}, \quad (13)$$

where d_1 and d_2 are modulation signals for phase leg Sh_a and Sh_b of shunt APF, respectively, and V_{C1} and V_{C2} are the capacitor voltages.

4.2 Control of the series APF

The purpose of the series APF is to compensate harmonic components in the distorted supply voltage to maintain the load voltage sinusoidal. The supply voltage (v_S) is assumed to be distorted, which includes the fundamental (v_{S1}) and harmonic components (v_{Sn}) as follows

$$v_S(\omega t) = v_{S1}(\omega t) + \sum_{n\neq 1} v_{Sn}(n\omega t), \quad (14)$$

where n is the n-th harmonic order.

To make load voltage sinusoidal, the harmonic components presented in (14) must be completely compensated. Some previous studies adopted hysteresis control for harmonic voltage compensation [12-15]. But the hysteresis control cannot assure a good performance of the load voltage due to the variation of the switching frequency. To overcome this drawback and to effectively compensate a large number of harmonic components, this paper adopts the repetitive control technique to regulate the

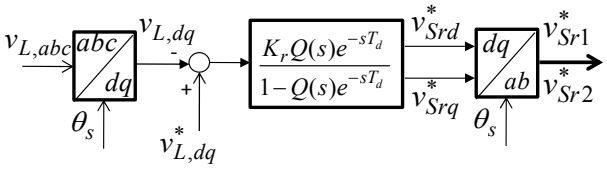

Fig. 4. Voltage controller for the series APF.

voltage harmonics [26].

The voltage controller for the series APF is illustrated in Fig. 4. The control strategy only needs the information of the load voltage. Thus, only two voltage sensors are required for the control scheme. In Fig. 4, the three-phase load voltage is measured and transformed into the *d-q* reference frame ($v_{L,dq}$).Then, the load voltage is compared with its reference value ($v_{Ld}^{*}=110V; v_{Lq}^{*}=0$) and the error is input to the repetitive controller (RC) to generate the control signal for the series APF. The transfer function of the RC is given as

$$G_{RC}(s)=\frac{K_r Q(s) e^{-sT_d}}{1-Q(s)e^{-sT_d}}, \tag{15}$$

where T_d is the time delay of the RC, $Q(s)$ is a filter transfer function, and K_r is the RC gain.

In Fig. 4, after executing the voltage controller to compensate voltage harmonics, the output control signals for the series APF (v_{Sr1}^{*} and v_{Sr2}^{*}) is calculated as

$$\begin{cases} v_{Sr1}^{*}=v_{Sra}^{*}-v_{Src}^{*} \\ v_{Sr2}^{*}=v_{Srb}^{*}-v_{Src}^{*} \end{cases}, \tag{16}$$

where

$$\begin{bmatrix} v_{Sra}^{*} \\ v_{Srb}^{*} \\ v_{Src}^{*} \end{bmatrix}=\sqrt{\frac{2}{3}}\begin{bmatrix} \cos(\theta_s) & -\sin(\theta_s) \\ \cos(\theta_s-\frac{2\pi}{3}) & -\sin(\theta_s-\frac{2\pi}{3}) \\ \cos(\theta_s+\frac{2\pi}{3}) & -\sin(\theta_s+\frac{2\pi}{3}) \end{bmatrix}\begin{bmatrix} v_{Srd}^{*} \\ v_{Srq}^{*} \end{bmatrix}.$$

Similar to the shunt APF control, the modulation signals for two phase legs Sr_a and Sr_b of the series APF are also adjusted as

$$\begin{cases} d_3=\dfrac{V_{C2}}{V_{C1}+V_{C2}}+\dfrac{v_{Sr1}^{*}}{V_{C1}+V_{C2}} \\ d_4=\dfrac{V_{C2}}{V_{C1}+V_{C2}}+\dfrac{v_{Sr2}^{*}}{V_{C1}+V_{C2}} \end{cases}, \tag{17}$$

where d_3 and d_4 are modulation signals for phase leg Sr_a and Sr_b, respectively.

Detail on design procedure of the RC for harmonic compensator is described clearly in [26].

5. Simulation results

To verify the validity of the proposed UPQC topology, digital simulation is carried out with the aid of the PSIM using the system parameters in Table 1. The distorted supply voltage is programed by injecting fifth and seventh order harmonic voltages. In addition, the load current is also highly distorted due to the use of three-phase diode rectifier at the load side. The total harmonic distortion (THD) values of the supply current and the load voltage are about 27.5% and 8.06%, respectively.

Fig. 5 shows the simulation results of the traditional UPQC by using the resonant control method introduced in [17]. In Fig. 5, the load voltage and the supply current are compensated to be sinusoidal despite of the severe condition of the supply voltage and the load current. The THD of the load voltage and the supply current after compensation are reduced to about 1.97% and 3.24%, respectively. In Fig. 5, the DC-link voltage is 350V in order to guarantee a proper operation in the conventional UPQC. This high voltage causes high cost, higher switching noises and power losses in the UPQC.

To verify the superiority of the proposed topology compared to the traditional one, the proposed UPQC is investigated under the same condition with Fig. 5 and the results are illustrated in Fig. 6. From Fig. 6, the load voltage and the supply current are effectively compensated to be sinusoidal with extremely low THD values of 1.22% and 1.35%, respectively. These values totally comply with the IEEE 519-1992 and IEC 61000-3-2 standards. Therefore, we can say that the performance of the proposed UPQC is not degraded compared to that of the conventional one despite of the reduced number of

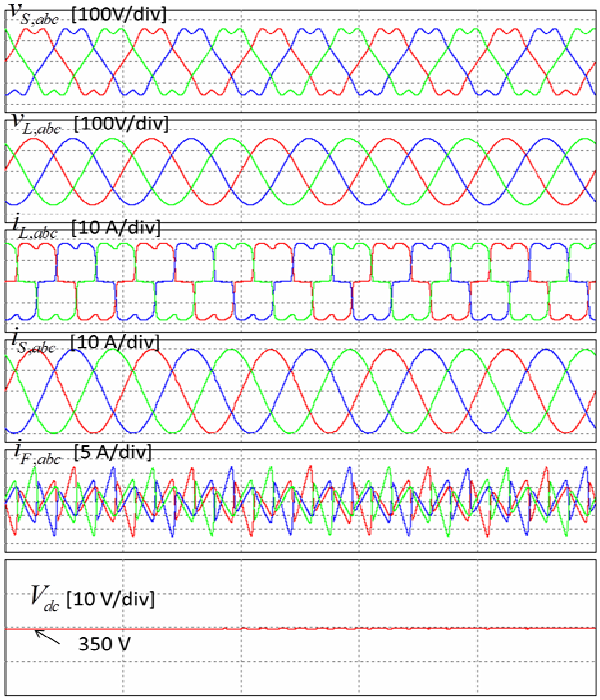

Fig. 5. Simulation results of the traditional UPQC, from top to bottom: supply voltage, load voltage, load current, supply current, filter current, and DC-link voltage.

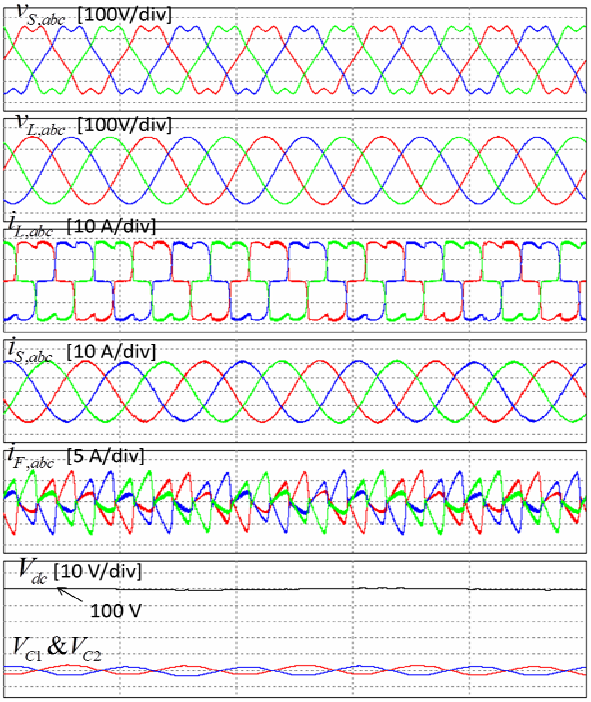

Fig. 6. Simulation results of the proposed UPQC, from top to bottom: supply voltage, load voltage, load current, supply current, filter current, and DC-link and capacitor voltages.

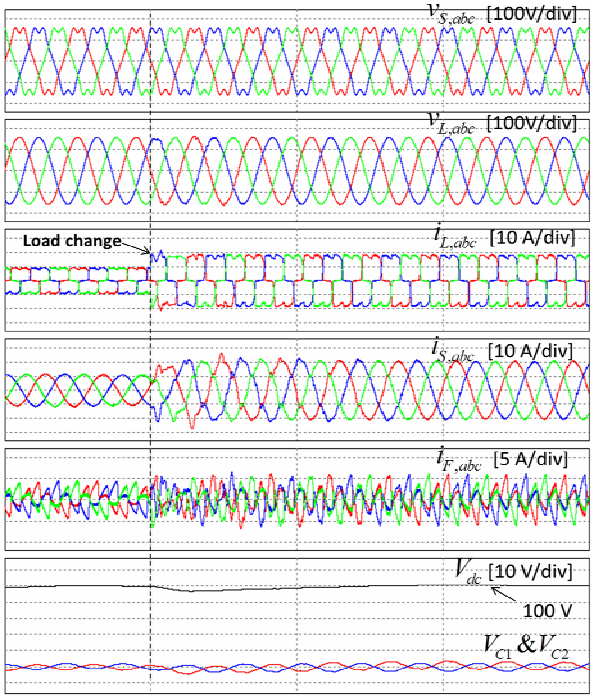

Fig. 7. Dynamic responses of the proposed UPQC with load change, from top to bottom: supply voltage, load voltage, load current, supply current, filter current, and DC-link and capacitor voltages.

switching devices.

Furthermore, a vital improvement of the proposed topology is that the required DC-link voltage for the UPQC is very low, i.e., 100V, which is less than one-third of that in the traditional UPQC. This low DC-link voltage leads to the decrement of the switching noises on the load voltage and the supply current waveforms, so that the THD values of the load voltage and the supply current have been slightly reduced compared to those in Fig. 5. In addition, the low DC-link voltage results in the reduction of power losses, which has the overall efficiency of the UPQC system improved. In fact, because we use the mid-point of two capacitors as a common phase leg of both shunt and series APFs, the voltages on two capacitors C_1 and C_2 are fluctuated in a small range as shown in Fig. 6. But, this voltage variation has no effects on the performance of the load voltage and the supply current. A summary on THD values of the load voltage and the supply current for the conventional and the proposed UPQC is given in Table 2. From Table 2, the proposed UPQC offers a slightly better THD performance thanks to the reduced DC-link voltage, which results in a smaller amount of switching noises.

To verify the robust operation of the proposed UPQC with load change, dynamic performance of the proposed UPQC is plotted in Fig. 7 with the increasing the load power from 50% to full load condition. In Fig. 7, the load voltage is maintained sinusoidal during the transition, and the UPQC takes only about three fundamental cycles to compensate the supply current to be sinusoidal. And also,

Table 2. Comparison on THD of the load voltage and the supply current by using the conventional and the proposed UPQC

	Conventional UPQC	Proposed UPQC
THD of load voltage	1.97 %	1.22 %
THD of supply current	3.24 %	1.35%

there are no overcurrent or resonance phenomena at the supply current in spite of the load variation. These results verify the fast dynamic response and the robust operation of the proposed UPQC topology under load variation. As a result, the proposed UPQC shows a good steady-state performance as well as a fast and robust response under the load change.

6. Experimetal Results

An experimental system is built as shown in Fig. 8 to show the possibility of the practical application. All system parameters in experimental system are the same as those used in simulation given in Table 1. The proposed UPQC is implemented by using four IGBT modules (FMG2G50 US60 from Fairchild). The control strategy is realized by a 32-bit floating-point DSP (TMS320F28335 of Texas Instruments). The supply voltage is generated by a Programmable AC Power Source (Chroma 61704) and a three-phase diode rectifier is used as the nonlinear load. The THD values of the load voltage and the supply current,

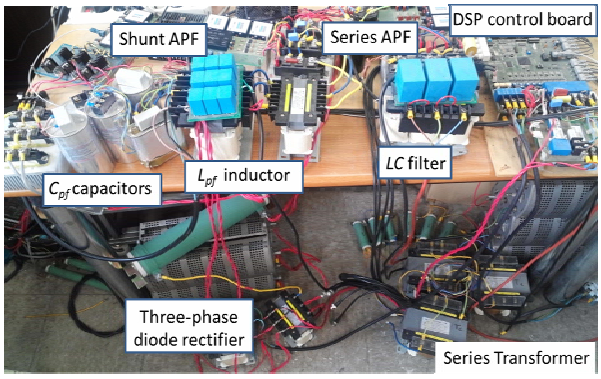

Fig. 8. Experimental platform for the proposed UPQC.

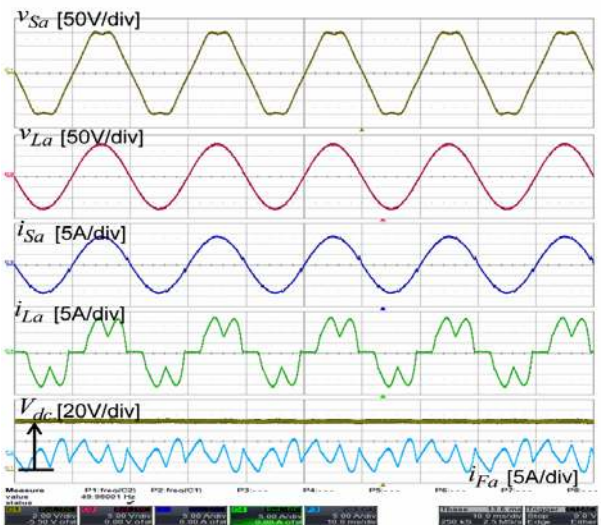

Fig. 9. Steady-state performance of the proposed UPQC, from top to bottom: supply voltage, load voltage, supply current, load current, DC-link voltage, and filter current.

and overall system efficiency are measured by a power analyzer (HIOKI 3193).

Experimental results of the proposed UPQC are shown in Fig. 9. As shown in Fig. 9, even though the supply voltage and the load current are highly distorted, the load voltage and the supply current are effectively compensated to be almost pure sinusoidal with very low THD values of 1.58% and 2.06%, respectively. These results are a little higher than those in simulation results due to the switching noises on experimental system. However, these values are still very low and completely comply with the IEEE 519-1992 and IEC 61000-3-2 standards. In Fig. 9, the injected current (i_{Fa}) of the shunt APF is lower than 30% of load current. Therefore, the use of additional capacitor C_{pf} in the proposed UPQC topology does not cause the whole system bulky and oversize. In addition, the DC-link voltage of the proposed UPQC is about 100V, which is much lower compared with that of the traditional UPQC, 350V, under the same supply voltage condition [20]. Therefore, the UPQC performance is not degraded even though the

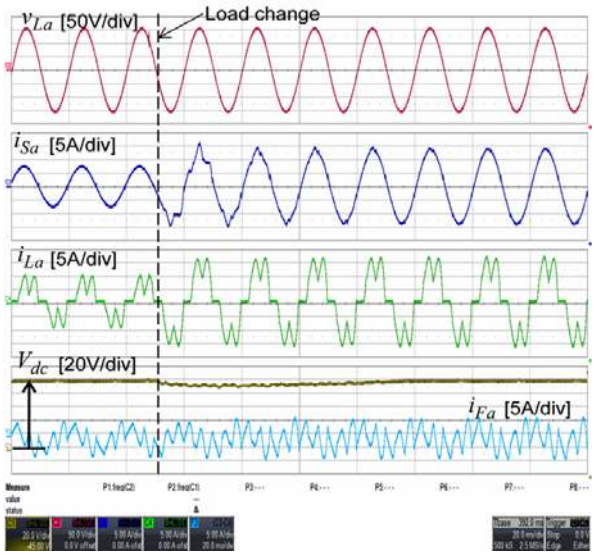

Fig. 10. Dynamic responses of the proposed UPQC under load change, from top to bottom: supply voltage, load voltage, supply current, load current, DC-link voltage, and filter current.

Table 3. Comparison on characteristics of conventional and proposed UPQC

	Conventional UPQC	Proposed UPQC
Number of switching devices	12	8
DC-link voltage	350 V	100 V
Number of sensors	13 (6 current sensors +7 voltage sensors)	7 (2 current sensors + 5 voltage sensors)
Overall system efficiency	94.7%	96.5%

proposed UPQC uses FSTPI with a reduced number of switching devices and lower DC-link voltage.

Besides a good steady-state performance, a robust operation under the load variation is also a vital assessment. The dynamic performance of the proposed UPQC is plotted in Fig. 10 by changing the load, which increases from 50% to full load condition. The experimental results in Fig. 10 are similar to the simulation results in Fig. 7, which shows that the proposed UPQC provides a robust response under the load change.

Power loss and the overall system efficiency are experimentally obtained by using power analyzer, and the results are summarized in Table 3. From Table 3, the proposed UPQC has lower power losses thanks to the reduced DC-link voltage (100V) compared to 350V for the traditional UPQC. As a consequence, the overall system efficiency of the proposed UPQC is higher than that of the traditional one in spite of a reduced number of switching devices and sensors as well as a decreased DC-link voltage. Therefore, we can say that the proposed UPQC achieves low cost, high efficiency, and high performance for the UPQC.

7. Conclusions

This paper proposed a low cost, high efficiency and high performance three-phase UPQC by using FSTPIs and an extra capacitor in the shunt APF side of the UPQC. The proposed UPQC accomplishes a lower cost as well as a lower power loss thanks to a reduced number of power switches and a low DC-link voltage. Even though the proposed topology requires extra capacitors, it is economically feasible in the system cost and efficiency because the current rating of additional capacitors is lower than one-third of the rated load current.

The validity of the proposed topology is verified through simulation and experiment. Simulation and experimental results show that the THD values of the supply current and the load voltage are kept very low and sufficiently comply with IEEE 519-1192 and IEC 61000-3-2 standards. The proposed topology is suitable to apply for the harmonic compensation in medium and high voltage distribution systems.

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