Stellingen bij het proefschrift getiteld:

Low-cost sensor interfacing

Frank van der Goes

1. De toepassing van een continue autocalibratietechniek, synchrone detectie, tweepoort-meettechnieken en dynamic element matching is noodzakelijk om goedkope universele en nauwkeurige sensor-interfaces te kunnen realiseren.

2. De toepassing van asynchrone modulatoren in goedkope en slimme sensorsystemen verdient veelal de voorkeur boven de toepassing van synchrone modulatoren.

3. In goedkope multi-purpose sensor-interfaces, gebaseerd op asynchrone modulatoren, heeft veelal de toepassing van eerste-orde oscillatoren de voorkeur boven hogere-orde oscillatoren.

4. De prijs van de gerealiseerde universele sensor-interface chip kan momenteel lager zijn dan die van een applikatie-specifieke.

5. De beleving die ervaren wordt bij het kijken naar sportprogramma's op TV kan aanzienlijk intenser worden door het toepassen van velerlei sensoren in ballen, banden, schaatsen, rackets, bokshandschoenen, etc. en het vervolgens omzetten van de sensorsignalen in door de menselijke zintuigen waarneembare signalen.

6. Het gegeven dat een harddisk van een computer altijd vol is, is geen goede reden om geen grotere aan te schaffen.

7. Als een schakeling in eerste instantie volgens verwachting werkt, kan met redelijke zekerheid gesteld worden dat een even aantal fouten gemaakt is.

8. De mens is niet gezonder dan het voedsel dat hij eet.

9. (Double)Click everywhere before reading your instruction manual.

10. De betekenissen van de begrippen ontspanning en beziggehouden worden neigen steeds meer naar elkaar toe.

11. Het gebruik van fossiele brandstoffen vormt voor het leven op aarde geen probleem mits de veranderingen die het teweegbrengt niet te snel verlopen.

12. Een beter milieu begint bij jezelf, maar grote verbeteringen vinden pas plaats na adequate reactie van een groep.

13. Veel van de fouten die de arbitrage in het betaalde voetbal maakt, zijn ontoelaatbaar.

Low-Cost Smart Sensor Interfacing

Low-Cost Smart Sensor Interfacing

PROEFSCHRIFT

ter verkrijging van de graad van doctor
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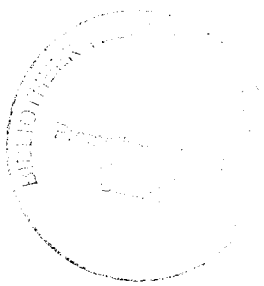
op gezag van de Rector Magnificus Prof. ir. K.F. Wakker,
in het openbaar te verdedigen ten overstaan van een commissie,
door het College van Dekanen aangewezen,
op maandag 15 april 1996 te 13:30 uur

door

Fransiscus Maria Leonardus VAN DER GOES

elektrotechnisch ingenieur
geboren te Delft



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Abstract

Current sensor systems are beset by a missing link, namely the lack of smart low-cost sensor interfaces between the sensor elements and the digital equipment such as microcontrollers.
This Ph.D. thesis discusses the design, simulation and realization of a multiple-purpose sensor interface chip for the read-out of external sensor elements such as capacitors, platinum resistors, thermistors, resistive bridges and potentiometers. This interface has been made commercially available.
It is shown that the consistent application of basic measurement techniques such as continuous auto-calibration, synchronous detection, two-port measurement techniques and dynamic element matching is required in order to obtain low-cost, accurate sensor systems.
The necessary Analog-to-Digital conversion is based on the use of a first-order asynchronous relaxation oscillator in combination with a microcontroller. Low-frequency interference signals and the effects of low-frequency 1/f noise have been suppressed by applying a special type of synchronous detection in combination with a second-order switched-capacitor filter.
The multiple-purpose sensor interface chip presented here operates on a single 3.3-5.5V supply voltage. The resolution and accuracy of capacitive measurements in the 0-2pF range amount to 50aF and 300aF. The resolution of the temperature measurements based on platinum resistors and thermistors amounts to respectively 10mk and 1mK for a measurement time of 100ms. The resolution of the resistive bridge measurement is 700nV. The accuracy of these measurements amounts to 500 ppm.

Contents

1. Introduction

1.1 Problems with sensor systems

Before dealing with the problems encountered in sensor systems, we have to explain what sensor systems are. A sensor system typically consists of one or more sensor elements and a modifier. The function of the sensor element is to convert energy from any energy domain (magnetic, chemical, optical, mechanical or thermal, as discussed by Middelhoek and Steigerwald-Audet [1]) into the electrical domain. Also conversion into other energy domains is possible, but electrical signals are usually best suitable for modification. The function of the modifier is to transform (modify) the electrical output signals of the sensor elements into other electrical signals which can easily be used for further processing such as, for instance, driving an actuator. The modifier usually consists of a number of analog circuits, digital circuits and an Analog-to-Digital converter.
In smart sensor systems, the sensor signal is not merely measured but the measurement result is obtained in a smart way. This means that, for instance, the measurement time is adapted when necessary, the sensor element and interface are put in power a down mode when no data is required or the measurement frequency is changed so that interference signals will have less effect on the measurement result.
The main problems with today's sensor systems are not caused by the sensor elements. Some commonly used sensor elements such platinum resistors and thermistors have existed for a long time, and will also be used in the future. The main problem with sensor systems is also not due to the digital part of the modifier. The price/performance ratio of digital modifiers, like computers and microcontrollers, has gone down greatly during the last 20 years. This makes them attractive to use. The main problem with sensor systems nowadays is the electronic part that interfaces between the sensor element and a digital modifier, especially when the sensor element is not integrated on the same substrate as the interface. Current interfaces have the following unattractive properties:

- they consist of complex circuitry, based on several amplifiers, filters, references etc.
- they are, therefore, too expensive
- they are too large
- they are not very reliable and accurate

Consequently, the use of sensor systems is not widely spread, particularly not in low-cost markets like consumer electronics or in more sophisticated markets. Moreover, sophisticated electronic equipment is blind and deaf to physical signals, a situation that needs to be changed.

The missing link in the signal conversion chain is a sensor interface with the following properties:

- low cost
- high reliability
- high accuracy
- easy-to-use (standardization of signals)

This type of interface would enable the use of sensor systems in a lot of new applications in both consumer electronics (coffee makers, washing machines etc., etc.), and more sophisticated (industrial) markets.

Recently, some interesting sensor interfaces have been developed. Interface ICs from Crystal Semiconductor Corporation [2] are able to read-out resistive bridge transducers and RTDs. They contain Delta-Sigma converters, digital filters and serial interfaces to communicate with a microcontroller. Interface ICs from Analog Devices [3] (for instance, the AD7710, AD7711 and the AD7712) are capable to readout resistive sensor elements and voltage-generating sensors. The setup of the interfaces of both companies show some similarity. Another interesting project [JAMIE, 4] resulted in interface IC named USIC. It is capable in performing many different types of measurements such as the measurement of voltage, resistance, current, capacitance and frequency. Of course this is hardly a complete list of interfaces.
A common disadvantage of these interfaces is that the important class of capacitive sensors cannot be read out in a low-cost way. Since capacitive sensor elements can be applied in many applications to measure many different types of signals, it would be a great advantage if they supported capacitive sensors. Another aspect is that complex external circuits are sometimes required to process part of the sensor signals.
When the complexity and costs of the above-mentioned sensor systems are considered, it can be concluded that these systems will not lead to a breakthrough in low-cost markets. Such a breakthrough would require a major decrease of the production costs. In this research, the key point to such a breakthrough is found in a consistent application of the best of all relevant basic measurement techniques.

We can now define the main problem to be treated in this thesis.

1.2 Statement of the problem and objectives

The main problem can now be stated simply: is it possible to develop low-cost sensor interfaces which are reliable, easy-to-use and do not have the above-mentioned drawbacks. The main objective of this work is to answer this question and, when the answer is yes, to realize such interfaces.

1.3 Organization of this thesis

Chapter 2 discusses a possible setup for a sensor system which has the attractive properties discussed above. Methods to meet the low-cost requirements will be shown.
Chapter 3 discusses several measurement techniques. Our objective can be achieved by combining these techniques.

Since the output signal of the modifier is considered to be digitally coded, an Analog-to-Digital (A/D) converter is necessary to convert the analog output signal of the sensor element. The central theme of Chapter 4 is to determine the optimal type of A/D conversion for use in the new-generation sensor systems.
It turns out that the optimal type of A/D conversion is based on the use of an oscillator, which is modulated by the sensor signal, in combination with a frequency counter. Chapter 5 discusses all the ins and outs of the modulator. Some important aspects are the modulator requirements, the suppression of low- and high-frequency interference signals and nonlinear behavior. Several sensor-specific modulator front-ends are also discussed.
Chapter 6 shows the design and realization of a general-purpose sensor interface.
Applications and measurement results are given in Chapter 7.
Chapter 8 contains conclusions.
Appendix A discusses the electrical and other important properties of sensor elements which can be read out by the general-purpose sensor interface discussed in Chapters 5 to 7.
Appendix B deals with the noise properties of the modulator discussed in Chapter 5.
Appendix C gives an application note of the general-purpose sensor interface.

1.4 Conclusion

Conventional sensor systems are not widely spread. This is mainly caused by the fact that interface electronics are too expensive, too large, and are not very reliable and accurate. A breakthrough in the sensor market will be enabled by low-cost sensor interfaces which are accurate, small, reliable and easy-to-use. This thesis will deal with the development of interfaces which meet the requirements.

1.5 References

1 S. Middelhoek and S.A. Steigerwald-Audet, "Silicon Sensors", Academic Press, London, 1989.
2 Crystal Semiconductor Corp. "Data acquisition databook", March 1995
3 Analog Devices, "Signal Conditioning ADCs", 1993
4 ERA Technology, "Target specification of the USIC", Eureka Project EU 579, February 1994.

2. System setup and starting points

2.1 Introduction

This paragraph discusses trends on sensor systems and gives a possible hardware configuration. This configuration leads to low-cost, reliable and easy-to-use sensor systems.
Thanks to new low-cost high-performance products such as PCs, software packages, integrated circuits and microcontrollers, and new technologies such as micro-machining and thin-film technologies, the costs of sensor systems are steadily decreasing and performance is increasing. In such designs, the complexity of the total system is reduced and overall calibration replaces calibration of the individual parts [1,2,3,4,5]. Features such as autocalibration and self-testing improve the accuracy and reliability. Traditional functions, such as A/D conversion and the generation of reference and compensating signals, are no longer performed by separate components, but will take place in analog signal processors and microcontrollers. Only the basic signals from the various sensor elements and reference sources or elements are amplified, converted and transferred to, for instance, a microcontroller. The availability of low-cost memory makes the implementation of several important functions feasible by collecting data over a longer period for a number of sensors. Examples of these functions are auto-calibration, self-testing and the compensation and filtering of undesired signals and effects. A possible hardware is proposed by Meijer and Herwaarden [6] and is shown in Figure 2–1. The microcontroller can be used to collect and to combine data, to make calculations and decisions, to control modes and ranges in the sensors, optimize the data rate, and to provide a standardized output format for higher computer levels.
To enable the processing of the sensor signal by microcontrollers and computers, circuitry for analoque processing, A/D conversion, multiplexing etc. is added. In smart sensors the processing circuits and the sensor elements are integrated on the same chip. The term Smart Signal Processor (SSP) is used to denote integrated circuits which operate according to the same principles as smart sensors, but lack on-chip sensing elements. In our opinion, the combination of a micrcocontroller and a smart sensor or a smart signal processor should be considered as the minimum unit in smart sensor systems.

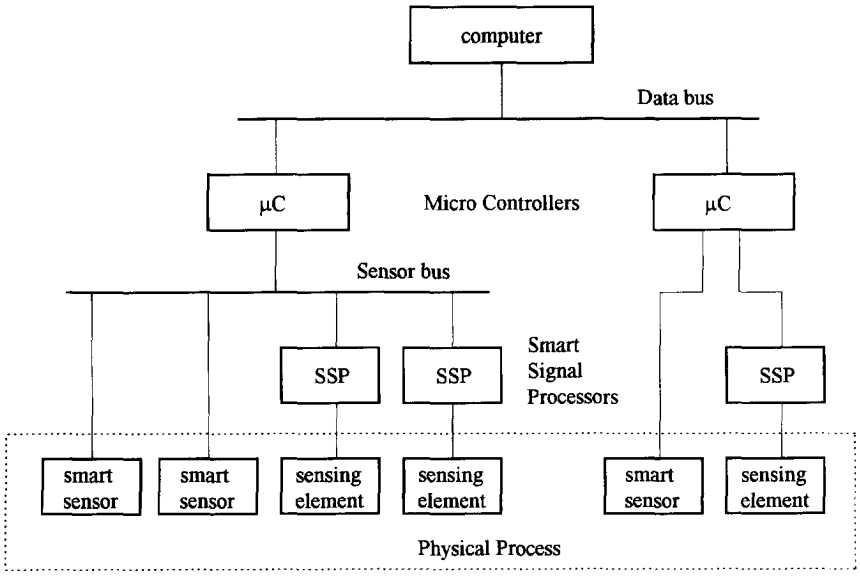

Figure 2–1. A possible hardware configuration of a sensor system.

In this thesis, we consider only the SSP and omit the interesting aspects that concern on-chip sensing elements. We assume that a reference element is available. The reference element should be of the same type as the sensing element in order to obtain the most accurate results, since, for instance, temperature effects on the sensing element and the reference element are equal and will have no effect on the final measurement result. Part of the hardware configuration shown in Figure 2–1, discussed in this thesis, is depicted in Figure 2–2. Note that this figure perfectly fits into the configuration shown in Figure 2–1.

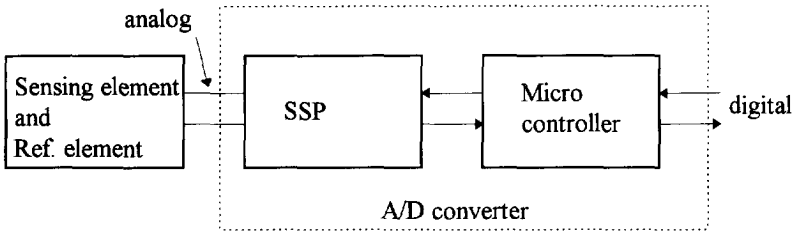

Figure 2–2. Part of the hardware configuration in Figure 2–1, which is the starting point of this thesis.

Three important items are related to the configuration in Figure 2–2. These are:

- Which measurement techniques will be used to readout the sensor element optimally. This will be discussed in Chapter 3
- The type of A/D conversion to be selected, which will be discussed in Chapter 4
- The architecture and implementation of the SSP, which will be discussed in Chapter 5

There are many possible configurations with very different properties with respect to costs, speed and accuracy. In the following section, we limit ourselves to configurations where low costs is a first requirement.

2.2 Low-cost concepts

we focus now on low-cost SSPs and sensor systems. Most of the low-cost applications require only a medium degree of accuracy and also a medium conversion speed. Typical values of accuracy and conversion are in the range of 10-16 bits and 10-1000 measurements per second. Another aspect related to low-cost is of course the cost of the hardware of the sensor system. In our opinion, a multiple-purpose SSP is currently preferable to a special-purpose SSP. As soon as the sensor market can be considered as a large-quantity market, special-purpose interfaces are preferably. Since this is not the case, we focus on general-purpose configurations. The greater complexity of such a multiple-purpose SSP is not a big problem if this SSP is implemented as an integrated circuit.
We will now depict the key points of our SSP:

- Low cost
- Accuracy 10-16 bits
- Conversion speed 10-1000 measurements per second
- Multiple-purpose
- Reliability.

We can now discuss several aspects of the sensor system setup as shown in Figure 2–2. These aspects concern the total system, the power, the chip and some electrical nonidealities.

System
The most important aspect is that the total system setup should be simple. The output signal of the SSP should be simple and easy to decode by the microcontroller.

Power
A standard single power (3-5V) supply and a low current consumption are desired.

Chip
The chip should be processed in a low-cost IC process, which is CMOS at the moment. Of course, a small chip area is preferable. Off-chip components often increase the flexibility, but also the costs, so we have to balance the pros and cons.

Electrical nonidealities of sensing elements
Sensing elements pick up disturbing signals from the environment so appropriate filtering of these signals should be applied. The measurement should not be influenced by parasitics of the sensing element and therefore proper measurement methods are necessary. Further, it is preferable that breakdown of the sensing element can be detected.

2.3 Measurement strategy

This section is on the measurement strategy which enables us to meet the above requirements. We use the following guidelines:

- In general, functions will be moved as much as possible from the interface to the microcontroller. One of the functions is linearization. Many sensing elements do not have a perfectly linear behavior. It is possible to linearize sensing elements with hardware solutions, however, in our opinion this is not desirable. The microcontroller is very capable

in doing calculations based on equations or look-up. This strategy results in simpler circuits. Only in the case of a very strong non-linearity, a hardware solution is required to obtain a rather constant resolution.

- The measurement technique, discussed in Chapter 3, is applied. An important technique is the three-signal technique, which is a continuous auto-calibration. This technique requires a reference element of the same kind as the sensor element.
- The reference element will be an external component.

2.4 Applications

We here limit ourselves to often-used low-cost off-chip sensing elements such as:

- Capacitors
- Platinum resistors
- Thermistors
- Resistive bridges
- Potentiometers.

Middelhoek and Audet [7] classified these elements as modulating sensing elements, which require some sort of energy input to produce a useful output.

Many sensing elements also have a temperature-dependent transfer. Normally, only a rough temperature indication is required to compensate for this effect. When the temperature of the sensing element and the SSP are approximately equal, the temperature of the SSP can be used for this purpose. An on-chip temperature sensor does not require extra external hardware and is therefore very attractive. Calibration of this temperature sensor increases its accuracy, but also increases the costs at the same time. In Chapter 5, we discuss the accuracy of an uncalibrated on-chip temperature sensor.

2.5 Conclusions

Combining microcontrollers and sensor interfaces (with or without on-chip sensor elements) is a good method to achieve low-cost and easy-to-use sensor systems. We limit ourselves to the readout of sensor elements with an accuracy up to 16 bits and which requires measurement times between 1ms and 100ms. At this moment, general purpose interfaces are superior to special-purpose interfaces when the costs are considered. This is caused by the fact that the sensor market can not (yet) be considered as a large-quantity market. One of the measurement strategies is to move functions as much as possible from the interface to the microcontroller. Another strategy is to use a continuous auto-calibration technique in combination with an external reference element.

2.6 References

1 K.D. Wise, "Analog data acquisition circuits in integrated sensing systems", in Proc. of the workshop Advances in Analoque Circuit Design, Leuven, 1993.

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6 G.C.M. Meijer and A.C. van Herwaarden, "Thermal Sensors", Adam Hilger, 1994.

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3. Measurement techniques

Below, we discuss the measurement techniques used to obtain accurate sensor systems in an easy way. We also discuss the sensor excitation when several sensing elements are measured.

3.1 The Three-Signal Technique

The three-signal technique is a technique to eliminate the effect of offset and unknown gain in a system G [1,2]. Application of this technique requires, in addition to the measurement of the sensor signal E_x, the measurement of two reference signals E_{ref1} and E_{ref2} in an identical way. These three signals result in three output signals Z_x, Z_{ref1} and Z_{ref2} of G. If the transfer of G only consists of an offset and a gain, the measurement result E_x can be obtained from the following calculation

$$M = \frac{Z_x - Z_{ref2}}{Z_{ref1} - Z_{ref2}} \tag{3-1}$$

We consider two different relations between E and Z describing the behavior of first-order oscillators and oscillating structures. These types of circuits play important roles in low-cost sensor systems, as we will see later. The first relation between E and Z is given by:

$$Z = \frac{a_1}{E} + a_0 \tag{3-2}$$

where a_0 and a_1 are the offset and "gain" of G, respectively. The three input signals normally contains an offset E_o and are given by:

$$E = \begin{cases} E_x + E_o \\ E_{ref1} + E_o \\ E_{ref2} + E_o \end{cases} \tag{3-3}$$

Substitution of (3-3) and (3-2) into (3-1) results in M_{inv}:

$$M_{inv} = \frac{E_{ref2} - E_x}{E_{ref2} - E_{ref1}} \frac{E_{ref1} + E_o}{E_x + E_o} \tag{3-4}$$

This result does not depend on a_0 and a_1. The signal E_x can only be obtained from (3-4) if E_o is known. It is also not permitted that E_{ref2} equals zero when E_o equals zero, since in this case Z_{ref2} would be infinite. All these problems can easily be avoided by applying the following relation between E and Z:

$$Z = a_1 E + a_0 \tag{3-5}$$

Substitution of (3-5) and (3-3) into (3-1) results in M_{prop}:

$$M_{prop} = \frac{E_x - E_{ref2}}{E_{ref1} - E_{ref2}} \tag{3-6}$$

This result also does not depend on a_0 and a_1. Further, E_o can have any value and it is permitted that E_{ref2} equals zero. We therefore need only one reference signal E_{ref1} and an arbitrary offset E_o. The relation in (3-5) requires the minimum number of reference signals and will therefore be applied.
The effect of drift of a_0 and a_1, due, for instance, to temperature effects or aging, can be eliminated by periodically measuring the three signals followed by calculation (3-6).
The only requirement for G to obtain accurate results is that of linearity. Achieving a high linearity of an electronic circuit is often no problem.
Usually, the three measurement signals are time multiplexed, so one measurement cycle consists of three measurement phases. We therefore need a memory to store at least two values of Z. The three-signal technique also requires a calculation unit. These two functions, storing and calculating, are two key functions of a microcontroller.

Conclusion
The three-signal technique is a very powerful technique to eliminate the effect of drift and uncertainties of additive and multiplicative errors.

3.2 Dynamic Element Matching

Dynamic Element Matching (DEM) is a known technique [3,4] to improve the overall accuracy of a system. It can be used when a number of nearly equal elements can be distinguished. By cyclically interchanging the elements, the overall accuracy can be orders better than the accuracy of the elements themselves. We explain this principle by considering the voltage divider from Klaassen [4], as shown in Figure 3–1.

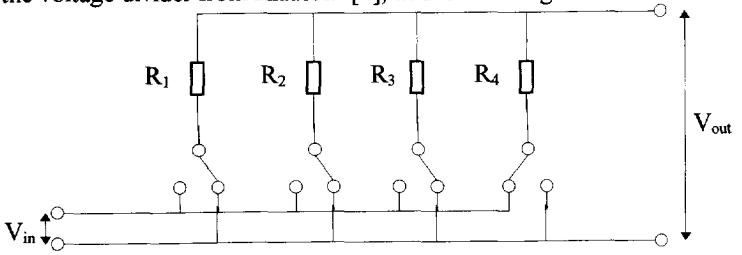

Figure 3–1. The DEM voltage divider of Klaassen with N=4.

The circuit consists of N almost equal resistors of which N-1 resistors are shunted. By putting the switches in different positions, we can obtain N different circuits. The ratio V_{out}/V_{in} for every circuit is almost equal to N^{-1}. A mismatch δ limits the accuracy of this ratio to δ. The average value of the N different ratios of the N circuits is exactly equal to N^{-1}. This is the advantage of DEM. When the time required to perform a full DEM cycle is short with respect to drift and temperature effects of the resistors, the final division ratio will not be affected by these effects. Application of this technique requires implementation of the average. This can be done very easily by the microcontroller.
In certain configurations, the effect of mismatch cannot be eliminated completely. The accuracy in the case of a mismatch δ is limited to the second order term δ^2.

Conclusion
Dynamic Element Matching is a very powerful technique to obtain high overall accuracy when a number of nearly equal elements are interchanged.

3.3 Synchronous detection

The measurement can be affected by disturbing signals, for instance 50Hz (or 60Hz) interfering signals from the mains supply. The fact that we limited ourselves to the read-out of modulating sensing elements enables us to apply synchronous detection. This enables us to reduce the interfering signal with respect to the main signal.

3.4 Two-port measurement

Normally, the connecting wires of the sensing element behave as parasitics, which may affect the accuracy. By a proper connection and measurement of the sensor, the effect of the parasitics is reduced or eliminated. The sensing element Z_x with the parasitics as modeled in Figure 3–2 a) forms a π-network. The sensing element should be measured by putting a voltage V_m on the input nodes and measuring the short-circuit current I_m. The ratio V_m/I_m depends only on the impedance Z_x. The dual case is shown in b). Now Z_x and the parasitics form a ladder network. The sensing element should be measured by putting a current I_m into the nodes and measuring the voltage V_m. Again, the ratio V_m/I_m depends only on Z_x. These are the two-port measurements.

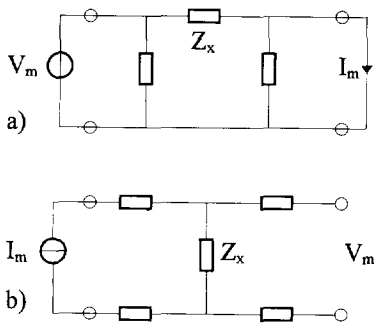

Figure 3–2. Two-port measurements for sensing elements where the sensing element and the parasitics form a π-network (a) and a ladder network (b).

When the sensing element cannot be modeled accurately with one of the circuits shown in Figure 3–2, the ratio of the excitation signal and the sense signal also depends on the parasitics.

Often, more than one sensing elements has to be measured. The circuit shown in Figure 3–3 shows the measurement of two sensing elements, where the parasitics and the sensing element form a π-network. The voltage V_m is used to measure both sensing elements Z_{x1} and Z_{x2}. Multiplexing at the sensing side of the element is not required. The ratio V_m/I_m depends only on Z_{x1} or Z_{x2}, depending on the position of the switch.

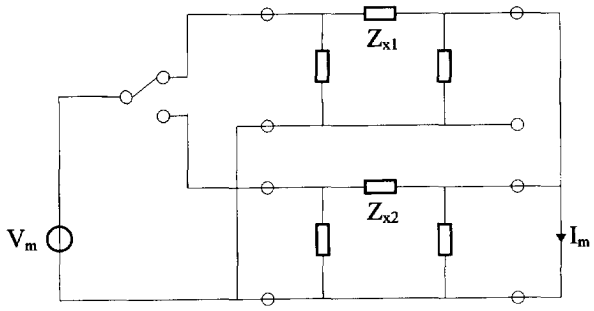

Figure 3–3. Measurement of two sensing elements where the sensing element and the parasitics form a π-network.

The circuit shown in Figure 3–4 shows the measurement of two sensing elements where the sensing element and the parasitics form a ladder network. Multiplexing at the excitation side is not required, but we need to multiplex the sensing side of the element. The ratio V_m/I_m depends only on the sensing elements Z_{x1} or Z_{x2}, depending on the position of the switches.

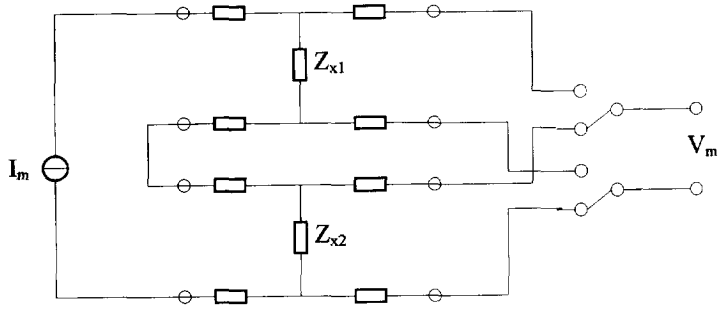

Figure 3–4. Measurement of two sensing elements where the sensing element and the parasitics form a ladder network.

Usually, the models of the sensing elements and the parasitics are far more complex than those discussed before. The effect of the extra parasitics can be greatly reduced by using proper connection and suitable excitation signals. We consider the circuit in Figure 3–5 as an example. This figure depicts the measurement of two capacitors, where C_{x1} is selected for measurement. The capacitance $C_{1,2}$ models the parasitic capacitor between the two transmitting electrodes. The resistances $R_{on,1}$ and $R_{on,2}$ model the ON-resistance of the switches.

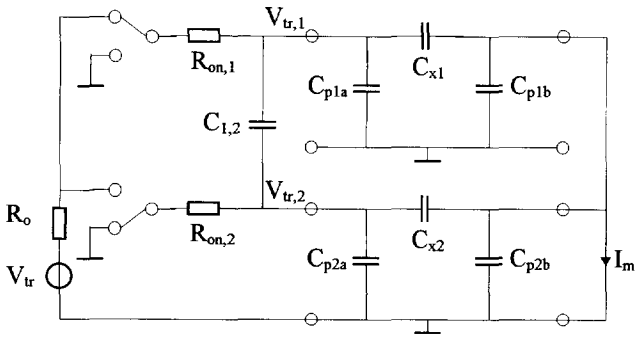

Figure 3–5. Measurement of two capacitors. The capacitance $C_{1,2}$ models the parasitic capacitors between the two transmitting electrodes.

A good method to reduce the effect of $C_{1,2}$ is to connect the transmitting electrode of a non-selected capacitor to GND (capacitor C_{x2} in the figure). This will reduce the signal $V_{tr,i}$ on the transmitting electrode of the non-selected capacitor. Proper signal type for V_{tr} may also help. When V_{tr} is a square wave, the charge built by I_m represents the capacitors C_{x1} or C_{x2}. When C_{x1} is selected, the contribution of C_{x2} to this charge decreases exponentially with the period of V_{tr}, since the voltage $V_{tr,2}$ on the transmitting electrode of C_{x2} exponentially decreases.
When V_{tr} is a sine wave, the amplitude of I_m represents a selected capacitor. When C_{x1} is selected, the contribution of C_{x2} to I_m is proportional to the frequency of V_{tr} (for frequencies far below the high-frequency pole).
The conclusion is that, in order to obtain the same level of cross talk, the maximum frequency of the sine wave is much lower than that of the square wave.

3.5 Conclusions

This chapter discusses several measurement techniques which will be applied in the Smart Signal Processor. Application of these techniques is required to obtain low-cost and reliable sensor systems. The three-signal technique is a continuous auto-calibration. Application of this technique result in accurate measurement results which can be obtained in a low-cost way, even when using low-cost IC processes. By using dynamic element matching techniques, for instance on-chip amplifiers can be realized with an accurate gain while calibration is not required. Synchronous detection is a very powerful technique to suppress interfering signals. Application of two-port measurement techniques strongly reduces the effect of parasitics of the connecting wires of both the sensor and the reference element on the measurement result.

3.6 References

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4. Analog-to-Digital conversion

4.1 Specifications

Before we determine the best type of A/D conversion for our system, we consider the most important specifications. These specifications have also been discussed in chapter 2, but are repeated here. Firstly, many of these sensors require a moderate accuracy of the A/D conversion to cover their accuracy and dynamic range. Secondly, many of these sensors require only a moderate conversion speed. Thirdly, to obtain a low-cost and accurate A/D conversion, integration technology has to be used. Since chip prices are proportional to chip area, only small chips, and thus simple modulators, are permitted. And, lastly, several types of sensors should be read out.
The specifications of the A/D conversion are listed below. This list also includes less specific items, like chip area, power supply and power consumption. These are more general specifications, considering the design of the A/D converter.

- absolute accuracy 10-16 bits
- conversion speed 1-100ms
- input multiple-purpose
- chip area a few mm^2
- power supply single 5V or 3V supply
- power consumption as small as possible

4.2 Indirect A/D conversion

Indirect A/D converters have proven to be very suitable for use in sensor systems [1,2,3,4,5,6]. They are capable of fulfilling the above-mentioned specifications. Such converters produce a digital signal in two steps. During the first step, they convert the sensor signal into a time signal: a frequency or a duty cycle. As a second step, this time signal is compared with a time reference and a digital signal is obtained. The first step is done by the SSP, while the microcontroller is very capable of doing the second step, so our indirect converter is implemented in the combination of the SSP and a microcontroller. Note that this concept fits perfectly into the hardware configuration discussed in chapter 2.
We now give an overview of the most important properties of our indirect converter.

- The output signal of the SSP is fully compatible with microcontrollers.
- Indirect converters are based on an oscillating structure, which generates the time signal. The structure can be kept simple, enabling a small chip area.

- The accuracy is *not* based on the matching of components, as in Flash or Successive Approximation A/D converters. Therefore, an accuracy of more than 10 bits can easily be obtained. The indirect converter is theoretically inherently linear and the combination with the three-signal technique produces a very accurate A/D converter.
- Indirect converters have a moderate conversion speed, which is sufficient for many sensors.
- The oscillating structure can be used to read out different types of sensing elements. Therefore, indirect conversion is very suitable in multiple-purpose sensor systems.

A property of indirect converters is the presence of a feedback loop, necessary to maintain oscillation. We make a distinction between two types of indirect converters: asynchronous and synchronous converters. The synchronous converter has a clocked gate incorporated in the feedback loop and the asynchronous converter has not. Both converters contain a modulator and a digital filter. The modulator consists of an analog filter, at least of the first order, and a comparator. The comparator is used for detection of the zero transitions. As the zero transitions only occur at discrete time moments, the signal is basically sampled [7].
Both types of conversion are briefly discussed below in order to make a good comparison and to select the best one for our sensor system.

4.2.1 Synchronous indirect conversion

When the clocked gate is also incorporated in the feedback loop, the SSP requires a clock signal from the microcontroller. Riedijk [8] distinguished two types of synchronized indirect modulators. These are the Delta-Sigma (Δ/Σ) modulator and the Dual-Slope modulator. A Delta-Sigma modulator with a generating sensing element is depicted in Figure 4-1.

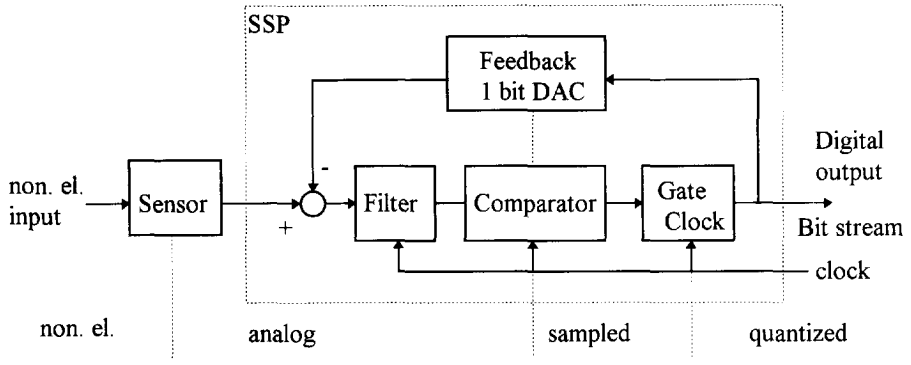

Figure 4-1. An example of a synchronous indirect modulator: the Delta-Sigma modulator with a generating sensing element.

The popular Delta-Sigma modulator is based on quantization error feedback, where the quantization is done very roughly by a 1 bit A/D converter (comparator)., A high accuracy can be obtained by applying oversampling techniques. The output of the modulator is a bit stream, which has to be digitally filtered. Often, proposed filters are one order higher than the order of the modulator [9]. The Dual-Slope modulator operates differently. The signal from the sensing element is continuously integrated for a whole number of periods of the main interfering signal. This is interference from the mains supply and has a frequency of 50 (or 60) Hz. This requires an integration time of minimally 20 (or 16.6) ms. The long integration time requires large capacitors or small currents, thus making the Dual-Slope modulator less suitable for use.

4.2.2 Asynchronous indirect conversion

If the clocked gate is not incorporated in the feedback loop, we obtain harmonic or relaxation oscillators, depending on the order of the filter. Since a property of the oscillator is modulated, we refer to it as a modulator. Examples of relaxation modulators with a generating and modulating sensing element are depicted in Figure 4-2 a and b, respectively.

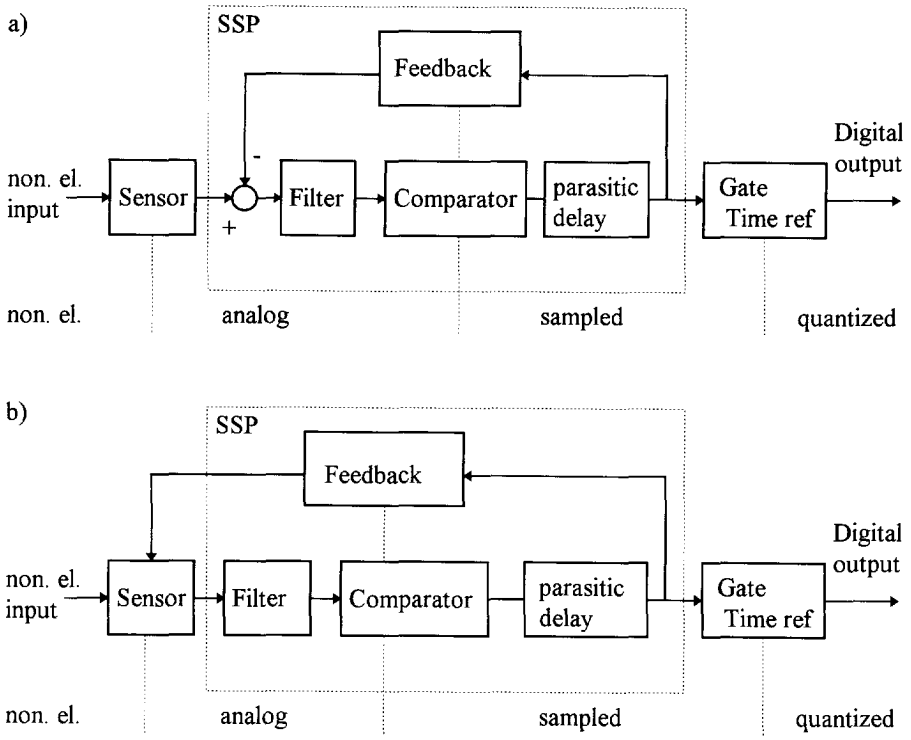

Figure 4-2. Examples of asynchronous indirect modulators: relaxation modulators with a generating sensing element (a) and a modulating sensing element (b).

Harmonic modulators are based on at least a second-order filter, while relaxation modulators are based on a first-order filter. The frequency (or duty cycle) of the modulator is directly related to the sensor signal. The microcontroller measures this frequency by counting the number of reference times that fit into a modulator period. Duty cycles are measured slightly differently. The advantage of the Delta-Sigma modulator, feedback of the quantization error, cannot be applied here. For accurate conversion, accurate time references are needed. These are available and rely on low-cost, accurate quartz crystals. Note that thanks to the three-signal technique, only short-term stability is required. Long-term instability of the quartz crystal's resonating frequency has, therefore, no influence on the accuracy of the measurement.

4.3 Asynchronous versus synchronous conversion

The differences between an asynchronous and a synchronous modulator enable us to select the best conversion principle for the SSP. We consider the number of wires, the output signal of

the SSP, the effort of the microcontroller to calculate the final result, the conversion time and digital interference.

4.3.1 Number of wires

The first and obvious difference is that an asynchronous modulator does not require a clock signal thus usually saving one wire. Saving wires is an important item in low-cost systems. In many applications, the SSP and the microcontroller are not on the same chip or in the same package. Imagine, for instance, a washing machine. The complete washing process is controlled by one microcontroller. Several sensing elements inside the machine measure the dirtiness of the laundry, the water level etc. These sensing elements, and thus the SSPs, are located throughout the machine. One of the consequences is that the SSP is not on the same chip or in the same package as the microcontroller. To limit the costs, we therefore have to limit the number of wires between the SSP and the microcontroller. We prefer to use only one wire to communicate with the microcontroller. This wire can be inside a bus.

4.3.2 SSP output signal

The second difference concerns the output signal of the modulator. The output signal of a synchronized modulator is usually a bit stream, which has to be transferred to the microcontroller and filtered digitally. If the digital filtering is performed by the microcontroller, the complete bit stream has to be transferred. This requires a relatively high-bandwidth communication line. The digital filter can be implemented on chip, but this requires a lot of calculation power if the filter order is higher than one. However, the output signal of an asynchronous modulator is very simple. The microcontroller measures the duration of a (number of) period(s) of the modulator output. To do this, the microcontroller needs at least two edges at its input. This corresponds to a very simple signal, which can be transmitted via a relatively low-bandwidth communication line.

4.3.3 Microcontroller effort

The microcontroller performs some digital processing, which is not equal for the two types of indirect conversion. The bit stream of a synchronized modulator has to be filtered digitally. Implementation of a second-order filter by the microcontroller requires a fast and well-equipped one. However, handling the output of an asynchronous modulator requires only a counter running on the sampling frequency and some memory to store the counted values. Now, the demands are much more relaxed, thus saving time for other applications.

4.3.4 Conversion time

The time required to achieve a certain resolution is determined by three aspects: the sampling frequency, the order of the digital filter and the internal electronic noise of the SSP itself. In the case of a Delta-Sigma modulator, higher-order filters combined with noise shaping rapidly reduce the quantization noise level. In the case of an asynchronous modulator, we apply only first-order filters, as will be discussed in section 4.4. To achieve the same quantization noise level as in the case of a Delta-Sigma modulator, more samples are required. When the sampling frequency is considered, the situation is different: since the modulator frequency in an asynchronous system does not depend on the sampling frequency, the latter can be chosen to be infinitely high. This means that only one modulator period may be sufficient to achieve the desired resolution. Of course, we need relatively high sampling frequencies. For Delta-Sigma modulators, the situation is different. Here, the sampling frequency equals the operating

frequency of the modulator. This frequency is now limited by the readout circuitry of the sensing element, and is therefore usually much lower than the sampling frequency in an asynchronous system.
As an example, we give estimations of the minimal conversion time to achieve a 14 bits resolution. For the time being, we neglect the thermal noise. Typical sampling frequencies are 200kHz and 3MHz for the Delta-Sigma and the asynchronous modulator, respectively. The typical conversion times are listed in Table 4-1 and are based on calculations by Leung [10]. These values hold under certain conditions. Firstly, in the case of asynchronous modulators, it is assumed that period modulation in combination with first-order digital filtering is used. Secondly, limit cycles in the case of first-order Delta-Sigma modulators have been removed by applying dithering techniques. Table 4-1 shows that the conversion time of a synchronous converter based on a first-order Delta-Sigma modulator combined with an ideal digital filter and an asynchronous converter are very competitive.

Type of modulator and filter	# samples	Conversion time <ms>
1st order Δ/Σ mod., 1st order filter	6690	33.5
1st order Δ/Σ mod., ideal filter	838	4.2
2nd order Δ/Σ mod., ideal filter	81	0.4
Asynchronous modulator, counter	6690	2.2

Table 4-1. Typical conversion times for different converters.

Thermal noise also determines the required number of samples or the measurement time. To achieve a certain resolution, a minimal measurement time is required. Thermal noise will finally limit the minimum conversion time.

4.3.5 Low-frequency interference

The dominant low-frequency interfering signal is interference from the mains supply. The frequency of this interference is 50Hz (or 60Hz) and harmonics. Since the sensing element is off-chip, we assume that the interference is present at the sensor input.
The interference can be filtered by choosing the measurement time to be equal to a complete number of interference periods. This is very simple to achieve in a synchronized system, it is done by adjusting the clock frequency to the frequency of the interference. In the case of modulators, the sensor information is represented by a time parameter of the modulator and a fixed measurement time can hardly be realized. By applying synchronous detection techniques in combination with modulators, as discussed in Chapter 5, low-frequency interference can be filtered properly.

4.3.6 High-frequency interference

The final difference concerns the high-frequency interference. The main high-frequency interference is digital interference from the microcontroller. This interference can affect the analog signal processing, or can interfere with the output signal of the modulator. Both conversion principles can be very competitive for the effect of digital interference on the signal processing. The effect of interference on the analog signal processing is different for the two types of modulators.
A synchronous modulator requires a clock signal, which acts as digital interference for the analog part. However, this interference is synchronously detected by the modulator and produces a DC term. Its effect is eliminated by the three-signal technique.

In the case of an asynchronous modulator, digital interference, which is filtered to the greatest possible content, can cause locking effects. The modulator frequency does not perfectly represent the signal from the sensing element. The use of dithering techniques [11] and applying a low bandwidth for all parts of the modulator reduce these locking effects.
The digital interference can also interfere with the output signal of the modulator. This interference is modeled in Figure 4-3 by V_{dig} and is valid for both conversion principles.

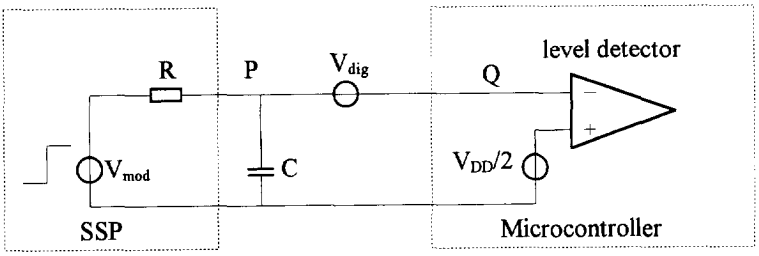

Figure 4-3. Model of digital interference at the output signal of the modulator.

The output signal V_{mod} of the (synchronous or asynchronous) modulator has a peak-to-peak amplitude of V_{DD}. The resistor R models the output resistance of the modulator, while C models the connecting cable between the modulator and the microcontroller. The level detector detects the level of its input signal V_Q.
In the case of a synchronous modulator, the information is stored in the level of V_Q at discrete moments. An error occurs when $V_{dig}>V_{DD}/2$. In the case of an asynchronous modulator, the information is actually stored in the crossing of $V_{DD}/2$ by V_Q. This moment is influenced by V_{dig} when the slope of V_P is not infinite. A time error ΔT occurs, which is given by:

$$\begin{aligned} \Delta T &= V_{dig}\left(\frac{dV_P}{dt}\right)^{-1} \\ &= 2\tau\frac{V_{dig}}{V_{DD}} \end{aligned} \tag{4-1}$$

where the time constant τ=RC. For a small time error, the interference and/or time constant should be small. The synchronous converter is less sensitive to interference at the output of the modulator.

4.3.7 Conclusion

An asynchronous modulator is superior to a synchronous modulator with respect to the number of wires required, the complexity of the output signal and the effort of the microcontroller, and they are almost competitive with respect to the conversion time. We expect that low- and high-frequency interference can be suppressed sufficiently when using an asynchronous modulator.
Therefore, in our opinion, the optimal type of A/D conversion to employ low-cost and accurate sensor systems is based on **asynchronous** indirect conversion. In Chapter 5, we make a selection between harmonic and relaxation modulators.

4.4 Quantization noise

An important aspect of A/D conversion is the quantization noise. In this section we discuss the quantization noise of A/D converters based on asynchronous modulators.
The process of quantization is shown in Figure 4-4. The input signal for the microcontroller is quantized. After quantization, the signal is digital. The duration of T is determined by counting the number of ones.

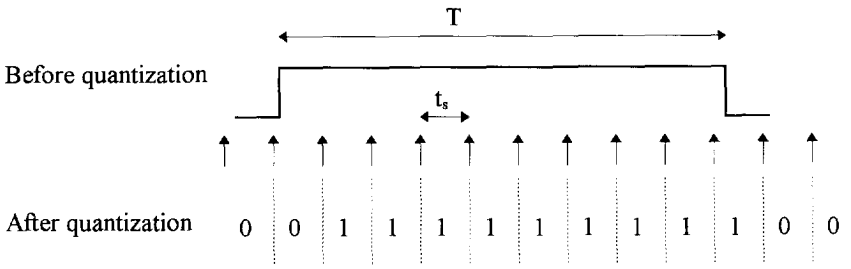

Figure 4-4. The process of quantization.

Two quantization errors are made during the determination of T: one at the beginning and one at the end of T. Every single quantization is assumed to have a mean of $t_s/2$ and a uniform distribution between 0 and t_s. The variance of a single quantization is given by σ^2 [12]:

$$\sigma^2 = \frac{1}{t_s}\int_0^{t_s}\left(t - \frac{t_s}{2}\right)^2 dt = \frac{t_s^2}{12} \qquad (4\text{-}2)$$

The variance for the sum of both quantizations is simply $2\sigma^2$, since both quantization errors are uncorrelated. Since both the starting and stopping are delayed, the mean error of a complete measurement of T, including two quantizations, is zero. The standard deviation of the relative error of T due to quantization noise is given by ε_q:

$$\varepsilon_q = \frac{\sigma\sqrt{2}}{T} = \frac{1}{\sqrt{6}}\frac{t_s}{T} \qquad (4\text{-}3)$$

We immediately see that the measurement time and the resolution are linearly related.
Example. The time T required to achieve a 16-bit resolution with a 1MHz sampling frequency is 26.7ms. The application of the three-signal technique requires the measurement of three signals. The total measurement time is then shorten than 100ms. This is within the specifications.
As we see later, the modulator period is much shorter than the required 26.7ms. This results in a decreased resolution when only one modulator period is quantized. To obtain the desired 16-bit resolution with the same sampling frequency, we have to take into account more periods. The number of required periods N depends on how the information is stored in the signal. When duty-cycle modulation (DCM) is applied, the information is stored in the duty-cycle of the output signal of the modulator (Figure 4-5 a).

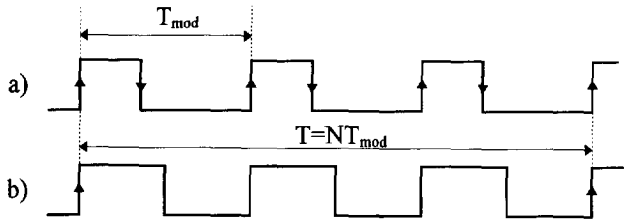

Figure 4-5. Output signal of the modulator when duty-cycle modulation (a) or period modulation (b) is applied.

A quantization error is made at every edge. These errors are not correlated. The standard deviation of the relative error of the duty cycle D, based on N periods, is given by $\varepsilon_{q,DCM}$

$$\varepsilon_{q,DCM} = \frac{1}{\sqrt{6}} \frac{1}{\sqrt{N}} \frac{t_s}{DT_{mod}} \tag{4-4}$$

This equation is valid for N>>1. Fewer periods are required when period modulation (PM) is applied, so the information is stored in the period, as shown in Figure 4-5b. A time interval T consists of N concatenated periods T_{mod}. Quantization errors are made only at the beginning and at the end of T. The standard deviation of the relative error of NT_{mod} is given by $\varepsilon_{q,PM}$:

$$\varepsilon_{q,PM} = \frac{1}{\sqrt{6}} \frac{1}{N} \frac{t_s}{T_{mod}} \tag{4-5}$$

Example. With T_{mod}=100µs, D=0.5 and t_s=1µs, DCM requires $286 \cdot 10^3$ periods to obtain a 16-bit resolution, corresponding to 29s measurement time. Under the same circumstances, PM requires only 267 periods, corresponding to 26.7ms. Increasing T_{mod} results in a decrease of $\varepsilon_{q,DCM}$. However, large modulator periods require large capacitors or small currents. The suppression of interference from the mains supply is also decreased, as we see later. For this reason, duty-cycle modulation is not desirable.

Previously, we assumed that the modulator period is determined by measuring the duration of N concatenated periods and make quantization errors just at the beginning and at the end of the N periods. The relative quantization error is then given by (4-5). It is also possible to measure each modulator period of the N concatenated periods separately. This might result in an improvement of the resolution.
A similar method is used in Delta-Sigma converters [13] and this results in noise shaping. In the case of first-order Delta-Sigma converters, the use of dither techniques will reduce the quantization noise peaks caused by limit cycles [14]. A problem with oscillators is that there is no feedback loop for the quantization error, so no noise shaping is possible. The technique for the improved resolution can, therefore, not be used.

4.5 Communication with the microcontroller

The possible hardware configuration discussed in Chapter 2 shows two ways to connect the SSP to the microcontroller: the bus and the star connection. One of the main differences between these two methods concerns the number of wires needed: in a bus system, every SSP is connected to the same bus, while in a star connection every SSP has its own wire. It is

beyond the scope of this thesis to discuss all existing busses, but we make an exception for a very promising one, the IS^2 bus [8,15]. This is the only bus that supports analog signals.
For the time being, we omit the addressing possibility and focus only on the output signal of the SSP. It is, of course, always possible to add the addressing circuitry and to communicate with the microcontroller via a bus.
In order to define a proper SSP output signal, we first recapitulate the choices made earlier. These concern the use of:

- Asynchronous A-to-D conversion, so the signaling is time continuous.
- Amplitude-discrete signals, which are also required by the microcontroller.
- A single data line between the SSP and the microcontroller.
- The three-signal technique, as discussed in Chapter 3.

The consequence of application of the three-signal technique in combination with a one-wire connection is that the SSP selects the measurement phases, since in low-cost systems we prefer half-duplex communication.

Until now, we have not considered the modulation method and the order of the modulator. This is one of the topics of the next chapter. It will there be shown that a first-order modulator with period modulation is most suited for our system. The period is than proportional to the sensor signal.
A very robust data communication protocol for this type of modulator is shown in Figure 4-6a.

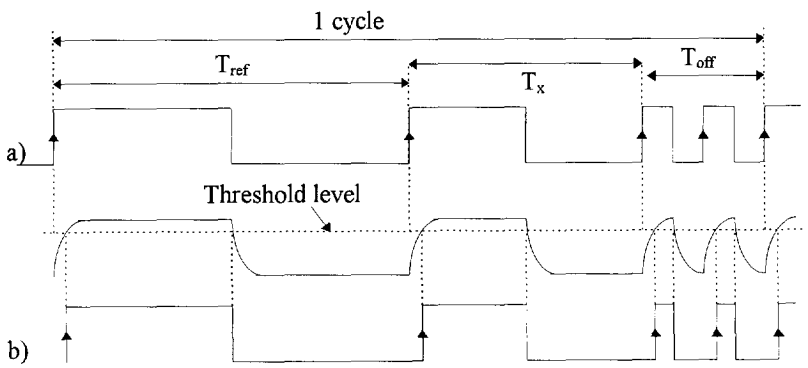

Figure 4-6. The output signal of the SSP (a), and after low-pass filtering (b).

One cycle consists of three measurement phases: one to measure the reference signal, another to measure the signal from the sensing element and the last to measure the offset. These phases correspond to T_{ref}, T_x and T_{off} respectively. Each measurement phase consists of N modulator periods. The value of N is related to the quantization noise, as discussed previously.
The microcontroller samples the output signal of the SSP by counting the number of internal clock cycles that fit in each phase. This results in the digital numbers D_{ref}, D_x and D_{off}. To obtain the ratio of the sensor signal and the reference signal, the microcontroller calculates M:

$$M = \frac{D_x - D_{off}}{D_{ref} - D_{off}} = \frac{E_x}{E_{ref}} \tag{4-6}$$

The microcontroller recognizes the offset measurement phase. This is enabled by doubling the output frequency during this phase. The result is that T_{off} consists of two short equal time intervals, which can easily be distinguished within one cycle.

This form of synchronization puts some restrictions on T_x. For robust detection, we have to guarantee that $T_x > {}^1/_2 T_{off}$. This is very easy to realize.

The signal shown in Figure 4-6b appears at the input of the microcontroller when the transmission channel is limited in bandwidth. The amplitude of this signal is not discrete. The microcontroller now uses its internal "comparator" with corresponding threshold level, depicted by the dashed line. This threshold level is usually not halfway the power supply.
The resulting signal to be sampled is not only a delayed version of the output signal of the SSP, but it is also distorted. The time between the up-going edges, however, remains the same so no information is lost and the result is very robust signaling.
Further, a non-linear output impedance of the modulator and hysteresis of the microcontroller does also not result in loss of information.

Phase sequence
The sequence of the phases is set in the SSP. The sequence of the communication shown in Figure 4-6 is E_{ref}, E_x, E_{off}, etc. The signal from the sensing element E_x is measured once every three measurement phases. It is also possible to change this sequence, depending on the bandwidth of E_x, E_{ref} and E_{off}.

4.6 Total A/D conversion system

Figure 4-7 shows the complete A/D conversion system. The system is based on asynchronous conversion. The signals from the sensing and reference element modulate the period of the modulator. The three-signal technique requires the measurement of three signals during three different measurement phases. Every measurement phase consists of N modulator periods. The SSP controls these phases. Two functional blocks of the microcontroller are used. These are the actual A/D converter and a block that performs the calculation to get the final measurement result M. This is a form of digital signal processing (DSP).

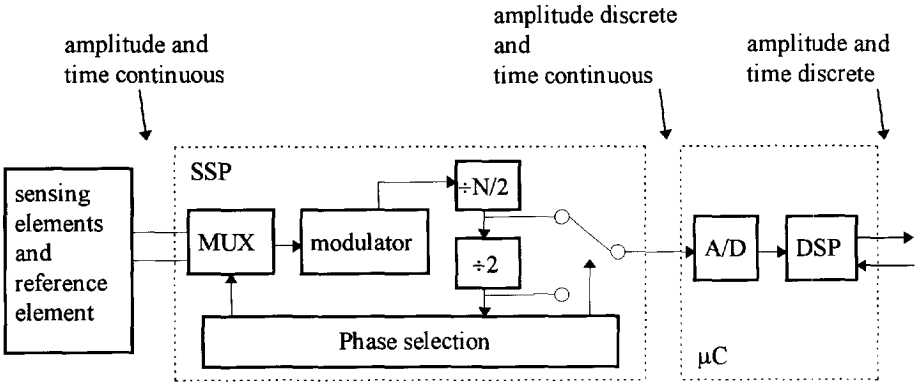

Figure 4-7. A detailed diagram of the indirect A/D conversion system, based on the use of an asynchronous modulator and a frequency counter. The divide-by-2 stage is used for synchronization purposes.

4.7 Conclusions

The type of Analog-to-Digital conversion which is most suited for use in low-cost smart sensor systems is based on an asynchronous oscillator (modulator) which is controlled by the sensor signal in combination with a frequency counter (the microcontroller). This is the conclusion after comparison of an asynchronous and a synchronous converter with respect to several aspects as the number of wires between the SSP and the microcontroller, the format of the output signal of the SSP, the effort of the microcontroller to obtain the measurement result, the required conversion time and the effect of low- and high frequency interfering signals. Application of the three-signal technique requires the selection of three different measurement phases and this is done by the SSP itself. The output signal of the SSP is very robust, requires only a small transmission bandwidth and can easily be decoded by the microcontroller.

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15 J.H. Huijsing, R.F Tuk, F.R Riedijk, M. Bredius and G. v.d. Horn, "Mixed Analog/Digital Two-line Bus System", Dutch Patent Application, Nr. 93201595-1, June 1993.

5. The modulator

In this chapter, the modulator is discussed in all its aspects. We start with discussing its most important requirements and characteristics. We continue with the filtering of interfering signals and thermal noise. Since linearity is a very important requirement, we examine the main causes of nonlinearity. The sensor-specific parts at the input of the modulator includes some interesting new circuits.

5.1 Modulator requirements

We have discussed the application of asynchronous indirect conversion, based on a modulator. In this section, the most important requirements and characteristics of the modulator are considered. These are:

- the order of the modulator
- the modulation method
- the sensitivity to interfering signals
- the instability due to thermal noise, especially 1/f noise
- the minimum and maximum frequency

After considering these aspects, we are able to design a modulator which is optimally suited for our application.

5.1.1 Modulator order

The required conversion from sensor signal to a time-modulated signal is performed by the modulator. We consider a first-order relaxation modulator and a second-order harmonic modulator. The main advantage of the relaxation modulator is that it can be excellently modulated in a simple way. The main advantage of the harmonic modulator is its insensitivity to interfering signals. A very suitable harmonic modulator which is easy to modulate, is the two-integrator modulator as discussed by Doorenbosch [1]. A typical two-integrator modulator is shown in Figure 5-1.

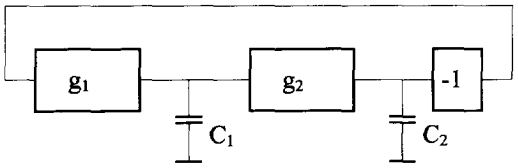

Figure 5-1. A typical two-integrator modulator.

The modulator is based on capacitors C_1 and C_2 as integrating elements. The blocks g_1 and g_2 are transconductance amplifiers with transconductance g_1 and g_2. The required amplitude-control loop is not depicted. The period of this two-integrator modulator is given by T_{ti}:

$$T_{ti} = 2\pi\sqrt{\frac{C_1C_2}{g_1g_2}} \tag{5-1}$$

A first-order relaxation modulator contains only one integrator. This integrator is preferably based on the use of a capacitor, because of its good characteristics and integratability. A typical relaxation modulator is shown in Figure 5-2 [Verhoeven, 2].

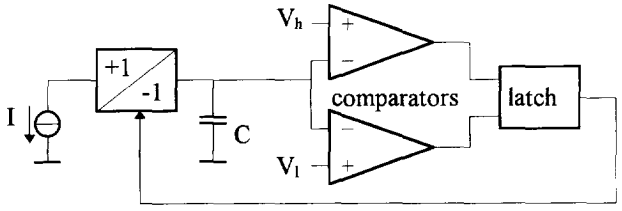

Figure 5-2. A typical first-order relaxation modulator.

A relaxation modulator contains at least one integrator, one comparator, a current source and a memory. The memory can be implemented by a delay time, hysteresis or a latch.
The period of this relaxation modulator is given by T_{rm}:

$$T_{rm} = \frac{2C(V_h - V_l)}{I} \tag{5-2}$$

We consider several aspects which are related to the order of the modulator. These are:

- the simplicity of the modulator
- the application as a multiple-purpose modulator
- the sensitivity to interfering signals
- the linearity of the analog-to-digital (A/D) conversion
- the dynamic behavior

Considering these aspects enables us to select the order of the modulator.

5.1.1.1 Simplicity

Normally, the complexity of harmonic modulators is greater than that of relaxation modulators. For instance, harmonic modulators require amplitude control loops which consume a lot of chip area, as showed by Doorenbosch. Further, the selection of different input signals to perform the three-signal technique is not simple. A relaxation modulator does not require an amplitude control loop and selection of the different input signals is very simple.

5.1.1.2 Application as a multiple-purpose modulator

The two-integrator modulator (Figure 5-1) seems to be a very suitable harmonic modulator which can easily be modulated in comparison with other harmonic modulators. This modulator can be adapted for resistive measurements when the transconductance of one of the transconductance amplifiers equals the reciprocal value of the resistor to be measured. Also resistive bridges can be measured in this way. At least two bridge resistors should be measured separately to determine the bridge imbalance. However, common-mode (CM) components are not eliminated by using this method. The CM components can be removed in the voltage domain by measuring the (amplified) output voltage of the bridge. Measuring voltages using a two-integrator modulator requires a voltage-dependent transconductance. The period is then related to the voltage to be measured. The disadvantage of this setup is that interfering signals are not filtered by the oscillator, since they are not incorporated in the filter loop. Any disturbing signal in these voltages has a direct effect on the period. Another problem of harmonic modulators is related to the implementation of dynamic element matching (DEM). As discussed in Chapter 3, DEM requires of lot of switches which are not desirable in harmonic modulators.
However, relaxation modulators are very suitable to measure signals, resistors and capacitors. The implementation of DEM is also not a problem.

5.1.1.3 Sensitivity to interference

Harmonic modulators are widely known for their excellent filter properties. De Jong [3] showed that adding an interfering signal to a harmonic modulator does not affect the average period if all active components remain correctly biased. This means that locking to the microcontroller interference is not possible, which is a great advantage.
The filter properties of a relaxation modulator are not as good as those of a harmonic modulator. By choosing the operating frequency of a relaxation modulator to be between the frequencies of the two main interfering signals, it is possible to reduce the effects of the interfering signals. The mains supply, with a frequency of 50 or 60 Hz, and the microcontroller clock, with a frequency of several MHz, produce interfering signals.
It is also possible that the sensing elements pick up other disturbing signals. This might be a problem for the relaxation modulator when the frequency of the disturbing signal is close to its operating frequency.

5.1.1.4 Linearity of the A/D conversion

Both modulators seem to be very competitive with respect to the achievable resolution and accuracy. More about modulator linearity of can be found in [1] and [4].

5.1.1.5 Dynamic behavior

As shown in Chapter 4, the measurement phases are concatenated. To prevent cross talk between two concatenated measurement phases, the frequency or duty cycle must change instantaneously when a new measurement phase starts. In practice, this is a problem for a harmonic modulator, although Doorenbosch showed that a change of C_i or g_i in (5-1) theoretically results in a step response of the frequency. However, generating a step response of the frequency or duty cycle of a relaxation modulator is very easy to achieve.

5.1.1.6 Conclusion

The best choice of a modulator depends on which requirements and characteristics are important. For our system, a relaxation modulator is selected because of its simplicity and multiple-purpose application.

5.1.2 The modulation method

In this section we discuss the modulation methods of a relaxation modulator. Three useful modulation methods for a relaxation modulator are:

1. Duty-cycle modulation (DCM). The information is stored in the duty-cycle of the output signal of the modulator.
2. Period modulation where the information is stored in the inverse value of the period (IPM).
3. Period modulation where the information is stored in the period (PM).

The difference between the last two methods depends on how the final result M related to the three-signal technique is calculated.

The selection between the three methods depends mainly on the quantization noise and on a fundamental aspect of relaxation modulators: dead time.

The quantization noise in the case of DCM is quite considerable, as discussed in Chapter 4. For this reason, DCM will not be applied. IPM and PM do not have this disadvantage and will therefore be applied.

To make a selection between IPM and PM, we first consider the typical wave form generated by a relaxation modulator. This is shown in Figure 5-3. The peak-to-peak amplitude of the ideal triangular wave equals V_h-V_l. Due to an internal delay time t_d, the period is increased by $4t_d$ with respect to the ideal period T_{ideal}.

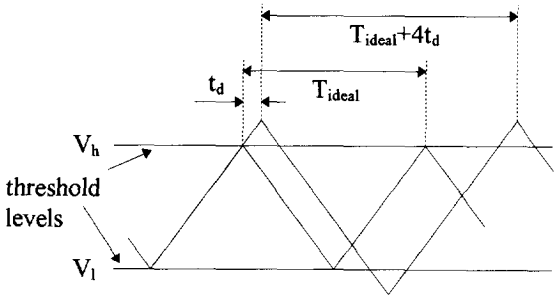

Figure 5-3. Typical wave form generated by a relaxation modulator. Due to the internal delay t_d, the period is increased by $4t_d$ with respect to the ideal period T_{ideal}.

In many applications, the normal range of the signal from the sensing element E_x lies in the range between zero and the reference signal E_{ref}: $E_x \in [0,E_{ref}]$. When the three input signals to perform the three-signal technique are E_0, E_0+E_x and E_0+E_{ref} (E_0 is an arbitrary signal to bias the modulator in the time domain), the input-output relation of the modulator to obtain a linear behavior (see Chapter 3) is given by:

$$X = a_1 E + a_0 \tag{5-3}$$

where E is the electrical input signal of the modulator (E_0, E_0+E_x and E_0+E_{ref}) and X a time signal.

When IPM is applied, the inverse value of the period depends linearly on the measurand. The period $T_{mod,IPM}$ is given by:

$$T_{mod,IPM} = \frac{1}{a_1 E + a_0} + 4t_d \tag{5-4}$$

where we accounted for the delay time t_d.

The final calculation M_{IPM} related to the three-signal technique is now given by:

$$M_{IPM} = \frac{T_{\text{mod},IPM,x}^{-1} - T_{\text{mod},IPM,0}^{-1}}{T_{\text{mod},IPM,ref}^{-1} - T_{\text{mod},IPM,0}^{-1}} \cong \frac{E_x}{E_{ref}}\left(1 + 4a_1 t_d\left(E_{ref} - E_x\right)\right) \tag{5-5}$$

To achieve a good linearity, only very small time delays can be permitted. With $a_1(E_{ref}-E_x)$=5kHz, the nonlinearity is smaller than 10^{-5} for t_d<500ps. This corresponds to a very high bandwidth with respect to the modulator frequency. Meijer and Voorwinden [5] applied IPM of a relaxation modulator as part of a Pt100 readout system. They dealt with this problem by choosing a low modulator frequency and tolerating a larger nonlinearity. This problem could be solved by making t_d inverse proportional to a_1E+a_0, but this is not easy.

When PM is applied, the period $T_{\text{mod,PM}}$ depends in a linear way on the measurand:

$$T_{\text{mod},PM} = a_1 E + a_0 + 4t_d \tag{5-6}$$

The calculation of M_{PM} related to the three-signal technique completely eliminates the effect of t_d:

$$M_{PM} = \frac{T_{\text{mod},PM,x} - T_{\text{mod},PM,0}}{T_{\text{mod},PM,ref} - T_{\text{mod},PM,0}} = \frac{E_x}{E_{ref}} \tag{5-7}$$

Not all relaxation modulators generate a wave form as shown in Figure 5-3. The period of, for instance, a charge balance modulator does not depend on internal delay. In this case, the nonlinearity as calculated by (5-5) reduces to zero and IMP can be applied. A property of a charge balance modulator is that a DC current is integrated, instead of an AC current. A typical wave form generated by such a modulator is shown in Figure 5-4.

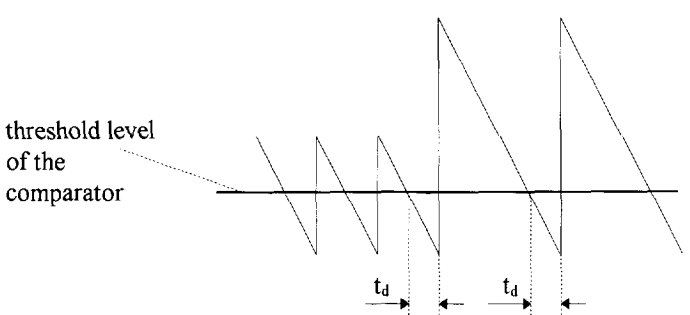

Figure 5-4. Typical wave form generated by a charge balance modulator. The delay time t_d has no effect on the period.

Figure 5-4 shows that the period is not affected by the delay time t_d. The nonlinearity as calculated by (5-5) reduces to zero, so IPM combined with a charge balance modulator can be applied to obtain a linear behavior. The main reason not to use a charge balance modulator is the great sensitivity to 1/f noise.

The most promising modulation method is PM and this method will be considered in detail.

Our aim is to implement the signal-to-time conversion for PM as expressed by (5-6) by a relaxation modulator. The relaxation modulator shown in Figure 5-2 can be modulated in two ways. These are:

1. Modulation of the current I
2. Modulation of the voltage swing V_h-V_l.

Modulation of C will not be considered, since this is not suitable for resistive measurements. Modulation of I, as shown in Figure 5-5, requires an inverse function before the actual modulator, since the actual modulator has an inverse relation between I and $T_{mod,PM}$. The total conversion from E to $T_{mod,PM}$ is linear, according to (5-6).

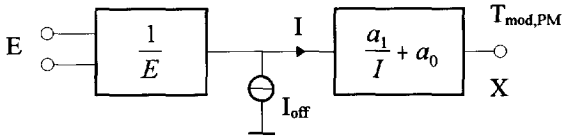

Figure 5-5. Setup of a PM modulator where the current I is modulated.

The main disadvantage of this setup is that the realization of the inverse function is very difficult. Another disadvantage is that the current I_{off}, which will usually be present, causes nonlinearity.

Modulation of the voltage swing V_h-V_l, as shown in Figure 5-6, does not have these disadvantages. Generation of a voltage proportional to a resistor or a capacitor is very simple to realize. In this case, V_{off} does not cause any nonlinearity.

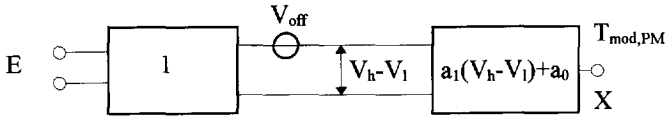

Figure 5-6. Setup of a PM modulator where V_h-V_l is modulated.

For these reasons, PM in combination with modulation of V_h-V_l will be applied.

5.1.3 Sensitivity to interfering signals

The modulator operates in an environment where interfering signals are present. The two main interfering signals are signals from the mains supply (with a frequency of 50 or 60 Hz and harmonics) and from the microcontroller (with a frequency of several MHz).

5.1.3.1 Mains supply interference

Mains supply interference is a common problem in sensor systems. The sensing elements are not integrated on the chip and therefore easily pick up disturbing signals. The interference can also be coupled to the modulator via the power supply lines, but we assume that the power supply is free of disturbing signals. This interference has to be removed with a filter. One of the restrictions to the filter is that information about the interfering signal is not available on the SSP, so tuned impedances cannot be used. Figure 5-7 shows three forms of synchronous detection, which do not rely on tuned impedances.

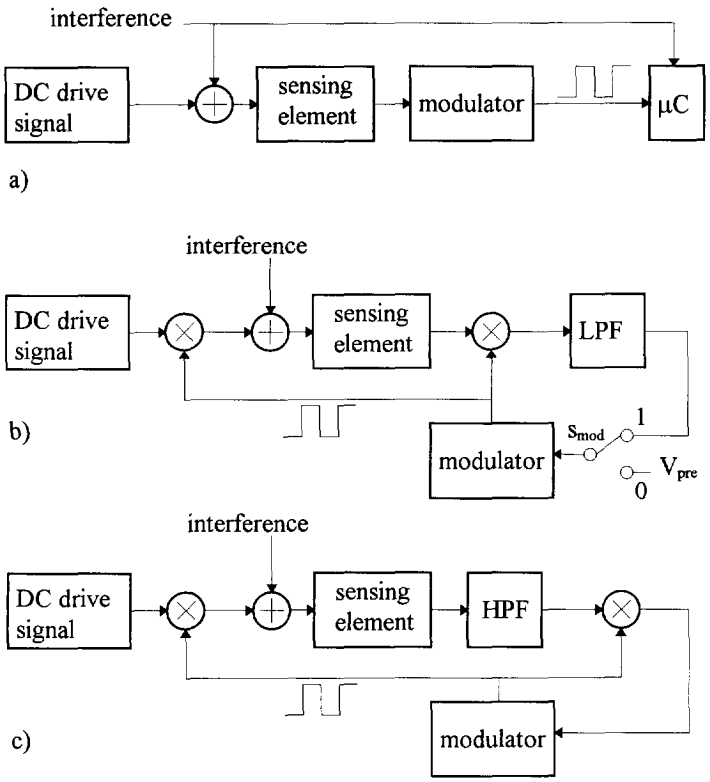

Figure 5-7. Synchronous detection to suppress the low-frequency interference from the mains supply without a filter (a), with a low-pass filter (b) and with a high-pass filter (c).

The modulator shown in all schemes is supposed to have a DC input.
The method in a) is based on a fixed measurement time, equal to a complete number of periods of the interference. This method cannot be applied here, since the duration of a measurement phase cannot be coupled to the interference as it is the carrier of the information.
The method in b) is based on a low-pass filter (LPF). The low-frequency (LF) interference is filtered by conversion to a higher frequency followed by a low-pass filtering.
The method in c) is based on a high-pass filter (HPF). The LF interference is simply high-pass filtered. The cut-off frequency of this filter is below the maximum modulator frequency which is approximately 100kHz, as will be discussed later. A high suppression for low frequencies requires a high filter order.

The methods in b) and c) rely on filters. Two useful types of filters which can be applied in the systems shown in Figure 5-7 b) and c) are:

1. Analog filters with fixed poles.
2. Sampled-data filters. Filters implemented by switched capacitor (SC) techniques where the clock signal of the filter is derived from the modulator are especially interesting.

Analog LPF

The advantage of applying an analog LPF is that high-order harmonics of the LF interference are also filtered properly when the bandwidth of the LPF is sufficiently small and the operating frequency of the modulator sufficiently high. A disadvantage of applying an analog LPF is that

the period of the modulator T_{mod} cannot change instantaneously. Since every measurement phase consists of N periods, this effect results in cross talk (nonlinearity) between concatenated measurement phases, as shown in Figure 5-8. Due to the transient at the start of a measurement phase, the duration of n periods is either too short or too long.

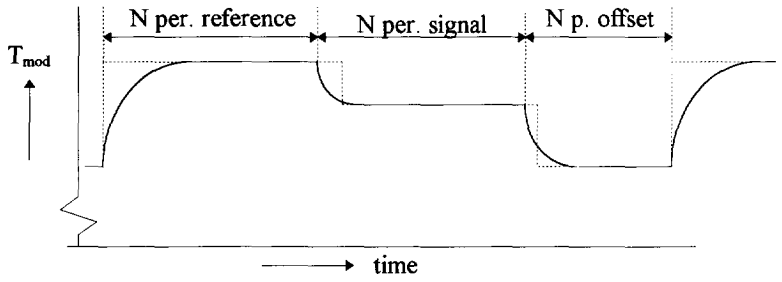

Figure 5-8. When the period cannot change instantaneously, cross talk occurs between concatenated measurement phases. The dashed line corresponds to the case without LPF.

This nonlinearity can be eliminated by introducing a fixed time interval at the beginning of each measurement phase. This time interval is used to settle the LPF completely. The time interval is generated by putting switch s_{mod} (see Figure 5-7 b) in position '0'. The input of the modulator is a fixed preset voltage V_{pre}. After this time interval, s_{mod} is put in position '1'. This action does not result in a transient. The fixed time interval is, for instance, the duration of a fixed number of modulator periods during an offset measurement and is canceled by the three-signal technique. The duration of this time interval can be kept low by prediction. Another disadvantage of using an LPF is that keeping the sensitivity to 1/f noise (that is generated after the second multiplier) sufficient low requires additional circuits and processing.
Example: A modulator frequency of 50kHz combined with an LPF bandwidth of 10kHz removes LF interference up to 40kHz. The settling time is less than 500µs. The duration of a measurement phase varies between 20ms and 40ms, so not more than 2.5% of a measurement phase is spent to settle the LPF.

Analog HPF
Applying an HPF does not require a fixed time interval to settle the filter, but this filter has another problem. The corner frequency should be rather high to obtain a good LF suppression, whereas the corner frequency should be low to obtain a good linearity. These two requirements cannot be met at the same time. This will be clear when we examine a first-order HPF. This filter has a zero in the origin and a pole on the real axis at $\omega=-1/\tau_{HPF}$. The input signal of the filter is a square wave with a typical frequency $f_{mod}/2$ (f_{mod} is the modulator frequency). Due to the pole, the output of the filter is no longer a square wave. The input signal V_{in} and the output signal V_{out} of the HPF are shown in Figure 5-9, where we assumed $T_{mod}<<\tau_{HPF}$.

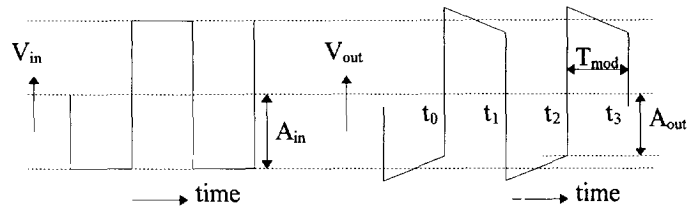

Figure 5-9. Input signal V_{in} and output signal V_{out} of the HPF for $T_{mod} << \tau_{HPF}$.

The signal level A_{out} on the sampling moments t_i is smaller than the amplitude A_{in} of the input signal. The ratio A_{out}/A_{in} is given by:

$$\frac{A_{out}}{A_{in}} = \frac{1}{2}\left(\exp\left(-\frac{T_{\mathrm{mod}}}{\tau_{HPF}}\right)+1\right) \tag{5-8}$$

This ratio is time dependent and thus different for the various measurement phases, resulting in a nonlinearity ε_{HPF}:

$$\begin{aligned}\varepsilon_{HPF} &= \frac{\left.\frac{A_{out}}{A_{in}}\right|_{T_{\mathrm{mod}}=T_{\mathrm{mod},x}}}{\left.\frac{A_{out}}{A_{in}}\right|_{T_{\mathrm{mod}}=T_{\mathrm{mod},ref}}} - 1 \\ &= \frac{\exp\left(-\frac{T_{\mathrm{mod},x}}{\tau_{HPF}}\right)+1}{\exp\left(-\frac{T_{\mathrm{mod},ref}}{\tau_{HPF}}\right)+1} - 1 \\ &\cong \frac{T_{\mathrm{mod},ref}-T_{\mathrm{mod},x}}{2\tau_{HPF}}\end{aligned} \tag{5-9}$$

Example: The required frequency of the filter pole to properly attenuate 50Hz interfering signals and harmonics should be roughly more than 1kHz. The maximum value for $T_{mod,ref}$-$T_{mod,x}$ to achieve a nonlinearity smaller than $\varepsilon_{HPF}=10^{-4}$ amounts to 33ns. This is much smaller than the sampling time of the microcontroller, so it cannot be detected. A second-order HPF with two equal poles on the real axis requires even a lower value to achieve the same linearity. An analog HPF is, therefore, not suitable to use.

Sampled-data SC LPF

Cross talk between two concatenated measurement phases can easily be prevented when an SC LPF is applied. A disadvantage of such a filter is the decreased LF suppression of the total system with respect to an analog LPF. A first-order SC LPF can be described in the z-domain by $1+z^{-1}$ ($z=\exp(j\omega T)$), resulting in a filter with a $\cos(\omega T/2)$ transfer. The modulus of this filter transfer function is shown in Figure 5-10. Higher-order harmonics of the modulated interference are less suppressed than the first harmonic.

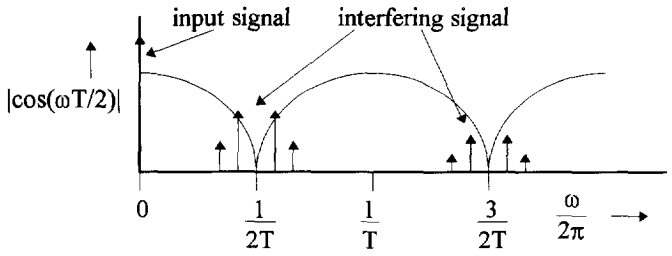

Figure 5-10. Modulus of the filter transfer function of a first-order SC LPF.

Sampled-data SC HPF

An SC HPF is almost the same as its low-pass equivalent. The first-order SC HPF is described by $1-z^{-1}$, resulting in a $\sin(\omega T/2)$ transfer. The modulus of the filter transfer function is shown in Figure 5-11.

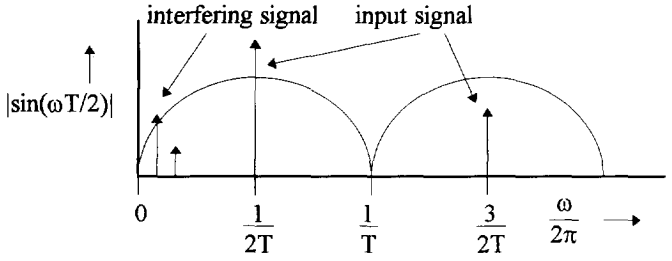

Figure 5-11. Modules of the filter transfer function of a first-order SC HPF.

Conclusion

Although an analog LPF filter would perform better, it has some disadvantages. These are the increased complexity necessary to avoid cross talk and to keep the sensitivity to 1/f noise low. Application of an analog HPF is not possible, since the application requires a modulator frequency which is too high for the microcontroller to measure. The requirements to achieve a good linearity and a good suppression of LF interference cannot be met at the same time. For these reasons, we focus on an SC filter. As will be seen later, the circuit with an LPF will be used.

5.1.3.2 Digital interference

Digital interference can cause a locking of the modulator frequency. When lock occurs, the frequency no longer accurately represents the signals to be measured. This situation has to be prevented. Several methods to reduce the locking effects in relaxation modulators are discussed in section 5.5. One method is based on low-pass filtering by keeping the bandwidth of all parts sufficiently low. Other methods are based on dithering and balancing.

5.1.4 1/f noise behavior

In this section we investigate the effect of 1/f noise on the modulator period. This noise is strongly present in low-cost CMOS processes. The 1/f noise can be modeled by the 1/f noise corner frequency. When the 1/f noise corner frequency is below the reciprocal value of the duration of one full measurement cycle, the three-signal technique will sufficiently reduce the

effect of 1/f noise on the final result M. Practical values for this corner frequency are then in the Hz range, which is rather low. We assume that this frequency is much higher. It is, therefore, required that the period is insensitive to 1/f noise.
In the synchronous detection schematics in Figure 5-7, several points can be indicated where adding 1/f noise does not result in a larger jitter of the modulator period. For instance, 1/f noise added before the second mixer shown in Figure 5-7b is properly removed.
It is more interesting to consider the modulator in more detail and to investigate which signal wave forms and how many comparators are required to obtain a low sensitivity to 1/f noise. Examine, therefore, Figure 5-12, showing two typical relaxation modulators. The modulator in a) is based on two DC current sources and two comparators and it generates a triangular wave. The modulator in b) is based on a single current source and a single comparator. It generates a sawtooth wave form.

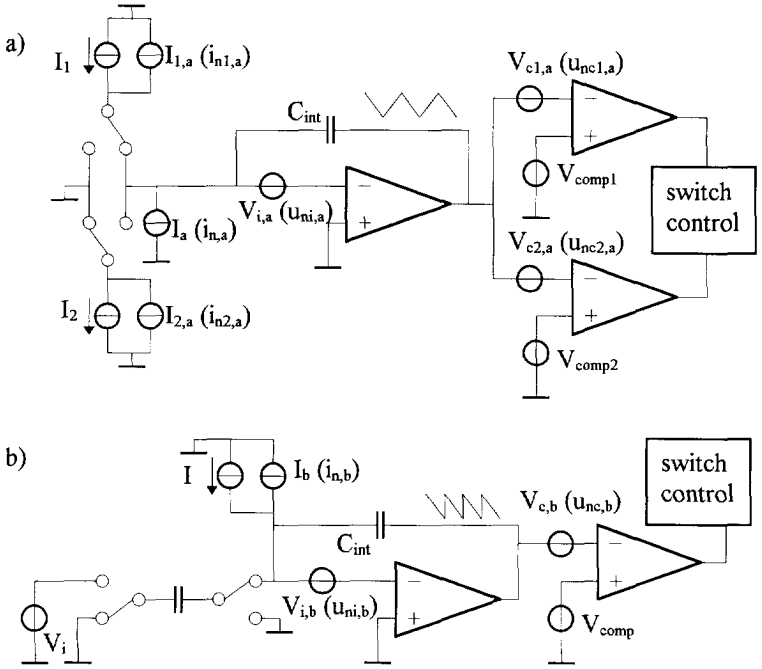

Figure 5-12. Two typical relaxation modulators to investigate the sensitivity to 1/f noise.

A very simple rule can be used to investigate the sensitivity of the period to low-frequency (LF) 1/f noise for noise with frequency components below the modulator frequency. Substitute the noise source by a DC voltage or current, depending on the source. If the period depends on this DC source, the period will also be sensitive to LF noise. We will use this simple rule to investigate the sensitivity to 1/f noise. All noise sources in Figure 5-12 have been substituted by DC sources. The name related to the noise source is placed between brackets.
It can be shown that the period $T_{mod,a}$ of the modulator in Figure 5-12 a) is given by:

$$T_{\mathrm{mod},a} = C_{\mathrm{int}}\left(V_{comp1,a} - V_{comp2,a} + V_{c1,a} - V_{c2,a}\right)\left(\frac{1}{I_1 + I_a + I_{1,a}} + \frac{1}{I_2 - I_a + I_{2,a}}\right)$$
$$\cong \frac{C_{\mathrm{int}}\left(V_{comp1,a} - V_{comp2,a} + V_{c1,a} - V_{c2,a}\right)}{I}\left(2 + \frac{I_{1,a} + I_{2,a}}{I}\right) \qquad (5\text{-}10)$$

The approximation is allowed when $I_1=I_2=I$ and $I>>I_a$. This last condition is met when small values for I_a are considered, as is the case for noise. The period $T_{mod,a}$ depends on $V_{c1,a}$ and $V_{c2,a}$ so the period is sensitive to 1/f noise of the noise voltages $u_{nc1,a}$ and $u_{nc2,a}$ of the comparators. The period also depends on $I_{1,a}$ and $I_{2,a}$, so the period is also sensitive to 1/f noise of $i_{n1,a}$ and $i_{n2,a}$. The period is not sensitive to 1/f noise of the non-chopped noise current $i_{n,a}$.
It can be shown that the period $T_{mod,b}$ of the modulator in Figure 5-12 b) is given by:

$$T_{\mathrm{mod},b} = \frac{C_{\mathrm{int}}\left(V_t - V_{t,b}\right)}{I + I_b} \tag{5-11}$$

The period is sensitive to 1/f noise from $u_{ni,b}$ and $i_{n,b}$. A chopped integration current is required to be insensitive to 1/f noise of $u_{ni,b}$, as is applied in the modulator shown in a).
We are now able to give recommendations to design a modulator which is insensitive to 1/f noise. These are:

- Use only one comparator.
- The integration current should be a square wave.
- Do not permit chopped noise currents at the input of the integrator.

5.1.5 Minimum and maximum frequency

The operating frequencies of the modulator are mainly determined by the frequencies of the interfering signals. The highest useful modulator frequency is related to the high-frequency poles of the modulator's active parts. The corresponding bandwidth should be sufficiently below the frequency of the microcontroller interference (several MHz) to filter the microcontroller interference. As a guideline, we keep the bandwidth at least 10 times smaller, resulting in several 100kHz which results in modulator frequencies below 100kHz.
However, the LF interference from the mains supply, having frequencies of 50 or 60 Hz and higher harmonics up to 1kHz, is filtered by a system using an SC filter. For good LF suppression, the modulator frequency should be as high as possible. For the time being, we set the minimum modulator frequency to 10kHz.

5.1.6 Conclusion

The SSP consists of a first-order relaxation modulator. The main properties, requirements and characteristics are:

- PM based on modulation of the voltage across the integration capacitor.
- LF suppression based on an SC filter.
- Only one comparator used
- The integration current has a square wave form
- The noise current source i_n not to be disconnected from the integrator
- The useful frequency range amounts to 10kHz-100kHz

5.2 Modulator input stage

In the previous section, several modulator requirements were considered and some useful guidelines discussed. This section is on the input stage of the relaxation modulator, which is mainly determined by the signal from the sensing element and by the method to suppress low-

frequency interfering signals. We will derive filter models based on circuits, but also derive circuits based on filter models.

5.2.1 Resistive measurement

We focus on a resistive bridge where the physical signal is represented by the ratio of the output voltage V_x of the bridge and the current I_{bridge} through the bridge. This is the I-bridge, as shown in Figure 5-13. All four bridge resistors depend on a physical signal, but this is not required. A practical method to measure both I_{bridge} and V_x is to first convert the current I_{brige} into a reference voltage V_{ref} by means of a resistor R_{ref} and measure V_x and V_{ref}. I_{bridge} is periodically alternated (modulated) by the modulator to enable the suppression of LF interfering signals. The amplitude of the voltage V_{bridge} across the bridge is approximately V_{DD}, since $R_b >> R_{ref}$.

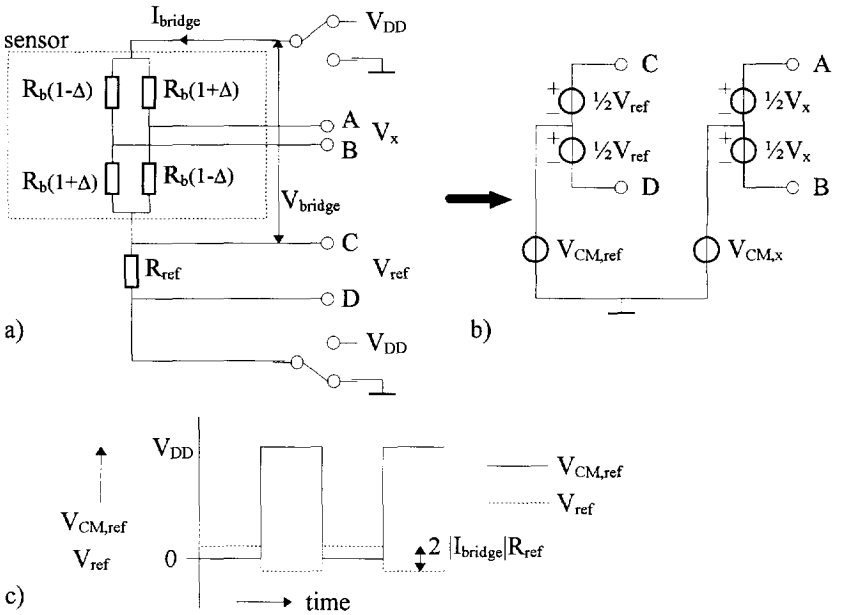

Figure 5-13. Measurement setup (a) and model (b) of a resistive I-bridge in series with a reference resistor. Figure c) shows wave forms of $V_{CM,ref}$ and V_{ref}.

The bridge in combination with R_{ref} can be modeled by common mode (CM) and differential mode (DM) voltage sources, which are defined by:

$$V_{DM} = V_A - V_B$$
$$V_{CM} = \frac{1}{2}(V_A + V_B) \qquad (5\text{-}12)$$

The same also holds for nodal voltages V_C and V_D. Figure 5-13c shows the wave forms of V_{ref} and $V_{CM,ref}$. When V_{ref} is measured, we have to deal with the CM signal $V_{CM,ref}$. The amplitude of V_{ref} equals $|I_{bridge}R_{ref}|$. The plot shows that $V_{CM,ref}$ makes a step change from 0 to V_{DD}. This is not completely true. In fact, the actual amplitude of $V_{CM,ref}$ is not important but this plot is used

to show the large amplitude difference of V_{ref} and $V_{CM,ref}$. It is interesting to see $V_{CM,ref}$ has an equal period as V_{ref}. Also the phase difference is zero.
Some practical peak-to-peak amplitudes for V_{ref} and $V_{CM,ref}$ are 0.2V and 5V respectively.
The LF interference can also be modeled by CM and DM voltage sources. Figure 5-14 shows a typical model of the sensor for a resistive measurement. It contains LF DM and LF CM disturbing signals, modeled by $V_{LF,DM}$ and $V_{LF,CM}$ respectively. The signal to be measured in Figure 5-14 is V_x, but this should be replaced by V_{ref} during a reference measurement phase. The CM signal is modeled by V_{CM}, representing $V_{CM,x}$ or $V_{CM,ref}$.

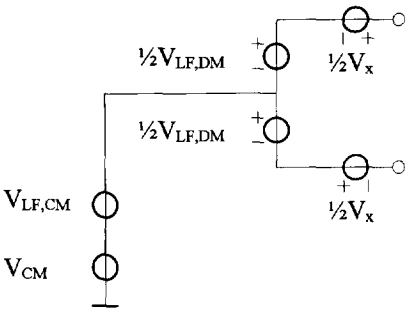

Figure 5-14. Typical model of a resistive measurement during the signal measurement phase. The voltage V_x should be replaced by V_{ref} during the reference measurement phase. The CM signal is modeled by V_{CM}, representing $V_{CM,x}$ or $V_{CM,ref}$.

Inspection of Figure 5-14 shows that the voltage V_x contains three disturbing voltages:
1. A CM voltage V_{CM} with the same wave form as V_x. The phase difference between V_{CM} and V_x is zero and the amplitudes are different.
2. A DM LF disturbing voltage $V_{LF,DM}$
3. A CM LF disturbing voltage $V_{LF,CM}$

We directly couple the circuit in Figure 5-14 to the input stage of the modulator. In previous discussions, it was shown that modulation of the period (PM) should be used. This can be implemented by adding two capacitors $C_{s,i}$ and connecting V_x to these capacitors. We than obtain the circuit in Figure 5-15. When V_x makes a step change, charge will be dumped into the integrator. The integration of both currents $I_{int,i}$ gives the charge-to-time conversion. The required comparator is not shown, since we only focus on the input stage of the modulator. The common mode voltage of the output of the integrator is controlled by the CM feedback loop and is ideally independent of V_{CM} and $V_{LF,CM}$. This circuit uses the integration currents to change the CM output of V_{int}.

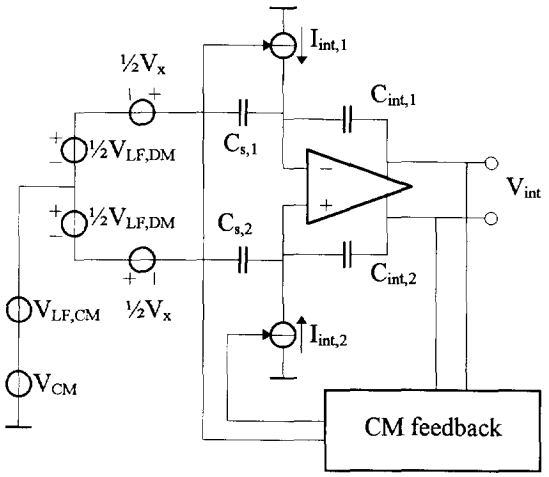

Figure 5-15. Coupling of the circuit in Figure 5-14 to the input stage of the modulator when period modulation (PM) is applied.

A problem related to this CM control loop is that its bandwidth must be very high, since the AC term of V_{CM} is a square wave. Another problem is that handling the large AC amplitude of V_{CM} requires a large control range. Further, the CMRR must be very high. With a peak-to-peak amplitude of V_x and V_{CM} of 0.2V and 5V respectively, the CMRR must be larger than 108dB to achieve an accuracy of 10^{-4}. These problems are difficult to solve.

A simple solution to the CM problems is to prevent the CM voltage from entering the integrator. This can be achieved by inserting switches between $C_{s,i}$ (Figure 5-15) and the integrator. This is shown in Figure 5-16. $C_{s,i}$ are temporarily disconnected (during phase φ_1) from the integrator just before a step change of V_{CM}. The large step change of V_{CM} is now stored on $C_{s,i}$. After this, $C_{s,i}$ are reconnected (phase φ_2) to the integrator and both capacitors $C_{s,i}$ transfer a charge $\hat{V}_x C_{s,i}$ ($\hat{V}_x$ is the peak-to-peak amplitude of V_x) to the integrator. The required charge-to-time conversion is obtained by the integration of $I_{int,i}$, where the alternation of V_x requires that $I_{int,i}$ are also chopped. Since V_{CM} is handled before the integrator, a CM control loop is not required to suppress V_{CM}. In practice, a CM feedback loop is required for the bias and this loop can also be used to suppress $V_{LF,CM}$. Since this loop has to suppress only slow-varying and small signals, the constraints to this loop are very much relaxed in comparison with the loop to suppress V_{CM} (in Figure 5-15).

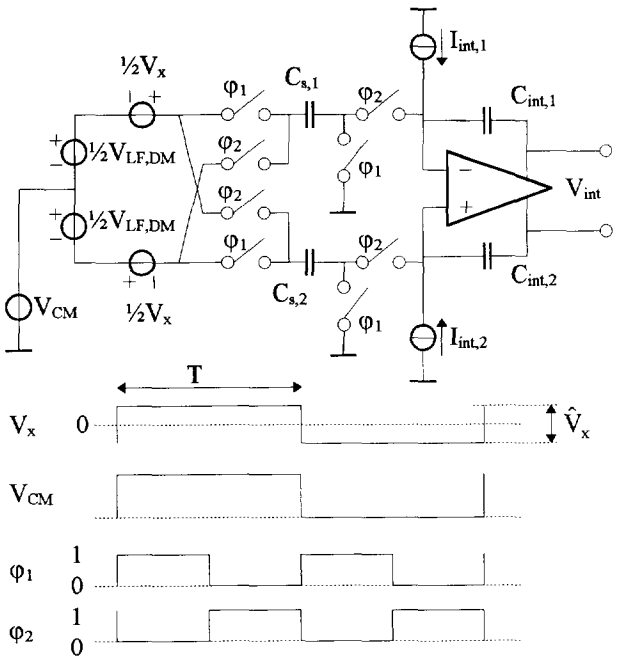

Figure 5-16. Coupling of the circuit in Figure 5-14 to the integrator via switches to prevent the voltage V_{CM} from entering the integrator.

Another solution to the CM problems is to shunt the integration capacitors $C_{int,i}$ in Figure 5-15 by switches. This is allowed, since a continuous integration is not required. These switches are operated periodically. They are closed (conducting) during the step change of V_{CM}. In this case, a CM feedback loop to handle V_{CM} is also not required. A disadvantage of this system is that an extra time block is necessary to define the time moment when these switches can be opened. This time block can be implemented by an extra relaxation modulator. We do not consider this solution.

Suppression of LF interference

We now discuss the suppression of LF interfering signals and derive a filter model based on the circuits discussed above.

We focus only on the DM signal, since the LF CM signal $V_{LF,CM}$ can be suppressed easily by the (simple) CM feedback loop for the bias. The DM signal cannot be suppressed by choosing a differential topology in combination with a feedback loop, but requires some sort of filtering. Suppose the DM signal causes a change ΔT_{mod} of the modulator period. The signal-to-interference ratio SIR_{mod} of the modulator can be defined as the ratio of the period T_{mod} and the maximum change $\Delta T_{mod,max}$ of the period: $SIR_{mod}=T_{mod}/\Delta T_{mod,max}$. We start analyzing the suppression by generating a small signal model. Since small signals affect the modulator period only very little, we model the modulator by a Switched-Capacitor filter, operated at a fixed clock frequency. This is shown in Figure 5-17. The signal-to-interference ratio of the SC filter is given by SIR_{SC} and equals the signal-to-interference ratio of V_{int}. For small interfering signals, both signal-to-interference ratios are equal:

$$SIR_{mod} = SIR_{SC} \tag{5-13}$$

The DC voltage V_i, representing the physical signal, is multiplied alternately by 1 and -1 (modulation by a square wave with period 2T), resulting in V_x. This is required to enable the synchronous detection as discussed in Figure 5-7. Note that the filter model as shown in Figure 5-17 implements the synchronous detection of that shown in Figure 5-7b. The mixer at the input of the integrator models the chopping of the integration current. We consider a single-sided model for the sake of simplicity.

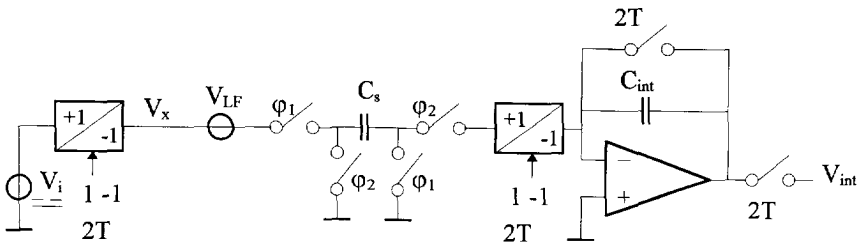

Figure 5-17. Filter model based on the circuit in Figure 5-16 to investigate the suppression of V_{LF}. The suppression is based on an SC filter operating on a fixed clock frequency. We consider a single-sided model for the sake of simplicity.

We assume the ratio $C_s/C_{int}=1$. The relation between V_{int} and V_{LF} in the time domain is than given by:

$$v_{int}[n] = v_{LF}[n] - v_{LF}[n-1] \tag{5-14}$$

where the minus sign originates from the modulation before the integrator. The sampling moments of the SC filter are equidistant, allowing the translation of an expression in the z-domain to the frequency domain. The two-times subsampling at the output of the integrator causes a decrease of the gain by 2. The hold function of the integrator compensates for this gain change. The transfer function $V_{int}(z)/V_{LF}(z)$ is given by $H_1(z)$:

$$H_1(z) = 1 - z^{-1} \tag{5-15}$$

Translation of (5-15) to the frequency domain results in $H_1(e^{j\omega T})$:

$$H_1\left(e^{j\omega T}\right) = 2j\exp\left(-\frac{j\omega T}{2}\right)\sin\left(\frac{\omega T}{2}\right) \tag{5-16}$$

The modulus of $H_1(e^{j\omega T})$ is depicted in Figure 5-18.

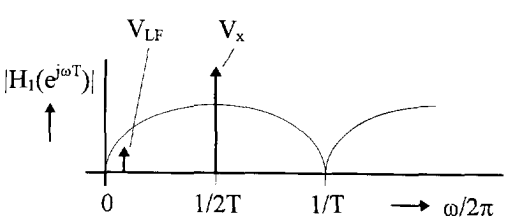

Figure 5-18. Modulus of the transfer $H_1(e^{j\omega T})$.

The frequency of V_x is located at the maximum of the sine function and passes the filter. The frequency of the LF interference is located near zero and is filtered.

5.2.2 Capacitive measurement

A typical capacitive measurement is shown in Figure 5-19a. We consider for the time being only capacitors with one common electrode. The capacitors are measured by applying the two-port measurement technique (in this case: voltage excitation and short-circuit current measurement). The voltage V_{LF} models low-frequency interference and has a coupling to both electrodes of both capacitors. The interference which is coupled to the excitation electrode has no effect, but the interference which is coupled to the other electrode is directly measured. We assume that the coupling capacitance C_{couple} equals $C_{ref}+C_x$. The circuit shown in Figure 5-19a can now be simplified into that shown in b). Note that a double-sided measurement setup cannot be applied here for the simple reason that we measure single capacitors.
The voltages on the transmitting electrodes, $V_{tr,ref}$ and $V_{tr,x}$, are square waves, as discussed in Chapter 3. Their peak-to-peak amplitudes equal $\hat{V}_{tr}$. The short-circuit current I_{cap} is processed to, for instance, an integrator. Note that a CM voltage is not present here, so no CM problems are to be expected.

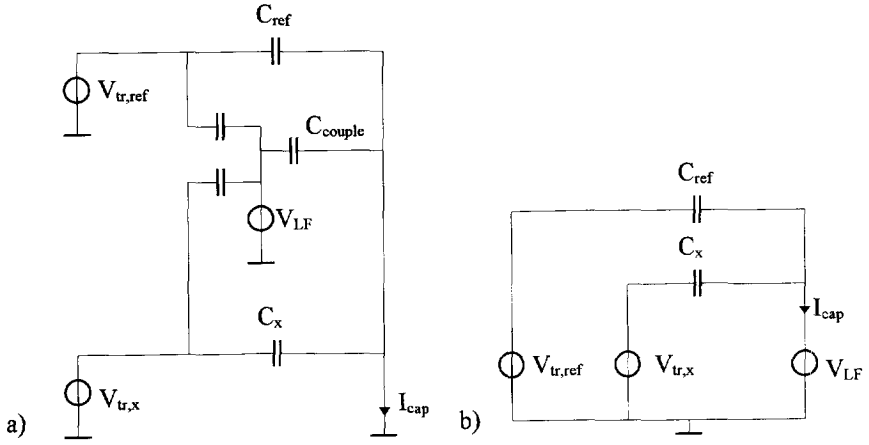

Figure 5-19. Typical setup of a capacitive measurement when the two-port technique is applied. (a) The voltage V_{LF} models low-frequency interference. We assume that $C_{couple}=C_{ref}+C_x$, so the circuit shown in a) can be simplified into the circuit shown in b).

When we couple the circuit in Figure 5-19b to the integrator of the relaxation modulator, we obtain the circuit shown in Figure 5-20a. Because of the step change of $V_{tr,x}$ (or $V_{tr,ref}$), a charge $\hat{V}_{tr} C_x$ is dumped into the integrator. The required charge-to-time conversion is obtained by the integration of I_{int}, which is a chopped current (Figure 5-20b). As shown in the following section, this circuit is part of the Modified Martin Modulator.

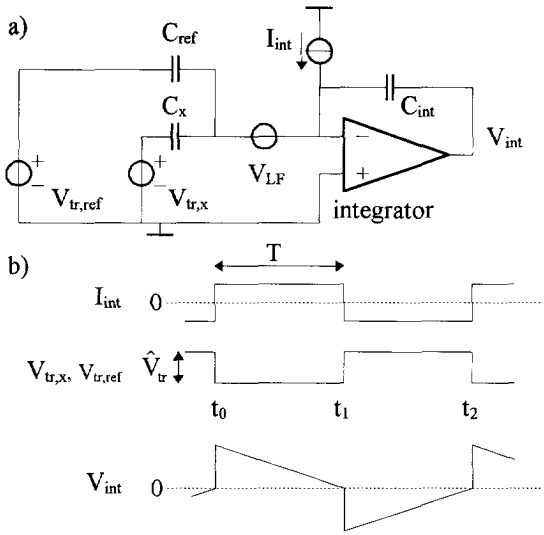

Figure 5-20. Possible measurement of capacitors: connection of the circuit in Figure 5-19 to an integrator (a) and some important signal patterns (b).

Suppression of LF interference

Here, we derive a model of the LF filter based on the circuit shown in Figure 5-20a. The suppression of LF interfering signals for capacitive measurement is somewhat different than it is for resistive measurements. In the case of resistive measurements, the LF voltage is sampled and stored in the integrator, whereas, in the case of this capacitive measurement, the LF voltage is firstly differentiated (by C_x+C_{ref}) before sampling and storing in the integrator. It is very easy to analyze this in the time domain. The LF voltage V_{LF} is assumed to be time dependent: $V_{LF}(t)$ During the first half of the modulator period (between t_0 and t_1; see Figure 5-20b), a charge proportional to $V_{LF}(t_1)$-$V_{LF}(t_0)$ causes this time interval to change whereas during the second half of the period (between t_1 and t_2) a charge proportional to $V_{LF}(t_2)$-$V_{LF}(t_1)$ causes the opposite effect. The difference between this measurement and the resistive measurement is the analog differentiation 1-exp(-sT). We can now easily derive the SC filter for capacitive measurements from Figure 5-17. This is shown in Figure 5-21.

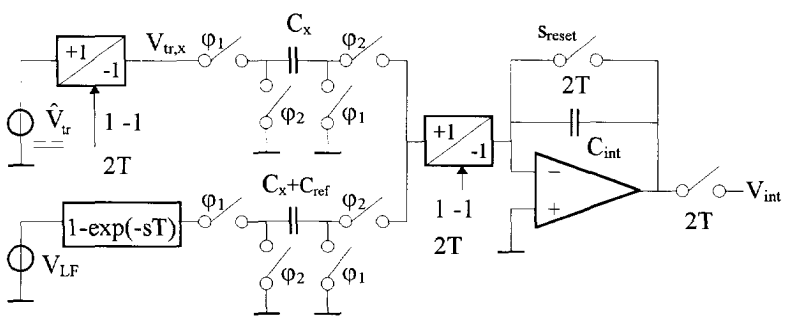

Figure 5-21. Model of the LF filter implemented by the circuit shown in Figure 5-20.

The transfer of V_{LF} to V_{int} corresponds in the z-domain to a filter with characteristic $G_2(z)$:

$$G_2(z) = \frac{C_x + C_{ref}}{C_{int}}\left(1 - 2z^{-1} + z^{-2}\right) = \frac{C_x + C_{ref}}{C_{int}}\left(1 - z^{-1}\right)^2 \quad (5\text{-}17)$$

Higher-order suppression

The filter described in Figure 5-21 has a second-order roll-off behavior for LF interference. The SC filter itself, implemented by $H_1(z)$, contributes one order to the total suppression. For a better suppression, a higher order of the filter can be used. We only permit SC filters with coefficients equal to 1 or -1. Other values of these coefficients result in non-equal modulator periods. This is considered to be undesirable. The SC filter contributes two orders of suppression when $H_2(z)$ is implemented, which is defined as:

$$H_2(z) = \left(1 - z^{-1}\right)\left(1 - z^{-2}\right) = 1 - z^{-1} - z^{-2} + z^{-3} \quad (5\text{-}18)$$

The function $H_2(e^{j\omega T})$ is given by:

$$H_2(e^{j\omega T}) = -4\exp\left(-\frac{3j\omega T}{2}\right)\sin\left(\tfrac{1}{2}\omega T\right)\sin(\omega T) \quad (5\text{-}19)$$

Implementing $H_2(z)$ in Figure 5-21 results in the SC filter as shown in Figure 5-22. The period of the control signal of the mixers becomes 4T. The mixers multiply (modulate) their inputs by the 1, -1, -1 and 1, alternately. This follows from (5-18).

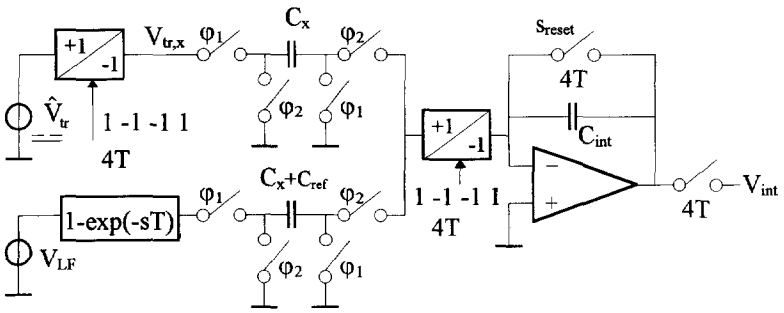

Figure 5-22. Model of the SC filter which is based on $H_2(z)$. Combination of this filter with an analog differentiation 1-exp(-sT) results in a third-order suppression of LF interfering signals.

Part of a modulator which implements the filter shown in Figure 5-22 is shown in Figure 5-23 [6]. The output voltage V_{va} of the capacitor-to-voltage (C-V) converter is sampled on C_s. Charge on this capacitor is transferred to the integrator. The desired charge-to-time conversion is obtained by the integration of I_{int}. The voltage V_{va} is the superposition of a signal and an interference part. The signal part is positive, negative, negative and positive successively during a time interval 4T. This is according to $H_2(z)$. The analog differentiation (for low frequencies) is implemented by switch s_r, operating of a frequency 1/T. The opening time of this switch equals T_1, where T_1 is the duration of phase φ_1. This results in the analog differentiation $1\text{-}\exp(-sT_1)$.

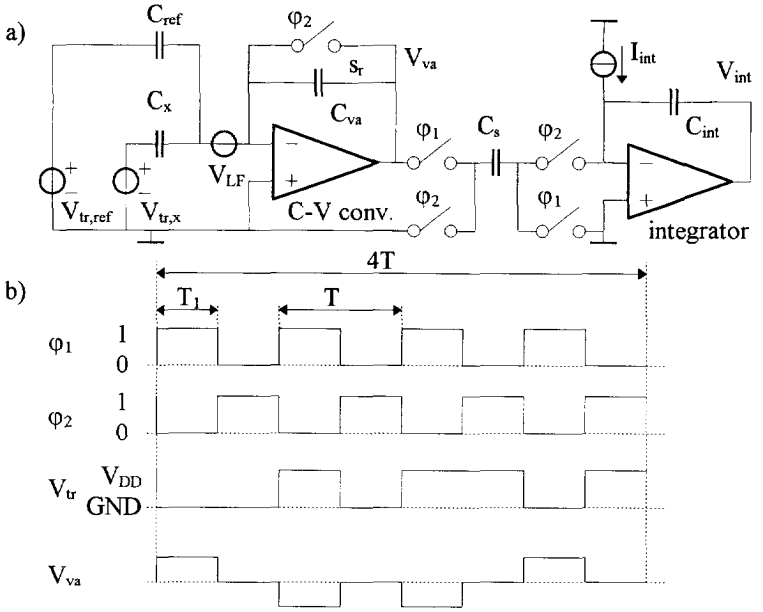

Figure 5-23. Part of a modulator which implements the filter in Figure 5-22 (a). The modulator has a third-order suppression for low-frequency interfering signals. Some relevant (control) signals of the modulator are shown in b).

We can further increase the suppression of the SC filter by using other SC filters. The SC filter, having coefficients 1 or -1, has a third-order suppression when the coefficients are determined by $H_3(z)$:

$$\begin{aligned} H_3(z) &= (1-z^{-1})(1-z^{-2})(1-z^{-4}) \\ &= 1-z^{-1}-z^{-2}+z^{-3}-z^{-4}+z^{-5}+z^{-6}-z^{-7} \end{aligned} \tag{5-20}$$

Note that a seventh-order SC filter is required to obtain a third-order LF suppression.
A filter resulting in a suppression of order P can be achieved by applying $H_P(z)$:

$$H_P(z) = \prod_{k=0}^{P-1}\left(1-z^{-2^k}\right) \tag{5-21}$$

These filters are considered in the following section.

5.3 Choice of relaxation modulator

Many different frequency converters have been realized. These converters convert capacitances, voltages, resistors, currents etc. into a frequency. We will not discuss all of them, but only a few of these which might fit into our concept. Gilbert's [7] voltage-to-frequency converter is based on a DC voltage-to-current converter. Its output current is used to charge and discharge a capacitor between two reference levels. Problems related to this converter are the use of DC inputs (no LF suppression) and the fact that IPM has been applied. Abidi's [8] VCO is linearized with a Switched-Capacitor feedback loop. This results in high-linear frequency converters. The main disadvantage of this topology is the presence of an LF time

constant, thus preventing the modulator from making a step change of the period. This problem cannot be solved in the way discussed in 5.1.3.1, where a step change of the period does not result in a transient at the output of the LPF. Other interesting converters [9,10,11,12] require an extra clock frequency for the conversion and can, therefore, not be used in our application. Since all these frequency converters, though they are very interesting, have one or more disadvantages, we present the design of other converters. They are based on the discussion in the previous sections.

5.3.1 The Modified Martin Modulator

When a comparator and an extra offset capacitor C_{off} are added to the circuit shown in Figure 5-20 and the feedback loop to maintain oscillation is closed, we obtain the modulator shown in Figure 5-24. Also shown the phase selection which is required to apply the three-signal technique. This modulator is known as the Modified Martin Modulator [13], which is based on the relaxation oscillator by Martin [14].

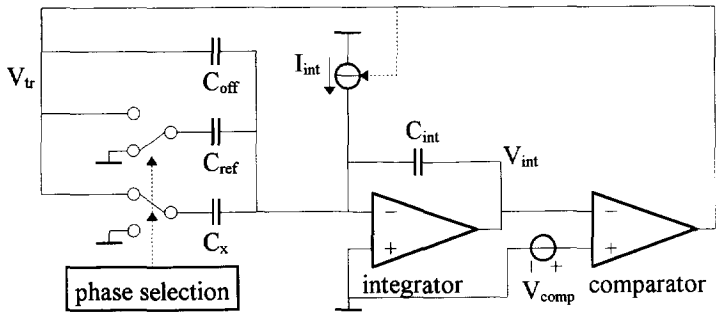

Figure 5-24. The Modified Martin Modulator, adapted to apply the three-signal technique.

The output of the comparator V_{tr} is directly applied on the transmitting electrodes and controls the current I_{int}. A capacitor C_{off} injects charge into the integrator in parallel with C_{ref} or C_x. This ensures proper oscillation when C_x is zero. Three different measurement phases are selected successively, according to the three-signal technique. During these phases, C_{off}, $C_{off}+C_{ref}$ and $C_{off}+C_x$ are measured successively. Some signals are shown in Figure 5-25.

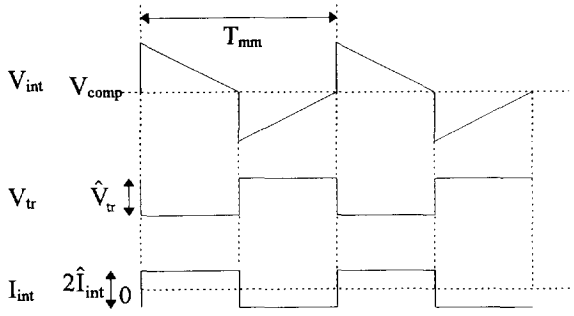

Figure 5-25. Signals in the Modified Martin Modulator.

The period of the Modified Martin Modulator $T_{mm,x}$ during the measurement of C_x is given by:

$$T_{mm,x} = 2\frac{\hat{V}_{tr}\left(C_x + C_{off}\right)}{\hat{I}_{\text{int}}} \tag{5-22}$$

where $\hat{V}_{tr}$ is the peak-to-peak amplitude of V_{tr} and $\hat{I}_{\text{int}}$ the amplitude of I_{int}.
The Martin Modulator is very suitable to measure capacitors [15,16,17]. With a full measurement range of 2pF, the articles reported a nonlinearity of 14 bits and a resolution of 10aF (almost 18 bits) within a measurement time of 100ms.

The Modified Martin Modulator has some disadvantages. These are:
It is less suitable for resistive measurement. The connection of the resistors to the integrator will then be the same as that shown in Figure 5-15. Problems related to this circuit were the handling of CM signals.
The suppression of LF interfering signals is not very high and can be improved.
The modulator discussed in the following section does not have these disadvantages. This modulator performs both resistive and capacitive measurements without CM problems and has better LF suppression.

5.3.2 The Multiple-Sensor Modulator

A new modulator, suited for all our applications of interest is discussed below. The modulator has an improved LF suppression and is referred to as a Multiple-Sensor Modulator.
Its main properties are:

- Large CM voltages during resistive measurement can be handled. Handling of the CM voltage is based on the circuit shown in Figure 5-16.
- The filtering of LF interference is based on synchronous detection with an LPF (see Figure 5-7 b). The transfer function of this filter in the z-domain is given by $H_2(z)$ in (5-18).
- Capacitive measurements are based on the circuit in Figure 5-23. The circuit has a third-order suppression for low-frequency interfering signals. This suppression is based on a combination of $H_2(z)$ and the differentiation $1-\exp(-sT_1)$.
- The sensitivity of the period to 1/f noise is very small.

The single-sided Multiple-Sensor Modulator is depicted in Figure 5-26. The modulator itself controls all switches and sources and provides the signal for the microcontroller.

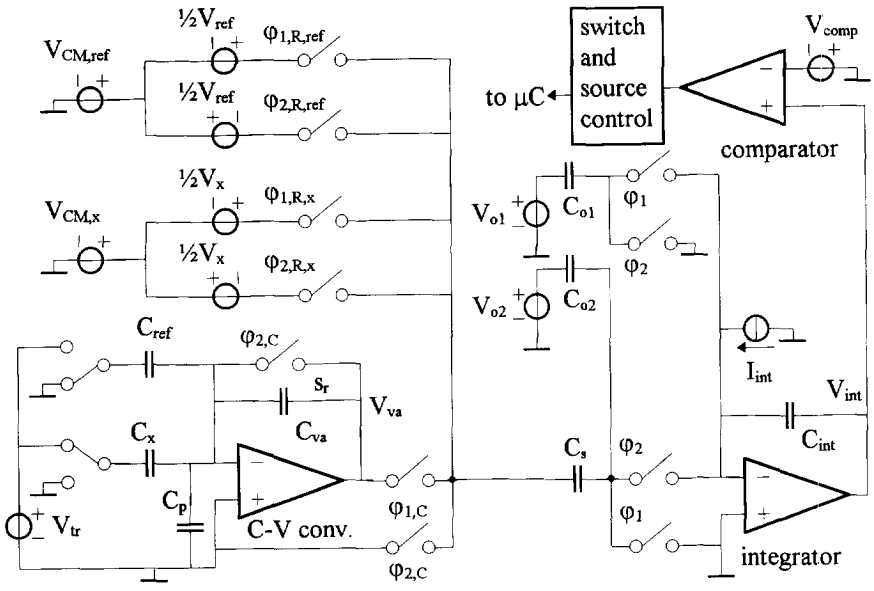

Figure 5-26. The Multiple-Sensor Modulator. All switches and sources are controlled by the modulator itself.

The modulator consists of an integrator followed by a comparator. The AC current I_{int} with amplitude $\hat{I}_{int}$ is continuously being integrated. Switches with control signals $\varphi_{i,C}$ are only active during capacitive measurements, while switches with control signals $\varphi_{i,R,x}$ and $\varphi_{i,R,ref}$ are only active during resistive measurements. The clock phases φ_1 and φ_2, corresponding to the time intervals $T_{1,i}$ and $T_{2,i}$ as shown in Figure 5-27, respectively, are generated internally. Charge is dumped into the integrator at the beginning of every time interval. The charge-to-time conversion is obtained by the integration of I_{int}. At the beginning of $T_{1,i}$ (φ_1), only C_{o1} dumps charge into the integrator, while C_{o2}+C_s dump charge into the integrator at the beginning of $T_{2,i}$ (φ_2). This ensures proper oscillation even when the input signals (C_x or V_x) are zero or negative. The capacitance C_p at the input of the capacitance-to-voltage (C-V) converter models the parasitic capacitance of the connecting cables of the capacitive sensing elements.

One period consists of four time intervals $T_{sub,1}..T_{sub,4}$. This corresponds to four samples, as defined by $H_2(z)$. Every time interval $T_{sub,i}$ consists of two separate time intervals $T_{1,i}$ and $T_{2,i}$. Figure 5-27 shows all relevant signals.

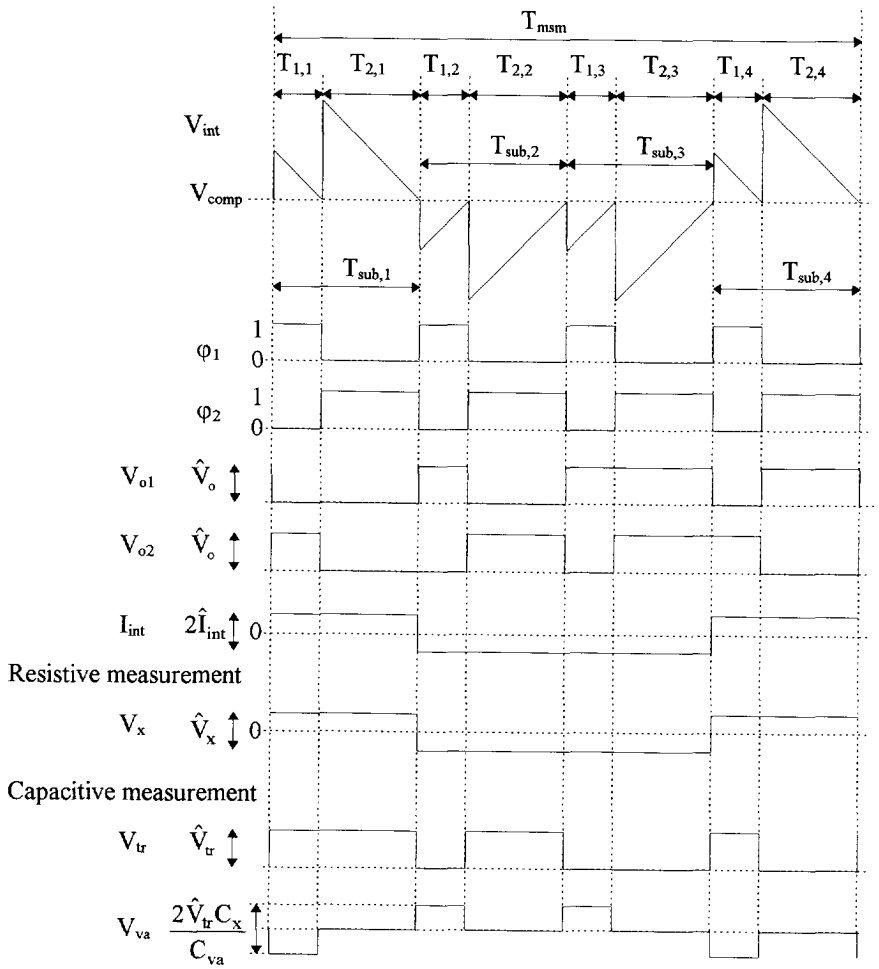

Figure 5-27. Relevant signal levels and control signals in the Multiple-Sensor Modulator for resistive and capacitive measurements.

Resistive measurement

During resistive measurements, the voltages V_x and V_{ref} are measured successively in time, selected by the modulator itself. The period T_{msm} during the (resistive) measurement of V_x is given by $T_{msm,Vx}$:

$$T_{msm,V_x} = 4\frac{\hat{V}_x C_s + \hat{V}_o\left(C_{o1} + C_{o2}\right)}{\hat{I}_{int}} \qquad (5\text{-}23)$$

where $\hat{V}_x$ models the amplitude of V_x and $\hat{V}_o$ the peak-to-peak amplitude of V_{o1} and V_{o2}. $\hat{I}_{int}$ equals the amplitude of I_{int}. A similar expression can be derived for the period $T_{msm,R,Vref}$ when V_{ref} is measured.

Capacitive measurement

During capacitive measurements, C_x and C_{ref} are measured successively in time. By multiplexing the voltage V_{tr}, the modulator is able to select a capacitor. Since only one voltage

is used to drive both C_{ref} and C_x, it becomes a multiplicative term which is eliminated by the three-signal technique. The period during the measurement of C_x is given by $T_{msm,Cx}$:

$$T_{msm,C_x} = 4\frac{\hat{V}_{tr}C_x\frac{C_s}{C_{va}} + \hat{V}_o(C_{o1} + C_{o2})}{\hat{I}_{\text{int}}} \tag{5-24}$$

where $\hat{V}_{tr}$ is the peak-to-peak amplitude of V_{tr}. A similar expression can be derived for $T_{msm,Cref}$ when C_{ref} is measured. The function of switch s_r is twofold: it biases the amplifier and it contributes to the LF suppression. The application of the C-V converter, used during capacitive measurements, has several advantages. These are:

- The suppression of LF interfering signals has been improved.
- The effect of C_p on the nonlinearity can be eliminated.
- A resistive leakage in parallel with C_x or C_{ref} forms a multiplicative factor, which will be eliminated by the three-signal technique.

5.3.3 Conclusion

Two modulators have been discussed in this section. The very simple Modified Martin Modulator is very suitable to measure capacitors, but has some problems with resistive measurement. The Multiple-Sensor Modulator is capable of measuring all our applications of interest and has an improved low-frequency suppression. This is analyzed in the following section.

5.4 Analysis of low-frequency suppression

We here discuss the sensitivity of the period of the Multiple-Sensor Modulator to LF interfering signals, like interference from the mains supply.
In the previous section, LF suppression was considered as if the modulator behaves like a SC filter which is controlled by a fixed clock frequency. This assumption results in equidistant sampling moments, allowing the translation of an expression in the z-domain into the frequency domain. Since the modulator itself controls the SC filter, the sampling moments depend on the interference. This results in a reduced suppression of large interfering signals. In addition to large interfering signals, nonidealities of the modulator also cause a reduction of the suppression. The most important nonideality is mismatch between the positive and negative value of the integration current I_{int}.

5.4.1 Small-signal behavior.

This section is on the small-signal suppression of LF interfering signals for resistive and capacitive measurements.

5.4.1.1 Resistive measurements

LF interference is suppressed by the SC filter as shown in Figure 5-17. We assume the ratio $C_s/C_{int}=1$. The SC filter is described by $H_2(z)$:

$$\begin{aligned} H_2(z) &= \left(1 - z^{-1}\right)\left(1 - z^{-2}\right) \\ &= 1 - z^{-1} - z^{-2} + z^{-3} \end{aligned} \tag{5-25}$$

When a measurement phase consists of N periods, the sequence of the moving average filter is given by $H_{2,N}(z)$:

$$\begin{aligned} H_{2,N}(z) &= \left(1-z^{-1}\right)\left(1-z^{-2}\right)\left(1+z^{-4}+z^{-8}+\ldots+z^{-4(N-1)}\right) \\ &= \left(1-z^{-1}\right)\left(1-z^{-2}\right)\sum_{k=0}^{N-1} z^{-4k} \end{aligned} \tag{5-26}$$

With the aid of

$$\sum_{k=0}^{N-1} z^{-4k} = \frac{1-z^{-4N}}{1-z^{-4}} \tag{5-27}$$

it is possible to write (5-26) in closed form:

$$H_{2,N}(z) = \frac{\left(1-z^{-1}\right)\left(1-z^{-2}\right)\left(1-z^{-4N}\right)}{1-z^{-4}} \tag{5-28}$$

Since we are only interested in the output of $H_{2,N}(z)$ after 4N samples, the filter $H_{2,N}(z)$ is followed by a 4N decimation stage. The decimation stage in its turn is followed by a 4N hold stage, which is a property of the modulator in the time domain. This is shown in Figure 5-28. The gain of this hold stage exactly compensates for the gain of the decimation stage. It is therefore allowed to consider the signal and the interference in V_{int}.

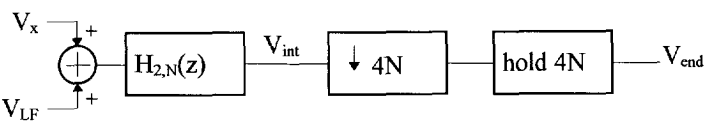

Figure 5-28. $H_{2,N}(z)$ followed by a 4N decimation stage and a 4N hold stage.

The modulus of the frequency transfer of the ratio V_{int}/V_{LF} is given by $|H_{2,N}(e^{j\omega Tsub})|$:

$$\left|H_{2,N}\left(e^{j\omega T_{sub}}\right)\right| = \left|4\sin\left(\tfrac{1}{2}\omega T_{sub}\right)\sin\left(\omega T_{sub}\right)\frac{\sin\left(2N\omega T_{sub}\right)}{\sin\left(2\omega T_{sub}\right)}\right| \tag{5-29}$$

The modulus of the ratio V_{int}/V_x after N periods is given by:

$$\left.\frac{V_{\text{int}}}{V_x}\right|_{N\ periods} = 4N \tag{5-30}$$

This ratio does not depend on the frequency. The residue of V_{LF} relative to V_x after N periods is now given by $R_{R,2,N}(\omega)$ and results from division of (5-29) by (5-30):

$$\left|R_{R,2,N}(\omega)\right| = \frac{\left|H_{2,N}\left(e^{j\omega T_{sub}}\right)\right|}{\left.\frac{V_{\text{int}}}{V_x}\right|_{N\ periods}} = \left|\frac{1}{N}\sin\left(\tfrac{1}{2}\omega T_{sub}\right)\sin\left(\omega T_{sub}\right)\frac{\sin\left(2N\omega T_{sub}\right)}{\sin\left(2\omega T_{sub}\right)}\right| \tag{5-31}$$

This is the reciprocal value of the suppression. The subscript 2 in $R_{R,2,N}(\omega)$ corresponds to the application of $H_2(z)$. Figure 5-29 shows plots of the modulus of $R_{R,2,N}(\omega)$ for two values of N (N=4 and N=8). Also shown is the modulus of $R_{R,3,N}(\omega)$, which is based on $H_3(z)$, for N=4. It is based on the same number of samples as $R_{R,2,N}(\omega)$ for N=8.

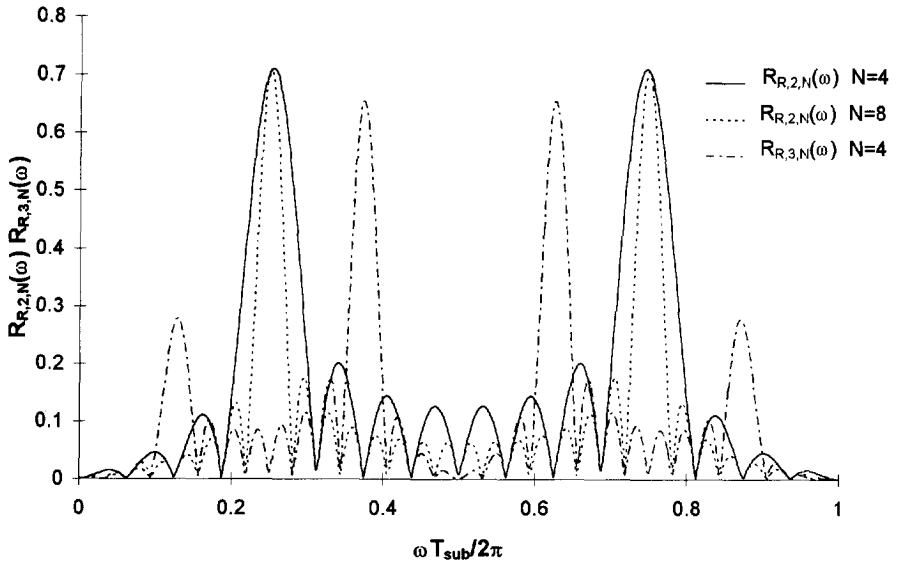

Figure 5-29. Relative residue $R_{R,2,N}(\omega)$ for N=4 and N=8 and $R_{R,3,N}(\omega)$ for N=4.

The plots given in Figure 5-30 show the relative residue for the low frequencies. This is the frequency range of interest.

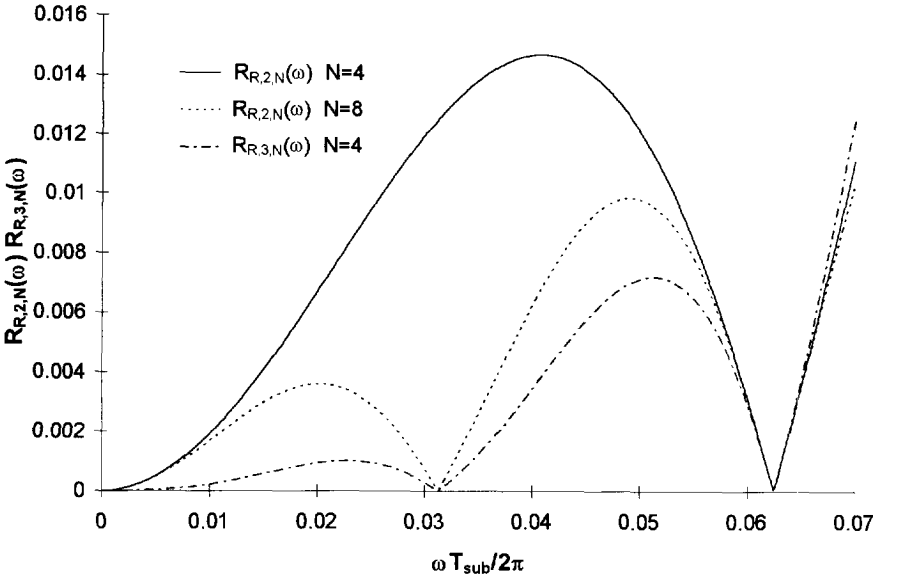

Figure 5-30. Low-frequency part of the plots given in Figure 5-29.

We clearly see the low values of $R_{R,2,N}(\omega)$ for low ω. This is the LF filtering we are looking for.

When $H_3(z)$ is implemented, the modulator has a larger sensitivity to LF 1/f noise than when $H_2(z)$ is implemented. This is because of the peak of $R_{R,3,N}(\omega)$ at $\omega T_{sub}/2\pi=1/8$. For this reason, implementation of $H_2(z)$ is to be preferred.
All plots in Figure 5-30 have a zero at $\omega T_{sub}/2\pi=0.062$, meaning that interfering signals with this frequency will be suppressed completely. However, when the sensing element forces another modulator frequency, the zero moves to another place. It is therefore better to focus on the envelope, which is a line connected to all peak values.
Due to offset charge from C_{o1} and C_{o2}, the value of $R_{R,2,N}(\omega)$ becomes smaller. This can be seen intuitively. When the offset charge is much larger than the charge on C_s (the period remains constant), the period becomes very stable. A problem is that the period can not be modulated in this case. The signal-to-interference ratio remains constant for different offsets. This effect of increased suppression is therefore not modeled in (5-31).
Expression (5-31) is based on an SC filter with a fixed clock frequency. Since T_{msm} is proportional to V_x and V_{LF}, the value of $R_{R,2,N}(\omega)$, multiplied by the amplitude ratio of V_{LF} and V_x, directly gives the relative error in the time domain for small amplitudes of V_{LF}.
To calculate the effect of the interference on the result obtained from the calculation related to the three-signal technique, which is the final measurement result, we have to include this calculation. However, the calculations become complex and do not give more insight into the problems. We therefore limit ourselves to the calculation of the error of just one measurement phase.

5.4.1.2 Capacitive measurements

The LF suppression for capacitive measurement is basically the same as for resistive measurements. The only difference is the extra differentiation $1-\exp(-sT_1)$ during capacitive measurements. The modulus of the small-signal suppression $R_{C,2,N}(\omega)$ for capacitive measurements can therefore be derived by multiplying (5-31) by $2\sin(\frac{1}{2}\omega T_1)$:

$$\left|R_{C,2,N}(\omega)\right| = \left|\frac{2}{N}\sin\left(\tfrac{1}{2}\omega T_1\right)\sin\left(\tfrac{1}{2}\omega T_{sub}\right)\sin\left(\omega T_{sub}\right)\frac{\sin\left(2N\omega T_{sub}\right)}{\sin\left(2\omega T_{sub}\right)}\right| \qquad (5\text{-}32)$$

5.4.2 Large-signal behavior

Below, we discuss the large-signal suppression of LF interfering signals for resistive and capacitive measurements.

5.4.2.1 Resistive measurements

The expression for $R_{R,2,N}(\omega)$ is not valid for large interfering amplitudes, since the sampling moments depend on the interference. The amplitude-dependent effects have been simulated by directly simulating the absolute value of the relative error $E_{R,2,N}(\omega,A)$ in the time domain, relative to the amplitude A of the interfering signal. The simulations were performed by simulating the modulator with a Pascal program.
Figure 5-31 depicts curves of $E_{R,2,N}(\omega,A)$ for three frequencies. The relative amplitude is the ratio of the amplitude of the interference and the amplitude of V_x (or V_{ref}). The value for T_{sub} is 50μs, so $\omega T_{sub}/2\pi$ for a 50 Hz signal amounts to $2.5\cdot10^{-3}$.

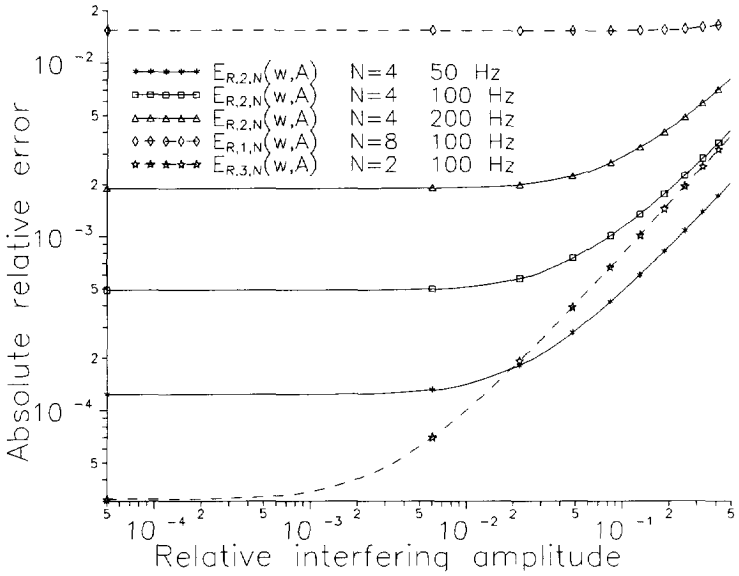

Figure 5-31. Simulated absolute relative error $E_{R,1,N}(\omega,A)$ in the time domain, relative to the amplitude A of the interfering signal for resistive measurements. The value for T_{sub} is 50μs. The plot shows three functions: $E_{R,1,N}(\omega,A)$ for N=8 (100 Hz), $E_{R,2,N}(\omega,A)$ for N=4 (50, 100 and 200 Hz) and $E_{R,3,N}(\omega,A)$ for N=2 (100 Hz).

The plot shows that the relative error increases for increasing amplitudes. This is the large-signal behavior. Example: A 50 Hz interfering signal with an amplitude of 0.5 times the amplitude of V_x has $E_{R,2,N}(\omega,A)=2\cdot10^{-3}$. The relative error in the time domain is then 10^{-3}.
The absolute relative error for small interfering signals is the same as discussed in 5.4.1. Consider, for instance, the absolute relative error for N=4 and $\omega=2\pi\cdot100$. The value for $E_{R,2,N}(2\pi\cdot100,A)=5\cdot10^{-4}$. Substitution of $\omega=2\pi\cdot100$, $T_{sub}=50\mu s$ and N=4 in (5-31) results in the same value for $R_{R,2,N}(2\pi\cdot100)$ so small-signal and large-signal behavior are in agreement for small signals.
Also shown are plots of $E_{R,1,N}(\omega,A)$ and $E_{R,3,N}(\omega,A)$, which are based on $H_1(z)$ and $H_3(z)$ respectively. All simulations are based on 16 samples. The conclusion is that the filter based on $H_1(z)$, which corresponds to normal chopping, performs very badly. The filter based on $H_3(z)$ suppresses very well, but only for very small signals.
Note that the flat part of $E_{R,2,N}(\omega,A)$ corresponds to very low relative time errors and this can only be measured if the electronic noise level is very low. We will make this clear with an example. The curve $E_{R,2,4}(\omega,A)$ for a 100Hz interference is increased with respect to the small signal value when the relative amplitude is larger than 10^{-2}. The relative error in the time domain for this amplitude amounts to $1.2\cdot10^{-6}$. This is smaller than the jitter due to electronic noise on one measurement phase. The conclusion is that the flat parts of the curves of $E_{R,2,N}(\omega,A)$ cannot be measured within the measurement time of one measurement phase. For these reasons, application of $H_3(z)$ is not useful.

5.4.2.2 Capacitive measurements

The plot in Figure 5-32 shows the simulated relative error in the time domain for capacitive measurements. The simulations are based on the filters $H_1(z)$, $H_2(z)$ and $H_3(z)$, resulting in $E_{C,1,N}(\omega,A)$, $E_{C,2,N}(\omega,A)$ and $E_{C,3,N}(\omega,A)$ respectively. We used T_{sub}=50μs and T_1=10μs.

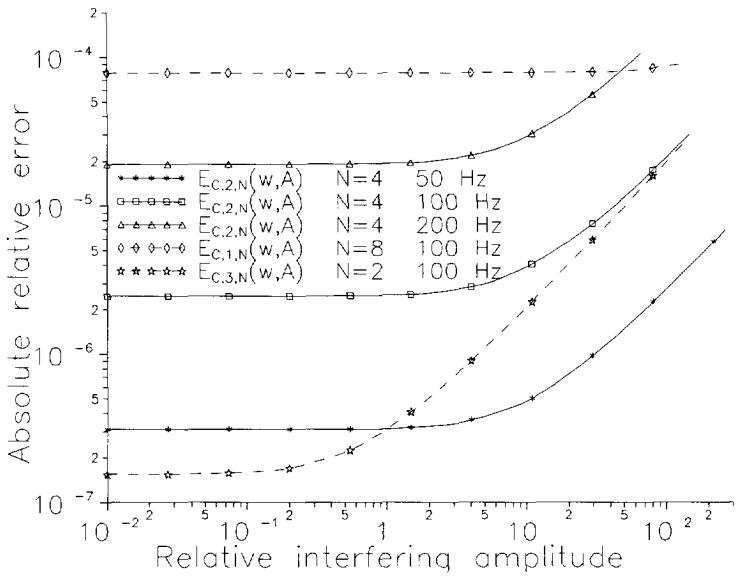

Figure 5-32. Simulated absolute relative error $E_{C,i,N}(\omega,A)$ in the time domain, relative to the interfering amplitude for capacitive measurements. The value for T_{sub} and T_1 are 50μs and 10μs respectively. The plot shows three functions: $E_{C,1,N}(\omega,A)$ for N=8 (100 Hz), $E_{C,2,N}(\omega,A)$ for N=4 (50, 100 and 200 Hz) and $E_{C,3,N}(\omega,A)$ for N=2 (100 Hz).

Example. The relative error of the filter based on $H_2(z)$ for a 50 Hz interfering signal with an amplitude of 100 times the amplitude of V_x is $2.7 \cdot 10^{-6}$, resulting in an error of $2.7 \cdot 10^{-4}$. This is very good.

The absolute relative error for small interfering signals agrees with the small-signal suppression. The flat parts of the curves for $E_{C,i,N}(\omega,A)$ can not be measured within the measurement time of one measurement phase, similar to resistive measurements.

5.4.2.3 Comparison of the Multiple-Sensor Modulator and the Modified Martin Modulator

It is very interesting to compare the Multiple-Sensor Modulator (based on $H_2(z)$) for capacitive measurements with the modified Martin modulator, which is also very suitable for measuring capacitors. We simulated the relative error in the time domain for both modulators having the same value of T_{sub} under the same conditions. (One period of the Modified Martin Modulator takes 2 time intervals T_{sub}). The results of the simulations are plotted in Figure 5-33. The number of the time intervals T_{sub} equals 16 and T_{sub}=50μs.

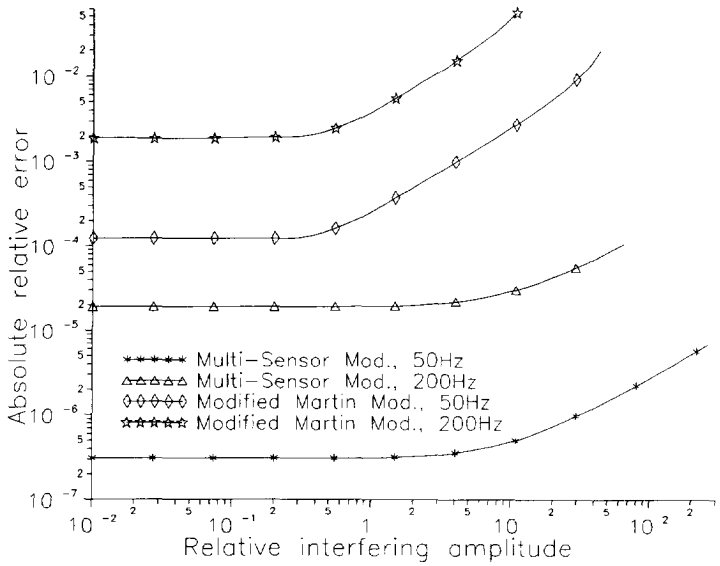

Figure 5-33. Simulated absolute relative error in the time domain for the Multiple-Sensor Modulator and the Modified Martin Modulator under the same conditions, both adapted for capacitive measurements.

It is clear that the Multiple-Sensor Modulator performs much better than the Modified Martin Modulator.

Example. The relative error in the time domain for the modified Martin modulator for an interfering signal having an amplitude of 10 times the amplitude of V_x is $5.2 \cdot 10^3$ times larger than for the Multiple-Sensor Modulator under the same conditions. This is a very large difference and is mainly caused by:

- The Multiple-Sensor Modulator has a third-order suppression, while the Modified Martin Modulator only has a second-order suppression. The absolute relative error for small signals is therefore different.
- The interference is coupled in the integrator of the Modified Martin Modulator as a current, whereas it is coupled in the integrator of the Multiple-Sensor Modulator as a voltage. The filtering is based on subtraction of the interfering signal in the time domain during the following period. Since the period is proportional to the interfering voltage, this subtraction will be effective as long as the interfering signal has not changed too much during the following period. The period is inversely proportional to the interfering current and subtraction in the time domain will not be effective. Due to this effect, the absolute relative error for the Modified Martin Modulator starts to increase for smaller interfering amplitudes.

5.4.3 Effects of modulator nonidealities on the suppression

The simulated values of the absolute relative error are based on an ideal modulator. An ideal modulator is a modulator having equidistant sampling moments in the absence of interference. A practical modulator shows nonequidistant sampling moments. This may be caused by the following nonidealities:

- different positive and negative values of the integration current I_{int}
- dead times

- switch charge injection (SCI) of the switches at the input of the integrator and of the reset switch s_r in the amplifier
- offset voltages
- hysteresis of the comparator

These effects influence the sampling moments and have a negative effect on the LF suppression. Note that all these effects form additive or multiplicative errors, so their effect on the final result M is eliminated by the three-signal technique. Table 5-1 shows the normalized values of the actual time intervals $T_{1,i}$ and $T_{2,i}$. Without interference, these time intervals have ideal values T_1 and T_2 respectively. We assume that $T_1=T_2$. Consider, for instance, dead time. A certain dead time causes a relative increase δ_1 of $T_{1,2}$. The effect on $T_{1,4}$ is exactly the same, while other time intervals remain constant. The table is based on the circuit in Figure 5-26.

	$T_{sub,1}$		$T_{sub,2}$		$T_{sub,3}$		$T_{sub,4}$	
Effect	$T_{1,1}$	$T_{2,1}$	$T_{1,2}$	$T_{2,2}$	$T_{1,3}$	$T_{2,3}$	$T_{1,4}$	$T_{2,4}$
Ideal modulator	1	1	1	1	1	1	1	1
Dead time	1	1	$1+\delta_1$	1	1	1	$1+\delta_1$	1
Hysteresis	1	1	$1+\delta_2$	1	1	1	$1+\delta_2$	1
Offset integrator	1	$1-\delta_3$	1	$1+\delta_3$	1	$1+\delta_3$	1	$1-\delta_3$
SCI s_r.	1	$1-\delta_4$	1	$1+\delta_4$	1	$1+\delta_4$	1	$1-\delta_4$
SCI s_i integrator	$1+\delta_5$	$1+\delta_5$	$1-\delta_5$	$1-\delta_5$	$1-\delta_5$	$1-\delta_5$	$1+\delta_5$	$1+\delta_5$
I_{int}-mismatch	$1+\delta_6$	$1+\delta_6$	$1-\delta_6$	$1-\delta_6$	$1-\delta_6$	$1-\delta_6$	$1+\delta_6$	$1+\delta_6$

Table 5-1. Relative deviation of the time intervals $T_{1,i}$ and $T_{2,i}$ for different effects.

We simulated all effects separately for a Multiple-Sensor Modulator (based on $H_2(z)$) for capacitive measurements. The ideal modulator in absence of interference has ideal values $T_1=T_2=10\mu s$, so the modulator operates at 12.5kHz. The interference is modeled by a 50Hz sine wave with an amplitude of 80 times the amplitude of V_{tr}. The simulated results, shown in Figure 5-34, display directly the absolute relative error in the time domain of one measurement phase for N=8 and can be denoted by $E_{C,2,N}(\omega,A,\delta)$.

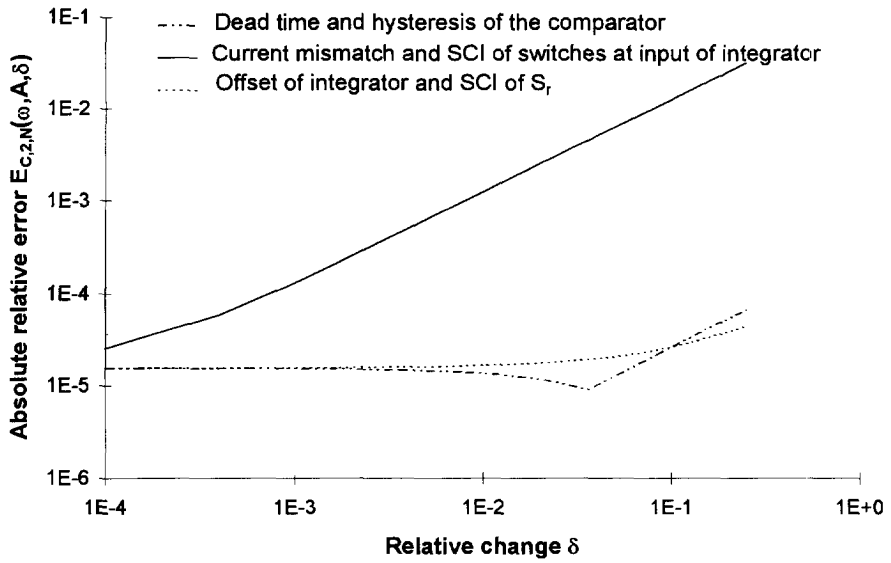

Figure 5-34. Absolute relative error in the time domain $E_{C,2,N}(\omega,A,\delta)$ (N=8) for the effects mentioned in Table 5-1. Every curve corresponds to two effects. The interfering signal is a 50Hz sine wave with an amplitude of 80 $\hat{V}_{tr}$ and $T_1=T_2=10\mu s$.

The absolute relative error in the ideal case (δ=0) amounts to $1.5\cdot10^{-5}$. This corresponds to the simulated absolute relative error $E_{C,2,N}(\omega,A)$ (see Figure 5-32) of an ideal modulator for $\omega=2\pi\cdot50$, A=80 $\hat{V}_{tr}$, T_{sub}=20μs and T_1=10μs. The plots in Figure 5-32 are based on T_{sub}=50μs and T_1=10μs. The value of $E_{C,2,4}(\omega,A)$ in Figure 5-32 for $\omega=2\pi\cdot50$ and A=80 $\hat{V}_{tr}$ amounts to $2\cdot10^{-6}$, resulting in a relative error in the time domain of $80\cdot2\cdot10^{-6}=1.6\cdot10^{-4}$. When T_{sub} is decreased to 20μs, this value becomes $1.5\cdot10^{-5}$.
Below, we discuss these effects and consider some practical values of relative changes δ_i.

Dead time
The dead time is the total dead time due to transition times. A practical value for the dead time is 500ns, resulting in δ_1=0.1. The absolute relative error $E_{C,2,N}(\omega,A,\delta)$ then amounts to $2.6\cdot10^{-5}$. The increase of the relative error is less than a factor two, so the conclusion is that the effect of dead times on the LF suppression is very small.

Hysteresis of the comparator
Hysteresis of the comparator behaves in a way similar to dead time. A hysteresis voltage of 10mV, V_{DD}=5V, C_{int}/C_{o1}=10 results in δ_2=0.02. The absolute relative error is barely increased.

Offset voltage of the integrator
The offset voltage of the integrator is sampled on C_s and results in a charge through C_{int} every time interval T_{sub}. Since the offset is not chopped, this charge flow consists of a DC component. With V_{DD}=5V, $C_{o1}=C_{o2}$, C_s/C_{o1}=30, and an offset voltage of 5mV, the value of δ_3 is 0.03. The absolute relative error is barely increased by an offset voltage.

Switch charge injection (SCI) from switch s_r

The reset switch s_r in the capacitance-to-voltage converter is closed during φ_2 and is opened during φ_1. Every time s_r opens, approximately half the channel charge flows through C_{va}. This is valid when the switch is opened fast. The resulting step voltage in V_{va} has for every time interval T_{sub} the same sign, so the effect is the same as the offset voltage of the integrator.

In a 1V-treshold CMOS process with oxide thickness of 20nm, operated at 5V, the switch s_r with L=1μm and W=10μm has a channel charge Q_{ox}=25fC. Combined with the charge from the gate-drain/source overlap capacitance of $2\cdot10^{-10}$F/m, $C_{va}=C_s$ and $C_{o1}=C_{o2}$=1pF, the value of δ_4 is $4.5\cdot10^{-3}$. The relative error is barely increased, so no special attention is needed here.

Switch charge injection (SCI) of switches at the input of the integrator

The switches s_1, s_2, s_3 and s_4 at the input of the integrator (see Figure 5-35) operate in Break-Before-Make (BBM) mode, as discussed in section 5.7.2.3. We assume that the control signals for the switches changes rapidly, so the channel charge of an MOS transistor is split into two equal parts, flowing through the switch terminals.

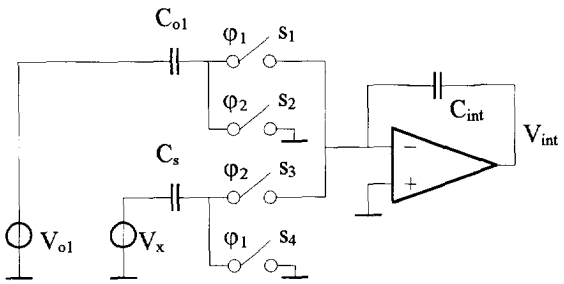

Figure 5-35. Switches at the input of the integrator of the Multiple-Sensor Modulator.

The sequence at the beginning of phase φ_1 is (see Figure 5-27):

1. Switches s_2 and s_3 open. Half of the channel charge $Q_{ox,3}$ from s_3 directly flows to C_{int} and $\frac{1}{2}Q_{ox,3}$ flows to C_s. For $Q_{ox,2}$ the same holds: $\frac{1}{2}Q_{ox,2}$ flows to C_{o1} and $\frac{1}{2}Q_{ox,2}$ to ground.
2. Switches s_1 and s_4 close. These switches now build charge in their channels. The charge $\frac{1}{2}Q_{ox,3}$ which is stored on C_s, flows to ground but $\frac{1}{2}Q_{ox,1}$ comes from C_{int}.

The theoretical result is that $\frac{1}{2}Q_{ox,1}$ fully compensates $\frac{1}{2}Q_{ox,3}$ if the switches have equal geometry. A similar compensation occurs at the beginning of φ_2.

Any mismatch or different behavior leads to a failure of the compensation. The result is that a constant charge is dumped into the integrator at the beginning of φ_1 and φ_2. The result is a change of $T_{sub,1}$ and $T_{sub,4}$ and an opposite change of $T_{sub,2}$ and $T_{sub,3}$.

The charge contribution of the overlap capacitances behaves the same as channel charge and can simply be added. If we take the same parameters as discussed before and a mismatch between the charges of s_1 and s_3 of 10%, δ_5 amounts to $4.5\cdot10^{-4}$. The relative error is increased almost 5 times with respect to the ideal modulator. The mismatch becomes important.

Since compensation will never be complete, it is wise to keep the channel charge as low as possible. The ON resistances of the switches is important in view of high-frequency poles. It is interesting to derive an expression of the channel charge Q_{ox} of a switch with a fixed ON-resistance R_{on}. By using strong-inversion equations, it follows that:

$$Q_{ox} = \frac{L^2}{\mu R_{on}} \qquad (5\text{-}33)$$

where μ is the mobility and L the length of the transistor. From (5-33) follows that a small-L process is useful to keep the channel charge small for a fixed ON-resistance. A small channel charge keeps the switch charge injection low and the LF suppression high.

Mismatch of the integration current.
Any mismatch between the positive and negative amplitude of the integration current I directly influences the time intervals T_{sub}. A 2% mismatch (δ_6=0.01) causes an decrease of the suppression by more than 100 times. It is, therefore, very important to keep the current mismatch very small. The suppression is only two times decreased in comparison with an ideal modulator for a current mismatch of $3 \cdot 10^{-4}$. We show in Chapter 6 how such a small mismatch can be realized.

5.4.4 Conclusion

The suppression of the LF interference has been analyzed in this section. The large-signal analysis showed a decrease of the suppression for large interfering signals and is in agreement with the small-signal analysis for small signals. Several nonidealities of the modulator, like switch charge injection, dead times, offset voltages etc., tend to further worsen the suppression. The nonideality causing the largest worsening is the matching of the integration current. To obtain accurately-matched currents requires special circuitry and this is discussed in Chapter 6.

5.5 Suppression of high-frequency interference

In this section, we discuss the suppression of high-frequency (HF) interfering signals. The main HF interference is the clock frequency from the microcontroller. This interference enters the SSP via the power supply lines or it is picked up by the sensing elements. Since the modulator is based on a relaxation oscillator, the HF interference is sampled. This can result in a measurement error and even in frequency locking effects. These effects has to be avoided, since the frequency is the carrier of the information.
Calculations of the HF suppression are complicated. This is partly caused by the fact that the substrate of the SSP chip is not an ideal ground, so transistors on the same chip cannot be completely shielded. This effect is hard to model.
The following measures can be taken to increase the HF suppression.

Filtering of the interference
A proven concept is low-pass filtering by, for instance, inserting an inductance in series with the power supply. Another form of filtering is keeping the bandwidth of the analog parts low compared to the frequency of the interference. This also holds for the sample switches, operating at the modulator frequency. Since these switches sample the interference, the bandwidth of the circuit before sampling, when the switch is conducting, must be low enough. This filters the HF interference.

Random sampling
If filtering is not sufficient to remove the HF interference, we can use another technique, based on random sampling. We therefore model the interference by the AC voltage source V_{HF} in Figure 5-36.

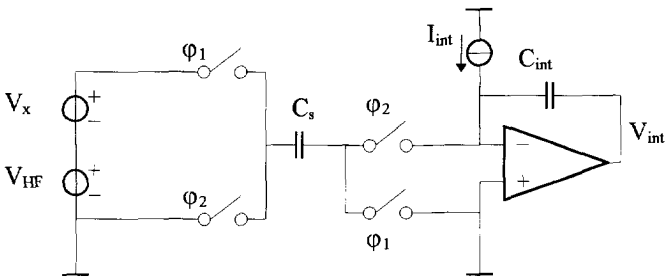

Figure 5-36. Model of the HF interference.

The voltage V_{HF} is sampled on C_s and processed to the integrator. Under certain circumstances, the modulator frequency is locked to the frequency of the interference. This means that a phase-locked loop (PLL) exists. When lock occurs, the sampled values of V_{HF} are constant for all samples. These constant samples cause a static frequency shift. A method to remove locking effects is to randomize the sampling moments by inserting noise into the PLL, thereby randomizing the samples of V_{HF}. In this case, a static frequency shift does not occur. The average of a lot of random samples of V_{HF} will tend to zero, so the modulator frequency is hardly shifted, thereby removing the locking effects. Note that the number of samples in one measurement phase will be up to 1024. J. Mulder [18] showed that the best method to randomize the sampling is by linearly increasing the time between successive samples (in the absence of interference). This can be obtained by increasing C_{o1} or C_{o2} every period, until a new measurement starts. When C_{o1} or C_{o2} is varied in the same way for all measurement phases, its effect is eliminated by the three-signal technique. The period of the Multiple-Sensor Modulator T_{msm} (shown in Figure 5-37) is not constant within a measurement phase, but shows a ramp now. Note that a measurement phase consists of 256 periods. For all measurement phases, the period T_{msm} increases by ΔT_{msm}. The optimal value of ΔT_{msm} is related to lock range: ΔT_{msm} needs to be just a little larger than the lock range.

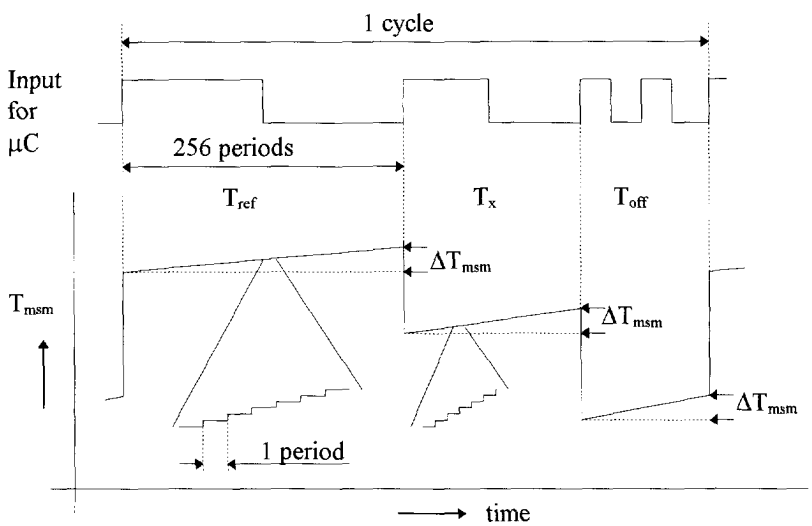

Figure 5-37. The period T_{msm} vs. time for three measurement phases. To reduce the effect of HF interference, the period within one phase increases by ΔT_{msm}.

It is important that C_{o1} and/or C_{o2} are changed at the end of a period and not at the end of a time interval T_{sub}. This is to ensure a good LF suppression.

Balancing
Another method to eliminate the effect of HF interference is to use balanced circuits. For instance, when the (single-sided) integrator picks up interference from the power supply, a symmetrical double-sided integrator would pick up an equal amount of interference in both channels, thereby turning the interference into a CM signal which can be eliminated.

Conclusion
The effect of HF interference can be the locking of the modulator frequency. Several methods, like low-pass filtering, balancing and random sampling, can be used to avoid this. The random sampling is based on inserting (nonstochastical) noise into a phase-locked loop.

5.6 Noise and resolution

The electronic noise of the Multiple-Sensor Modulator and the resulting resolution is discussed below. The electronic noise calculations include all types of noise sources that result in jitter of the modulator period, like thermal noise, shot noise, 1/f noise etc.

5.6.1 Noise sources and noise model

The circuit with the noise sources is depicted in Figure 5-38. The capacitor C_p models the parasitic capacitance of the cables whereas C_{pb} models the parasitic capacitance of C_s to the substrate.

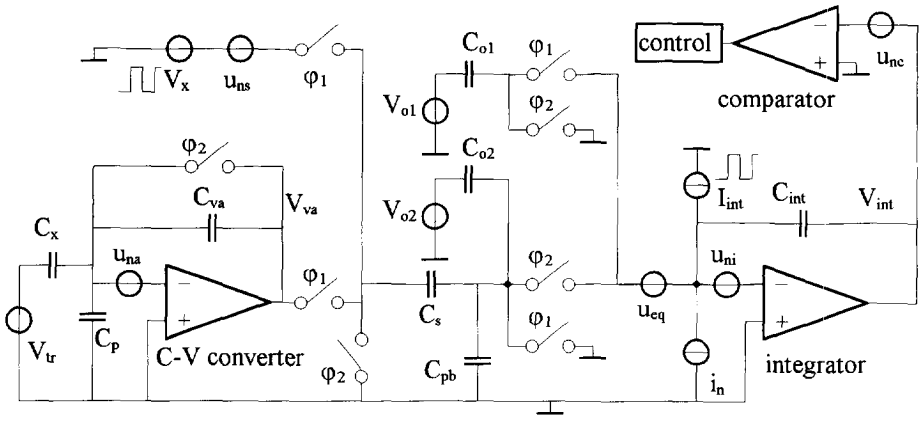

Figure 5-38. Noise sources in the Multiple-Sensor Modulator.

Figure 5-39 shows the output voltage V_{int} of the integrator and the clock phases φ_1 and φ_2.

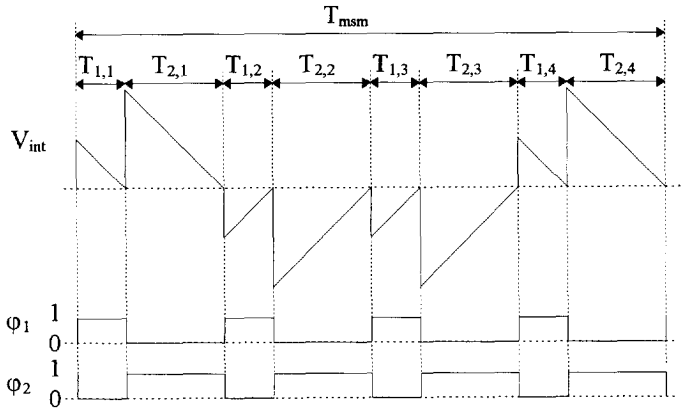

Figure 5-39. The output voltage V_{int} of the integrator and the clock phases φ_1 and φ_2.

The following noise sources are considered:

- noise voltage u_{ni} of the amplifier in the integrator
- noise voltage u_{ns} of the source
- noise current i_n at the input of the integrator
- noise voltage u_{nc} of the comparator
- noise voltage u_{na} of the amplifier of the capacitance-to-voltage (C-V) converter
- thermal noise of the ON resistance of the switches, resulting in kT/C noise

The noise calculations are based on the Bennet model [19]. Bennet showed that white noise can be described as the infinite sum of discrete sinusoidal components. These components have different frequency, equal amplitude and a random phase, which is uniformly distributed in the interval $[-\pi,\pi]$. The sum of the powers of the individual components equals the total power of the modeled noise source. By using this model, the effect of the noise on the resolution can be calculated in a simple way. We determine the influence of one Bennet component on N modulator periods and calculate the variance due to only one component. We then use all Bennet components to find the total variance, where we need the relation between the amplitude of the Bennet components and the Power Spectral Density (PSD). To handle 1/f noise, the amplitude of the Bennet components depends on the frequency.

5.6.2 The noise voltage of the integrator amplifier

Here, we only briefly discuss the effect of the noise voltage u_{ni} of the amplifier in the integrator. More details can be found in Appendix B.

According to the Bennet model, the noise source u_{ni} is modeled as the infinite sum of Bennet components. These components are given by:

$$\hat{u}_{ni}\cos(\omega t+\varphi) \tag{5-34}$$

where $\hat{u}_{ni}$ is the amplitude, ω the frequency and φ the random phase.

The noise voltage can be transferred into an equivalent noise voltage u_{eq} at the input of the integrator, as shown in Figure 5-38. This noise voltage is sampled at the end of phase φ_1 on C_{o1} and at the end of phase φ_2 on $C_s+C_{pb}+C_{o2}$. This results in a noise charge which is transferred to the integrator, causing a jitter of T_1 and T_2.

In Appendix B, an expression in the time domain for the duration of N noisy periods NT_{msm}' based on one Bennet component of u_{ni} has been derived:

$$NT_{msm}' = 4NT_{sub} + \frac{\hat{u}_{ni}C_{total}}{\hat{I}_{int}} \sum_{k=0}^{N-1} \left[\cos(4k\omega T_{sub} + \varphi) - \cos((4k+1)\omega T_{sub} + \varphi) - \cos((4k+2)\omega T_{sub} + \varphi) + \cos((4k+3)\omega T_{sub} + \varphi) \right] \quad (5\text{-}35)$$

where $T_{sub}=T_1+T_2$ and $C_{total}=C_s+C_{pb}+C_{int}=C_{o1}+C_{o2}$. With this expression, the variance $\rho_{ni}^2(\omega)$ of N periods due to the Bennet component in u_{ni} can be derived:

$$\rho_{ni}^2(\omega) = \frac{1}{2\pi} \int_{-\pi}^{\pi} \left(NT_{msm}' - \overline{NT_{msm}'} \right)^2 d\varphi = \left(\frac{\hat{u}_{ni}C_{total}}{\hat{I}_{int}} \right)^2 H_u(\omega) \quad (5\text{-}36)$$

The function $H_u(\omega)$ represents the sensitivity to certain frequencies. Figure 5-40 shows a plot of $H_u(\omega)$ for $\omega \in [0, 2\pi/T_{sub}]$ for N=2 and N=4. As can be seen, the low-frequency values of $H_u(\omega)$ are very small, representing a very small sensitivity to noise in this range (1/f noise).

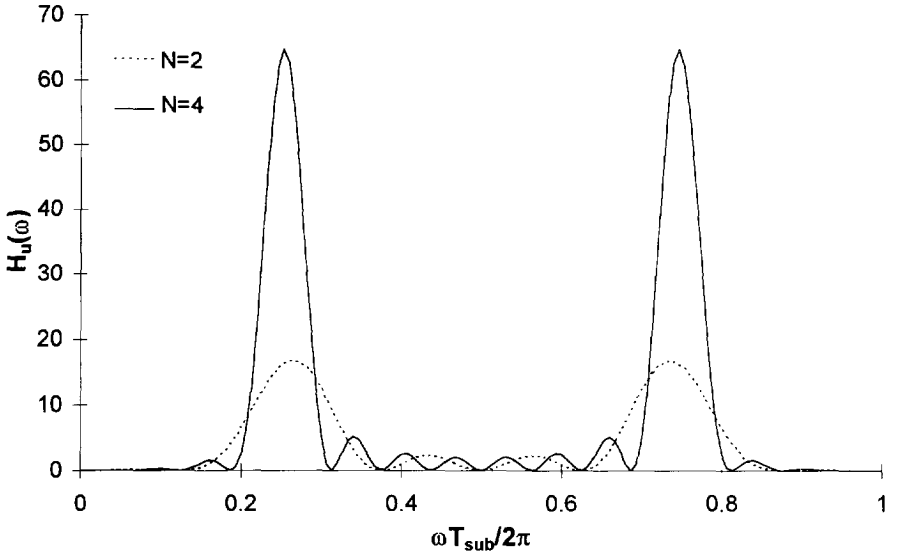

Figure 5-40. Sensitivity function $H_u(\omega)$ for noise voltage u_{ni} of the amplifier in the integrator for N=2 and N=4.

The total variance σ_{ni}^2 of N periods for all Bennet components can be calculated by summation of all $\rho_{ni}^2(\omega)$. We therefore need the relation between the amplitude and the PSD $S_{u_{ni}}(f)$ of u_{ni}. The power of one component equals the power in a frequency band $\Delta f=\Delta\omega/2\pi$:

$$\tfrac{1}{2}\hat{u}_{ni}^2 = \frac{\Delta\omega}{2\pi} S_{u_{ni}}(f) \quad (5\text{-}37)$$

The variance σ_{ni}^2 is given by summation over the relevant bandwidth:

$$\sigma_{ni}^2 = \sum_{\Delta\omega} \rho_{ni}^2(\omega) \tag{5-38}$$

This summation becomes an integration when $\Delta\omega \downarrow 0$. The relevant bandwidth is the closed loop bandwidth B_{int} in Hz of the integrator. With aid of (5-36) to (5-38), the variance σ_{ni}^2 is given by:

$$\sigma_{ni}^2 = \left(\frac{C_{total}}{\hat{I}_{int}}\right)^2 \frac{1}{\pi} \int_0^{2\pi B_{int}} S_{u_{ni}}(f) H_u(\omega) d\omega \tag{5-39}$$

The noise source u_{ni} consists of white noise and 1/f noise with corner frequency $f_{c,ni}$. The PSD of this source is given by:

$$S_{u_{ni}}(f) = S_{u_{ni}}\left(1 + \frac{f_{c,ni}}{f}\right) \tag{5-40}$$

Substitution of (5-40) in (5-39) results in:

$$\sigma_{ni}^2 = \left(\frac{C_{total}}{\hat{I}_{int}}\right)^2 4NB_{int}S_{u_{ni}}\left(1 + \frac{4f_{c,ni}}{B_{int}}\right) \tag{5-41}$$

The relative jitter of N periods due to u_{ni} is given by ε_{ni}:

$$\begin{aligned} \varepsilon_{ni}^2 &= \frac{\sigma_{ni}^2}{(NT_{msm})^2} \\ &= \left(\frac{C_{total}}{\hat{V}_o(C_{o1} + C_{o2}) + \hat{V}_x C_s}\right)^2 \frac{B_{int}S_{u_{ni}}}{4N}\left(1 + \frac{4f_{c,ni}}{B_{int}}\right) \end{aligned} \tag{5-42}$$

Example. With N=256, C_s=30pF, C_{pb}=10pF, C_{int}=10pF, C_{o1}=C_{o2}=1pF (C_{total}=52pF), B_{int}=500kHz, $S_{u_{ni}}$=$6 \cdot 10^{-16}$V²/Hz (25nV/√Hz), $f_{c,ni}$=0 (we neglect the 1/f noise), $\hat{V}_o$=5V, $\hat{V}_x$=0.2V, the relative jitter amounts to 1.7 ppm. This is low enough for our application.

5.6.3 Resolution after application of the three-signal technique

Part of the three-signal technique is the calculation of the final measurement result M, based on three measurement phases T_x, T_{ref} and T_{off}:

$$M = \frac{T_x - T_{off}}{T_{ref} - T_{off}} = \frac{E_x}{E_{ref}} \tag{5-43}$$

Expression (5-41) gives the variance in the time domain due to u_{ni}, which holds for all measurement phases. The variance $\sigma_{M,ni}^2$ of M due to u_{ni} is now given by [20]:

$$\begin{aligned} \sigma_{M,ni}^2 &\cong \sigma_{ni}^2 \left(\left(\frac{\partial M}{\partial T_x}\right)^2 + \left(\frac{\partial M}{\partial T_{ref}}\right)^2 + \left(\frac{\partial M}{\partial T_{off}}\right)^2\right) \\ &\cong \sigma_{ni}^2 \frac{K}{(T_{ref} - T_{off})^2} \end{aligned} \tag{5-44}$$

where K is defined by:

$$K = 2\frac{T_{ref}^2 + T_x^2 + T_{off}^2 - T_x T_{ref} - T_{ref} T_{off} - T_x T_{off}}{\left(T_{ref} - T_{off}\right)^2} \tag{5-45}$$

Since $T_{off}<T_x<T_{ref}$, the value of K is between 1.5 and 2, depending on T_x. We are now able to calculate the resolution, which is defined as the minimal detectable change of the input signal. The resolution $\Delta v_{u_{ni}}$ in V_x due to u_{ni} is now determined by $\partial M/\partial V_x$ and the standard deviation $\sigma_{M,ni}$:

$$\Delta v_{u_{ni}} \left(\frac{\partial M}{\partial V_x}\right) = \sigma_{M,ni} \tag{5-46}$$

With help of (5-23) and (5-43) to (5-46), the resolution $\Delta v_{u_{ni}}$ due to u_{in} is given by:

$$\Delta v_{u_{ni}}^2 = K\sigma_{ni}^2 \left(\frac{\hat{I}_{\text{int}}}{4NC_{\text{int}}}\right)^2 \tag{5-47}$$

Substitution of (5-41) and (5-45) into (5-47) results in:

$$\Delta v_{u_{ni}}^2 = \left(\frac{C_{total}}{C_s}\right)^2 \frac{KB_{\text{int}} S_{u_{ni}}}{4N}\left(1 + \frac{4f_{c,ni}}{B_{\text{int}}}\right) \tag{5-48}$$

Example: With the same values as before and K=2, the resolution equals 4μV. When a platinum resistor Pt100 is measured, the sensitivity is approximately 780μV/K if the current through the Pt100 is 2mA. The final resolution in temperature is then 5.1mK. The resolution $\Delta c_{u_{ni}}$ for capacitive measurements due to u_{ni} can be found by multiplying $\Delta v_{u_{ni}}$ in (5-47) by C_{va}/V_{DD}. With C_{va}=10pF and V_{DD}=5V and the same conditions as above, the resolution in capacitance amounts to 5.6aF. In capacitive measurements, the noise u_{na} of the amplifier in the capacitance-to-voltage converter plays a more important role, as we see in the next section.
As can be seen from (5-48), a large value of N results in a small resolution. This is clear. Also the bandwidth B_{int} should be as small as possible. Keeping the measurement time constant, a higher modulator frequency has no influence on the resolution, since B_{int} and N are proportional to the modulator frequency in this case. This holds for a frequency independent power spectral density (PSD) of u_{ni}, which is not very likely. It is, however, more likely that the PSD is inversely proportional to the modulator frequency: a higher bandwidth normally asks for more current, resulting in a decreased PSD. The resolution is then inversely proportional to the square root of the modulator frequency, but we have to pay with a high current consumption.

5.6.4 Other electronic noise sources and quantization noise

This section presents the voltage and capacitance resolution, caused by both electronic and quantization noise. These resolutions, which are derived from the variances of the measurement phases, are listed in Table 5-2 and calculated in Appendix B. Only white electronic noise has been considered.
The capacitive resolution can easily be calculated by multiplying the voltage resolution by C_{va}/V_{DD}. This has already been done for the noise u_{na} of the amplifier.

Noise	Variance of measurement phase time	Variance in voltage/capacitance
u_{ni}	$\sigma_{ni}^2 = \left(\frac{C_{total}}{\hat{I}_{int}}\right)^2 4NB_{int}S_{u_{ni}}$	$\Delta v_{u_{ni}}^2 = \left(\frac{C_{total}}{C_s}\right)^2 \frac{KB_{int}S_{u_{ni}}}{4N}$
u_{ns}	$\sigma_{ns}^2 = \left(\frac{C_s}{\hat{I}_{int}}\right)^2 4NB_{int}S_{u_{ns}}$	$\Delta v_{u_{ns}}^2 = \frac{KB_{int}S_{u_{ns}}}{4N}$
i_n	$\sigma_i^2 = \frac{NT_{msm}S_{i_n}}{2\hat{I}_{int}^2}$	$\Delta v_{i_n}^2 = \frac{KT_{msm}S_{i_n}}{32NC_s^2}$
u_{nc}	$\sigma_{nc}^2 = \left(\frac{C_{int}}{\hat{I}_{int}}\right)^2 4NB_{comp}S_{u_{nc}}$	$\Delta v_{u_{nc}}^2 = \left(\frac{C_{int}}{C_s}\right)^2 \frac{KB_{comp}S_{u_{nc}}}{4N}$
u_{na}	$\sigma_{na}^2 = \left(\frac{(C_{ref}+C_p)C_s}{C_{va}\hat{I}_{int}}\right)^2 4NB_{va}S_{u_{na}}$	$\Delta c_{u_{na}}^2 = \left(\frac{C_p+C_{ref}}{V_{DD}}\right)^2 \frac{KB_{va}S_{u_{na}}}{4N}$
kT/C	$\sigma_{SC}^2 = \frac{8NkTC_{total}}{\hat{I}_{int}^2}$	$\Delta v_{SC}^2 = \left(\frac{C_{total}}{C_s}\right)\frac{kTK}{2NC_s}$
quant. noise		$\Delta v_q^2 = \frac{K}{6}\left(\frac{t_s\hat{I}_{int}}{4NC_s}\right)^2$

Table 5-2. Variances in time and in voltage or capacitance due to the noise sources in Figure 5-38 and due to the quantization noise.

In these formula's, B_{va} equals the closed loop bandwidth of the C-V converter, B_{comp} equals the bandwidth of the comparator, $S_{u_{ns}}$ equals the white noise density of u_{ns}, S_{i_n} equals the white noise density of i_n, $S_{u_{nc}}$ equals the white noise density of u_{nc}, $S_{u_{na}}$ equals the white noise density of u_{na} and t_s the sampling time of the microcontroller.
From $\Delta c_{u_{na}}$ we see that the capacitive resolution is proportional to C_p for $C_p >> C_{ref}$. This is not completely true, since the bandwidth of the amplifier B_{va} is inversely proportional to C_p. The capacitive resolution is therefore proportional to the square root of C_p.
Example. With C_p=50pF, C_{ref}=2pF, V_{DD}=5V, K=2, B_{amp}=1.6MHz, $S_{u_{na}}=10^{-16}$ V^2/Hz and N=256, the capacitive resolution is 8aF. Increasing the parasitic capacitance C_p to 500pF results in a decrease of B_{va} to 160kHz and an increase of the capacitive resolution to 25aF.

5.6.4.1 Comparison of the resolution of a modulator and an SC Delta-Sigma converter

It is interesting to compare the modulator with an SC Delta-Sigma converter for the resolution which is caused by electronic noise. It is possible to obtain an SC Delta-Sigma converter from the modulator by removing the current source I_{int} and driving the control signals for all switches from a clock with a fixed frequency. The only difference between the modulator and the SC Delta-Sigma converter for electronic noise is then the noise current i_n.
We compare the resolution of the modulator caused by i_n with the resolution caused by u_{ni}. We therefore assume that i_n is totally produced by the current source I_{int}. We also assume that I_{int} is generated by a resistor R_{int} and an amplifier with the same noise behavior as the amplifier in the integrator. The (flat) power spectral density of i_n is then given by S_{i_n}:

$$S_{i_n} = \frac{S_{u_{ni}}}{R_{\text{int}}^2} + \frac{4kT}{R_{\text{int}}} \tag{5-49}$$

We assume that the noise contribution of R_{int} dominates so we neglect the contribution of u_{ni} to i_n. This is valid when the equivalent noise resistor R_{eq} of u_{ni} ($S_{u_{ni}}$ =4kTR$_{eq}$) is smaller than R_{int}. This will be easy to achieve. The ratio of both resolutions (as listed in Table 5-2) is compared with unity:

$$\frac{\Delta v_{u_{ni}}^2}{\Delta v_{i_n}^2} = 1 \tag{5-50}$$

When the noise source u_{ni} is modeled by R_{eq}, evaluation of (5-50) results in:

$$R_{\text{int}} R_{eq} = \frac{T_{sub}}{2C_{total}^2 B_{\text{int}}} \tag{5-51}$$

Example: With T_{sub}=30µs, B_{int}=500kHz, C_{total}=52pF and R_{eq}=50kΩ, equation (5-51) is satisfied when R_{int} equals 220kΩ. A 30pF sampling capacitance results in signal charges of maximally 10pC. It takes a current of 330nA to remove this charge from the integrator within T_{sub}. This current flows through R_{int}, resulting in a voltage drop of 73mV. This low voltage is far below the power supply (3V or 5V), so it is permitted to choose a much larger value for R_{int}. The noise current i_n can then be neglected. When this is true, the total electronic noise of the modulator equals the total electronic noise of an SC Delta-Sigma converter.

5.6.4.2 Dominant electronic noise sources

It is interesting to find the dominant noise source. As shown before, the contribution of i_n can easily be kept smaller than that of u_{ni}. The resistive sensing elements produce thermal noise and this noise is already included in the kT/C noise. The noise can easily be kept small by choosing a sufficiently large value for C_s. When we assume that u_{ni} and u_{nc} have an equal spectral density, we may also neglect the contribution of u_{nc}, since C_s>>C_{int}.
The most important electronic noise sources are:

- for resistive measurements: u_{ni}
- for capacitive measurements: u_{ni} and/or u_{na}, depending strongly on C_p.

5.6.4.3 1/f flicker noise of the period

Due to the chopping of all relevant signals, 1/f behavior of any source shown in Figure 5-38 does not result in 1/f behavior of the period (flicker noise). A problem arises when the integration current I_{int} is implemented by two chopped DC current sources, as shown in Figure 5-41. This setup is required to obtain equal source and sink currents, which results in an optimal low-frequency suppression.

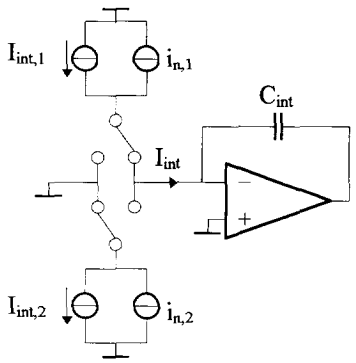

Figure 5-41. Implementation of I_{int} by two DC current sources.

Normally, the noise currents $i_{n,1}$ and $i_{n,2}$ are not correlated and then the above-mentioned equations for the jitter are no longer valid. When the noise sources are not correlated and have a 1/f spectral density, the period of the modulator also has a 1/f component. This is referred to as flicker. Barnes et. al. [21] showed that the variance of a flicker process is infinite. The resolution is then also infinite. The variance is therefore in this case not a good measure of the noise properties. Also the well-known Allan variance comes up with an infinite resolution and is therefore also not suitable. (see Appendix B).
However, it is possible to calculate the resolution by taking into account the three-signal technique and using the noise correlation between the measurement phases. Variations which are slow in comparison with the time of one full measurement cycle will have no effect on the measurement result. This behavior corresponds with a high-pass characteristic for very low frequencies. The calculation related to the three-signal technique is given by:

$$M = \frac{T_x - T_{off}}{T_{ref} - T_{off}} \tag{5-52}$$

where T_x, T_{ref} and T_{off} are the durations of the measurement phases.
The resolution can be calculated by using the variance of M. The variance of M due to one Bennet component in $i_{n,1}$ or $i_{n,2}$ (consisting of white and 1/f noise) with a frequency ω has been plotted in Figure 5-42 for different values of the 1/f noise corner frequency $f_{c,i}$. The variance of M is calculated in a similar way as shown in Figure 5-40 but now the three-signal technique has been included. The corner frequency is related to T_{cycle}, which is the sum of T_x, T_{ref} and T_{off}. The plots in the figure have been calculated for T_{off}:T_x:T_{ref}=1:2:3 and with an arbitrary white noise level. The total variance of M can be calculated by integration of the plots in Figure 5-42 over the full frequency range.

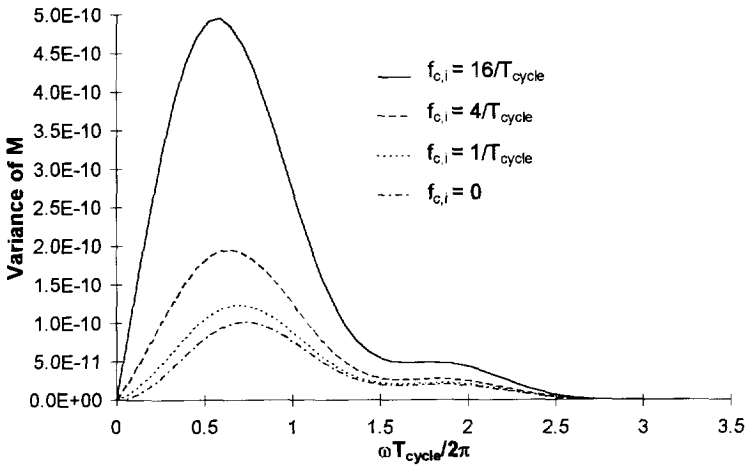

Figure 5-42. Variance of M (after the three-signal technique) due to one Bennet component with frequency ω for different values of the 1/f noise corner frequency $f_{c,i}$. The time T_{cycle} equals the sum of T_x, T_{ref} and T_{off}.

It can be seen that for $f_{c,i}=1/T_{cycle}$, the variance of M is barely increased. As shown in Chapter 6, the circuit shown in Figure 5-41 is applied to generate I_{int} and the corner frequency is designed to be lower than T_{cycle}^{-1}. Also a circuit based on switched current (SI) techniques is presented which requires only one stable (free of 1/f noise) current to obtain a stable frequency.

5.6.5 Conclusion

In this section, the resolution caused by electronic noise has been calculated. Calculations are derived by using Bennet's noise model. He represented a noise source as an infinite sum of discrete components, having a different frequency and a uniformly distributed phase. The modulator period is not sensitive to low-frequency 1/f noise as long as the 1/f corner frequency falls below the modulator frequency. The dominant noise sources are the noise voltages of the amplifiers of the integrator and of the C-V converter. The requirements for the corner frequency on the integration current are more stringent when this current is implemented by two chopped current sources.

5.7 Nonlinear signal-to-period conversion

To here, we have assumed that the Multiple-Sensor Modulator has a linear signal-to-period conversion, according to (5-23) or (5-24). In this section, we investigate the effect of several nonidealities on the linearity of the signal-to-period conversion and on the final measurement result M. We consider the following effects:

- Finite DC gain of the amplifiers
- Poles of the modulator
- Switch charge injection
- Voltage dependency of capacitors
- Nonideal effects of the comparator
- Current mismatch

5.7.1 Finite DC gain of the amplifiers

In this section, we investigate the effect of the finite DC gain of the amplifiers in the integrator and in the capacitance-to-voltage converter.

Finite DC gain of the amplifier in the integrator

To investigate the effect of the DC gain of the integrator amplifier on the nonlinearity, consider the circuit in Figure 5-43. The voltage V_x makes a step change at time t_0. The comparator detects when V_{int} equals zero and this corresponds to t_0+T_2. We investigate the linearity of the conversion of V_x to T_2.

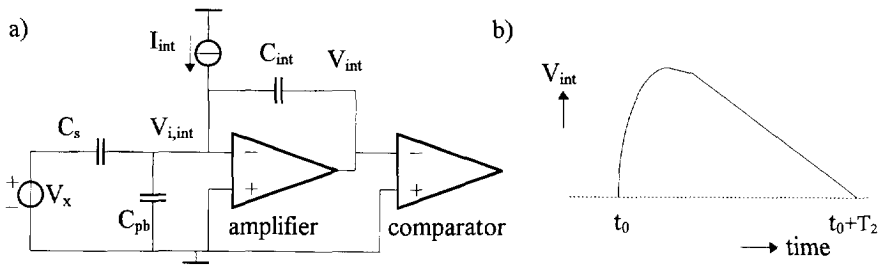

Figure 5-43. The integrator (a) and its output voltage V_{int} after a step change of V_x (b).

The gain of the amplifier is given by $A_{int}(s)$:

$$A_{\text{int}}(s) = \frac{A_{\text{int}}}{s\tau_{\text{int}} + 1} \tag{5-53}$$

where A_{int} is the DC gain. The wave form of V_{int} can be expressed in the time domain. The expression of V_{int} consists of an exponential decreasing component and a ramp. We assume that the exponential component at time t_0+T_2 can be neglected and that all initial conditions at time t_0 are zero. It can then be shown that:

$$T_2 = \tau_{HF} + \frac{\hat{V}_x C_s}{\hat{I}_{\text{int}}} \tag{5-54}$$

where the high-frequency time constant τ_{HF} is given by:

$$\tau_{HF} = \tau_{\text{int}} \frac{C_s + C_{pb} + C_{\text{int}}}{C_s + C_{pb} + C_{\text{int}} + A_{\text{int}} C_{\text{int}}} \tag{5-55}$$

The time interval T_2 in (5-54) depends in a nonlinear way on A_{int}, but this has no effect. It is only important that relation between $\hat{V}_x$ and T_2 is linear and this is true.

Finite DC gain of the amplifier in the capacitance-to-voltage converter

The finite DC gain of the amplifier in the capacitance-to-voltage (C-V) converter causes a nonlinearity. To see this, examine the circuit shown in Figure 5-44. The capacitance C_p models the capacitance of the connecting cables.

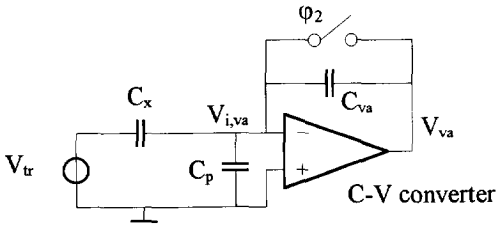

Figure 5-44. The DC gain of the amplifier in the C-V converter causes a nonlinear capacitance-to-voltage conversion.

When the amplifier has a DC gain A_{va}, the steady-state value of V_{va} after a step change of V_{tr} at the beginning of phase φ_1 is given by:

$$V_{va}\Big|_{t\to\infty} = -V_{tr}\frac{C_x}{C_{va}+\dfrac{C_{tot}}{A_{va}}} \tag{5-56}$$

where $C_{tot}=C_x+C_p+C_{va}$.
From (5-56) it follows that the steady-state value depends in a nonlinear way on C_x. The nonlinearity ε_{va} is given by the ratio of two steady-state values for capacitors C_x and $2C_x$, decreased by 1:

$$\begin{aligned}\varepsilon_{va} &= \frac{2V_{va}(C_x)\Big|_{t\to\infty}}{V_{va}(2C_x)\Big|_{t\to\infty}} - 1 \\ &= \frac{C_x}{(A_{va}+1)C_{va}+C_p+C_x} \\ &\cong \frac{C_x}{A_{va}C_{va}}\end{aligned} \tag{5-57}$$

The approximation is allowed when $A_{va}>>1$ and $A_{va}C_{va}>>C_p+C_x$. A small nonlinearity can be obtained by choosing a high value of the DC gain.
Example: With C_x=1pF, C_p=100pF, C_{va}=7pF and $A_{va}=10^4$, the nonlinearity over a 2pF range amounts to 14 ppm.

5.7.2 Poles of the modulator

This section discusses the effect of poles of the modulator on the nonlinearity. These poles introduce an exponential component in the conversion from the electrical signal to a period and thereby causes nonlinearity. Low-frequency poles are introduced by resistors at the input of the integrator and the capacitance-to-voltage (C-V) converter. Parasitic capacitors cause a bandwidth decrease.

5.7.2.1 Low-frequency pole of the integrator

The output resistance of the current source I_{int} in combination with the DC gain of the integrator amplifier causes a low-frequency pole. The input resistance of the amplifier also causes an LF pole, but this resistance is infinite when MOS technology is applied.
The resistor at the input of the integrator is modeled by R_i, as shown in Figure 5-45a.

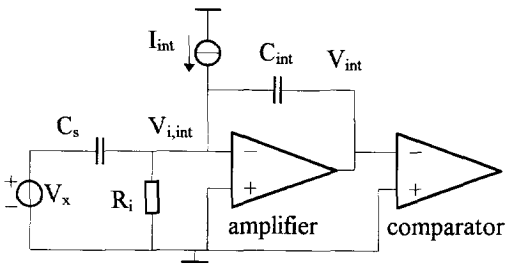

Figure 5-45. Circuit to calculate the nonlinearity caused by the low-frequency integrator pole.

The DC gain of the amplifier equals A_{int}. The low-frequency time constant of this system is then given by $\tau_{LF,int}$:

$$\begin{aligned}\tau_{LF,\text{int}} &= R_i\left(C_s + \left(A_{\text{int}} + 1\right)C_{\text{int}}\right) \\ &\cong A_{\text{int}}R_iC_{\text{int}}\end{aligned} \tag{5-58}$$

The effect of this pole on the period is investigated in the time domain. The wave form of V_{int} after a step change of V_x at time t_0 is shown in Figure 5-46, where we assumed that the duration of T_2 is fixed. The dashed line is related to the response without an LF pole and the line drawn to the response with a LF pole. We assume that the time constant is much larger than the time interval T_2.

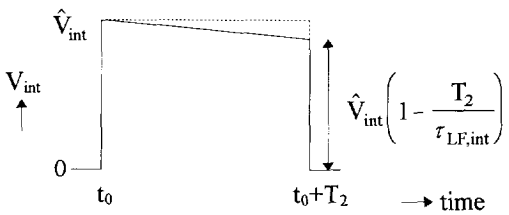

Figure 5-46. Output voltage of the integrator after a step change of V_x at time t_0. Due to the low-frequency pole, the output voltage is decreased.

The ratio of $V_{int}(t_0+T_2)$ and $V_{int}(t_0)$ is given by:

$$\begin{aligned}\frac{V_{\text{int}}\left(t_0 + T_2\right)}{V_{\text{int}}\left(t_0\right)} &= \exp\left(-\frac{T_2}{\tau_{LF,\text{int}}}\right) \\ &\cong 1 - \frac{T_2}{\tau_{LF,\text{int}}}\end{aligned} \tag{5-59}$$

The duration of φ_2 is now smaller than the ideal value T_2 (no LF pole) and is given by $T_{2,LF}$:

$$T_{2,LF} = T_2\left(1 - \frac{T_2}{\tau_{LF,\text{int}}}\right) \tag{5-60}$$

The nonlinearity can be calculated with the aid of $T_{2,LF,x}$ and $T_{2,LF,ref}$, which are related to a signal and reference measurement, respectively, and is given by $\varepsilon_{LF,int}$:

$$\varepsilon_{LF,\text{int}} = \frac{T_{2,LF,x}}{T_{2,LF,ref}} \frac{T_{2,ref}}{T_{2,x}} - 1 \cong \frac{T_{2,ref} - T_{2,x}}{\tau_{LF,\text{int}}} \tag{5-61}$$

where $T_{2,x}$ and $T_{2,ref}$ are the durations of φ_2 in the case without an LF pole for a signal and a reference measurement respectively.
Example: With $T_{2,ref}$-$T_{2,x}$=30µs and $\tau_{LF,int}$=2s, the nonlinearity amounts to 15 ppm. This is good enough for our application.

Very simple implementation of I_{int}
Suppose the resistance R_i models the output resistance of the current source I_{int}. It is interesting to verify whether the nonlinearity is low enough when I_{int} is implemented by a very simple switched resistor as shown in Figure 5-47. The desired value for $\hat{I}_{int}$ amounts to 500nA, as will be shown later. With V_{DD}=5V, the required value for R_i amounts to 5MΩ. The required DC gain with C_{int}=10pF to obtain $\tau_{LF,int}$=2s then amounts to $40 \cdot 10^3$. This value is not very high and can be realized with standard CMOS components.

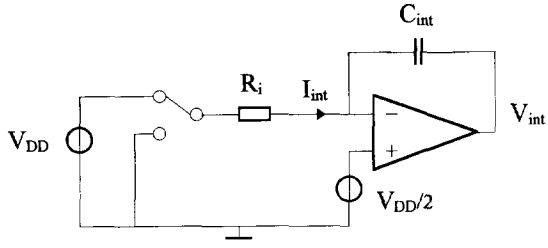

Figure 5-47. Generation of the integration current I_{int} by a switched resistor R_i.

The advantage of this simple solution is that the problem related to 1/f noise of i_n, mentioned in 5.6.4, does not occur. The disadvantage is that due to mismatches, the positive and negative value of I_{int} are not equal, resulting in a reduced suppression of the 50/60 Hz interference.

5.7.2.2 Low-frequency pole of the capacitance-to-voltage converter

A low-frequency (LF) pole of the C-V converter, caused, for instance, by a resistor at its input, seems to introduce nonlinearity in the same way as the integrator LF pole, but this is not true. The pole causes an exponential wave form at the output of the C-V converter in a similar way as (5-59), where we have to substitute T_2 by T_1. Since T_1 is constant, the effect of the pole is a multiplicative error which is eliminated by the three-signal technique.

5.7.2.3 High-frequency pole of the integrator

The high-frequency (HF) pole of the integrator causes two effects:
1. A nonlinear signal-to-period conversion
2. Cross talk between two concatenated measurement phases.

This last effect has been shown in Figure 5-8. Due to the high-frequency time constant, the frequency can not change instantaneously. Due to this effect, the duration of some measurement phases is too short or too long, depending on the sequence. The high-frequency time constants of the modulator are normally much smaller than the period. Since each

measurement phase consists of N periods (N is a large number), this cross talk effect can be neglected with respect to the first-mentioned effect.

The integrator HF pole is caused by, for instance, the limited bandwidth of the amplifier which is expressed by (5-53). The limited bandwidth causes a HF pole as given by (5-55).
We can model the effect of the pole by considering an exponential charge transfer to the integrator. The charge which is transferred during T_2 for the measurement of V_x is given by $Q_x(T_{2,x})$:

$$Q_x\left(T_{2,x}\right) = Q_x \exp\left(-\frac{T_{2,x}}{\tau_{HF}}\right) \tag{5-62}$$

where Q_x is the steady-state value. Since not all charge has been transferred, the period decreases. The nonlinearity ε_{HF} can be calculated by comparing $Q_x(T_{2,x})$ with $Q_{ref}(T_{2,ref})$, which is obtained from a reference measurement:

$$\begin{aligned}\varepsilon_{HF} &= \frac{Q_x\left(T_{2,x}\right)}{Q_{ref}\left(T_{2,ref}\right)}\frac{Q_{ref}}{Q_x} - 1 \\ &\cong \exp\left(-\frac{T_{2,ref}}{\tau_{HF}}\right) - \exp\left(-\frac{T_{2,x}}{\tau_{HF}}\right) \quad < \exp\left(-\frac{T_{2,off}}{\tau_{HF}}\right)\end{aligned} \tag{5-63}$$

where we assumed $\exp(-T_{2,ref}/\tau_{HF}) \ll 1$.
Example: With $T_{2,x}$=10µs, $T_{2,ref}$=40µs and τ_{HF}=500ns, the nonlinearity amounts to 0.2ppm.

5.7.2.4 High-frequency pole of the capacitance-to-voltage converter

The high-frequency (HF) pole of the capacitance-to-voltage (C-V) converter seems to introduce nonlinear behavior in the same way as the HF pole in the integrator, but this is not true. The HF pole causes a multiplicative error in a way similar to the LF pole in the C-V converter. To see this, examine the circuit in shown Figure 5-44. The gain of the amplifier in the C-V converter is given by $A_{va}(s)$:

$$A_{va}(s) = \frac{A_{va}}{s\tau_{va} + 1} \tag{5-64}$$

When V_{tr} makes a step change $\hat{V}_{tr}$ at the beginning of φ_1, the value of V_{va} at the end of φ_1 can be calculated with the aid of (5-56) and is given by $V_{va}(T_1)$:

$$V_{va}\left(T_1\right) = V_{va}\big|_{t\to\infty} \cdot \left(1 - \exp\left(-\frac{T_1}{\tau_{va}\dfrac{C_{tot}}{C_{tot} + A_{va}C_{va}}}\right)\right) \tag{5-65}$$

where $C_{tot}=C_p+C_x+C_{va}$.
Since T_1 is a constant time, the exponential component forms a multiplicative error which is eliminated by the three-signal technique.
Equation (5-65) holds only when the initial condition of the voltage $V_{i,va}$ is constant for all measurement phases. This fixed initial condition has to be reached within the time interval T_2. We can, for instance, reset all capacitors, including C_p. The fixed initial condition for all capacitors is then zero. This is very simple to achieve when the amplifier is implemented by an

Operational Amplifier (OpAmp), as shown in Figure 5-48. During φ_2, the feedback switch is closed and the bandwidth of the system now equals the unity-gain frequency. This frequency is large enough to settle $V_{i,va}$ within T_2 completely.

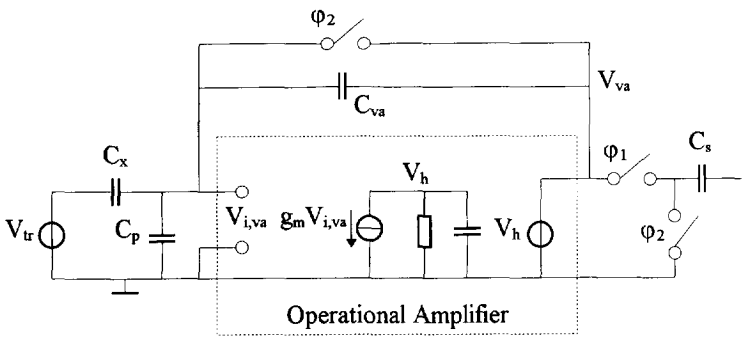

Figure 5-48. The amplifier in the C-V converter is implemented by an OpAmp to force a fixed initial condition of $V_{i,va}$ at the beginning of phase φ_1.

A problem related to the application of an OpAmp is the HF stability. The OpAmp has a unity feedback during phase φ_2. When we assume that the gain of the OpAmp consists of two poles, the unity feedback normally requires pole splitting such that the HF pole lies above the unity gain frequency. When the input is loaded with the capacitor C_p, a third pole is present. The pole is caused by the output resistance of the OpAmp, and C_p and can easily have a frequency between the other two poles for a unity feedback and large values of C_p. This results in instability. Measures can be taken to guarantee stability of this third-order system, but a stable C-V converter can be obtained in a simpler way by applying an Operational Transconductance Amplifier (OTA), especially when C_p causes the dominant pole.

The fixed initial condition at the beginning of φ_1, required to obtain a good linearity, can be forced by short-circuiting C_p and C_{va} during φ_2, as shown in Figure 5-49. We assumed that the bandwidth of the OTA itself is very high. Short-circuiting C_p and C_{va} at the same time is no problem for the OTA.

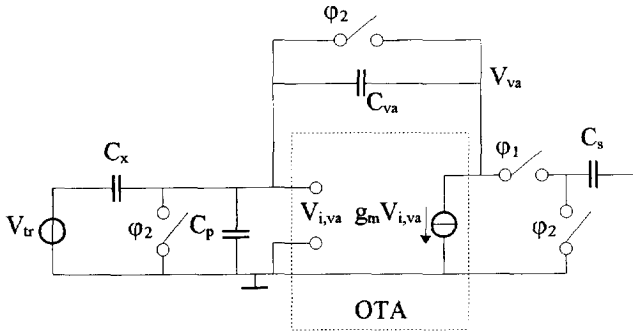

Figure 5-49. The amplifier in the C-V converter is implemented by an OTA. The fixed initial condition is forced by short-cutting C_p and C_{va} during φ_2.

The setup in Figure 5-49 has one disadvantage. Due to an offset voltage of the OTA, an output current is generated during φ_2. This current flows through the switches which are in parallel to

C_{va} and C_p. This has no effect on the functionality. When the effect is undesirable, offset cancellation can be applied.

5.7.2.5 Conclusion

We are now able to define the useful frequency range of the modulator where the nonlinearity due to poles is less than ε. The time constant of the poles τ_{HF} and τ_{LF}. This frequency range is based on (5-61)and (5-63) and can approximated by:

$$\tau_{HF} \ln(\varepsilon) < T_2 < \tau_{LF} \varepsilon \qquad (5\text{-}66)$$

This is a useful expression and can be used to investigate the effect of low- and high-frequency poles on the nonlinearity.

5.7.3 Switch charge injection

We discuss the switch charge injection (SCI) by considering the basic switched capacitor (SC) circuit in Figure 5-50.

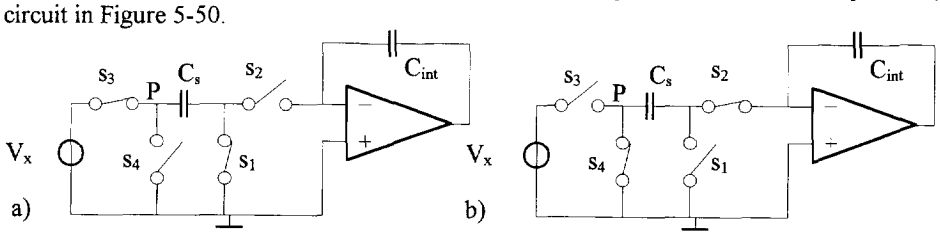

Figure 5-50. Basic Switched Capacitor circuit.

The situation before switching is shown in Figure 5-50 a) and the final situation after switching in b). The desired charge flow to the integrator equals V_xC_s, but also a constant signal-independent charge Q_{const} flowing also to the integrator is permitted. The effect of Q_{const} is eliminated by the three-signal technique. The switch charge injection from s_3 depends in a nonlinear way on V_x, so we must prevent this charge from entering the integrator.

The only way to achieve this is to first switch s_1 and s_2 in a break-before-make (BBM) mode to prevent from charge loss. After this, s_3 opens (a closed switch is assumed to be conductive). After s_4 is closed, the total voltage swing of node P exactly equals V_x, so the charge flow through C_s while s_2 is closed equals V_xC_s. This means that switch charge from s_3 does not enter the integrator.

The switch charges from s_1 and s_2 contribute to Q_{const}. Since the voltage of the inverting node of the integrator at the sampling moments (the end of time intervals T_1 and T_2) is always constant, the switch charges from s_1 and s_2 do not depend on V_x. Their effects are eliminated by the three-signal technique.

5.7.4 Voltage dependency of capacitors

The voltage dependency of C_{int} has no effect on the nonlinearity, since the threshold of the comparator is a constant voltage. During capacitive measurement, the voltage dependence of C_{va} exactly compensates for the voltage dependence of C_s. This is a form of balancing. During resistive measurement, a nonlinearity occurs due to the voltage dependence of C_s. Assume a voltage-dependent capacitor C(V) can be modeled by

$$C(V) = C_0\left(1 + c_1 V + c_2 V^2 + c_3 V^3\right) \tag{5-67}$$

where V is the voltage across the capacitor and C_0 the zero-voltage value. The odd-order components c_1 and c_3 can easily be removed by the anti-parallel connection of two equal capacitors. The even-order terms result in a nonlinearity. Throughout the signal and the reference measurement phase, V has values V_x and V_{ref} respectively. The charge flow through C_s equals $Q=C_sV$, resulting in Q_x and Q_{ref}. The nonlinearity can be obtained from the ratio Q_x/Q_{ref}:

$$\frac{Q_x}{Q_{ref}} = \frac{V_x}{V_{ref}}\left(\frac{1 + c_2 V_x^2}{1 + c_2 V_{ref}^2}\right) \tag{5-68}$$

Good capacitors such as poly/oxide/high-doped silicon show c_2=5ppm/V^2. With V_x=0.1V and V_{ref}=0.2V, the nonlinearity is less than 1ppm. This is very low.

5.7.5 Nonideal effects of the comparator

A nonideal effect of the comparator is the memory effect. Since the comparator is strongly nonlinear, it is not allowed to model this memory effect by poles. It is better to consider the time delay. When the delay time $t_d(t)$ is time dependent:

$$t_d(t) = b_0 + b_1 t + b_2 t^2 \tag{5-69}$$

the three-signal technique eliminates the effect of the zero and first-order terms. Higher-order terms cause nonlinearity.

Another nonideal effect of the comparator is hysteresis. Its effect is the same as delay time, since the slope of the output voltage of the integrator is constant. Its effect can be eliminated by the three-signal technique as long as the hysteresis behaves linearly to the period.

5.7.6 Current mismatch

A difference between the positive and negative amplitude of I_{int} causes a multiplicative error, as can be seen with the assistance of (5-23) or (5-24). This error is eliminated by the three-signal technique. As discussed in 5.4.3, a current mismatch causes a large decrease of the LF suppression.

5.7.7 Conclusion

In this section, we have investigated the effect on the nonlinearity of several effects. To obtain a linear signal-to-period conversion, some requirements have to be fulfilled. This does not require extremely good or high-bandwidth circuit parts, nor high-ohmic resistors. The most important requirement is that the low-frequency and high-frequency time constants have to be sufficiently larger and smaller than the modulator period, respectively.

5.8 Sensor-specific signal processing

5.8.1 Capacitors

Multiple capacitors

The read-out circuit for two capacitors, including the reference capacitor, has already been discussed and is shown in Figure 5-26. It is possible to measure multiple capacitors in a very easy way. All capacitors, including the reference capacitor, can be connected to the input of the C-V converter. The measurement of L capacitors (excluding the reference) requires L+2 measurement phases: L phases for the 'signal' capacitors and two for the offset and reference measurement.

When the total capacitance at the input of the C-V converter becomes too large, the amplifier does not reach the full unity gain bandwidth. This will result in nonlinearity, which can be avoided by multiplexing the receiving electrodes. This method is used by Toth [16] and is shown in Figure 5-51.

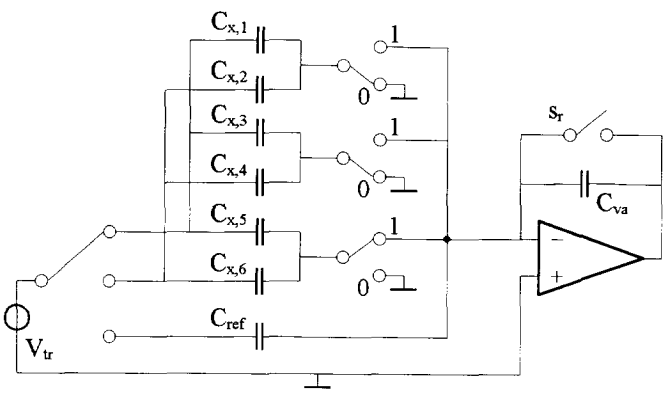

Figure 5-51. The measurement of multiple capacitors requires multiplexing of the receiving electrodes when the total capacitance is too large.

One of the switches at the input is in position '1', the others in position '0'. The reference capacitor C_{ref} is not multiplexed. The measurement of every set of capacitors selected by these switches requires an offset and a reference measurement, since multiplexing at the input results in a change of multiplicative and additive terms. The measurement of the six capacitors as shown in the figure therefore requires 3 reference measurements, 3 offset measurements and 6 signal measurements, a total of 12 measurement phases.

Improved LF suppression

In 5.4.2, we calculated the suppression for LF interference during capacitive measurements. It is possible to obtain a better suppression. The basic idea is to sample the output voltage V_{va} during φ_3, which has a shorter duration than φ_1. Examine the circuit in Figure 5-52.

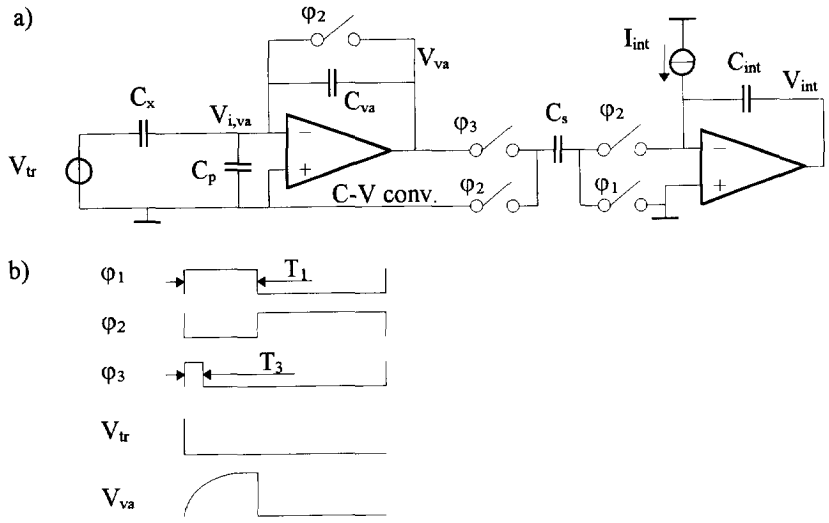

Figure 5-52. An improvement of the LF suppression can be obtained by sampling the output voltage of the C-V converter on C_s during φ_3, which has a shorter duration than φ_1. The circuit is shown in a) and the wave forms in b).

Due to the limited bandwidth, the voltage V_{va} at the end of φ_3, is not settled. This forms a multiplicative term, as calculated by (5-65). Due to the decreased sampling time, the small-signal suppression $R_{C,2,N}(\omega)$ as calculated in (5-32) improves and can be calculated after the substitution of $\sin(\frac{1}{2}\omega T_1)$ by $\sin(\frac{1}{2}\omega T_3)$, where T_3 equals the duration of φ_3.
Example: When T_3 equals the HF time constant $\tau_{HF,va}$ and $T_1=15\tau_{HF,va}$, the signal transfer is reduced to 63% of the steady-state value and the LF interference transfer is 15 times reduced. The result is a 19 dB improvement of the Signal-to-Interference ratio.

5.8.2 Platinum resistors

Platinum resistors are used to measure temperature. They can be used in the wide temperature range from -200°C to 850°C. The resistive change of platinum is not exactly linear with temperature (see Appendix A). Many good ways of linearizing this behavior have been presented [22, 23]. In our design, no effort is spent on linearization, since this task is easily performed by the microcontroller.
It is required to have an almost constant temperature resolution over the total temperature range. This can be obtained by a constant current flowing through the platinum resistor in combination with a constant resolution in the measurement of the voltage V_x or V_{ref}. A simple read-out circuit to achieve this is given in Figure 5-53.

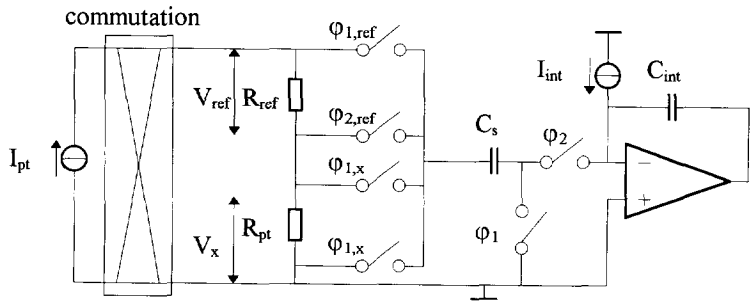

Figure 5-53. A read-out circuit for platinum resistors. A constant temperature resolution is obtained if the current I_{pt} does not depend on the temperature.

The constant current I_{pt} is multiplexed and flows through both the platinum resistor R_{pt} and the reference resistor R_{ref}, thus forming a multiplicative term. The maximum allowable value of I_{pt}, in view of self-heating effects, depends on the thermal resistance. For normal values of the thermal resistance, a current of 2mA flowing through a Pt100 causes a self-heating which is smaller than its initial inaccuracy at 0°C.

5.8.3 Thermistors

Thermistors are used for the measurement of temperature. The resistance of a thermistor varies exponentially with the temperature. When the voltage resolution in V_x is constant and a constant current flows through the thermistor, the exponential behavior results in an exponential resolution in temperature. This is not desired. In order to obtain a more constant resolution in temperature, we need to linearize the resistance-to-voltage conversion. We consider two linearization methods. Note that these methods are not used to obtain a perfect linear relation between temperature and the modulator period, but only to obtain a more constant resolution. An expression modeling the resistance R_T of the thermistor is given by

$$R_T = A\exp\left(\frac{B}{T}\right) \tag{5-70}$$

where T is the absolute temperature. Values of the constants A and B are given in Appendix A. The first linearization method is based on cascading the exponential function of the thermistor by its inverse (logarithmic) function. The only on-chip device with this function is a pn-junction. Its current-to-voltage conversion is logarithmic. An alternative method is based on the series connection of the thermistor and a reference resistor. When a constant voltage is applied across the series connection, the voltage across the thermistor is partly linearized. Circuits implementing these two methods are shown in Figure 5-54. Also shown is the circuit without linearization.

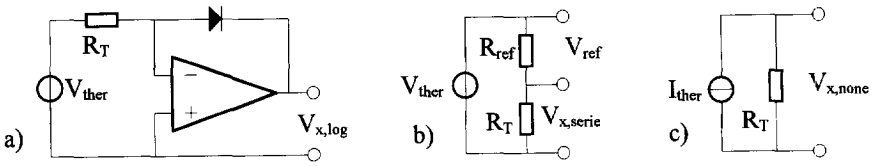

Figure 5-54. Two linearization methods to obtain an almost constant temperature resolution. Method a) is based on the logarithmic function. Method b) is based on the series connection with a reference resistor and method c) does not use linearization.

To calculate the maximum achievable resolution, we assume that the maximum input range of the modulator equals the range of V_x. The voltage resolution Δv_x in V_x (V_x represents $V_{x,log}$, $V_{x,serie}$ or $V_{x,none}$) is assumed to be constant within the full range and equal to $\Delta v_x = 2^{-n}(V_{x,max} - V_{x,min})$, where n is the number of bits and $V_{x,max}$ and $V_{x,min}$ the maximum and minimum value of V_x respectively. The resolution ΔT in temperature can be calculated with

$$\Delta T = \left(\frac{\partial V_x}{\partial R_T} \cdot \frac{\partial R_T}{\partial T} \right)^{-1} \Delta v_x \tag{5-71}$$

After some calculation, three resolutions ΔT_{log}, ΔT_{serie} and ΔT_{none} for the circuits in Figure 5-54 a), b) and c), respectively, can be obtained. They are given by:

$$\begin{aligned}
\Delta T_{log} &= 2^{-n} T^2 \left(\frac{1}{T_{min}} - \frac{1}{T_{max}} \right) \\
\Delta T_{serie} &= 2^{-n} T^2 \frac{\left(R_{ref} + R_T\right)^2}{B R_{ref} R_T} \frac{\exp\left(\frac{B}{2T_{min}} - \frac{B}{2T_{max}} \right) - 1}{\exp\left(\frac{B}{2T_{min}} - \frac{B}{2T_{max}} \right) + 1} \\
\Delta T_{none} &= 2^{-n} T^2 \frac{R_{T,max} - R_{T,min}}{B R_T}
\end{aligned} \tag{5-72}$$

where T is expressed in K. Figure 5-55 shows these resolutions for a thermistor from YSI (B=3891) in the temperature range 0°C-70°C. In this range $R_{T,min}$=402Ω and $R_{T,max}$=7508Ω. We used R_{ref}=1200Ω and n=15.

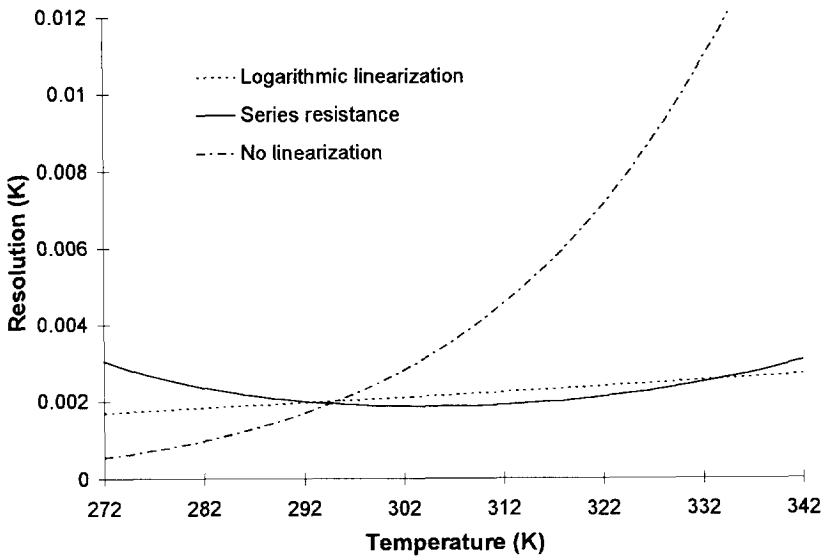

Figure 5-55. Maximum achievable resolutions in temperature for the two linearization methods with n=15.

The resolutions of the two linearization methods are almost the same. Note that the voltage V_{ref} in Figure 5-54 b) has the same temperature sensitivity as $V_{x,serie}$. This improves the resolution of the final measurement result by a factor of two. The method based on the logarithmic function has some disadvantages. The first disadvantage is that implementation of the 4-wire setup requires additional circuitry to convert V_{ther} into a current. Another disadvantage is that a real offset measurement ($V_{ther}=0$) is not allowed. We need a second reference resistor or an accurate multiplication factor of V_{ther} to overcome these problems. The method based on the series connection is very simple and is, therefore, used.
The value of the reference can be designed such that the resolutions at both temperature extremes are equal. This is shown in Figure 5-55.
Normally, the maximum amplitude of the drive voltage V_{ther} (Figure 5-54 b) is determined by self-heating. With normal thermal resistance values, the error caused by self-heating is smaller than the inaccuracy of the thermistor for $|V_{ther}|<0.4V$.

5.8.4 Resistive bridges

In Appendix A, we distinguish two types of resistive bridges. For the U-bridges, the physical signal is best represented by the ratio of the output voltage of the bridge and the voltage across the bridge. In the case of I-bridges, the ratio of the output voltage and the current through the bridge represent the physical signal. For both bridges, the temperature sensitivity of the ratio is very small.
The main problem for the measurement of U-bridges is the large difference between the reference voltage (the voltage across the bridge) and the bridge's output voltage. The measurement of both voltages with a certain degree of accuracy requires a measurement system with much greater accuracy. These dynamic-range problems will be solved.

5.8.4.1 U-bridges

Many different circuits to read-out resistive bridges have been proposed. A considerable number of these circuits either need an external reference, require calibration, or need an accurate supply voltage to drive the bridge [24,25,26] In this section, a new circuit is presented which is able to read out a resistive bridge very accurately without the need for calibration, accurate bridge supply voltage or external reference. The effect of lead resistance is very simply eliminated.

During the signal and the reference measurement phase, we measure the output voltage V_{out} of the bridge and the bridge supply voltage V_{BS}, respectively. When the same front-end is used to process both voltages, its linearity should be very high in order to obtain accurate results, since $V_{BS}>>V_{out}$. When the maximum bridge unbalance is Δ_{max} and the bridge accuracy is ε_b, the nonlinearity of the front-end, processing both voltages, should be less than $\Delta_{max}\varepsilon_b$. With $\Delta_{max}=1\%$ and $\varepsilon_b=10^{-4}$, the maximum nonlinearity amounts to 1ppm. This is very hard to realize. It is easier to amplify V_{out} or divide V_{BS}. The amplifier gain or the division ratio must be fixed, since they do not form a multiplicative or additive factor and can, therefore, not be eliminated by the three-signal technique. The inaccuracy of the divider or of the amplifier should then be smaller than ε_b to read out the bridge with an inaccuracy ε_b. The use of calibration to obtain the desired accuracy of the amplifier or divider is not very attractive, since calibration is rather expensive and requires, probably, a recalibration. Calibration is, therefore, not used. Another method to obtain the accuracy is to rely on matching. However, the maximum achievable accuracy is limited to approximately 0.1%, which is not enough. We use Dynamic Element Matching to achieve an inaccuracy of less than 10^{-4}. The problem to solve first is whether to use a voltage amplifier or a voltage divider. The selection depends mainly on two aspects:

- noise and current consumption
- interference

In the circuit shown in Figure 5-56 a), V_{out} is amplified by P before sampling and processing to the integrator. During the measurement of V_{BS}, switch s_p is in position '0' and V_{BS} is directly sampled on C_s. The circuit in b) is based on a divider for V_{BS}. This circuit has the same values of I_{int} and C_{int}. To obtain the same time excursion, the sampling capacitor is increased to PC_s. In fact, V_{out} is also amplified, but in a different way than in a). A simple implementation of the divide-by-P stage is to sample V_{BS} directly on a sampling capacitor with value C_s, whereas V_{out} is sampled on a capacitor with value PC_s. V_{BS} is now processed in the same way as in a).

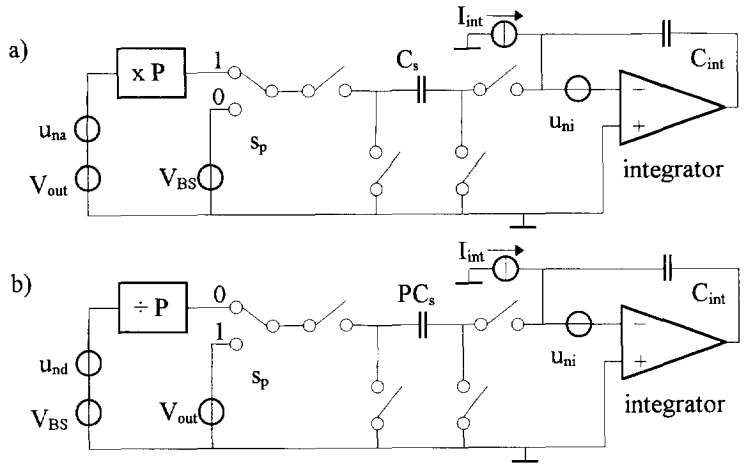

Figure 5-56. Processing circuitry to read out a U-bridge with the use of an amplifier for V_{out} (a) or with the use of a divider for V_{BS} (b).

Noise and current consumption

We consider the most important noise sources which determine the total SNR. These are the noise voltage u_{na} of the amplifier, the noise voltage u_{nd} of the divider and the noise voltage u_{ni} of the active part of the integrator. When the simple implementation of the divider is used, the noise voltage u_{nd} equals zero. We assume that the bandwidths of the active parts are equal. The result of this assumption is that both circuits have equal SNR when the power spectral density of u_{ni} in b) and u_{na} are equal. This results in equal bias currents for the input transistors of the amplifier or integrator.

Interference

As soon as interference is present in the output voltage of the bridge, it can not be reduced by a different processing circuit. Further, coupling of the interference into the circuit at the input or output of the integrator does not make any difference, since the signal levels are equal in both cases. A difference occurs when the amplifier adds either more or less interference than a P times increased sampling capacitor PC_s. Usually, interference is coupled into a circuit via the power supply lines and/or via the substrate. The coupling of the interference into the circuit depends many unknown aspects, such as the interference on the power supply lines and the grounding of the substrate. These aspects are determined by the layout.

Conclusion

Since the above discussions have not enabled us to select between amplification or division, we base our choice on other criteria. A good reason to apply a voltage divider is that the range of V_{out} for a lot of commercially available bridges (0.4V when supplied with V_{BS}=5V: Δ_{max}=4%) is the same as the range of the voltages across a Pt100 platinum resistor or a thermistor. This means that measuring a Pt100 requires a sampling capacitor PC_s and this capacitor can be directly used to sample V_{out}. This points to the application of a divider. Another selection criterion is the chip area consumption. As shown in the following chapter, the value PC_s amounts to 30pF. Such a capacitor has approximately the same size as one OpAmp. Again, the divider is to be preferred.

The divider for V_{BS}

As mentioned before, the divide-by-P stage can easily be implemented be sampling V_{BS} on C_s and V_{out} on PC_s. The use of Dynamic Element Matching (DEM) guarantees an accurate value of P. This requires P almost equal sampling capacitors with value C_s and a lot of switches. A practical value for P for Δ_{max}=4% is 32. The divider then consists of many components. By adding a resistive divider in front of the capacitive divider [27], the factor P can be realized with many fewer components. This circuit is shown in Figure 5-57.

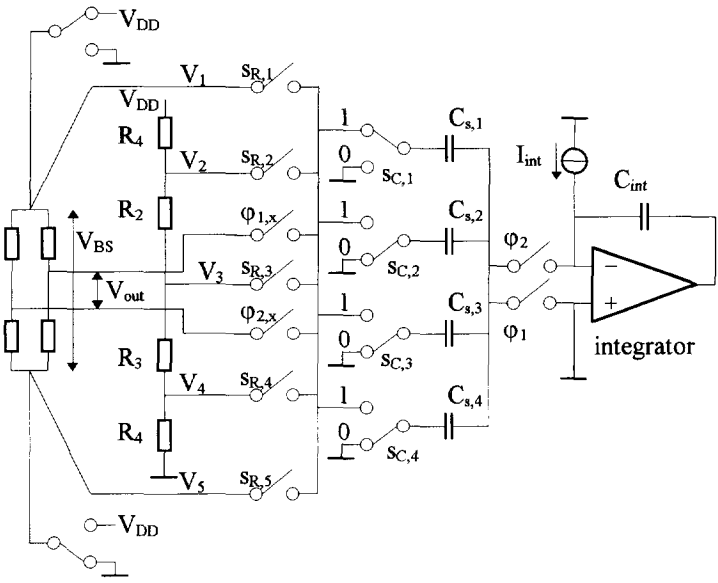

Figure 5-57. The new voltage divider with N_R=4 and N_C=4.

The divider consists of N_R resistors and N_C capacitors, resulting in a division ratio N_RN_C. During the reference measurement (measurement of V_{BS}), the switches sensing V_{out} are open (not conducting). One of the switches $s_{C,i}$,i∈[1,N_C], is in position '1'. Every time interval T_{sub}, one capacitor $C_{s,i}$ transfers a charge $(V_j-V_{j+1})C_{s,i}$, j∈[1,N_R], to the integrator. It takes N_R time intervals T_{sub} for $C_{s,i}$ to sample the complete voltage V_{BS}. After this, the next sampling capacitor samples V_{BS} in N_R time intervals T_{sub}. The charge Q_{BS} transferred to the integrator during N_RN_C time intervals T_{sub} amounts to:

$$Q_{BS} = V_{BS}\sum_{i=1}^{N_C} C_{s,i} + N_R N_C Q_{off} \qquad (5\text{-}73)$$

where Q_{off} represents a charge which is also transferred to the integrator every T_{sub}. Q_{off} includes C_{o1} and C_{o2} (see Figure 5-26) and the offset voltage of the active part of the integrator. During the measurement of V_{out}, switches $s_{R,j}$ are open and all $s_{C,i}$ are in position "1". The drive signals $\varphi_{1,x}$ and $\varphi_{2,x}$ are shown in Figure 5-27. During N_RN_C time intervals T_{sub}, a charge Q_x is transferred to the integrator, where Q_x is given by:

$$Q_x = N_R N_C V_{out}\sum_{i=1}^{N_C} C_{s,i} + N_R N_C Q_{off} \qquad (5\text{-}74)$$

Note that $V_{out,max}\Sigma C_{s,i}$ lies in the same range as $(V_j-V_{j+1})C_{s,i}$, so the DR of the integrator is optimally used.
Finally, during N_RN_C time intervals of the offset measurement, where all switches $s_{C,i}$ are in position '0', a charge Q_{os} is transferred to the integrator, where Q_{os} is given by:

$$Q_{os} = N_R N_C Q_{off} \tag{5-75}$$

The final measurement result M_{div} is given by:

$$M_{div} = \frac{Q_x - Q_{os}}{Q_{BS} - Q_{os}} = \frac{N_R N_C V_{out}}{V_{BS}} \tag{5-76}$$

Mismatch between $C_{s,i}$ and nonidealities of R_j have no effect on M_{div}. This is a big advantage.
The ON resistance of the switches only contributes to a high-frequency time constant, which effect has been previously calculated. Both switches $s_{R,j}$ for j=1 and $j=N_R+1$ ideally sense the voltage across the bridge, thus completely eliminating the effect of the resistances of the connecting wires.

Very small maximum imbalance Δ_{max}

Reading out bridges with a very small maximum imbalance ($\Delta_{max}<<1\%$) would require a very large division ratio. This has some unwanted consequences.
Firstly, the number of periods during the measurement of V_{BS} to perform one full DEM cycle will be large. The minimum measurement time, which is limited to one full DEM cycle, will also be long. Secondly, the sum of the sampling capacitors $\Sigma C_{s,i}$ will be very large, thus consuming a large chip area. As we saw before, reading out a bridge with $\Delta_{max}=4\%$ and supplied with $V_{BS}=5V$ requires a sampling capacitor of 30pF. When Δ_{max} is decreased by 16 times to $\Delta_{max}=0.25\%$, the required value of the sampling capacitor amounts to 480pF. The area occupied by such a capacitor is very large. These consequences can be bypassed by applying a divider for V_{BS} in combination with an amplifier for V_{out}. Just as the division ratio, the gain of this amplifier must be accurately known. A new amplifier with a very accurate gain is proposed by P.C. de Jong [28]. The amplifier is based on DEM. Calibration is not required and slow drift of the applied resistors does not affect the gain. The circuit is shown in Figure 5-58.

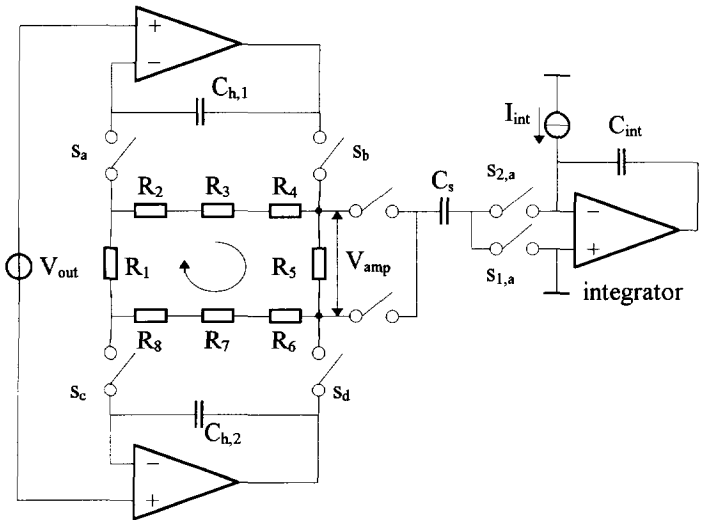

Figure 5-58. A calibration-free amplifier with a very accurate and stable gain.

The DEM amplifier consists of two Opamps, N_{amp} almost equal resistors connected in a loop and numerous switches. The output voltage V_{amp} of the amplifier is ideally sensed by the sampling capacitor. The value of N_{amp} of the depicted amplifier in the figure amounts to 8. When switches $s_a,\ldots,s_d$ are closed (conducting), one of the resistors functions as a load and the gain is approximately 7. During the next DEM phase, the loop of resistors turns clockwise for one step by closing switches which are not shown in the figure. Now R_4 becomes the load. Again, the gain in this situation is approximately 7. After N_{amp} DEM phases, the loop has made one complete cycle. The average of the N_{amp} different gain values approximately equals N_{amp}-1. The inaccuracy of this average value is due to mismatch m and is of the order m^2. Any linear term in m ($R_k=R_0(1+\alpha k)$; $k\in[1,N_{amp}]$) has no effect on the average gain.
The capacitors $C_{h,i}$ guarantee a stable feedback.

The effect of offset from both OpAmps is eliminated by the chopping of V_{out}. The effect of voltage-dependent resistors is also eliminated, since the voltages across the resistors contributing to the gain are equal. The voltage difference between the applied poly-silicon resistors and the well beneath them might be a problem. This well is required by the process and modulates the resistivity of the poly-silicon, just like an MOS transistor. The applied differential topology eliminates odd-order modulation effects.
The accuracy is also limited by the finite DC gain of the OpAmps. Since the DC gain of MOS OpAmps can be very high (more than 120dB), its effect can usually be neglected.

5.8.4.2 I-bridges

The reference signal for I-bridges is the current through the bridge. A very simple method to measure this current is to convert this current into a reference voltage by using a resistor. We then obtain a measurement which is similar to the measurement of platinum resistors.

5.8.5 Temperature measurement

In this section we discuss the accuracy and implementation of an on-chip temperature sensor, which is required to compensate the temperature dependence of the sensing elements. This is useful when the temperature of the sensing element and of the SSP are equal. A good method to measure the temperature is based on bipolar transistors [29, 30]. The temperature-dependent voltages are the base-emitter junction voltage V_{be} and the voltage difference V_{PTAT} of two V_{be}'s. The temperature of the chip can be calculated from any linear combination of V_{be} and V_{PTAT}:

$$M_T = \frac{aV_{be} + bV_{PTAT}}{cV_{be} + dV_{PTAT}} \tag{5-77}$$

To calculate the inaccuracy in temperature ΔT, we assume that V_{be} has an inaccuracy ΔV_{be}. The voltage V_{PTAT}, which is based on a current ratio, can be realized to be very accurate with aid of Dynamic Element Matching, as shown by Khadouri et. al. [31] The inaccuracy ΔT can be calculated by:

$$\Delta T = \Delta V_{be} \frac{\partial M_T}{\partial V_{be}} \left(\frac{\partial M_T}{\partial T} \right)^{-1} \tag{5-78}$$

When we approximate $V_{be}=V_{g0}-\lambda T$ and combine (5-77) with (5-78), we obtain:

$$\Delta T = T \frac{\Delta V_{be}}{V_{g0}} \tag{5-79}$$

With T=300K, ΔV_{be}=20mV and V_{g0}=1.2V, it follows that ΔT=5K.
We have to deal with the self-heating. With a power consumption of 5mW and a standard package, the self-heating will be less than 2K. For most of the applications, an accuracy of 5K is good enough to achieve a first-order compensation of the temperature effects.

5.8.6 Conclusions

This section has presented sensor-specific signal processing circuits. By applying these circuits, problems related to specific sensing elements have been solved. For instance:

- Multiple capacitors can be measured in a very simple way.
- Platinum resistors in series with a reference resistor are excited with a constant current.
- The exponential behavior of thermistors has been linearized to obtain an almost constant resolution.
- The dynamic range problems related to the measurement of resistive bridges have been solved by applying a divider and/or an amplifier based on Dynamic Element Matching.

5.9 Conclusions

In this chapter we have discussed all aspects related to the modulator. We started with investigating the modulator requirements. A relaxation modulator has been found to be the most suitable to operate in our system. This relaxation modulator is based on period modulation combined with modulation of the voltage swing across the integration capacitor. The low-frequency interfering signals are suppressed by synchronous detection in combination with a second-order switched capacitor filter. The low-frequency suppression has been

analyzed for both small and large interfering signals. Further, high-frequency interfering signals have been suppressed by applying, among others, dithering techniques. The modulator noise behavior was calculated by using Bennet's noise model. Due to the chopping of all signals in the modulator, the period is not sensitive to low-frequency 1/f noise as long as the corner frequency falls below the modulator frequency. A lower corner frequency is required for the current source I_{int}, since it consists of two chopped uncorrelated DC sources. The effect of limited bandwidth, finite DC gain and other effects on the linearity of the signal-to-period conversion has been investigated. There are no extreme modulator requirements that have to be met in order to obtain good linear behavior. Sensor-specific signal processing circuits have been discussed. By applying these circuits, specific problems related to the sensing elements have been solved.

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6. Design and realization

6.1 Introduction

This chapter is on the design and realization of the SSP as discussed in Chapter 5. An important aspect of the design here is that the requirements concerning resolution and accuracy, as discussed in Chapter 5, are met. We base our discussions on a 0.7μm CMOS technology featuring high-ohmic polysilicon resistors and capacitors with low-ohmic plates.

6.2 Relevant choices

In this section, we define the level of signal charges and currents flowing through the modulator. These signals set the values for several capacitors. We also discuss the noise level.

Modulator frequency

We first select a proper value for the time intervals $T_{1,i}$ and $T_{2,i}$, as defined in the previous section. These values are based only on the two main disturbing signals, which are interference from the mains supply and from the microcontroller. The frequency of these disturbing signals are 50 (or 60) Hz and several MHz, respectively. A good LF suppression requires a low value for $T_{1,i}$ and $T_{2,i}$, whereas a low sensitivity to interference from the microcontroller requires that all analog parts of the modulator have a sufficiently low bandwidth and thereby rather high values for $T_{1,i}$ and $T_{2,i}$. A good compromise is:

$$\begin{aligned} T_{1,i} &= 10\mu s \\ T_{2,i,\min} &= 10\mu s \end{aligned} \qquad (6\text{-}1)$$

When the bandwidth of an analog part can be modeled by only one pole at $\omega=-1/\tau_{HF}$, a practical value when (6-1) holds is than τ_{HF}=500ns. The related bandwidth approximates 300kHz. This is sufficiently low for a low sensitivity to interference from the microcontroller.

The choices related to the number of resistors, the number of capacitors and signal levels are listed in Table 6-1.

Item	Value	Comment
V_{DD}	5 V	power supply
$\hat{V}_o$	V_{DD}	Peak-to-peak amplitude of V_{o1} and V_{o2}
$\hat{V}_{tr}$	V_{DD}	Peak-to-peak amplitude of voltage on transmitting electrodes
N	256	Number of periods in one measurement phase
N_R	8	Number of resistors in DEM voltage divider
N_C	4	Number of capacitors in DEM voltage divider
N_{amp}	16	Number of resistors in DEM amplifier

Table 6-1. Choices for the Multiple-Sensor Modulator

Capacitors have values in the range between 1pF and 30pF. The amplitude of the integration current is below 1μA.

6.3 Complete circuit

An overview of almost all applications is shown in Figure 6-1. The connections of the sensing and reference elements to the chip are labeled by A .. F. These connections have different functions for different applications. All applications convert the sensor signal into a voltage change of node Z. The voltage on this node is sampled on $C_s = \Sigma C_{s,i}$,$i \in [1,4]$. Charge on C_s is transferred to the integrator, based on amplifier 1. By integration of I_{int}, this charge is linearly converted into a period. All applications were discussed in Chapter 5. The circuit shows the measurement of:

- Platinum resistors. The voltages across R_{pt} and R_{ref} are sampled on C_s and transferred to the integrator. The sampled voltages lies in the range 0-0.4V.
- Capacitors. The C-V converter based on amplifier 2 converts the sensor (or reference) capacitor into a voltage V_{va}, which is sampled on C_s.
- Resistive bridges with maximum imbalance $\Delta_{max}=0.04$. The output voltage V_{out} of the bridge is directly sampled on C_s. The voltage V_{BS} across the bridge is divided by 32 before it is sampled on C_s. This division stage is based on resistors $R_1..R_8$ and $C_{s,1}..C_{s,4}$.
- Resistive bridges with maximum imbalance $\Delta_{max}=2.5 \cdot 10^{-3}$. The output voltage V_{out} is amplified 15 times by the DEM voltage amplifier based on amplifiers 3 and 4. The voltage V_{BS} across the bridge is processed in the same way as for $\Delta_{max}=0.04$.
- Thermistors. The buffer stages based on amplifiers 5 and 6 drive the series connection of a thermistor R_{th} and reference resistor R_{ref}. The peak-to-peak amplitude of the drive voltage amounts to $0.08V_{DD}$. The voltage across R_{th} and R_{ref} is sampled on C_s.

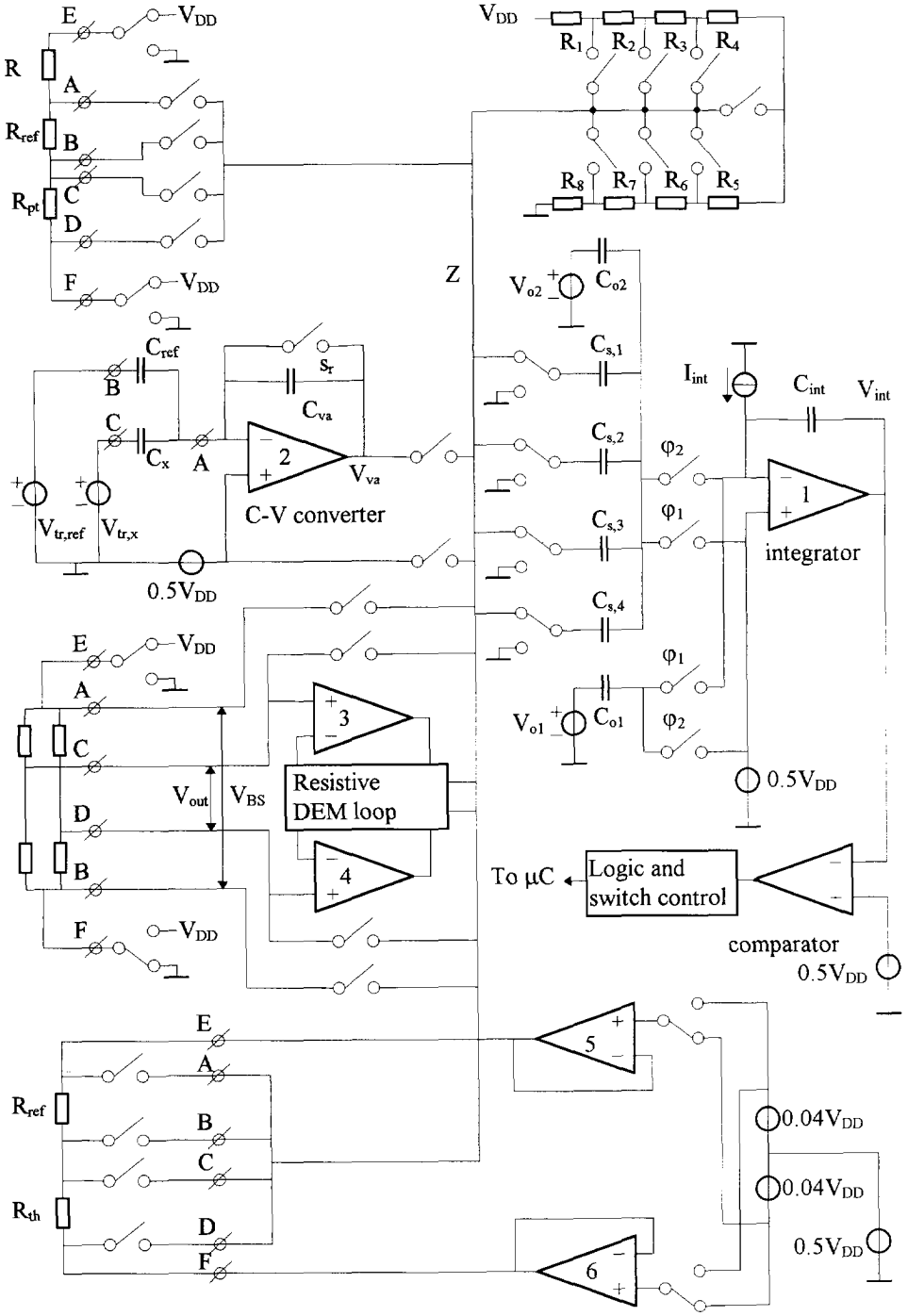


Figure 6-1. Overview of the measurement of several applications.

The realized Smart Signal Processor is able to read out more than the applications as showed in the figure. Other applications are:

- Potentiometers. These sensing elements are measured in a way similar to the measurement of platinum resistors. The bias resistor R is removed. The voltage swing V_Z of node Z equals V_{DD}. The value of the sampling capacitor is decreased to handle the large voltage swing of V_Z.
- Resistive bridges where the physical signal is represented by the ratio of the output voltage of the bridge and the current through the bridge (I-bridges). These sensing elements are also measured similar to platinum resistors. The interface offers the possibility to amplify the output voltage V_{out} of the bridge before sampling on C_s.

A buffer stage generates the reference voltage $0.5V_{DD}$, which is used for the non-inverting nodes of the C-V converter, the integrator and the comparator. The layout of this buffer stage is obtained from a standard library. The amplifiers 3, 4, 5 and 6 are combined. Only two amplifiers are used to perform the amplification of small voltages of V_{out} and to drive the sensor for the measurement of thermistors. The layout of these amplifiers is also obtained from a standard library. The layout of the comparator is also obtained from the a standard library. Specifications for the amplifiers and comparator are listed in Table 6-2.

Parameter	Amplifier 1	Amplifier 2	Amplifiers 2 .. 5	Comparator
Type	OTA	OTA	OpAmp	Comparator
Supply current	100 µA	530 µA	280 µA	65 µA
White noise	50 nV/√Hz	12 nV/√Hz	25 nV/√Hz	?
f_{-3dB} / f_T / delay	75 MHz	25 MHz	5 MHz	0.3µs
g_m	250 µA/V	1.3 mA/V	--	--
DC gain	95 dB	90 dB	120 dB	120 dB

Table 6-2. Simulated specifications of the amplifiers and comparator.

The white noise levels of the amplifiers 1 and 2 have been designed to meet the specifications as mentioned in Chapter 2. The use of CMOS implies rather large values for the 1/f noise corner frequency. Due to the applied chopping techniques, the requirement is that this corner frequency falls below the frequency of the modulator. The resolution will not be affected by 1/f noise in this case. The requirements for the corner frequency of the integration current I_{int} are more stringent, since I_{int} is implemented by two chopped DC current sources. This is explained later. The resolution will not be affected if the 1/f noise corner frequency of I_{int} falls below the reciprocal value of one full measurement cycle.

The block containing the logic and switch control consists of a number of digital cells, like flip-flops, NAND's, inverters etc. It consists of more than 400 digital cells and the main parts are:

- The control of the 160 analog switches, including sampling switches, switches in the DEM amplifier, switches in the DEM divider etc.
- The period counter for counting N modulator periods
- The counter for selection of the measurement phases
- Logic for generating the input signal for the microcontroller

A microphotograph of the complete interface is shown in Figure 6-2.
The die size measures 5.5 mm^2 (2.9 x 1.9 mm) and is mounted in a 16-pins DIL package. The active area (the area within the ring of the power supply lines) measures 3.6 mm^2.

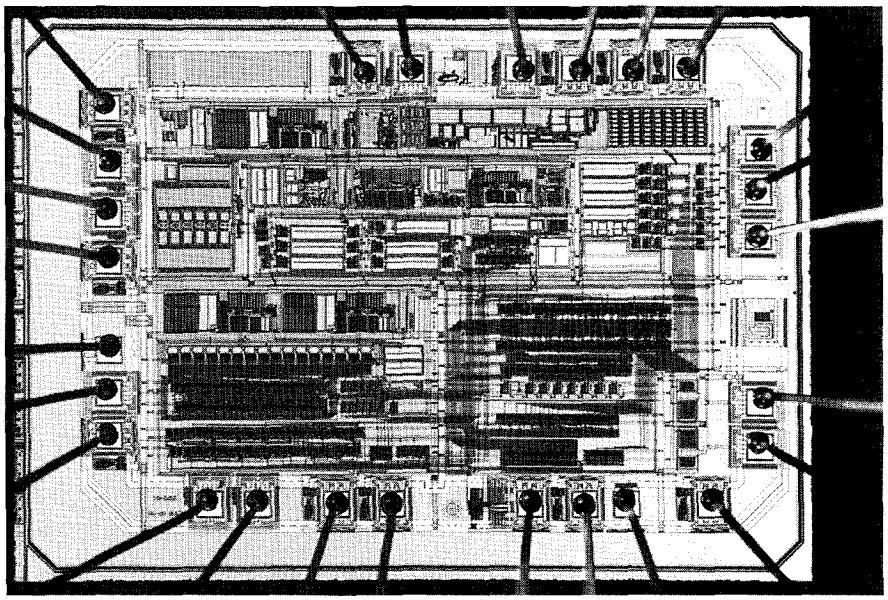


Figure 6-2. Microphotograph of the interface. The chip was realized in a 0.7μm CMOS process, measures 5.5mm^2 and is mounted in a 16-pins DIL package.

6.3.1 The integrator

We implemented the amplifier as an Operational Transconductance Amplifier (OTA) , because of its excellent output voltage swing and the simplicity of obtaining HF stability. We used a single-stage topology. A two-stage topology has a much higher DC gain, but this does not play a role in connection with the nonlinearity, as long as the output resistance of the current source I_{int} is sufficiently large. This is not very difficult to realize.
Voltage-dependence of the feedback capacitor does not result in nonlinear behavior and is, therefore, allowed. The bottom plate is embedded in the substrate and can pick up substrate noise. It is, therefore, connected to the output of the amplifier.

Bandwidth and stability
The bandwidth of the integrator should be limited to 500kHz. A narrow bandwidth results in nonlinear behavior, while a wider bandwidth results in an increase of the sensitivity to interference from the microcontroller. Since the capacitor C_s ($=\Sigma C_{si}$) is disconnected from the integrator during phase φ_1, the bandwidth of the integrator during φ_1 is wider than during φ_2. A method to obtain a constant bandwidth is to add a dummy capacitor C_{dum} which is equal to C_s. This capacitor is connected to the integrator during φ_1, as shown in Figure 6-3. A disadvantage of using a dummy capacitor is that there is an increase in the noise level. The dummy capacitor has not been applied.

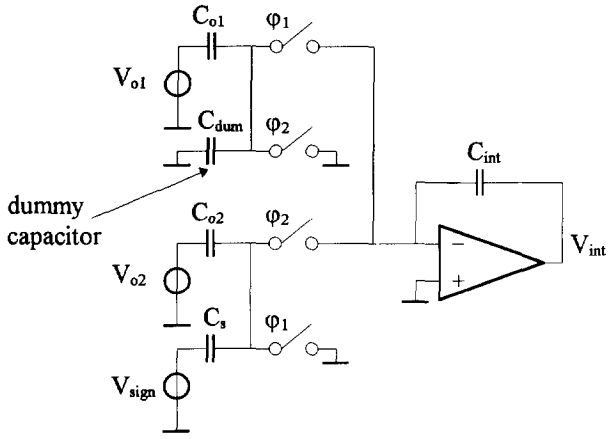


Figure 6-3. A dummy capacitor C_{dum} can be added to achieve a constant bandwidth.

The simulated bandwidth of the transconductance amplifier equals 75 MHz, as listed in Table 6-2. This bandwidth is very high with respect to the integrator's closed-loop bandwidth, so the closed-loop bandwidth will be determined by the feedback network. The OTA can now be modeled by an infinite-bandwidth system, as shown in Figure 6-4.

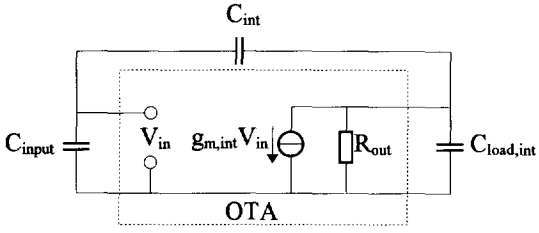


Figure 6-4. A simple model of the integrator to calculate the high-frequency bandwidth.

The high-frequency time constant $\tau_{HF,int}$ of the system in Figure 6-4 is given by:

$$\tau_{HF,\text{int}} = \frac{R_{out}\left(C_{input}C_{\text{int}} + C_{load,\text{int}}C_{\text{int}} + C_{input}C_{load,\text{int}}\right)}{\left(g_{m,\text{int}}R_{out} + 1\right)C_{\text{int}} + C_{input}} \tag{6-2}$$

When $g_{m,int}R_{out}>>1$ and $g_{m,int}R_{out}>>C_{input}/C_{int}$, (6-2) can be simplified into:

$$\tau_{HF,\text{int}} = \frac{C_{input}}{g_{m,\text{int}}}\left(1+\frac{C_{load,\text{int}}}{C_{\text{int}}}\right)+\frac{C_{load,\text{int}}}{g_{m,\text{int}}} \tag{6-3}$$

With $C_{int}=C_{load,int}=10pF$ and $C_{input}=45pF$ (we consider φ_2), the required transconductance to achieve $\tau_{HF,int}=500ns$ amounts to $200\mu A/V$. Operation in the strong inversion region, where $|V_{GS}-V_{TH}|>0.2V$ for the $0.7\mu m$ CMOS process, requires a bias current of at least $20\mu A$ per transistor. The bias currents through the input and output stage are chosen to be equal and the required minimal total bias current becomes $80\mu A$. The minimal bias current is not only determined by the bandwidth, but also by the noise requirements.

Class AB operation

The Castello and Gray's class-AB OTA [1] enables a large output current. The bias current through the output stage of this OTA equals the bias current through the input stage. Since the integration current is only 500nA, a 20μA bias current flowing through the output stage will be enough to properly integrate I_{int}. A class AB configuration will, therefore, not have an advantage over a class A OTA.

6.3.2 The capacitance-to-voltage converter

The capacitor-to-voltage (C-V) converter converts the sensor and reference capacitance into a voltage V_{va}. This voltage is sampled on C_s and processed to the integrator, as shown in Figure 6-5.

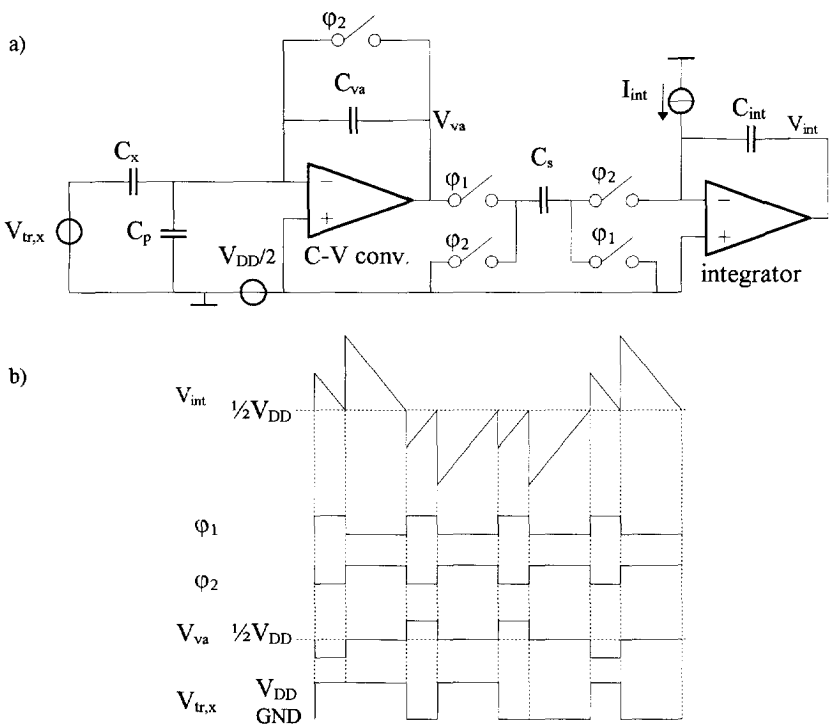


Figure 6-5. The capacitor-to-voltage converter followed by the integrator (a) and related signal forms (b).

The bottom plate of C_{va}, which is embedded in the substrate, can easily pick up interference and is therefore connected to the output of the amplifier.

The amplifier can be implemented as an OpAmp or as an OTA. As discussed in Chapter 5, an OTA is preferable in view of HF stability aspects. The main pole is determined by C_p, since the OTA is based on a single-stage topology. The high-frequency time constant $\tau_{HF,va}$ can be calculated in a way similar to (6-3):

$$\tau_{HF,va} = \frac{C_p}{g_{m,va}}\left(1+\frac{C_{load,va}}{C_{va}}\right)+\frac{C_{load,va}}{g_{m,va}} \qquad (6\text{-}4)$$

where we neglected C_x. The capacitor $C_{load,va}$ is the capacitance at the output of the OTA and is formed by C_s (only during φ_1) and the substrate capacitance of C_{va}. We expect that the nonlinearity due to the limited bandwidth becomes important when $\tau_{HF,va}$ becomes larger than $T_1/15=0.66\mu s$. With $g_{m,va}=1.3mA/V$ (see Table 6-2) and $C_{load,va}/C_{va}=1$, values of C_p up to 430pF are allowed to obtain a linearity better than 100ppm. Larger values for C_p can be handled with the same linearity by increasing $g_{m,va}$ or by shunting C_p by a switch which is closed during φ_2. This was discussed in Chapter 5.
The DC gain of the OTA (90dB) is large enough to obtain a linearity better than 10ppm.

6.3.3 Switch sequence

The switches connected to C_s, as shown in Figure 6-6, operate in a certain sequence. The first step is the break-before-make (BBM) operation of the switches at the input of the integrator (s_1 and s_2). After this, s_3 and s_4 operate in an arbitrary sequence. The result of this is that switch charge injection into the integrator originates only from s_1 and s_2. The switch charge injection of these switches is constant and causes, therefore, an offset. The switches have been implemented by an NMOS and a PMOS transistor in parallel.

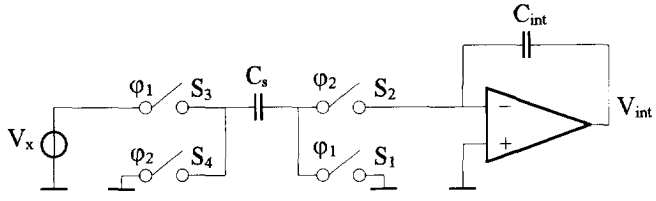


Figure 6-6. The switches connected to C_s operate in a certain sequence.

The required logic to generate the control signals for the switches is shown in Figure 6-7. The signal "in" is derived from the output signal of the comparator. As can be seen from the time signals in b), switches s_3 and s_4 operate after the BBM operation of s_1 and s_2.

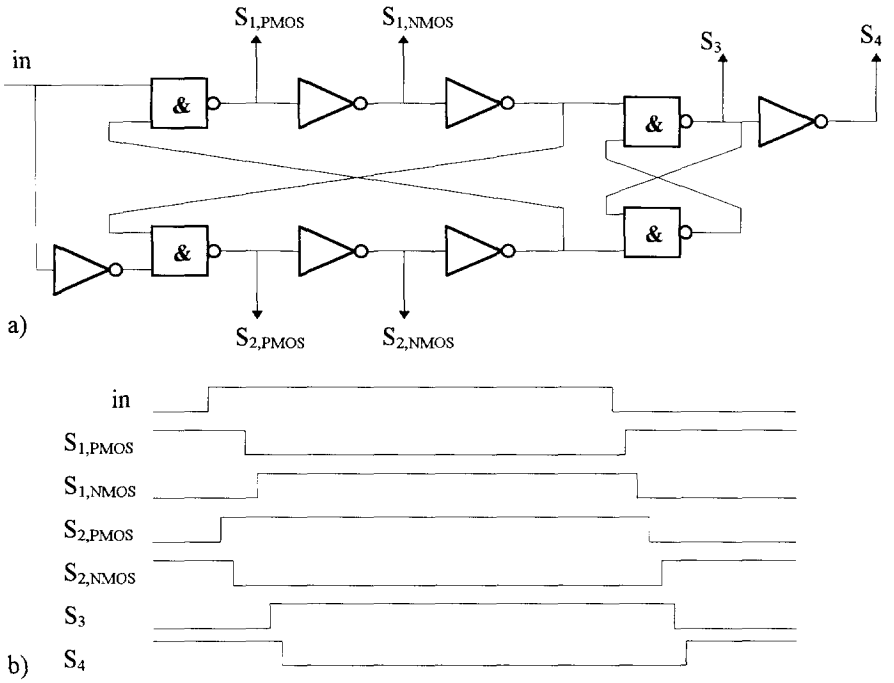


Figure 6-7. Logic generating the control signals for switches s_1 to s_4 (a) and time signals (b).

6.3.4 The integration current source I_{int}

The integration current source I_{int} of the Multiple-Sensor Modulator is an important part of the modulator. It converts charges into time intervals.

Important requirements for this current source are:

1. The positive and negative value of the current should be very closely matched. A mismatch of $3 \cdot 10^{-4}$ results in a decrease of the LF suppression by a factor two, as discussed in Chapter 5.
2. The output resistance should be large in order to obtain a linear charge-to-time conversion.
3. When I_{int} is implemented by two current sources which are alternately connected and disconnected to the integrator, the modulator loses its insensitivity to the LF 1/f noise of the two currents.

The implementation of I_{int} as shown in Figure 6-8 has the advantages of a low sensitivity to LF 1/f noise and a sufficiently low nonlinearity. The main disadvantage is that the positive and negative value of I_{int} can only be made equal by choosing matched on-chip components. These matched components are required to generate $V_{DD}/2$. However, a mismatch of less than 10^{-3} can hardly be achieved by relying on matching.

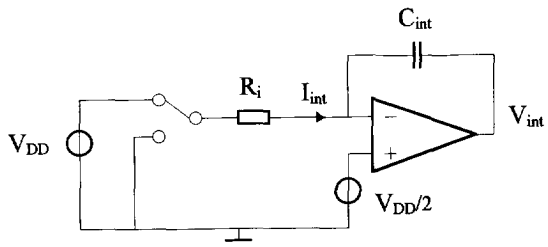


Figure 6-8. Generation of the integration current I_{int} by a switched resistor R_i.

A current source which allows a better matching between the positive and negative value of I_{int} is based on a dynamic current mirror where the input and output transistor are the same, as shown in Figure 6-9. This principle has been used by Groeneveld et. al. [2] and is based on switched-current (SI) techniques. One of the problems of SI techniques is related to switch charge injection, but these have been solved.

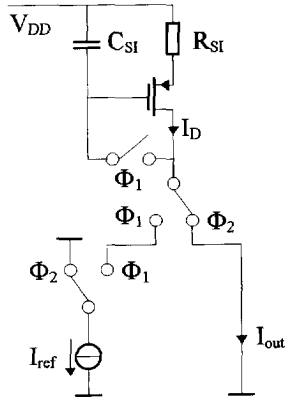


Figure 6-9. Dynamic current mirror with a very accurate gain.

During phase Φ_1, the reference current I_{ref} is copied to I_D. At the end of this phase, the feedback switch opens and a voltage is held on C_{SI}. During phase Φ_2, the transistor is switched as a current source and I_{out} equals I_{ref}. Resistor R_{SI} is added to decrease the noise level.
The total current source I_{int} is based on three of those copy cells and is shown in Figure 6-10. The circuit needs three phases Φ_i to generate I_{int}. I_{ref} is copied directly to $I_D(M_2)$. I_{ref} is copied to $I_D(M_1)$ with help of the copy cell based on M_3.

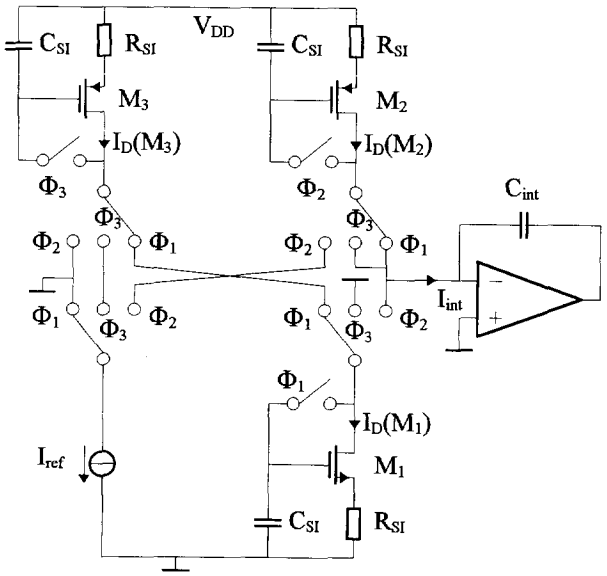


Figure 6-10. An SI-based current source with equal positive and negative value for I_{int}.

The control signals for the switches is shown in Figure 6-11. During phase Φ_1, the current $I_D(M_3)$ is copied to $I_D(M_1)$, while $I_D(M_2)$ is integrated. During phase Φ_2, I_{ref} is copied to $I_D(M_2)$, while $I_D(M_1)$ is integrated. Finally, during phase Φ_3, I_{ref} is copied to $I_D(M_3)$.

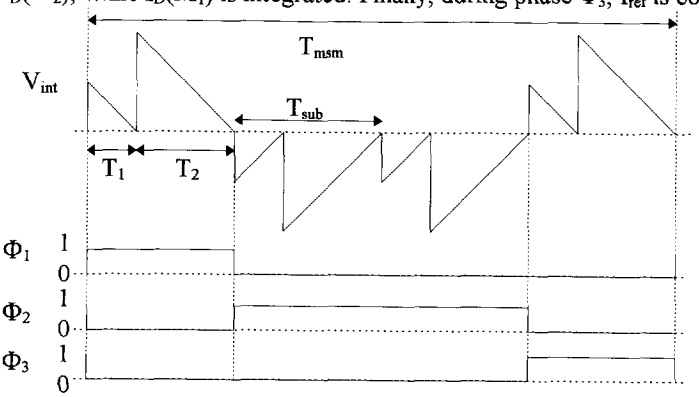


Figure 6-11. Control signals for the current source in Figure 6-10.

Noise

The sampling operation in each copy cell causes an increase in the noise level. The original noise current of each block is assumed to be $4kT/R_{SI}$ ($R_{SI}>>1/g_m$). We calculate the value of C_{SI} for which the noise is increased by 3 dB.

During the sampling phase of a copy cell (the feedback switch is conducting), the thermal noise $4kTR_{SI}$ is filtered by the $R_{SI}C_{SI}$ LPF. This is valid for $R_{SI}>>1/g_m$ and this assumption will be checked later. The noise power on C_{SI} now equals kT/C_{SI}. This noise power can be shifted in series with R_{SI}, thereby generating a noise current. The main voltage across R_{SI} equals $I_{ref}R_{SI}$. The SNR for N periods T_{msm} (N samples) is given by:

$$SNR_{kT/C} = \frac{NI_{ref}^2 R_{SI}^2 C_{SI}}{kT} \tag{6-5}$$

The SNR for the original noise current $4kT/R_{SI}$ is given by the ratio if the duration $(NT_{msm})^2$ of a measurement phase and the variance σ_i^2 (see Table 5-2):

$$SNR_{orig} = \frac{2NT_{msm}I_{ref}^2 R_{SI}}{4kT} \tag{6-6}$$

Equalizing equations (6-5) and (6-6) results in:

$$R_{SI}C_{SI} = \tfrac{1}{2}T_{msm} = 2T_{sub} \tag{6-7}$$

When the value for C_{SI} satisfies (6-7), the noise level of the current source is increased by 3dB. It is no problem that the time constant $R_{SI}C_{SI}$ is larger than T_{sub}, since this will only cause a transient after switching on the power supply.

The required 1/f noise corner frequency of I_{ref} is lower than the reciprocal value of one complete measurement cycle (approximately 100ms). The contribution of 1/f noise of I_{ref} can then be neglected. The restrictions to the dynamic current sources are much more relaxed. This is the result of the periodical updating of the dynamic current sources.

Output resistance

The output resistance of the current source causes a LF pole in the charge-to-time transfer. It is no problem to keep the nonlinearity caused by this pole below 1ppm, as discussed in section 5.7. The output resistance can be calculated from the standard strong inversion relation between drain current I_D and drain-source voltage V_{DS}:

$$I_D = \tfrac{1}{2}\frac{W}{L}\mu C_{ox}\left(V_{GS} - V_{TH}\right)^2\left(1 + \lambda V_{DS}\right) \tag{6-8}$$

where μ is the mobility and C_{ox} the oxide capacitance per unit area.
The output resistance of the MOS transistor is given by r_d:

$$\begin{aligned} r_d^{-1} &= \frac{\partial I_D}{\partial V_{DS}} \\ &= \lambda I_D\big|_{V_{DS}=0} \cong \lambda I_D \end{aligned} \tag{6-9}$$

The output resistance of the current source is now given by $R_{out,SI}$:

$$R_{out,SI} = r_d\left(1 + g_m R_{SI}\right) \tag{6-10}$$

We assume that the transistor operates in strong inversion, near moderate inversion. The voltage $|V_{GS}-V_{TH}|$ equals 0.2V. The transconductance with a fixed 500nA bias current then equals 5µA/V. With $\lambda = 3\cdot10^{-3}$, R_{SI}=1MΩ, the output resistance $R_{out,SI}$=4GΩ. In combination with a 95dB amplifier DC gain in the integrator stage and C_{int}=10pF, the LF time constant equals $2.2\cdot10^3$s. This large time constant results in a negligible nonlinear behavior.

Switch charge injection of feedback switches

The opening of the MOS feedback switch causes a flow of charge to C_{SI}. This switch charge injection (SCI) disturbs the gain factor of a copy cell. We have to deal with two problems. These are:

1. The current $I_D(M_2)$ is generated by using only one copy cell, while $I_D(M_1)$ is generated by using two copy cells. Since the gain factors differs from 1, the result is that $I_D(M_1)$ and $I_D(M_2)$ are not equal.
2. The gain change due to SCI of a copy cell based on an NMOS transistor (M_1, current sink) differs from that based on a PMOS transistor (M_2 and M_3, current source). This is also true when every feedback switch consists of an NMOS and a PMOS transistor in parallel.

These problems can be solved by using only PMOS transistors as switches in the copy cell based on M_2 and M_3, and an NMOS transistor as a switch in the copy cell based on M_1. The length and width of these transistors also have to satisfy certain rules.

The length of the switch transistors are denoted by $L_{n,1}$, $L_{p,2}$ and $L_{p,3}$ for the transistors in the copy cells based on M_1, M_2 and M_3, respectively. The width is denoted in the same way by $W_{n,1}$, $W_{p,2}$ and $W_{p,3}$.

Two contributions to SCI from MOS switches can be distinguished:

1. A contribution due to gate-drain/source overlap capacitance
2. A contribution due to the channel charge. The channel charge of an MOS transistor operated in strong inversion and in its linear region is given by Q_{ox}:

$$Q_{ox} = (V_{GS} - V_{TH})WLC_{ox} \tag{6-11}$$

where V_{TH} is the threshold voltage V_{GS} the voltage between gate and source, W the width, L the length and C_{ox} the unit capacitance.

We compensate separately for both contributions to SCI.

For the contribution from the overlap capacitance can be compensated when the following equation is satisfied:

$$W_{n,1} = W_{p,3} = \frac{1}{2}W_{p,2} \tag{6-12}$$

When (6-12) is true, the gain change due to the overlap capacitance of the copy cell based on M_2 is twice that of the other two copy cells.

With $L_{p,2}=L_{p,3}=L_p$, the length $L_{n,1}$ should satisfy:

$$L_{n,1} = L_p \frac{\Delta V_{gate} - I_{ref}R_{SI} + 2V_{TH,p}}{\Delta V_{gate} - I_{ref}R_{SI} - 2V_{TH,n}} \tag{6-13}$$

where ΔV_{gate} is the swing of the gate voltage. With ΔV_{gate}=5V, $I_{ref}R_{SI}$=0.5V, $V_{TH,n}$=0.8V and $V_{TH,p}$=-1V, the value for $L_{n,1}$ amounts to $0.86L_p$.

When (6-12) and (6-13) have been satisfied, the SCI due to overlap capacitance and channel charge have been compensated and the effect of SCI on the current mismatch is theoretically eliminated. Further, we have locally compensated the SCI by applying dummy switches, as described by Yen and Gray [3].

6.3.5 Bias circuit

The bias current is used for biasing all active parts like OTAs, amplifiers etc. Its accuracy and noise is not very critical. The bias current is generated by a PTAT source, as shown in Figure

6-12. The transistors M_1 and M_2 operate in the weak inversion region. Transistor M_2 has a doubled width with respect to M_1. The current I_{bias} is than given by:

$$I_{bias} = \frac{kT\ln(2)}{nqR_{bias}} \qquad (6\text{-}14)$$

where the constant n is 1.5 and q the charge of an electron.

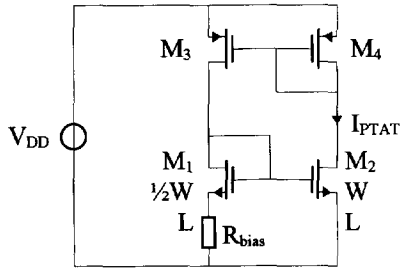


Figure 6-12. A PTAT current is used to bias the complete modulator.

The current I_{bias} has a PTAT character when R_{bias} is temperature independent. An N-well resistor has a positive temperature coefficient, which compensates for the temperature coefficient of the PTAT voltage. The result is a bias current with a reduced temperature coefficient.

6.3.6 Watch dog

The function of the watch dog is to start the oscillation process when desired. This is, for instance, after switching on the power supply, or after an unwanted stop of the oscillation process. We consider two methods to detect whether the modulator has stopped oscillating. These are:

Comparison of V_{int} with two reference levels

The output voltage V_{int} of the integrator is compared with two reference levels V_1 and V_2, as shown in Figure 6-13 . When V_{int} falls outside the range determined by these voltages, a start-up trigger should be generated.

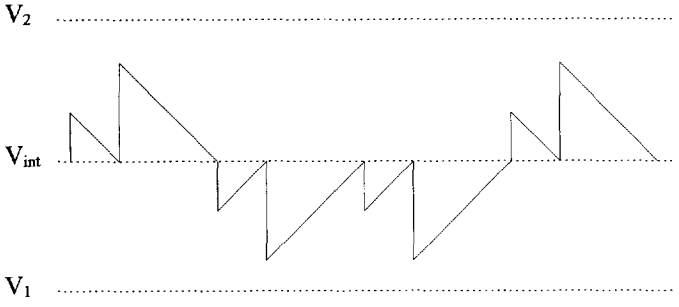


Figure 6-13. Detection of the oscillation process by comparison V_{int} with two reference levels.

A disadvantage of this method is that the part of the maximum voltage swing of V_{int} has to be reserved for detection purposes. This decreases the usable voltage swing of V_{int}.

Compare the period of the modulator with a time interval

Another method to detect whether the modulator is oscillating or not is to compare the period of the modulator T_{msm} with an on-chip time interval T_{wd}. When T_{msm} is larger than T_{wd}, a start-up trigger pulse should be generated. In normal operation, the relation $T_{wd}>T_{msm,max}$ holds.
The time interval T_{wd} can be generated by charging a capacitor to a certain reference voltage. The capacitor is periodically reset. When the time between two resets becomes greater than T_{wd}, a start-up pulse is generated. A circuit implementing these functions is shown in Figure 6-14. When V_{mod} (with period T_{msm}) is high, capacitor $C_{wd,2}$ is reset and $V_{wd,1}$ increases. During normal operation, capacitor $C_{wd,1}$ is reset before the threshold voltage is reached. The one-shot generator is triggered when one of the voltages V_{wd} reaches the threshold. The time interval T_{wd} is given by:

$$T_{wd} = \frac{C_{wd}V_{DD}}{2I_{wd}} \qquad (6\text{-}15)$$

The value for T_{wd} must be longer than $T_{msm,max}$. It is safe to use a sufficiently large margin to obviate unwanted activation of the start-up circuit. With C_{wd}=1pF, V_{DD}=5V and I_{wd}=2nA, the time interval T_{wd} amounts to 2.5ms.

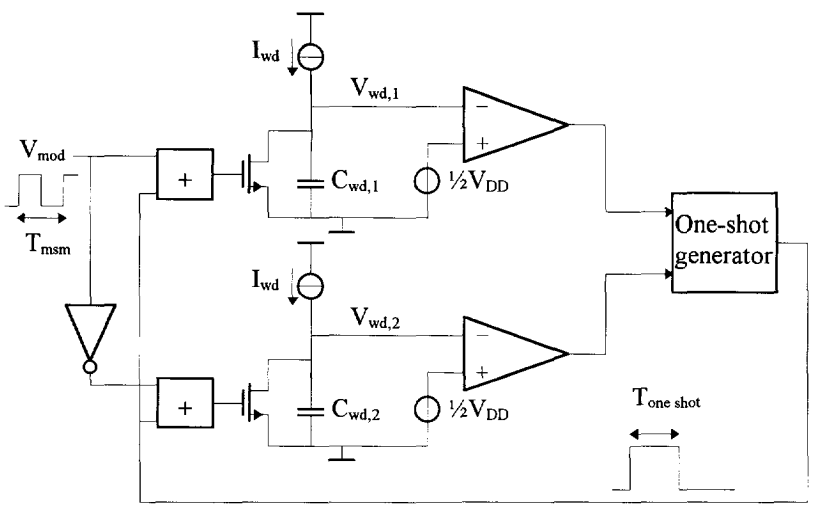


Figure 6-14. Detection of the oscillation process by comparing the modulator period T_{msm} with a time interval T_{wd}.

The reset pulse forces a fixed value for V_{int} and I_{int}. The modulator is released after a time interval $T_{one\ shot}$ and the oscillation process starts.

6.4 Conclusions

The Smart Signal Processor was designed in a 0.7µm CMOS process, measures 5.5mm^2 and is mounted into a standard 16 pins DIL package. Although many different sensor elements can be connected to the SSP, the number of connections for the sensor elements to the SSP is limited to six. The function of every connection pad, therefore, depends of the type of sensor element. The modulator consists of several sensor-specific front-ends and a common part. The latter

consists of a switched-capacitor integrator, a comparator, a square-wave current source and logic circuits. Several switches, controlled by logic circuits, guarantee the sampling of the right voltages and the transfer of the right charges. In order to achieve the maximum available suppression of low-frequency interfering signals, the generation of the integration current is based on switched-current (SI) techniques. Application of this technique results in the required accurately-matched positive and negative values of the integration current. A watch dog detects whether the oscillation process has stopped for a certain time and (re)starts the oscillator when this is necessary.

6.5 References

1 R. Castello and P.R. Gray, "A High-Performance Switched-Capacitor Filter", IEEE J. of Solid-State Circuits, vol. SC-20, pp 1122-1132, December 1985.

2 D. Groeneveld, H. Schouwenaars, H. Termeer and C. Bastiaansen, "A Self-Calibration Technique for Monolithic High-resolution D/A Converters", IEEE J. of Solid-State Circuits, vol. 24, pp 1517-1522, December 1989.

3 Robert C. Yen and Paul R. Gray, "A MOS Switched-Capacitor Instrumentation Amplifier", IEEE J. of Solid-State Circuits, vol. SC-17, pp 1008-1013, December 1982.

7. Applications and measurement results

7.1 Introduction

The complete multiple-purpose sensor interface has been realized in a 0.7μm CMOS process. The interface has 16 different applications. All these applications are discussed separately in Appendix C. Several applications have specific circuit parts in common. Applications sharing the same electronics can be characterized by characterizing only one application. We, therefore, characterize the performance of the following applications:

- Capacitors
- Platinum resistors
- Resistive bridges
- Thermistors

We start with the measurement of the resolution and the linearity, followed by the measurement of low-frequency and high-frequency suppression. Also temperature and power-supply effects have been measured.

7.2 Measurement of resolution and nonlinearity

Measurement setup

The measurement of resolution and nonlinearity have been performed with the measurement setup as shown in Figure 7-1. The system is based on a sensing and reference element, the interface, a microcontroller and a PC.

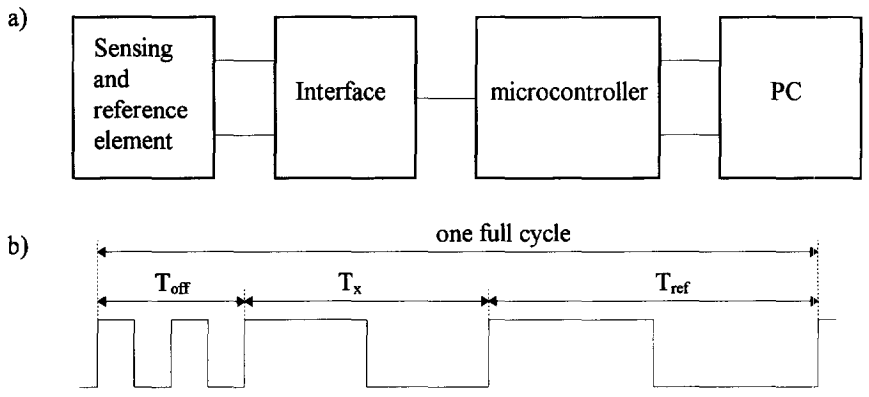


Figure 7-1. Measurement setup (a) and the output signal of the interface (b).

The microcontroller is an Intel 87C51FB with a clock frequency of 12 MHz. The sampling frequency equals 3MHz. The output signal is shown in b). The interface selects automatically the three measurement phases to perform the three-signal technique. The offset measurement phase is labeled by temporarily doubling the output frequency of the interface. Every measurement phase consists of N modulator periods. The value of N equals 256 or 32, depending on an external selection bit. The nominal period varies between 80µs and 150µs. The duration of one full cycle then approximately amounts to 10ms (N=32) or 80ms (N=256).

Definition of nonlinearity

The calculation of the nonlinearity is based on four measurements instead of the three measurements as shown in Figure 7-1. In addition to the measurement of the offset signal E_{off}, the signals $E_{x1}+E_{off}$ and $E_{x2}+E_{off}$ are measured separately, and, finally, the sum $E_{x1}+E_{x2}+E_{off}$ is measured. This results in four measurement phases:

1. Measurement of $T_{off}=GE_{off}$
2. Measurement of $T_{x1}= G(E_{off}+E_{x1})$
3. Measurement of $T_{x2}=G(E_{off}+E_{x2})$
4. Measurement of $T_{x1+x2}=G(E_{off}+E_{x1}+E_{x2})$

The nonlinearity λ is now defined by:

$$\lambda = \frac{T_{x1} + T_{x2} - 2T_{off}}{T_{x1+x2} - T_{off}} - 1 \qquad (7\text{-}1)$$

When the modulator is perfectly linear, the nonlinearity amounts to zero.

7.2.2 Measurement of capacitors

The connection of the signal and reference capacitor to the interface and its input stage are shown in Figure 7-2. The output of the capacitance-to-voltage (C-V) converter is sampled and charge on the sampling capacitor is converted into a period.

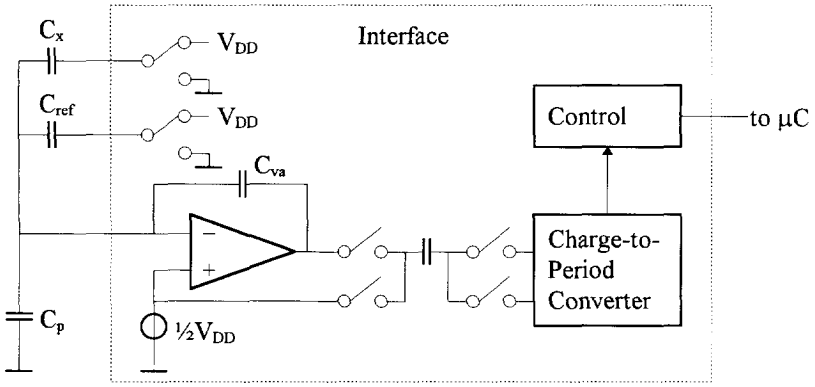


Figure 7-2. Connection of two capacitors to the interface and its input stage.

The interface is able to measure capacitors in several ranges. Different ranges can be selected by changing the feedback capacitor in the C-V converter and/or by changing the amplitude of the signal V_{tr} on the transmitting electrode. Capacitors can be measured in three different ranges:

1. 0-2pF (C_{va}=7pF, $\hat{V}_{tr}=V_{DD}$)
2. 0-12pF (C_{va}=42pF, $\hat{V}_{tr}=V_{DD}$)
3. Any range between 0-300pF (C_{va}=42pF and variable amplitude $\hat{V}_{tr}$)

7.2.2.1 Resolution

Table 7-1 shows the calculated and the measured capacitive resolution for the measurement range of 0-2pF and for C_p=50pF and N=256. The measurement time of one cycle is 80ms.

Noise source	Calculated resolution	Measured resolution
u_{ni}	5 aF	
u_{na}	11 aF	
$u_{n,buf}$	22 aF	
quantization	5 aF	
Total	26 aF	50aF

Table 7-1. Calculated and measured capacitive resolution in the 0-2pF range for C_p=50pF and N=256. The measurement time of one cycle amounts to 80ms.

The measured resolution is only 6 dB worse than the calculated resolution. The calculated resolution is based only on white noise. The difference between the calculated and the measured resolution could be caused by 1/f noise, but this noise does not play a role. This is discussed later. The difference can be caused by an increased white noise level or by increased bandwidths of analog parts.

The largest contribution to the resolution is caused by $u_{n,buf}$. This is the noise voltage of the amplifier which buffers the reference voltage $V_{DD}/2$. This voltage is used as a reference voltage for the non-inverting inputs of the C-V converter and the integrator. Calculation of its effect on the resolution is given in Appendix B. The contribution to the resolution of this noise can easily be decreased by decreasing the bandwidth of the amplifier. The bandwidth of this buffer

amplifier can be decreased four times without running into bandwidth-limitation problems. The contribution of $u_{n,buf}$ will then be 11 aF, which results in a total calculated resolution of 17aF.

Resolution versus measurement time

The resolution has also been measured as a function of the measurement time. It is possible to bypass the three-signal protocol of the interface by selecting a special interface mode. The interface now behaves like a capacitive-controlled oscillator without a multiplexer. The microcontroller now implements the three-signal technique by selecting the measurement phases. This setup is shown in Figure 7-3. The signal V_{tr} is multiplexed to none, one, or both of the capacitors C_{x1} and C_{x2}. The length of a measurement phase is determined by the microcontroller and varies between 1 to 10^5 periods.

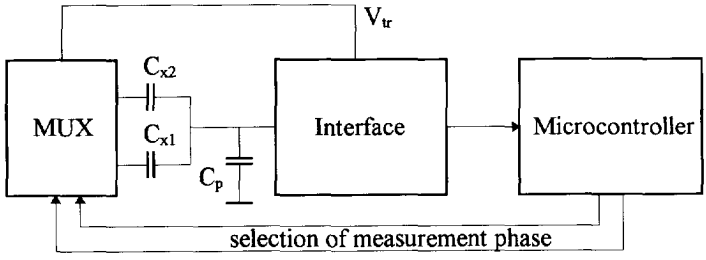


Figure 7-3. Measurement setup to measure the resolution versus the measurement time. The interface is put in a special mode and behaves like a capacitive-controlled oscillator. The measurement phases are now selected by the microcontroller instead of the interface.

The measured resolution as a function of the total measurement time (time of three measurement phases) is shown in Figure 7-4. The parasitic capacitance amounts to 50pF and the measurement range equals 0-2pF.

For short measurement times, the quantization noise is dominant. The resolution in this range is inverse proportional to the measurement time T_{meas}. When the electronic white noise of the modulator dominates, the resolution varies inverse proportional to the square root out of the measurement time. These two relations are clearly visible in the plot. Any 1/f component in the period would cause a flat curve in the plot. Since no such flat curve is visible, the 1/f corner frequency can not be measured but is below 0.5Hz.

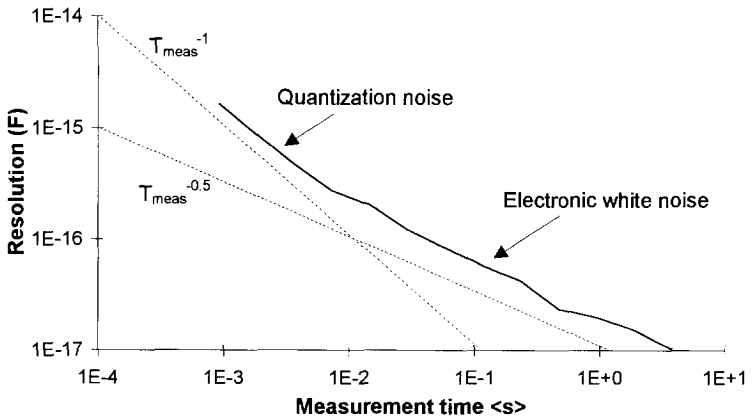


Figure 7-4. Resolution after the calculation of the three-signal technique versus the total measurement time. The measurement range equals 0-2pF and C_p=50pF.

Resolution versus parasitic capacitance

The resolution is also measured as a function of the parasitic capacitance C_p. The measurement setup is showed in Figure 7-2. Since 1/f noise plays no role, we only focus on white noise. The dominant noise sources for large values of C_p is the noise voltage u_{na} of the amplifier in the C-V converter. another dominant source is the noise voltage u_{nbias} of the buffer amplifier. The bandwidth B_{va} of the C-V converter is inverse proportional to C_p. The resolution then becomes proportional to the square root out of C_p. This relation is visible in Figure 7-5.

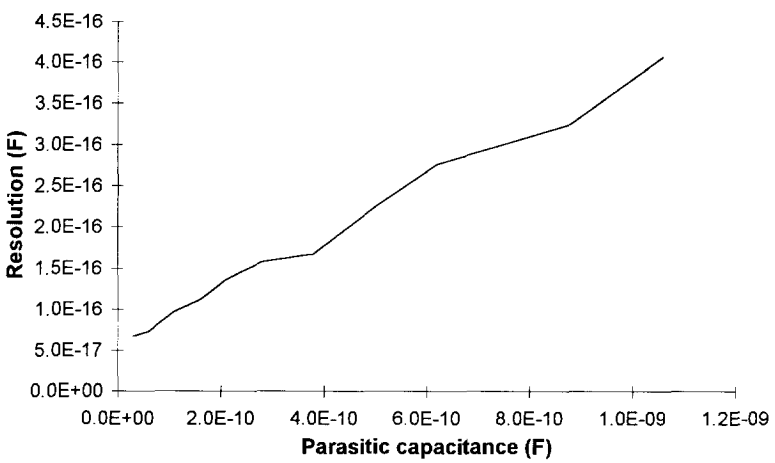


Figure 7-5. Resolution after the calculation related to the three-signal technique versus the parasitic capacitance C_p. The measurement range equals 0-2pF.

7.2.2.2 Offset

When the internal multiplexer is used, we expect offset problems due to the parasitic

capacitance between the terminals of the transmitting and the receiving electrodes. The interface mounted in a package is shown in Figure 7-6. The transmitting terminals are the pins B and C, and pin A is the receiving terminal. The parallel parasitic capacitances $C_{p,AB}$, $C_{p,AC}$ and $C_{p,AD}$ are air-capacitors or are caused by the package.

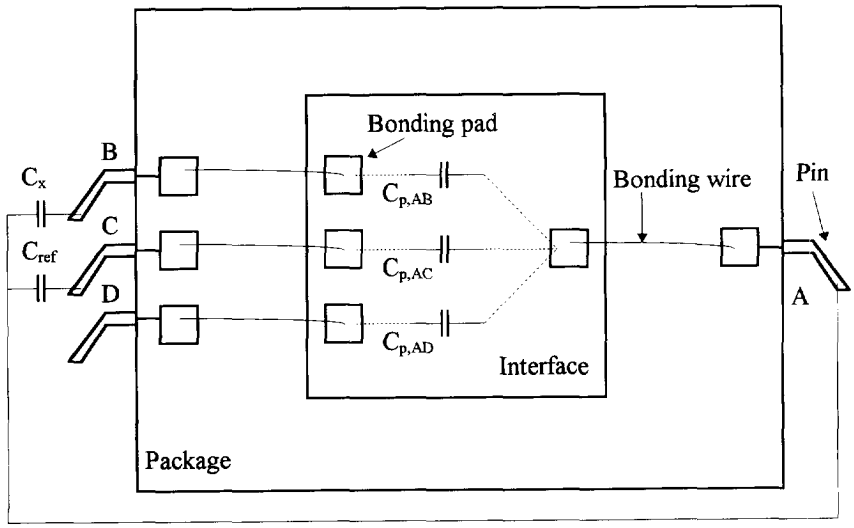


Figure 7-6. Interface mounted in a package. Pin A is used for the receiving electrodes and pins B to D for the transmitting electrodes. The parallel parasitic capacitors $C_{p,AB}$, $C_{p,AC}$ and $C_{p,AD}$ are air-capacitors or are caused by the package. Their effect is eliminated when they are equal.

The parallel parasitics form an additive error when they are equal. Their effect on the final measurement result C_x/C_{ref} can be eliminated in this case. The offset measurement is performed by measuring pin D to which no capacitor has been connected. The measurement phases are now given by;

$$\begin{aligned} T_{off} &= T_0 + K_{\mathrm{mod},C} C_{p,AD} \\ T_{ref} &= T_0 + K_{\mathrm{mod},C}\left(C_{ref} + C_{p,AC}\right) \\ T_x &= T_0 + K_{\mathrm{mod},C}\left(C_x + C_{p,AB}\right) \end{aligned} \tag{7-2}$$

where T_0 and $K_{mod,C}$ are constants of the modulator. Calculation of the final result M gives:

$$\begin{aligned} M &= \frac{T_x - T_{off}}{T_{ref} - T_{off}} \\ &= \frac{C_x + C_{p,AB} - C_{p,AD}}{C_{ref} + C_{p,AC} - C_{p,AD}} \end{aligned} \tag{7-3}$$

When the parallel parasitics are equal, their effect is completely eliminated by the three-signal technique. Any mismatch between these parallel parasitics leads to an error. The measured offsets in the 0-2pF range are smaller than 25fF. This is caused by mismatch between the parallel parasitics. Smaller offsets can only be obtained by applying an external multiplexer in

combination with shielding or maintaining a sufficiently large distance between the transmitting and receiving terminals.

7.2.2.3 Nonlinearity

The nonlinearity in the range 0-2pF has been measured with two capacitors of 1pF each. The capacitors are made of Teflon, which has a very small dielectric absorption. The nonlinearity has been measured using an external multiplexer, as shown in Figure 7-3. This is to guarantee a low offset, as discussed previously.
The measured nonlinearity for C_p=50pF amounts to -200ppm. It is difficult to explain why the nonlinearity is not better. In any event, it is not plausible that this is caused by the finite DC gain, since this would result in a positive nonlinearity.

Nonlinearity versus parasitic capacitance

The nonlinearity in the 0-2pF range has also been measured as a function of the parasitic capacitance C_p. This is shown in Figure 7-7. The nonlinearity starts to increase for C_p>200pF. This value is below the calculated value (430pF; see Chapter 6). This is partly caused by extra capacitances which have not been accounted for. These extra capacitances are, for instance, the capacitances of switches (from source/drain to bulk), from bonding pads and from the package.

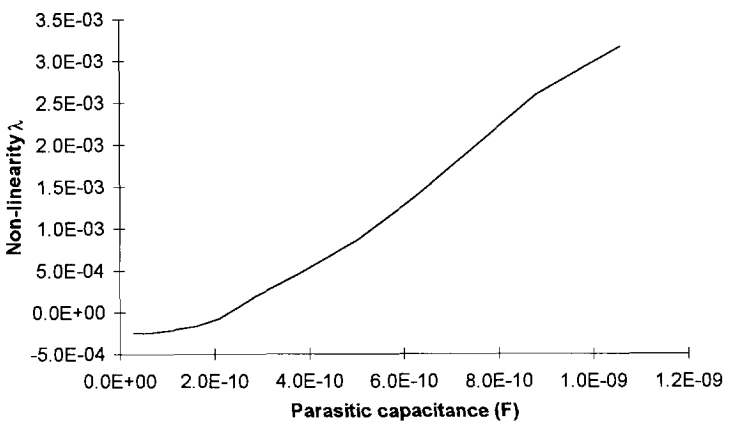


Figure 7-7. Nonlinearity λ versus the parasitic capacitance C_p. Two Teflon capacitors of 1pF have been used. The measurement range equals 0-2pF.

7.2.3 Measurement of platinum resistors

The connection of the platinum (R_{pt}) and reference (R_{ref}) resistor to the interface and its input stage are shown in Figure 7-8. The voltages V_x (V_{CD}) and V_{ref} (V_{AB}) are sampled on C_s. The charge on C_s is converter into a period. A resistor R determines the current through the chain, since normal values for V_x and V_{ref} are much smaller than V_{DD}. The interface is able to measure platinum resistors in several ranges by changing the value of R. The voltages V_{ref} and V_x are measured using the four-wire technique, which eliminates the effect of lead resistances.

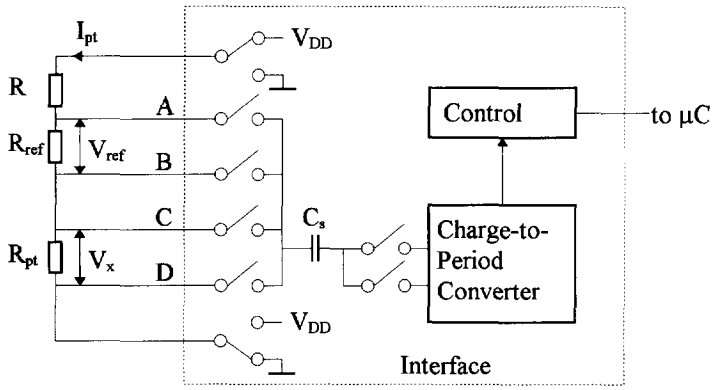


Figure 7-8. Connection of a platinum resistor and a reference resistor to the interface and its input stage.

The nonlinearity was measured using a special interface mode. The interface performs automatically four instead of three measurement phases. In addition to an offset measurement, the interface measures V_{AB}, V_{BD} and the sum $V_{AD}=V_{AB}+V_{BD}$. The duration of the measurement phases are given by:

$$\begin{aligned} T_{off} &= T_0 \\ T_{x1} &= T_0 + K_{mod,R}V_{AB} \\ T_{x2} &= T_0 + K_{mod,R}V_{BD} \\ T_{x1+x2} &= T_0 + K_{mod,R}V_{AD} \end{aligned} \qquad (7\text{-}4)$$

where T_0 and $K_{mod,R}$ are constants of the modulator. The measured values for these four time intervals have been substituted in (7-1) in order to obtain the nonlinearity.
The offset has been measured by applying $R_{ref}=R_x=0$. Ideally, the measurement phases related to R_{ref} and R_x should be equal to the duration of the offset measurement phase.
Table 7-2 shows the measurement results for platinum resistors (N=256).

Item	Measured value	Condition
Resolution	7µV (9mK)	N=256, R_{ref}=100Ω, R=2.2kΩ, Pt100 ($\hat{I}_{pt}$=2mA)
Nonlinearity	50 ppm	$R_x=R_{ref}$=100Ω, R=2.2kΩ ($\hat{I}_{pt}$=2mA)
Offset	50µV (64mK)	$R_{ref}=R_{pt}$=0, R=2.2kΩ

Table 7-2. Measured results for platinum resistors.

The measured resolution amounts to 7µV, which corresponds to 9mK for a Pt100 biased at 2mA. This result is in very good agreement with the theoretical 4.7µV resolution. The contribution to the theoretical resolution are 3.1µV from the amplifier in the integrator (u_{ni}), 3.1µV from the buffer amplifier ($u_{n,buf}$) and 1.7µV from the quantization noise. This calculated resolution is based only on white noise. Since all analog parts which are used during the measurement of platinum resistors are also used during the measurement of capacitors, we conclude that the 1/f noise plays no role. The 3.5dB difference between the calculated and the measured resolution is very small and could be caused by an increased noise level or higher bandwidths than expected.

Clipping
When the peak-to-peak amplitudes of V_x and/or V_{ref} are beyond a certain level (0.5V), the output voltage of the integrator V_{int} will clip to the power supply. The nonlinearity is below 1000 ppm for peak-to-peak amplitudes of 2.5V.

7.2.4 Measurement of resistive bridges

The connection of a resistive bridge to the interface and the input stage of the interface are shown in Figure 7-9. Dynamic range problems caused by the large difference in amplitude between V_x and V_{ref} have been solved by division of V_{ref} and/or amplification of V_x. The division ratio and gain are very accurate and this has been achieved by applying Dynamic Element Matching. The voltages V_{ref} and V_x were measured using the four-wire technique, which eliminates the effect of lead resistances completely.

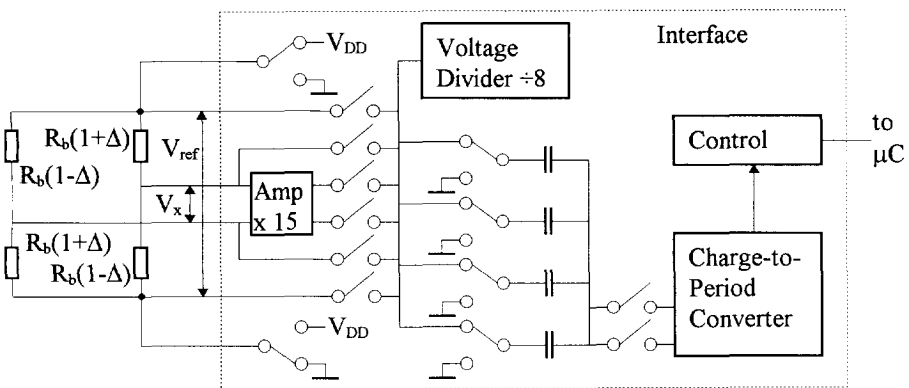


Figure 7-9. Connection of a resistive bridge to the interface and its input stage.

The interface measures the bridge imbalance $\Delta=V_x/V_{ref}$. The selectable ranges for this imbalance are $\Delta_{max}=2.5\cdot10^{-3}$ (The voltage V_x is amplified) and $\Delta_{max}=0.04$ (V_x is not amplified). Measurement results have been obtained using bridge resistors $R_b=2k\Omega$. A bridge with an accurately known imbalance is applied for each measurement range. Thus, the accuracy of the divider and the amplifier can be verified. The bridge has an imbalance such that the reference and the signal measurement phases are equal. Any nonlinearity of the charge-to-period converter and offset has no effect on the determination of the accuracy of the divider and the amplifier.
The offset is measured by short-circuiting the input terminals. The period during a signal measurement should then be equal to the period during an offset measurement phase.
The measurement results are listed in Table 7-3.

Item	Measured value	Condition
Resolution	7µV	N=256, $\Delta_{max}=0.04$
Resolution	700nV	N=256, $\Delta_{max}=2.5\cdot10^{-3}$
Accuracy DEM divider	$5\cdot10^{-4}$	
Accuracy DEM amplifier	10^{-3}	
Offset	3µV	$\Delta_{max}=0.04$
Offset	50µV	$\Delta_{max}=2.5\cdot10^{-3}$

Table 7-3. Measured results for resistive bridges.

The resolution for Δ_{max}=0.04 equals the resolution for platinum resistors, since almost the same input stage is used. During the measurement for $\Delta_{max}=2.5\cdot10^{-3}$, a differential voltage amplifier based on 16 resistors and two amplifiers is used. The noise voltages are sampled 4 times per period. In appendix B, it is shown that when the white spectral density equals $S_{u_{amp}}$ and the closed loop bandwidth equals B_{amp}, the equivalent input noise voltage (in series with V_x) is given by Δv_{amp}

$$\Delta v_{amp}^2 = \frac{2S_{u_{amp}}B_{amp}}{4N} \tag{7-5}$$

with $\sqrt{S_{u_{n,amp}}}$=25nV/√Hz and B_{amp}=500kHz and N=256, the contribution to the resolution due to these noise voltages amounts to 780nV. The measured resolution is even better than the calculated value and this is related to the limited bandwidth of the integrator.

The measured accuracy of the divider and amplifier is good enough to be used in a lot of applications based on commercially available bridge sensors.

The difference in equivalent input offset between a measurement with and without the DEM amplifier is approximately 15 times. The conclusion is that the equivalent input offset is not related to an offset voltage of the DEM amplifier itself. A practical value for the offset voltage of the DEM amplifier is 1mV. The measured equivalent input offset voltage equals 3μV, so the applied chopping technique results at least in a 50 dB suppression of the offset.

7.2.5 Measurement of thermistors

The connection of thermistors to the interface and the input stage of the interface are shown in Figure 7-10. An alternating voltage with an amplitude of $0.08V_{DD}$ drives the series connection of the reference resistor R_{ref} and thermistor R_{th}. The voltages V_x and V_{ref} are sampled and converted into a charge. The charge is converted into a period. Both voltages V_{ref} and V_x are measured using the four-wire technique, which eliminates the effect of lead resistances.

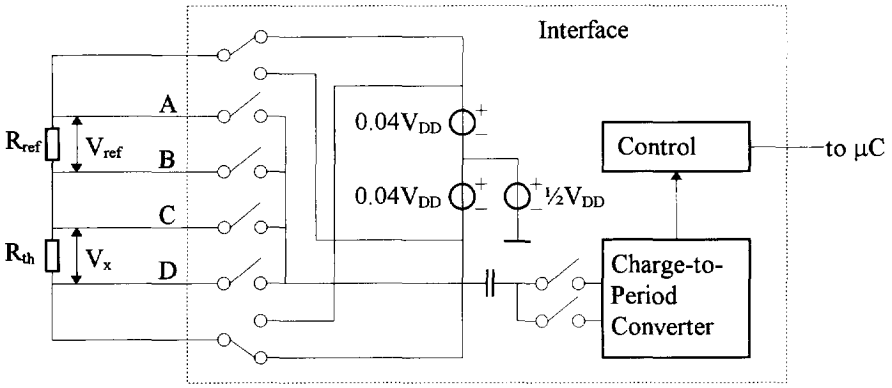


Figure 7-10. Connection of a thermistor and a reference resistor to the interface and its input stage.

The measurement results were obtained using R_{ref}=1kΩ and R_{th}=1kΩ at 25°C.

The nonlinearity has been measured in the same way as the nonlinearity of platinum resistors is measured. In addition to the measurement of the offset, the voltages V_{AB}, V_{BD} and the sum $V_{AD}=V_{AB}+V_{BD}$ were measured. The duration of the measurement phases is given by (7-4). Equation (7-1) is used to obtain the nonlinearity.

Item	Measured value	Condition
Resolution	7μV, 0.9mK	N=256, 4%/K
Nonlinearity	100 ppm	$R_{ref}=R_{th}=1k\Omega$
Offset	50μV	$R_{ref}=R_{th}=0$

Table 7-4. Measured results of thermistors.

The difference between the measurement of platinum resistors and that of thermistors is that in the latter case two extra buffer amplifiers are applied to generate the drive voltage $0.08V_{DD}$ for the resistive chain. These buffers are used throughout all measurement phases. Both noise voltages are sampled 4 times per period. The equivalent input noise can be calculated in a way equal to (7-5). The only difference is that due to the three-signal technique, a factor K as described in Chapter 5 should be accounted for. With $\sqrt{S_{u_{amp}}}=25nV\sqrt{Hz}$, $B_{amp}=5MHz$, K=2 and N=256, the equivalent RMS input voltage due to the noise voltage of these buffer amplifiers amounts to 3.5μV. When we account for the limited bandwidth during clock phase φ_2, this value becomes 2.5μV. The dominant noise sources are the noise voltage of the amplifier in the integrator and the quantization noise.

7.3 Low-frequency suppression

The suppression of low-frequency interfering signals has been measured for capacitive measurements. The measurement setup is shown in Figure 7-11. The interface is put in a special mode, where it operates only as a modulator. The phase selection, required for the three-signal technique, has been disabled. The interfering signal is modeled by V_{LF}. Both the sensor and the interfering capacitor equal 1pF. The output of the interface is sampled by a counter HP 5335A, having a sampling frequency of 1GHz. The quantization noise becomes negligible. The counter is controlled by a PC. The period of the oscillator without interference equals 140μs (T_1=10μs and T_2=25μs).

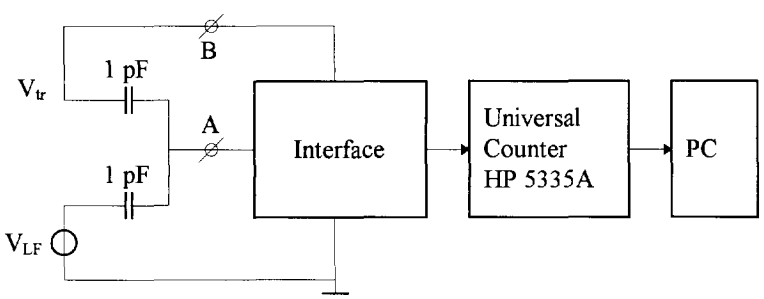


Figure 7-11. Measurement setup for the measurement of the suppression of low-frequency interfering signals V_{LF}. The interface is put in a special mode, operating only as an modulator.

The plots in Chapter 5 show the relative error $S_{C,2,N}(\omega,A)$ in the time domain, relative to the amplitude of the interfering amplitude versus this relative amplitude. This result in flat curves if the suppression is independent of the amplitude of V_{LF}. However, due to electronic noise, $S_{C,2,N}(\omega,A)$ tends to increase when the amplitude of V_{LF} decreases. It is therefore better to calculate just the relative error in the time domain. The relative error will also increase proportional to the amplitude of V_{LF}, also when the suppression is independent of the interference signal. For a very small interfering amplitude, the relative error will be equal to the electronic noise level.
The relative error in the time domain is shown in Figure 7-12. The plots show the simulated (dashed line) and measured (solid line) relative error versus the relative interfering amplitude. This is the ratio of the amplitudes of V_{LF} and V_{tr}. The measured relative error for a 50Hz and a 100Hz interfering signal are little larger than the simulated relative error. The differences between measurements and simulations are between 2 and 5 times. The main reason for this slightly worse behavior is probably the mismatch in the integration current. As we saw in Chapter 5, a current mismatch of 0.1% causes an increase of the relative error of 4 times. Note that the measured relative error for a 200Hz interfering signal is even smaller than the simulated relative error.

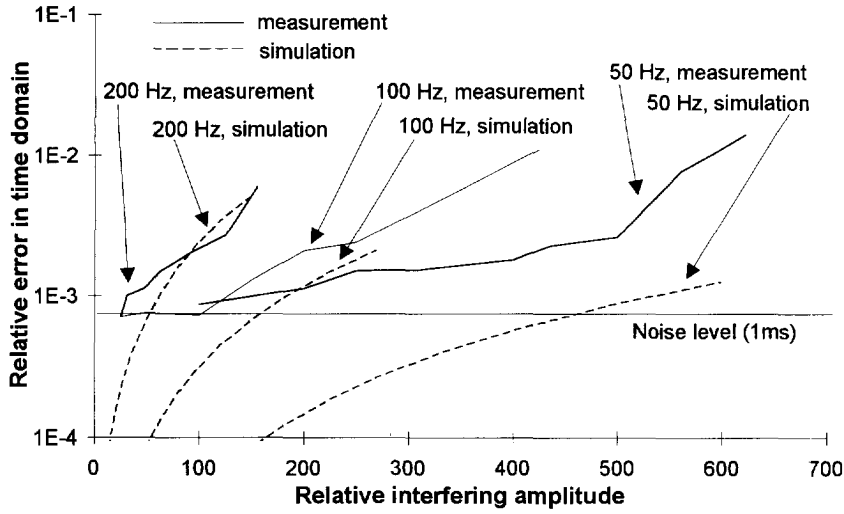


Figure 7-12. Simulated and measured relative error in the time domain for three different frequencies of the low-frequency interfering signal V_{LF}. The measurement time equals 1ms.

7.4 Ratings

The performance of the interface has been tested for different power supply voltages and at different temperatures. We measured the performance by measuring the nonlinearity for capacitive measurement by using the setup shown in Figure 7-3. We applied two 1 pF Teflon capacitors and C_p equals 30pF. The results are listed in Table 7-5.

Effect	Nonlinearity (ppm)
Normal operation (5V, 25°C)	-200
5V, -20°C	-250
5V, +80°C	200
3.3V, 25°C	-250
5.5V, 25°C	-200

Table 7-5. Measured nonlinearity for capacitive measurements under different circumstances.

The operation frequency over the temperature range of 100°C varied by 25%, but still the nonlinearity has hardly changed. This shows that the applied techniques, especially the three-signal technique, perform very good and leads to good results in an easy way.

7.5 Conclusions

This chapter discusses the measurement results for all different applications.
The interface operates on supply voltages in the range 3.3V to 5.5V and consumes less than 2mA. Generally, the resolution in any application for a 100ms measurement time amounts to 15 bits.
The resolution for capacitive measurements amounts to 50aF in the 0-2pF range. This value holds for values of the and parasitic capacitance smaller than 30pF and for a 100ms measurement time. The resolution increases up to 400aF for a parasitic capacitance of 1nF. The nonlinearity for a small parasitic capacitance in the interface temperature range of -40°C to 80°C amounts to 200ppm.
The resistive measurements can be considered as voltage measurements. The resolution amounts to 7μV for a 100ms measurement time. When a Pt100, biased at 2mA, is used, the resolution in temperature amounts to 9mK. The nonlinearity in the interface temperature range -40°C to 80°C amounts to 150ppm.
The inaccuracy of the on-chip DEM voltage divider and on-chip DEM voltage amplifier amount to 500ppm and 1000ppm, respectively. The voltage divider shows an almost temperature-independent inaccuracy and the inaccuracy of the amplifier starts to worsen for temperatures above 60°C.
The suppression of low-frequency interfering signals by a second-order SC filter is effective and is almost equal to the maximum achievable suppression.

8. Conclusions

Main conclusions
It is necessary to apply continuous auto-calibration techniques, synchronous detection, two-port measurement techniques and dynamic element matching in order to realize low-cost, multiple-purpose accurate sensor interfaces.

The best type of Analog-to-Digital conversion to be applied in low-cost smart sensor systems is based on the use of an asynchronous oscillator in combination with a frequency counter.

Chapter 1
Conventional sensor systems are not widely spread. This is mainly caused by the fact that the interface electronics are too expensive, too large, and not very reliable and accurate. A breakthrough in the sensor market will be enabled by low-cost sensor interfaces which are accurate, reliable and easy-to-use. This thesis will deal with the development of interfaces which meet the requirements.

Chapter 2
Combining microcontrollers and sensor interfaces is a good method to achieve low-cost and easy-to-use sensor systems. At the moment, general-purpose interfaces are superior to special-purpose interfaces. This can be attributed to the fact that the sensor market cannot (yet) be considered as a high-volume market. One of our measurement strategies is to move the required functions as much as possible from the interface to the microcontroller in order to obtain simple circuits and accurate systems.

Chapter 3
Application of good measurement techniques must be applied to obtain low-cost multiple-purpose and reliable sensor systems. These techniques are:

- the three-signal technique, which is a continuous auto-calibration technique that enables accurate results to be obtained at low costs, even when low-cost IC processes are used,
- synchronous detection for the suppression of interference signals,
- two-port measurement techniques for the suppression of parasitics of the sensor element connecting wires,
- dynamic element matching to realize, for instance, calibration-free voltage amplifiers.

Chapter 4
The type of Analog-to-Digital conversion which is most suitable for use in low-cost smart sensor systems is based on an asynchronous oscillator (modulator), which is modulated by the sensor signal, in combination with a frequency counter (the microcontroller). This conclusion is based on such aspects as the number of wires between the interface and the microcontroller, the format of the interface output signal, the effort of the microcontroller to calculate the final measurement result, the required conversion time and the effect of low- and high-frequency interference signals. The selection of the three different measurement phases, resulting from the

three-signal technique, is done by the interface itself. The interface output signal is very robust, requires only a small transmission bandwidth and can easily be decoded by the microcontroller.

Chapter 5

The heart of the Analog-to-Digital converter consists of a first-order relaxation modulator, in which the voltage swing across the integration capacitor is modulated. The low-frequency interference signals are suppressed by synchronous detection in combination with a second-order switched-capacitor (SC) filter. This filter also suppresses the effects of low-frequency 1/f noise. Further, high-frequency interference signals have been suppressed by applying dithering techniques. There are no extreme modulator requirements that have to be met in order to obtain a high-linear signal-to-period conversion. Specific problems related to the read-out of sensing elements have been solved by applying sensor-specific signal-processing circuits.

Chapter 6

The interface was designed in a 0.7μm CMOS process. Although many different sensor elements can be connected to the interface, the number of sensor elements connections to the interface is limited to six. The function of every connection pad, therefore, depends of the type of sensor element. The modulator consists of several sensor-specific front-ends and a common part. Several switches, controlled by logic circuits, guarantee that the right voltages will be sampled and that the right charges transfer will be transferred. In order to achieve the maximum available suppression of low-frequency interference signals, the generation of the integration current is based on switched-current (SI) techniques. A watchdog detects whether the oscillation process has stopped for a certain amount of time and (re)starts the oscillator when necessary.

Chapter 7

The interface operates on supply voltages ranging from 3.3V to 5.5V and consuming less than 2mA. Generally, the resolution in any application for a measurement of 100ms time amounts to 15 bits.

The resolution for capacitive measurements amounts to 50aF in the 0-2pF range. This value holds for a parasitic capacitance smaller than 30pF and for a measurement time of 100ms. The resolution increases up to 400aF for a parasitic capacitance of 1nF. In the case of a small parasitic capacitance and an interface temperature range of -40°C to 80°C, the nonlinearity amounts to 200ppm.

The resistive measurements can be considered as voltage measurements. The resolution amounts to 7μV for a measurement time of 100ms. When a Pt100, biased at 2mA, is used, the resolution in temperature will be 9mK. The resolution of the thermistor measurement is better than 1mK. The nonlinearity in the interface temperature range from -40°C to 80°C amounts to 150ppm. The inaccuracy of the on-chip DEM voltage divider and on-chip DEM voltage amplifier amounts to respectively 500ppm and 1000ppm. The voltage divider shows a nearly temperature-independent inaccuracy. The inaccuracy of the amplifier starts to increase for temperatures above 60°C.

The suppression of low-frequency interference signals by a second-order SC filter is effective and is almost equal to the maximum achievable suppression.

The final version of the interface has been made commercially available.

A. Electrical characteristics of sensing elements

This appendix describes the most important electrical characteristics of the sensing elements which can be read out by the Smart Signal Processor (SSP). The following sensing elements will be considered:

- Capacitors
- Platinum resistors
- Thermistors
- Resistive bridges
- Resistive potentiometers

A.1 Capacitors

The model of the capacitor C_x, including the connection cables, is shown in Figure A-1. The parasitic capacitors C_{p1} and C_{p2} model the capacitance of the connection cables.

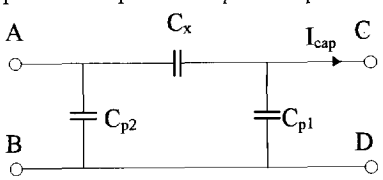


Figure A-1. Model of C_x including the connection cables.

The effect of C_{p1} and C_{p2} can be eliminated by forcing a voltage between node A and B and measuring the current I_{cap} when nodes C and D are short-cutted. This current than only depends on V_{AB} and C_x. This is a two-port measurement.

A.2 Platinum resistors

Platinum resistors are used for temperature measurements. The usefull range amounts to -200°C to 850°C. Commonly used platinum resistors are the PT100 and Pt1000, which have a value of 100Ω and 1kΩ at 0°C respectively. According to the DIN-IEC 751 [1] standard the platinum resistor $R_{pt}(T)$ for $T \in [-200°C, 0°C]$ is given by:

$$R_{pt}(T) = R_{pt}(0)\left(1 + a_1 T - a_2 T^2 + a_3 T^3 - a_4 T^4\right) \qquad \text{(A-1)}$$

where T is the temperature in °C. For the range $T \in [0°C, 850°C]$, $R_{pt}(T)$ is given by:

$$R_{pt}(T) = R_{pt}(0)\left(1 + a_1 T - a_2 T^2\right) \qquad \text{(A-2)}$$

The values for a_1, a_2, a_3 and a_4 are given in Table A-1 and can easily be stored in the microcontroller.

Coefficient	Value	Unit
a_1	$3.90802 \cdot 10^{-3}$	$(°C)^{-1}$
a_2	$0.5802 \cdot 10^{-6}$	$(°C)^{-2}$
a_3	$0.42735 \cdot 10^{-9}$	$(°C)^{-3}$
a_4	$4.2735 \cdot 10^{-12}$	$(°C)^{-4}$

Table A-1. Values of coefficients in the equation for $R_{pt}(T)$.

We consider two sources of errors in the measurement of the temperature. These are:
1. the initial uncertainty
2. the error due to self-heating

Initial uncertainty

The initial uncertainty $\Delta T_{pt,ini}(T)$ for class A platinum resistors is specified by the same standard:

$$\Delta T_{pt,ini}(T) = \pm\left(0.15 + 2 \cdot 10^{-3}|T|\right) \tag{A-3}$$

where T is the temperature in °C. Based on the values of $R_{pt}(T)$ and $\Delta T_{pt,ini}(T)$, we can derive the relative uncertainty $\varepsilon_{pt,ini}(T)$. This is the relative resistor change which is required to obtain the same temperature change as $\Delta T_{pt,ini}(T)$ and is defined by:

$$\varepsilon_{pt,ini}(T) = \Delta T_{pt,ini}(T) \frac{\frac{\partial R_{pt}(T)}{\partial T}}{R_{pt}(T)} \tag{A-4}$$

The curve for $\varepsilon_{pt,ini}(T)$ does not depend on $R_{pt}(0)$ and is shown in Figure A-2.

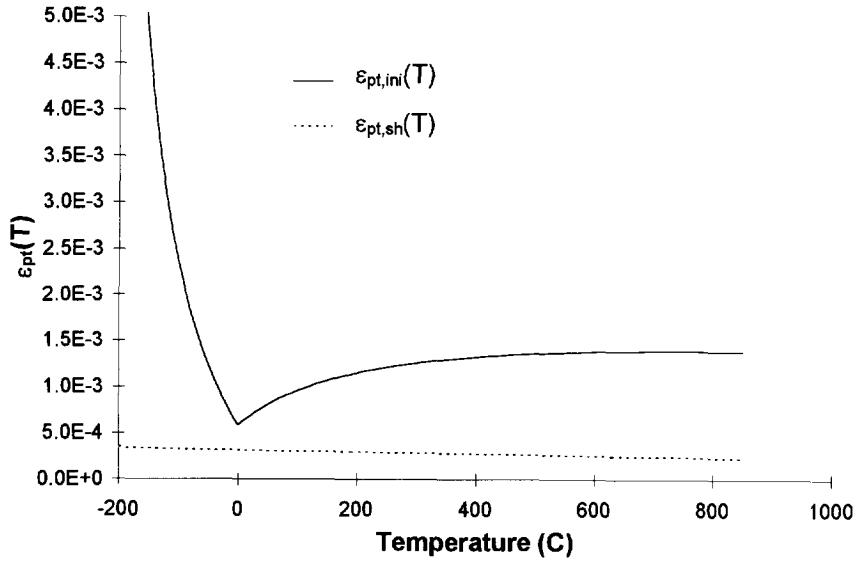


Figure A-2. The relative uncertainty due to the initial uncertainty ($\varepsilon_{pt,ini}(T)$) and due to the self-heating ($\varepsilon_{pt,sh}(T)$) of a Pt100 biased at 2mA.

The smallest value for $\varepsilon_{pt,ini}(T)$ occurs at T=0°C and amounts to $6 \cdot 10^{-4}$.

Self-heating

Due to the thermal resistance $R_{th,pt}$ and a current I_{pt} flowing through the platinum resistor, the temperature of the platinum resistor is increased (self-heating) with $\Delta T_{pt,sh}(T)$:

$$\Delta T_{pt,sh}(T) = I_{pt}^2 R_{pt}(T) R_{th,pt} \tag{A-5}$$

We can also define a relative uncertainty $\varepsilon_{pt,sh}(T)$. This is defined as the relative resistor change which is required to obtain a temperature change $\Delta T_{pt,sh}(T)$ and is given by:

$$\begin{aligned} \varepsilon_{pt,sh}(T) &= \Delta T_{pt,sh}(T) \frac{\frac{\partial R_{pt}(T)}{\partial T}}{R_{pt}(T)} \\ &= I_{pt}^2 R_{th,pt} \frac{\partial R_{pt}(T)}{\partial T} \end{aligned} \tag{A-6}$$

A curve for $\varepsilon_{pt,sh}(T)$ for a Pt100 for I_{pt}=2mA and $R_{th,pt}$=200K/W (still air) is also shown in Figure A-2. The value for $\varepsilon_{pt,sh}(0)$ for these values is $3.1 \cdot 10^{-4}$, which is almost two times smaller than $\varepsilon_{pt,ini}(0)$.

A.3 Thermistors

Thermistors are used to measure temperature in the range -100°C to 200°C. The resistive value $R_{th}(T)$ can be approximated by a simple relation:

$$T = B \ln\left(\frac{R_{th}(T)}{A}\right) \tag{A-7}$$

where T is the temperature in K and A and B two constants. The error of (A-7) in the range 250K to 390K (-20°C to 120°C) has values between -0.8K to 0.9K. A better approximation of T can be obtained with the model of Steinhart and Hart:

$$\frac{1}{T} = a + b\left(\ln\left(\frac{R_{th}(T)}{1\Omega}\right)\right) + c\left(\ln\left(\frac{R_{th}(T)}{1\Omega}\right)\right)^3 \tag{A-8}$$

The temperature error in the same range has values between -7mK and 28mK.

Table A-2 shows the values for $R_{th}(T)$, its absolute tolerance $\Delta T_{th,ini}(T)$ and the corresponding relative initial uncertainty $\varepsilon_{th,ini}(T)$ for three thermistors of YSI [2].

Type	parameter	-80°C	0°C	70°C	150°C	200°C
44004	$\Delta T_{th,ini}(T)$ (°C)	1	0.0	0.2	1	
44004	$\varepsilon_{th,ini}(T)$ (%)	8.6	1	0.7	2.3	
44004	$R_{th}(T)$ (Ω)	$2.9 \cdot 10^6$	$7.51 \cdot 10^3$	407	46.5	
46043	$\Delta T_{th,ini}(T)$ (°C)	1	0.05	0.05	1	1.3
46043	$\varepsilon_{th,ini}(T)$ (%)	8.6	0.26	0.17	2.3	2.4
46043	$R_{th}(T)$ (Ω)	$2.9 \cdot 10^6$	$7.51 \cdot 10^3$	407	46.5	17.5
46046	$\Delta T_{th,ini}(T)$ (°C)	1	0.05	0.05	1	1.3
46046	$\varepsilon_{th,ini}(T)$ (%)	8.6	0.26	0.17	2.3	2.4
46046	$R_{th}(T)$ (Ω)	$12.9 \cdot 10^6$	$33.3 \cdot 10^3$	$1.78 \cdot 10^3$	206	77.7

Table A-2. Important parameters of three thermistors from YSI.

Table A-3 shows the thermal resistance $R_{th,th}$ in K/W for the thermistors in Table A-2 under different conditions. Also shown are the constants A and B in (A-7).

Type	Still air	Oil	A (Ω)	B (K)
44044	1000	125	$4.6 \cdot 10^{-3}$	3891
46043	250	100	$4.6 \cdot 10^{-3}$	3891
46046	250	100	$20.4 \cdot 10^{-3}$	3891

Table A-3. Thermal resistances $R_{th,th}$ in K/W and the constants A and B in (A-7) for the thermistors in Table A-2.

A.4 Resistive bridges

A resistive bridge is a circuit consisting of four resistors as shown in Figure A-3. At least one resistors depends on a physical signal, resulting in a relative change Δ.

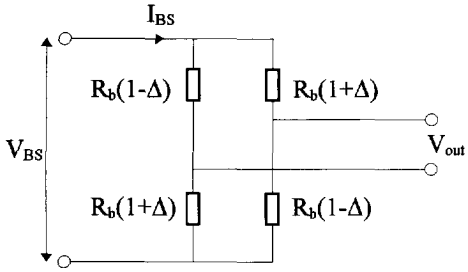


Figure A-3. Model of a resistive bridge.

The physical signal is normally represented by the ratio of the output voltage V_{out} of the bridge and the voltage V_{BS} across the bridge. This ratio is given by:

$$\frac{V_{out}}{V_{BS}} = \Delta \qquad \text{(A-9)}$$

We consider two types of resistive bridges. They are based on different principles:

1. Resisistive bridges based on strain gages. A relative change Δ of R_b is caused by a change of its geometrical dimensions [3].
2. Resistive bridges based on the piezo-resistive effect [4,5].

Strain gages

The bridge imbalance Δ is given by:

$$\Delta = G_{sg}\varepsilon \qquad \text{(A-10)}$$

where G_{sg} is the gage factor and ε the relative strain. G_{sg} depends on the material. Linear bridges can be obtained from constantan bridges (G_{sg}=2.05). A practical maximum relative strain is +/- 2%, resulting in Δ_{max}=+/- 4%. Normal values for R_b lie in the range between 120Ω and 350Ω.

Piezo-resistive bridges

The bridge imbalance from bridges based on the piezo-resistive effect can be described by the product of a gain G_{pr} and the physical signal E_{phys}:

$$\Delta = G_{pr}E_{phys} \qquad \text{(A-11)}$$

When G_{pr} is independent of the temperature (U-bridges), the physical signal E_{phys} should be measured by measuring Δ as in (A-9). In a lot of cases, G_{pr} is cursed with a temperature coefficient α. The result is that Δ is also temperature dependent. This effect can be compensated for. A simple compensation is based on an equal, but opposite temperature coefficient $-\alpha$ for R_b. In this case, the ratio of V_{out} and the bridge current I_{BS} is temperature independent:

$$\begin{aligned} \frac{V_{out}}{I_{BS}} &= R_b(0)(1+\alpha T)G_{pr}(T)(1-\alpha T)E_{phys} \\ &\cong R_b(0)G_{pr}(0)E_{phys} \end{aligned} \qquad \text{(A-12)}$$

The current I_{BS} can easily be measured by inserting a reference resistor in series with the bridge and measuring the voltage across it. The total circuit can then be excited with a voltage. This voltage does not have to be accurately known or constant. We refer to bridges having a temperature independent ratio V_{out}/I_{BS} as I-bridges.

The normal maximum accuracy of piezo-resistive bridges amounts to 0.1%, the sensitivity has values in the range 2.5mV/V to 20mV/V and R_b has values between 400Ω and 5kΩ.

A.5 Resistive potentiometers

The model of a resistive potentiometer is shown in Figure A-4. Common values for R_{pot} lie in the range between 1kΩ and 50kΩ.

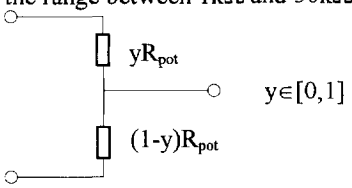


Figure A-4. Model of a resistive potentiometer.

A.6 References

[1] Data Sheet, "Temperaturmessung mit Widerstandsthermometern", Heraeus GmbH, Germany, 1986.
[2] Data Sheet, "Precision thermistors", YSI, Yellow Springs USA, 1989.
[3] Data Sheet, "Catalog 500, part A and B", Micro-Measurement Division, 1988
[4] Data Sheet, "Pressure Sensor Handbook", Sensym, 1989.
[5] Data Sheet, "Product catalog", ICSensors, Milpitas, 1988.

B. Noise of relaxation modulators

B.1 Noise model

The noise calculations are based on the Bennet model [1]. Bennet showed that noise can be described as the infinite sum of discrete sinusoidal components. These components have different frequency, equal amplitude and a random phase, which is uniformly distributed in the interval $[-\pi,\pi]$. The sum of the power of all Bennet components equals the total noise power, which is given by the product of the Power Spectral Density (PSD) and the bandwidth. By using this model, the effect of the noise on the resolution can be calculated in a simple way. We determine the influence of one Bennet component on N modulator periods and calculate the variance due to this component. We then use all Bennet components to find the total variance. To handle 1/f noise, the amplitude of the Bennet components are inversely proportional to the square root of the frequency.

B.2 Noise of the Multiple-Sensor Modulator

This section is on the noise of the Multiple-Sensor Modulator as depicted in Figure B-1. The control block controls all switches and V_{sign}, V_{tr}, V_{o1}, V_{o2}, and I_{int}. Some signal levels and control signals are shown in Figure B-2. The capacitors C_p and C_{pb} model the parasitic capacitance of the cables and the parasitic capacitance of C_s to the substrate respectively.
The following noise sources are considered:

- noise voltage u_{ni} of the amplifier in the integrator
- noise current i_n at the input of the integrator
- noise voltage u_{nc} of the comparator
- noise voltage u_{na} of the amplifier in the C-V converter
- noise voltage u_{ns} of a resistive source
- thermal noise of the ON-resistance of the switches, resulting in kT/C noise.

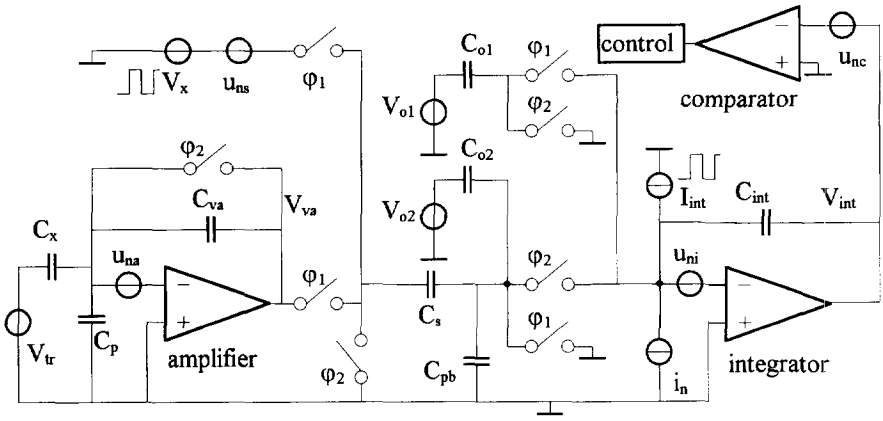


Figure B-1. Noise sources in the Multiple-Sensor Modulator.

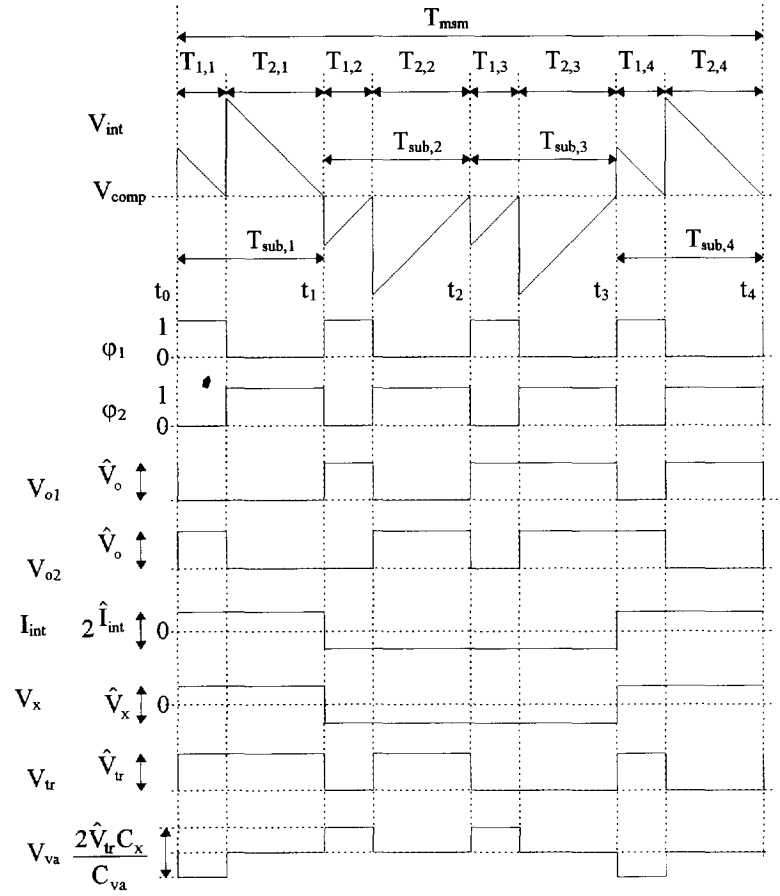


Figure B-2. Some relevant signal levels and control signals for the Multiple-Sensor Modulator.

B.2.1 The noise voltage u_{ni} of the amplifier in the integrator

In this subsection, we calculate the variance due to the noise voltage u_{ni} of the active part of the integrator. According to the Bennet model, the noise source u_{ni} is modeled as the infinite sum of Bennet components. One component is given by:

$$\hat{u}_{ni}\cos(\omega t+\varphi) \tag{B-1}$$

where $\hat{u}_{ni}$ is the amplitude, ω the frequency and φ the uniformly distributed random phase.
The noise voltage can be transferred into an equivalent noise voltage $u_{ni,eq}$ at the input of the integrator, as shown in Figure B-3.

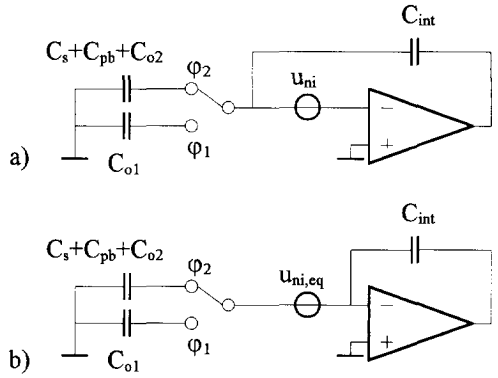


Figure B-3. The noise voltage u_{ni} of the amplifier (a) has been transferred to an equivalent input noise voltage $u_{ni,eq}$ (b).

The equivalent noise voltage $u_{ni,eq}$ depends on the voltage gain of the complete stage. The gain depends on the capacitance between the input and GND. The capacitance equals C_{o1} and $C_s+C_{pb}+C_{o2}$ during phase φ_1 and φ_2 respectively. The equivalent input noise during phases φ_1 and φ_2 is then given by $u_{ni,eq,1}$ and $u_{ni,eq,2}$:

$$\begin{aligned} u_{ni,eq,1} &= u_{ni}\left(1+\frac{C_{\text{int}}}{C_{o1}}\right) \\ u_{ni,eq,2} &= u_{ni}\left(1+\frac{C_{\text{int}}}{C_s+C_{pb}+C_{o2}}\right) \end{aligned} \tag{B-2}$$

The noise voltage $u_{ni,eq,i}$ is sampled at the end of phase φ_1 on C_{o1} and at the end of φ_2 on $C_s+C_{pb}+C_{o2}$. The noise sampling results in jitter of time intervals $T_{1,i}$ and $T_{2,i}$ respectively.
The time intervals $T_{1,i}$ are based on the ideal value T_1 and a jitter. The jitter originates from the noise charge $u_{ni,eq,1}C_{o1}$ which is transferred to the integrator during $T_{1,i}$. The time intervals $T_{1,i}$ are given by:

$$\begin{aligned} T_{1,i} &= T_1 + \frac{C_{o1}}{\hat{I}_{\text{int}}} u_{ni,eq,1}(t_i - T_{2,i}) \\ &= T_1 + \frac{C_{o1} + C_{\text{int}}}{\hat{I}_{\text{int}}} u_{ni}(t_i - T_2) \quad i = 1,4 \\ T_{1,i} &= T_1 - \frac{C_{o1}}{\hat{I}_{\text{int}}} u_{ni,eq,1}(t_i - T_{2,i}) \\ &= T_1 - \frac{C_{o1} + C_{\text{int}}}{\hat{I}_{\text{int}}} u_{ni}(t_i - T_{2,i}) \quad i = 2,3 \end{aligned} \tag{B-3}$$

where $u_{ni,eq,1}(t)$ is the value of $u_{ni,eq,1}$ at time t and t_i-T_2 corresponds to the start of phase φ_1. $\hat{I}_{\text{int}}$ represents the peak-to-peak amplitude of I_{int}. We see that the effect of the noise on $T_{1,1}$ and $T_{1,4}$ is opposite to that on $T_{1,2}$ and $T_{1,3}$. This is due to the alternation of signal voltages and currents. Similar expressions can be found for $T_{2,i}$:

$$\begin{aligned} T_{2,i} &= T_2 + \frac{C_s + C_{pb} + C_{o2}}{\hat{I}_{\text{int}}} u_{ni,eq,2}(t_i) \\ &= T_2 + \frac{C_s + C_{pb} + C_{o2} + C_{\text{int}}}{\hat{I}_{\text{int}}} u_{ni}(t_i) \quad i = 1,4 \\ T_{2,i} &= T_2 - \frac{C_s + C_{pb} + C_{o2}}{\hat{I}_{\text{int}}} u_{ni,eq,2}(t_i) \\ &= T_2 - \frac{C_s + C_{pb} + C_{o2} + C_{\text{int}}}{\hat{I}_{\text{int}}} u\ (t_i) \quad i = 2,3 \end{aligned} \tag{B-4}$$

With aid of (B-2) to (B-4), the expression for a noisy period T'_{msm} is given by:

$$\begin{aligned} T'_{msm} &= \sum_{i=1}^{4} T_{1,i} + T_{2,i} \\ &= 4T_{sub} + \frac{C_{o1} + C_{\text{int}}}{\hat{I}_{\text{int}}} \left[u_{ni}(t_1 - T_2) - u_{ni}(t_2 - T_2) - u_{ni}(t_3 - T_2) + u_{ni}(t_4 - T_2) \right] \\ &\quad + \frac{C_s + C_{pb} + C_{o2} + C_{\text{int}}}{\hat{I}_{\text{int}}} \left[u_{ni}(t_1) - u_{ni}(t_2) - u_{ni}(t_3) + u_{ni}(t_4) \right] \\ &\cong 4T_{sub} + \frac{C_{total}}{\hat{I}_{\text{int}}} \left[u_{ni}(t_1) - u_{ni}(t_2) - u_{ni}(t_3) + u_{ni}(t_4) \right] \end{aligned} \tag{B-5}$$

where $C_{total}=C_s+C_{pb}+C_{int}+C_{o1}+C_{o2}$. Substitution of (B-1) in (B-5) results in:

$$T'_{msm} = 4T_{sub} + \frac{\hat{u}_{ni} C_{total}}{\hat{I}_{\text{int}}} \left[\cos(\omega t_1 + \varphi) - \cos(\omega t_2 + \varphi) - \cos(\omega t_3 + \varphi) + \cos(\omega t_4 + \varphi) \right] \tag{B-6}$$

This expression cannot be handled analytically, unless we make an assumption. We assume that the amplitude $\hat{u}_{ni}$ is very small so we approximate t_{i+1}-t_i by T_{sub}, which is the ideal value of $T_{sub,i}$. When we extend the time to N modulator periods, we obtain the following expression for NT'_{msm}:

$$NT'_{msm} = 4NT_{sub} + \frac{\hat{u}_{ni}C_{total}}{\hat{I}_{\text{int}}} \sum_{k=0}^{N-1}\Big[\cos(4k\omega T_{sub}+\varphi) - \cos((4k+1)\omega T_{sub}+\varphi) - \cos((4k+2)\omega T_{sub}+\varphi) + \cos((4k+3)\omega T_{sub}+\varphi)\Big] \tag{B-7}$$

The variance $\rho_{ni}^2(\omega)$ of NT'_{msm} due to one Bennet component is defined by:

$$\rho_{ni}^2(\omega) = \frac{1}{2\pi}\int_{-\pi}^{\pi}\left(NT'_{msm} - \overline{NT'_{msm}}\right)^2 d\varphi = \left(\frac{\hat{u}_{ni}C_{total}}{\hat{I}_{\text{int}}}\right)^2 H_u(\omega) \tag{B-8}$$

where the function $H_u(\omega)$ is defined by:

$$H_u(\omega) = \frac{1}{2\pi}\int_{-\pi}^{\pi}\left[\sum_{k=0}^{N-1}\Big[\cos\big(4kT_{sub}\omega+\varphi\big) - \cos\big((4k+1)T_{sub}\omega+\varphi\big) - \cos\big((4k+2)T_{sub}\omega+\varphi\big) + \cos\big((4k+3)T_{sub}\omega+\varphi\big)\Big]\right]^2 d\varphi \tag{B-9}$$

Figure B-4 shows a plot of $H_u(\omega)$ for ω in the interval $[0,2\pi/T_{sub}]$ for N=2 and N=4.
As can be seen, the low frequency (LF) values of $H_u(\omega)$ are very small, representing a very small sensitivity to noise in this range (1/f noise).

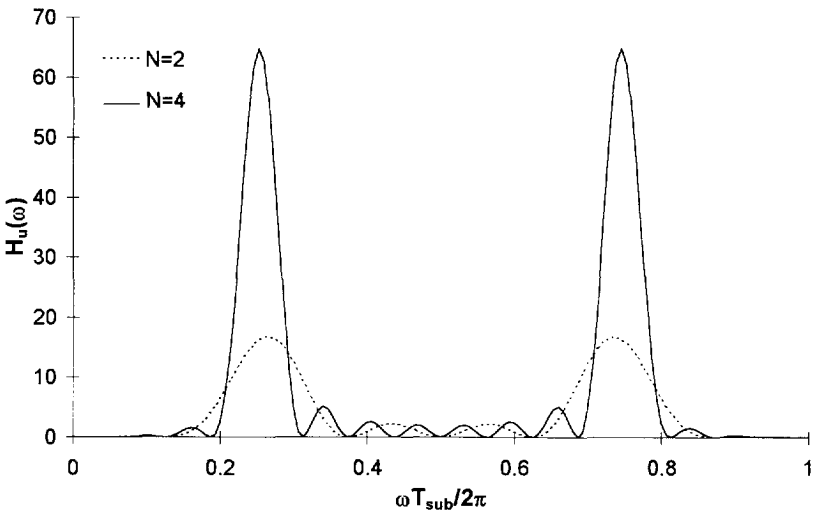


Figure B-4. Sensitivity function $H_u(\omega)$ for noise voltages u_{ni} of the amplifier in the integrator for N=2 and 4.

The total variance σ_{ni}^2 of NT'_{msm} for all Bennet components can be calculated by summation of all $\rho_{ni}^2(\omega)$. We therefore need the relation between the amplitude and the PSD $S_{u_{ni}}(f)$ of u_{ni}.
The power of one component equals the power in a frequency band $\Delta f=\Delta\omega/2\pi$:

$$\tfrac{1}{2}\hat{u}_{ni}^2 = \frac{\Delta\omega}{2\pi} S_{u_{ni}}(f) \tag{B-10}$$

The variance σ_{ni}^2 is given by summation over the relevant bandwidth:

$$\sigma_{ni}^2 = \sum_{\omega} \rho_{ni}^2(\omega)\Delta\omega \tag{B-11}$$

This summation becomes an integration when $\Delta\omega\downarrow 0$. The relevant bandwidth is the closed loop bandwidth B_{int} in Hz of the integrator. With the aid of (B-8) to (B-11), the variance σ_{ni}^2 is given by:

$$\sigma_{ni}^2 = \left(\frac{C_{total}}{\hat{I}_{int}}\right)^2 \frac{1}{\pi} \int_0^{2\pi B_{int}} S_{u_{ni}}(f) H_u(\omega) d\omega \tag{B-12}$$

The noise source u_{ni} consists of white noise and 1/f noise with corner frequency $f_{c,ni}$. The PSD of this source is given by:

$$S_{u_{ni}}(f) = S_{u_{ni}}\left(1 + \frac{f_{c,ni}}{f}\right) \tag{B-13}$$

where $\omega = 2\pi f$. Substitution of (B-13) into (B-12) results in:

$$\sigma_{ni}^2 = \left(\frac{C_{total}}{\hat{I}_{int}}\right)^2 4NB_{int} S_{u_{ni}}\left(1 + \frac{4f_{c,ni}}{B_{int}}\right) \tag{B-14}$$

This expression shows the low sensitivity for 1/f noise. The contribution of the 1/f part to the variance can not be calculated analytically and is approximated with the help of a mathematical program. The relative jitter ε_{ni} of N modulator periods NT_{msm} is defined by the ratio of the square root of the variance and the nominal time of N periods:

$$\begin{aligned} \varepsilon_{ni}^2 &= \frac{\sigma_{ni}^2}{(NT_{msm})^2} \\ &= \left(\frac{C_{total}}{\hat{V}_o(C_{o1} + C_{o2}) + \hat{V}_x C_s}\right)^2 \frac{B_{int} S_{u_{ni}}}{4N}\left(1 + \frac{4f_{c,ni}}{B_{int}}\right) \end{aligned} \tag{B-15}$$

Example: With N=256, C_s=30pF, C_{pb}=10pF, C_{int}=10pF, $C_{o1}=C_{o2}$=1pF, B_{int}=500kHz, $S_{u_{ni}}$=6·10^{-16} V^2/Hz (25 nV/√Hz), $f_{c,ni}$=0 (we neglect the 1/f noise), $\hat{V}_o$=5V and $\hat{V}_x$=0.2V the relative jitter amounts to 1.7 ppm.

Simple calculation

The variance as calculated in (B-14) can be calculated in a very simple way when $S_{u_{ni}}(f)$ only consists of white noise. We just use the fact that for every T_{sub} the equivalent input noise $u_{ni,eq}$ is sampled on C_{total}, as expressed by (B-5). This sampling results in a noise charge q_{ni}. We assume that the samples of the noise have no correlation. The noise power of u_{ni} is given by the product of the bandwidth B_{int} and the flat spectral density. The variance of q_{ni} for one sample is simply q_{ni}^2:

$$q_{ni}^2 = B_{int} S_{u_{ni}} C_{total}^2 \tag{B-16}$$

This variance in the charge domain can be converted into a variance in the time domain by dividing by $\hat{I}_{int}^2$. When P samples are performed, the time variance is given by σ'^2_{ni}

$$\sigma'^2_{ni} = \left(\frac{C_{total}}{\hat{I}_{int}}\right)^2 PB_{int}S_{u_{ni}} \tag{B-17}$$

This is exactly the same as (B-14) for P=4N and $f_{c,ni}$=0. This shows that the Multiple-Sensor Modulator does not remove noise, but is only insensitive to noise in certain frequency areas. For white noise, this local insensitivity does not lead to a better resolution. However, the insensitivity to LF (1/f) noise is a great advantage.

B.2.2 The noise current i_n

We again use the Bennet model to calculate the effect of the noise current i_n. One Bennet component is given by:

$$i_n = \hat{i}\sin(\omega t + \varphi) \tag{B-18}$$

The noise current causes a slight change of the integration current. The charge balance for one modulator period equals:

$$\begin{aligned} 4Q_{tot} &= \int_{t_0}^{t_1}\left(\hat{I}_{int} + i_n\right)dt + \int_{t_1}^{t_3}\left(\hat{I}_{int} - i_n\right)dt + \int_{t_3}^{t_4}\left(\hat{I}_{int} + i_n\right)dt \\ &= \hat{I}_{int}T'_{msm} + \int_{t_0}^{t_1} i_n dt - \int_{t_1}^{t_3} i_n dt + \int_{t_3}^{t_4} i_n dt \end{aligned} \tag{B-19}$$

where Q_{tot} is the total charge which is dumped into the integrator during one time interval $T_{sub,i}$:

$$Q_{tot} = \hat{V}_x C_s + \hat{V}_o\left(C_{o1} + C_{o2}\right) \tag{B-20}$$

We assume that the noise current does not change the modulator period very much, so we assume that all subperiods have the ideal duration T_{sub}. The charge balance for N modulator periods is given by

$$4NQ_{tot} = N\hat{I}_{int}T'_{msm} + \sum_{k=0}^{N-1}\left(\int_{t_0+4kT_{sub}}^{t_0+(4k+1)T_{sub}} i_n dt - \int_{t_0+(4k+1)T_{sub}}^{t_0+(4k+3)T_{sub}} i_n dt + \int_{t_0+(4k+3)T_{sub}}^{t_0+(4k+4)T_{sub}} i_n dt\right) \tag{B-21}$$

We now substitute i_n by its Bennet component, as given by (B-18), and calculate the integrals. The arbitrary start time t_0 is omitted for the sake of simplicity but is accounted for by the random phase φ. The result is:

$$\begin{aligned} 4NQ_{tot} = {} & N\hat{I}_{int}T'_{msm} + \frac{\hat{i}}{\omega}\sum_{k=0}^{N-1}\Big[\cos\left(4k\omega T_{sub} + \varphi\right) - 2\cos\left((4k+1)\omega T_{sub} + \varphi\right) \\ & + 2\cos\left((4k+3)\omega T_{sub} + \varphi\right) - \cos\left((4k+4)\omega T_{sub} + \varphi\right)\Big] \end{aligned} \tag{B-22}$$

The summation in (B-22) can be simplified, resulting in

$$4NQ_{tot} = N\hat{I}_{\text{int}}T'_{msm} + \frac{\hat{i}}{\omega}\left[\cos(\varphi) - \cos(4N\omega T_{sub} + \varphi)\right] - 2\frac{\hat{i}}{\omega}\sum_{k=0}^{N-1}\left[\cos((4k+1)\omega T_{sub} + \varphi) - \cos((4k+3)\omega T_{sub} + \varphi)\right] \quad \text{(B-23)}$$

The variance $\rho_i^2(\omega)$ due to just one Bennet component can be found by:

$$\rho_i^2(\omega) = \frac{1}{2\pi}\int_{-\pi}^{\pi}\left(NT'_{msm} - \overline{NT'_{msm}}\right)^2 d\varphi = \left(\frac{\hat{i}}{\omega\hat{I}_{\text{int}}}\right)^2 H_i(\omega) \quad \text{(B-24)}$$

where $H_i(\omega)$ is given by

$$H_i(\omega) = \frac{1}{2\pi}\int_{-\pi}^{\pi}\left\{\cos(\varphi) - \cos(4N\omega T_{sub} + \varphi) - 2\sum_{k=0}^{N-1}\left[\cos((4k+1)T_{sub}\omega + \phi) - \cos((4k+3)T_{sub}\omega + \phi)\right]\right\}^2 d\varphi \quad \text{(B-25)}$$

This expression can be simplified into:

$$H_i(\omega) = \left(\frac{\cos(\omega T_{sub}) - 1}{\cos(\omega T_{sub})}\right)^2\left(1 - \cos(4N\omega T_{sub})\right) \quad \text{(B-26)}$$

The modules of $H_i(\omega)$ is shown in Figure B-5 for N=2 and N=4.

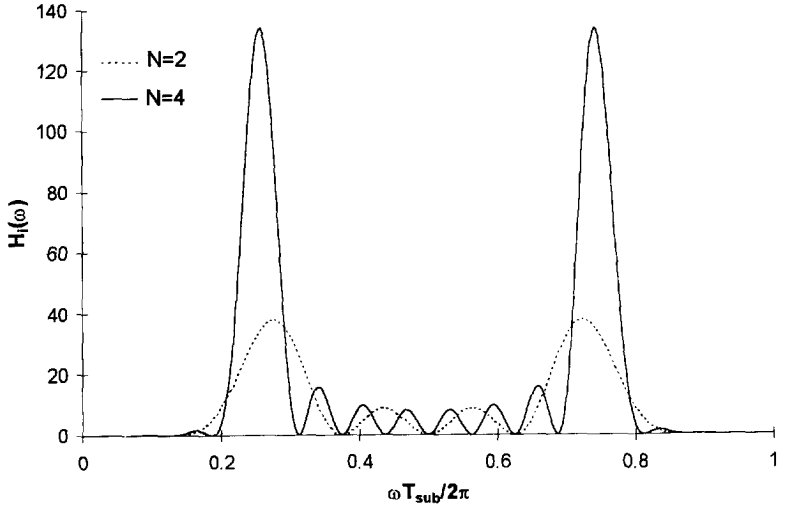


Figure B-5. Transfer function $H_i(\omega)$ for noise currents for N=2 and 4.

The variance in (B-24) is based on the ratio of $H_i(\omega)$ and ω^2. This ratio is shown in Figure B-6, showing that $\rho_i^2(\omega)$ will not explode for small ω.

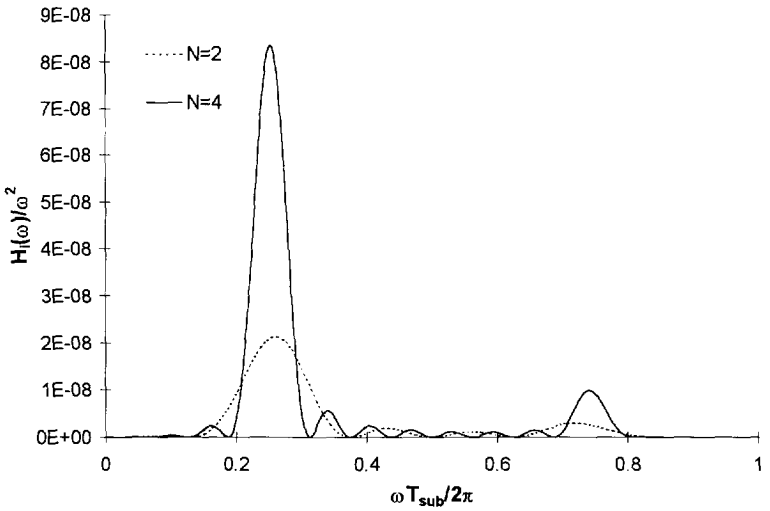


Figure B-6. Ratio of the transfer function $H_i(\omega)$ and ω^2 for N=2 and 4.

We directly see that the modulator is insensitive to low-frequency noise in i_n.
The total variance σ_i^2 follows by summation of all $\rho_i^2(\omega)$. We therefore need the relation between the amplitude of the Bennet component and the spectral density. The power of one Bennet component equals the power in a frequency range $\Delta f=\Delta\omega/2\pi$:

$$\frac{1}{2}\hat{i}^2 = \frac{\Delta\omega}{2\pi} S_{i_n}(f) \tag{B-27}$$

The variance σ_i^2 is given by summation over the relevant bandwidth:

$$\sigma_i^2 = \sum_{\omega} \rho_i^2(\omega)\,\Delta\omega \tag{B-28}$$

The summation becomes an integration when $\Delta\omega\downarrow 0$ and the relevant bandwidth is the closed loop bandwidth B_{int} (in Hz) of the integrator:

$$\sigma_i^2 = \frac{1}{\pi \hat{I}_{\text{int}}^2} \int_0^{2\pi B_{\text{int}}} S_{i_n}(f) \frac{H_i(\omega)}{\omega^2} d\omega \tag{B-29}$$

To here, we have not made any distinction between white and colored noise. The spectral density consists of white and 1/f noise:

$$S_{i_n}(f) = S_{i_n}\left[1 + \frac{f_{c,i}}{f}\right] \tag{B-30}$$

Substitution of (B-30) into (B-29) results in:

$$\sigma_i^2 = \frac{2NT_{sub}S_{i_n}}{\hat{I}_{\text{int}}^2}\left(1 + \pi f_{c,i} T_{sub}\right) \tag{B-31}$$

The relative jitter ε_i for N modulator periods is given by

$$\varepsilon_i^2 = \frac{\sigma_i^2}{\left(4NT_{sub}\right)^2} = \frac{S_{i_n}}{8N\hat{I}_{\text{int}}^2 T_{sub}}\left(1+\pi f_{c,i}T_{sub}\right) \tag{B-32}$$

Example: With $S_{i_n}=10^{-25}$ A^2/Hz (This corresponds to the noise current 4kT/R of a resistor R for R=160kΩ and T=300K) N=256, T_{sub}=30μs, $f_{c,i}$=0 and $\hat{I}_{\text{int}}$=500nA, the relative jitter amounts to ε_i=2.5ppm.
As could be expected, the jitter decreases when the number of periods N is increased. This results in a longer measurement time.

1/f flicker noise of the period
Due to the chopping of all relevant signals, the 1/f behavior of any source shown in Figure B-1 does not result in 1/f behavior of the period (flicker noise). A problem arises when the integration current I_{int} is implemented by two chopped DC current sources, as shown in Figure B-7. This setup is required in order to obtain equal source and sink currents and it results in an optimal low-frequency suppression.

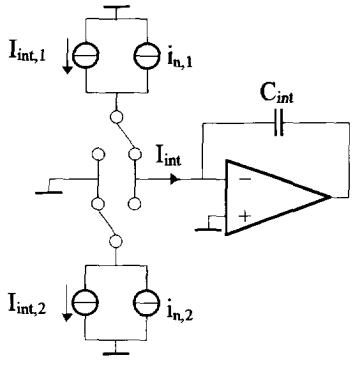


Figure B-7. Implementation of I_{int} by two DC current sources.

Normally, the noise currents $i_{n,1}$ and $i_{n,2}$ are not correlated. The equations for the jitter derived above are no longer valid. When the noise sources are not correlated and have a 1/f spectral density, the period of the modulator also has a 1/f component. This is referred to as flicker. Barnes et. al. [2] showed that the variance of a flicker process is infinite. The resolution is then also infinite. The variance is, therefore, in this case not a good measure of the noise properties. The Allan variance also comes up with an infinite resolution and is, therefore, also not suitable to calculate the resolution.
However, it is possible to calculate the resolution by taking into account the three-signal technique and use the noise correlation between the measurement phases. Variations which are slow in relation to the measurement time of one full measurement cycle will have no effect on the measurement result. This behavior corresponds with a high-pass characteristic for very low frequencies. The calculation of M, which is the result of the three-signal technique, is given by:

$$M = \frac{T_x - T_{off}}{T_{ref} - T_{off}} \tag{B-33}$$

where T_x, T_{ref} and T_{off} are the durations of the measurement phases.
The resolution can be calculated by using the variance of M. The variance of M due to one Bennet component in $i_{n,1}$ or $i_{n,2}$ (consisting of white and 1/f noise) with a frequency ω has been plotted in Figure B-8 for different values of the 1/f noise corner frequency $f_{c,i}$. The variance of M is calculated in a way similar to that shown in Figure B-4 but now the three-signal technique has been included. The corner frequency is related to T_{cycle}, which is the sum of T_x, T_{ref} and T_{off}. The plots in the figure have been calculated for T_{off}:T_x:T_{ref}=1:2:3 and with an arbitrary white noise level. The total variance of M can be calculated by integration of the plots in Figure B-8 over the full frequency range.

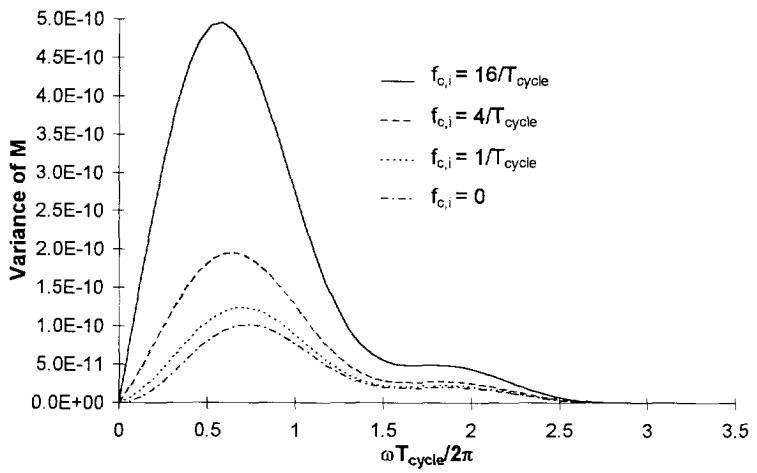


Figure B-8. Variance of M (after the three-signal technique) due to one Bennet component with frequency ω for different values of the 1/f noise corner frequency $f_{c,i}$. The time T_{cycle} equals the sum of T_x, T_{ref} and T_{off}.

It can be seen that for $f_{c,i}/T_{cycle}$=1, the variance of M is barely increased. As shown in Chapter 6, the circuit in Figure B-7 has been applied to generate I_{int} and the corner frequency is designed to be lower than T_{cycle}^{-1}. The application of switched-current (SI) techniques required only one stable current.

B.2.3 The comparator noise voltage u_{nc}

One method to calculate the effect of the comparator noise voltage u_{nc} is to transfer this noise into a noise current at the input of the integrator. The spectrum of the current can then be substituted into (B-29) to calculate the variance. The equivalent noise current at the input of the integrator depends on the frequency response of the integrator. For noise frequencies far beyond the bandwidth of the integrator, the equivalent input noise tends to infinite. It is, therefore, more practical not to transfer the noise voltage.
We consider Figure B-9, showing the integrator and the comparator and the output voltage of the integrator of part of the period.

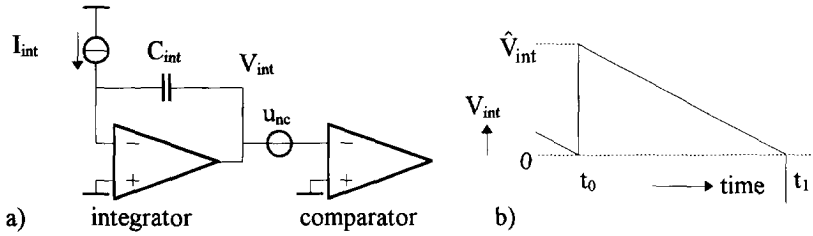


Figure B-9. Part of the Multiple-Sensor Modulator (a) to calculate the jitter due to the noise voltage u_{nc} of the comparator. The diagram in b) shows the output voltage of the integrator for a part of the period.

The absolute value of the slope of V_{int} is $\hat{I}_{int}/C_{int}$ and the amplitude of V_{int} equals $\hat{V}_{int}$. The time interval t_1-t_0 is given by:

$$\hat{V}_{\text{int}} + u_{nc}(t_0) - \frac{\hat{I}_{\text{int}}}{C_{\text{int}}}\left(t_1 - t_0\right) = u_{nc}(t_1) \tag{B-34}$$

where $u_{nc}(t_i)$ is the actual value of u_{nc} at time $t=t_i$. Also relations for other time intervals t_2-t_1, t_3-t_2 and t_4-t_3 can be derived with the aid of Figure B-2. Combining these four time intervals leads to an expression of one noisy period T'_{msm}:

$$t_4 - t_0 = T'_{msm} = \frac{C_{\text{int}}}{\hat{I}_{\text{int}}}\left(4\hat{V}_{\text{int}} + u_{nc}(t_0) - 2u_{nc}(t_1) + 2u_{nc}(t_3) - u_{nc}(t_4)\right) \tag{B-35}$$

Extending (B-35) to N oscillator periods and approximating the time intervals $T_{sub,i}$ by their ideal value T_{sub} result in:

$$\begin{aligned} NT'_{msm} &= \frac{4N\hat{V}_{\text{int}}C_{\text{int}}}{\hat{I}_{\text{int}}} + \frac{C_{\text{int}}}{\hat{I}_{\text{int}}}\left(u_{nc}(t_0) - u_{nc}(t_0 + 4NT_{sub})\right) \\ &- 2\frac{C_{\text{int}}}{\hat{I}_{\text{int}}}\sum_{k=0}^{N-1}\left(u_{nc}(t_0 + (4k+1)T_{sub}) - u_{nc}(t_0 + (4k+1)T_{sub})\right) \end{aligned} \tag{B-36}$$

We next substitute the Bennet components $\hat{u}_{nc}\cos(\omega t+\varphi)$ into (B-36). Also t_0 is accounted for by the phase φ. The result is:

$$\begin{aligned} NT'_{msm} &= \frac{4NV_{\text{int}}C_{\text{int}}}{\hat{I}_{\text{int}}} + \frac{\hat{u}_{nc}C_{\text{int}}}{\hat{I}_{\text{int}}}\left(\cos(\varphi) - \cos(4N\omega T_{sub} + \varphi)\right) \\ &- 2\frac{\hat{u}_{nc}C_{\text{int}}}{\hat{I}_{\text{int}}}\sum_{k=0}^{N-1}\left(\cos(\omega(4k+1)T_{sub} + \varphi) - \cos(\omega(4k+3)T_{sub} + \varphi)\right) \end{aligned} \tag{B-37}$$

This is the same type of expression as (B-23). The variance $\rho_{nc}^2(\omega)$ due to one Bennet component of u_{nc} can be found according to (B-24) and is given by:

$$\rho_{nc}^2(\omega) = \left(\frac{\hat{u}_{nc}C_{\text{int}}}{\hat{I}_{\text{int}}}\right)^2 H_i(\omega) \tag{B-38}$$

To calculate the total variance σ_{nc}^2, we substitute the Bennet components by the spectral density and integrate over the noise bandwidth B_{comp} (in Hz) of the comparator:

$$\sigma_{nc}^2 = \left(\frac{C_{\text{int}}}{\hat{I}_{\text{int}}}\right)^2 \frac{1}{\pi} \int_0^{2\pi B_{comp}} S_{u_{nc}}(f) H_i(\omega) d\omega \qquad \text{(B-39)}$$

We assume that the power spectral density consists of white noise with spectral density $S_{u_{nc}}$ and 1/f noise. The corner frequency equals $f_{c,nc}$:

$$S_{u_{nc}}(f) = S_{u_{nc}}\left[1 + \frac{f_{c,nc}}{f}\right] \qquad \text{(B-40)}$$

Substitution of (B-40) into (B-39) gives:

$$\sigma_{nc}^2 = \left(\frac{C_{\text{int}}}{I_{\text{int}}}\right)^2 4NB_{comp}S_{u_{nc}}\left(1 + \frac{4f_{c,nc}}{B_{comp}}\right) \qquad \text{(B-41)}$$

B.2.4 The noise voltage u_{na} of the amplifier in the C-V conv.

In this section discuss the jitter due to the noise voltage u_{na} of the amplifier in the C-V converter. This noise voltage is amplified to the output of the amplifier and sampled on C_s. The sampled value of the noise at time moments $t=t_i+T_1$ determines the time intervals $T_{2,i+1}$ (see Figure B-1). The noise voltage u_{out} at the output of the amplifier at time $t=t_i+T_1$ is given by $u_{out}(t_i+T_1)$:

$$u_{out}(t_{i-1}+T_1) = u_{na}(t_{i-1}) + G\left[u_{na}(t_{i-1}+T_1) - u_{na}(t_{i-1})\right] \quad i = 1,2,3,4 \qquad \text{(B-42)}$$

where the gain G is defined by:

$$G = \frac{C_x + C_p}{C_{va}} \qquad \text{(B-43)}$$

The time intervals $T_{sub,i}$ are given by

$$\begin{aligned} T_{sub,1} &= T_{sub} + \frac{u_{out}(t_{i-1}+T_1)C_s}{\hat{I}_{\text{int}}} \qquad i = 1, 4 \\ T_{sub,i} &= T_{sub} - \frac{u_{out}(t_{i-1}+T_1)C_s}{\hat{I}_{\text{int}}} \qquad i = 2, 3 \end{aligned} \qquad \text{(B-44)}$$

When we assume that $T_1=0$, the duration of one noisy period is given by T_{msm}`:

$$T_{msm}` = 4T_{sub} + \frac{GC_s}{\hat{I}_{\text{int}}}\left(u_{na}(t_0) - u_{na}(t_1) - u_{na}(t_2) + u_{na}(t_3)\right) \qquad \text{(B-45)}$$

The next step is to substitute the Bennet components by $\hat{u}_{na}\cos(\omega t+\varphi)$ into (B-45):

$$T_{msm}` = 4T_{sub} + \frac{GC_s\hat{u}_{na}}{\hat{I}_{\text{int}}}\left(\cos(\omega t_0+\varphi) - \cos(\omega t_1+\varphi) - \cos(\omega t_2+\varphi) + \cos(\omega t_3+\varphi)\right) \qquad \text{(B-46)}$$

This is the same type of expression as (B-6), except for a constant time shift. To calculate the variance ρ_{na}^2 for each Bennet component, we extend the time interval to N periods and integrate for φ over the interval $[-\pi,\pi]$. The result of these calculations can be approximated by

$$\rho_{na}^2 \cong \left(\frac{\hat{u}_{na} G C_s}{\hat{I}_{\text{int}}}\right)^2 H_u(\omega) \tag{B-47}$$

The power spectral density of u_{na} is given by $S_{u_{na}}(f)$:

$$S_{u_{na}}(f) = S_{u_{na}}\left(1 + \frac{f_{c,na}}{f}\right) \tag{B-48}$$

The variance σ_{na}^2 is now given by

$$\begin{aligned} \sigma_{na}^2 &= \left(\frac{GC_s}{\hat{I}_{\text{int}}}\right)^2 \frac{1}{\pi} \int_0^{2\pi B_{amp}} S_{u_{na}}(f) H_u(\omega) d\omega \\ &= \left(\frac{GC_s}{\hat{I}_{\text{int}}}\right)^2 4NB_{amp} S_{u_{na}}\left(1 + \frac{4f_{c,na}}{B_{amp}}\right) \end{aligned} \tag{B-49}$$

where B_{amp} equals the bandwidth of the C-V converter. In the case where the amplifier is implemented by an OTA with transconductance g_m, B_{amp} can be approximated by:

$$B_{amp} = \frac{g_m}{C_p} \tag{B-50}$$

Substitution of (B-50) into (B-49), using (B-43) and assuming $C_p >> C_x$ results in:

$$\sigma_{na}^2 = \left(\frac{C_s}{C_{va}\hat{I}_{\text{int}}}\right)^2 4Ng_m C_p S_{u_{na}}\left(1 + \frac{4f_{c,na}}{B_{amp}}\right) \tag{B-51}$$

This expression shows that the variance is proportional with C_p.

B.2.5 Switched Capacitor noise

An important noise source is the switched capacitor noise, which originates from the thermal noise of resistors. As follows by inspection of Figure B-1, all shown switches open and close every subperiod. Noise is sampled when a switch opens so the thermal noise of the ON resistance of the switches is sampled twice during every subperiod. We now calculate the noise charge q_n which flows through the integrator each subperiod. This noise charge comes from sampled noise voltages on C_s, C_{pb}, C_{o1} and C_{o2}. The noise charge is given by

$$\begin{aligned} q_n^2 &= 2\left(C_s + C_{pb} + C_{o1} + C_{o2}\right)^2 \frac{kT}{C_s + C_{pb} + C_{o1} + C_{o2}} \\ &= 2kT\left(C_s + C_{pb} + C_{o1} + C_{o2}\right) \end{aligned} \tag{B-52}$$

where k is Boltzmann's constant and T the absolute temperature. The total charge Q_{tot} flowing through the integrator is the sum of the charges flowing through C_s, C_{o1} and C_{o2}:

$$Q_{tot} = \hat{V}_x C_s + \hat{V}_o(C_{o1} + C_{o2}) \tag{B-53}$$

For 4N subperiods, the jitter is than given by ε_{SC}:

$$\varepsilon_{SC}^2 = \frac{1}{4N}\frac{q_n^2}{Q_{tot}^2} = \frac{kT\left(C_s + C_{pb} + C_{o1} + C_{o2}\right)}{2N\left(\hat{V}_x C_s + \hat{V}_o\left(C_{o1} + C_{o2}\right)\right)^2} \quad \text{(B-54)}$$

Example. With T=300K, N=256, $\hat{V}_x$=0.2V, $\hat{V}_o$=5V, C_s= C_{pb}=30pF and C_{o1}=C_{o2}=1pF, the jitter becomes 1ppm.

B.2.6 Other noise sources

In this section, we discuss the effect of other noise sources than described above. We will consider the noise of:

- The buffer amplifier which generates the reference voltage $V_{DD}/2$
- The DEM amplifier which is used during the measurement of resistive bridges with a small maximum bridge imbalance
- The buffer amplifier which drives the resistive chain during the measurement of thermistors

B.2.6.1 The noise voltage $u_{n,buf}$ of the bias voltage $V_{DD}/2$

A bias voltage of $V_{DD}/2$ is generated on chip. This voltage is used as a reference for the inverting nodes of the C-V converter, the integrator and the comparator. The buffer stage with noise voltage $u_{n,buf}$ is shown in Figure B-10. We consider only capacitive measurements.

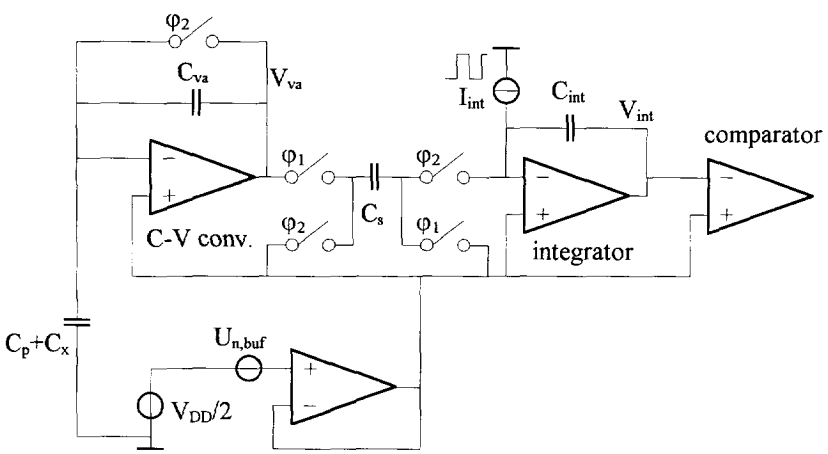


Figure B-10. The buffer amplifier, generating $V_{DD}/2$, has a noise voltage $u_{n,buf}$.

The noise voltage $u_{n,buf}$ only affects the charge which is sampled on C_s. Signals in the integrator and at the input of the comparator are not disturbed by $u_{n,buf}$. The simplified schematic is shown in Figure B-11. We also included for the substrate capacitance $C_{p,va}$ of C_{va}.

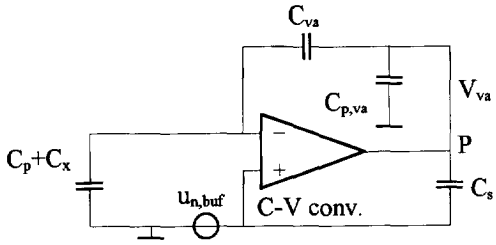


Figure B-11. The simplified schematic to calculate the effect of the noise voltage $u_{n,buf}$.

We do not derive an expression of one noisy period as a function of $u_{n,buf}$, but we use the simple calculation as proposed before. The noise voltage at the output of the C-V converter equals G time $u_{n,buf}$, where G is defined by (B-43). Within the closed loop bandwidth B_{va} of the C-V converter, the noise power of $u_{n,buf}$ equals the white spectral density $S_{u_{n,buf}}$ times the closed loop bandwidth B_{va} of the C-V converter, resulting in the noise charge $S_{u_{n,buf}}{}^{0.5}B_{va}{}^{0.5}C_p$ in C_{va}. The voltage across C_x equals V_{DD}, resulting in a signal charge of C_xV_{DD} in C_{va}. The equivalent noise capacitance for 4N samples is now given by the ratio of these charges and is given by $\Delta c_{n,buf}$:

$$\Delta c_{n,buf}^2 = \frac{C_p^2 S_{u_{n,buf}} B_{va}}{4NV_{DD}^2} \qquad \text{(B-55)}$$

where we assumed $C_p >> C_x$.
Example: With C_p=50pF, N=256, V_{DD}=5V, B_{va}=1MHz and $S_{u_{n,buf}}{}^{0.5}$=25nV/√Hz, the equivalent noise capacitance amounts to 8aF. This value will be larger due to noise at frequencies above B_{va}. For these frequencies, node P in Figure B-11 will be almost grounded and $u_{n,buf}$ is sampled on C_s.

B.2.6.2 Noise voltage of the DEM amplifier

The amplifiers inside the DEM amplifier have a noise voltage with spectral density $S_{u_{amp}}(f)$. When the bandwidth of the DEM amplifier equals B_{amp} and we consider 4N samples, the equivalent input noise voltage (in series with the output voltage of the bridge) is given by Δv_{amp}

$$\Delta v_{amp}^2 = \frac{2S_{u_{amp}} B_{amp}}{4N} \qquad \text{(B-56)}$$

where we only considered white noise. The factor 2 accounts for the fact that two identical amplifiers are used.
Example: With $S_{u_{amp}}{}^{0.5}$=25nV/√Hz, N=256 and B_{amp}=500kHz, Δv_{amp} equals 780nV.

B.2.6.3 Noise voltage of the drive amplifier for thermistors

The noise voltages of the amplifiers which drive the thermistor and the reference resistor result in a resolution which can be calculated in a way similar to the above by substituting the spectral density and the bandwidth of the DEM amplifiers by the spectral density and the bandwidth of the amplifiers which are used when measuring thermistors.

B.3 Noise of the Modified Martin Modulator

In this section, the resolution of the Modified Martin Modulator is calculated. We consider only the noise voltage u_{ni} of the amplifier inside the integrator. Figure B-12 shows one period of this modulator, consisting of two subperiods T_{sub}.

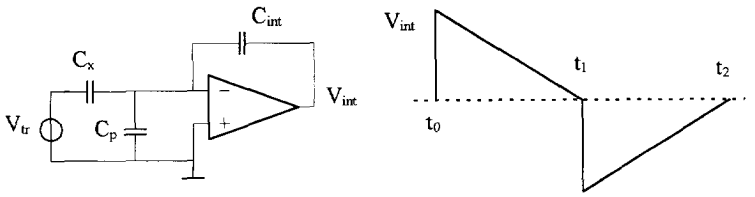


Figure B-12. The integrator of the Modified Martin Modulator and one period of the output voltage V_{int} of the integrator.

The duration of both subperiods t_1-t_0 and t_2-t_1 is given by

$$\begin{aligned} t_1 - t_0 &= T_{sub} + \frac{C_p + C_x}{\hat{I}_{\text{int}}}\left(u_{ni}(t_1) - u_{ni}(t_0)\right) \\ t_2 - t_i &= T_{sub} - \frac{C_p + C_x}{\hat{I}_{\text{int}}}\left(u_{ni}(t_2) - u_{ni}(t_1)\right) \end{aligned} \tag{B-57}$$

where $u_{ni}(t_i)$ is the value of u_{ni} at t_i. If we extend (B-57) to N modulator periods, we obtain the following expression for N noisy periods:

$$\begin{aligned} NT'_{mm} &= 2NT_{sub} \\ &+ \frac{C_p + C_x}{\hat{I}_{\text{int}}} \sum_{k=0}^{N-1}\Big[- u_{ni}(t_0 + 2kT_{sub}) + 2u_{ni}(t_0 + (2k+1)T_{sub}) - u_{ni}(t_0 + (2k+2)T_{sub})\Big] \end{aligned} \tag{B-58}$$

If we substitute the Bennet components $\hat{u}_{ni}\cos(\omega t+\varphi)$ into (B-58), the variance ρ_{ni}^2 due to just one Bennet component is given by:

$$\begin{aligned} \rho_{ni}^2 &= \frac{1}{2\pi}\int_{-\pi}^{\pi}\left(NT'_{mm} - \overline{NT'_{mm}}\right)^2 d\varphi \\ &= \left(\frac{\hat{u}_{ni}\left(C_p + C_x\right)}{\hat{I}_{\text{int}}}\right)^2 H_{mm}(\omega) \end{aligned} \tag{B-59}$$

where $H_{mm}(\omega)$ is defined as:

$$H_{mm}(\omega) = 2\frac{\cos(\omega T_{sub})\cos(N\omega T_{sub}) - \cos(\omega T_{sub}) - \cos^2(N\omega T_{sub}) + 1}{1 + \cos(\omega T_{sub})} \tag{B-60}$$

The total variance $\sigma_{ni,mm}^2$ can be calculated by summation over all Bennet components. This summation results in an integration, and the upper integration limit is equal to the closed loop bandwidth B_{int} (in Hz) of the integrator. The total variance is given by:

$$\sigma_{ni,mm}^2 = \left(\frac{C_p + C_x}{\hat{I}_{\text{int}}}\right)^2 \frac{1}{\pi} \int_0^{2\pi B_{\text{int}}} H_u(\omega) S_{u_{ni}}(f) d\omega$$
$$= \left(\frac{C_p + C_x}{\hat{I}_{\text{int}}}\right)^2 8NB_{\text{int}} S_{u_{ni}} \tag{B-61}$$

The relative jitter $\varepsilon_{ni,mm}^2$ is given by

$$\varepsilon_{ni,m}^2 = \frac{\sigma_{ni,mm}^2}{\left(2NT_{sub}\right)^2} = \left(1 + \frac{C_p}{C_x}\right)^2 \frac{2S_{u_{ni}} B_{\text{int}}}{NV_{DD}^2} \tag{B-62}$$

where we used $T_{sub}=V_{DD}C_x/\hat{I}_{\text{int}}$. When we assume that the bandwidth B_{int} is given by ratio of the feedback capacitor C_{int} and the parasitic capacitor C_p times the unity gain bandwidth f_T

$$B_{\text{int}} = \frac{C_{\text{int}}}{C_p} f_T \tag{B-63}$$

the relative jitter $\varepsilon_{ni,mm}$ is given by

$$\varepsilon_{ni,mm}^2 = \frac{2f_T C_p C_{\text{int}} S_{u_{ni}}}{NC_x^2 V_{DD}^2} \tag{B-64}$$

Note that the relative jitter ε_{ni} is proportional the square root of the parasitic C_p.

B.4 References

1 W. Bennet, "Spectra of quantized signals", Bell Syst. Tech. J., vol. BSTJ-27, pp 446-472 July 1948.

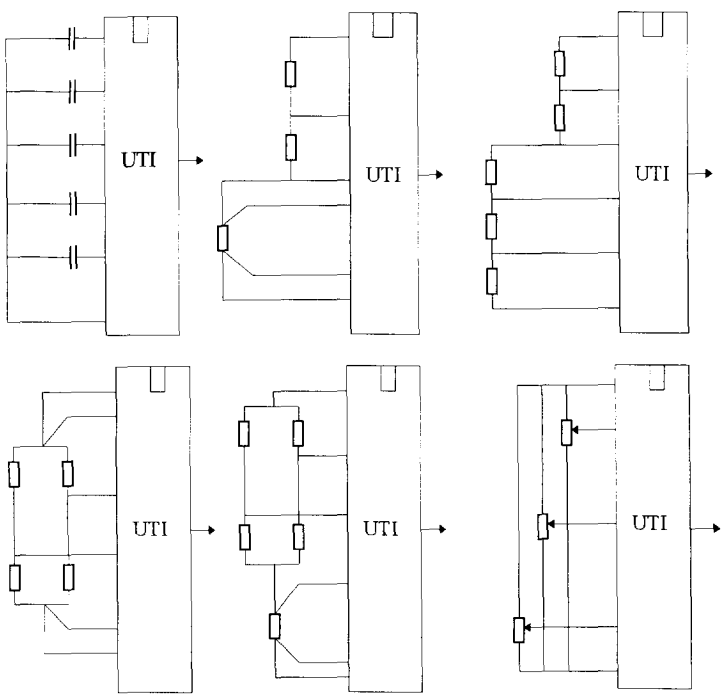
2 J. Barnes et. al., Characterization of Frequency Stability, IEEE Trans. Instrum. and Meas., vol. IM-20, pp 105-120, May 1971.

C. Application note

Universal Transducer Interface
Revolution in Sensor Interfacing

Product highlights:

- Smart interface for: **capacitors, platinum resistors, thermistors, bridges and potentiometers**
- Low-cost CMOS with standard input protection
- One line three-state output
- Resolution and accuracy up to 16 bits
- Easy interfacing with any type of microcontrollers
- No calibration required
- Suppression of 50/60 Hz interference
- Single 3.3V-5.5V power supply, current consumption below 2.5mA
- 16 pins DIL package
- Measurement time 10ms or 100ms typically



Application note of the UTI

Most important features

- Provides interfacing for many types of sensor elements: capacitors, platinum resistors, thermistors, resistive bridges and potentiometers
- Measurement of multiple sensor elements
- Single 3.3-5.5V power supply, current consumption below 2.5mA
- Resolution and accuracy up to 16 bits
- Low-cost CMOS
- No additional circuitry required
- Continuous auto-calibration of offset and gain
- Simple output signal which is compatible with microcontrollers
- Three-state output
- Typical measurement time 10 or 100ms
- 2/3/4-wire measurement available for almost all measurements
- Suppression of 50/60 Hz interference.
- Power down mode
- Temperature range -30°C to 70°C

1. Operation

The Universal Transducer Interface (UTI) is a sensor-signal-to-time converter, based on a period-modulated oscillator. The oscillator frequency varies between 20kHz and 50kHz, depending on the sensor signal. Sensing elements can be directly connected to the UTI without the need for extra electronics. Only a single reference element of the same kind as the sensor is required. Note that the reference is already included in resistive bridges, so no external components are required in this mode. The UTI provides interfacing for:

- Capacitive sensors 0-2pF, 0-12pF, variable range up to 300pF
- Platinum resistors Pt100, Pt1000
- Thermistors 1kΩ-25kΩ at room temperature
- Resistive bridges 250Ω-10kΩ with maximum imbalance +/- 4% or +/- 0.25%
- Potentiometers 1kΩ-50kΩ
- Combinations of the above mentioned

The drive signals for the sensor elements are chopped at 1/4 of the oscillator frequency to remove low-frequency interfering signals. Continuous auto-calibration of offset and gain of the complete system is performed. To perform this auto-calibration, a reference signal and a constant part (including offset voltages) are measured in exactly the same way as the sensor signal during two additional phases. During a third phase, the sensor signal itself is measured. The output signal of the UTI is very simple and has a discrete amplitude (V_{DD}), so it is compatible with microcontrollers. Figure 1 shows two complete cycles, each consisting of three phases.

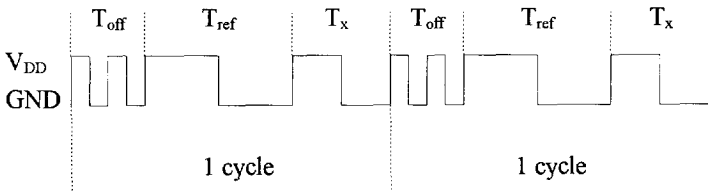


Figure 1. The output signal of the UTI for a three-phase mode.

During the first phase, the offset of the complete system is measured. During the second phase, the reference signal is measured and during the last phase, the signal itself is measured. These phases are automatically controlled by the UTI itself.
The duration of each phase is proportional to the signal which is measured during that phase. The duration of the three phases is given by:

For capacitive measurement:

$$T_{ref} = NK_1(C_{ref} + C_0)$$
$$T_x = NK_1(C_x + C_0)$$
$$T_{off} = NK_1C_0$$

For resistive measurement:

$$T_{ref} = NK_2(V_{ref} + V_0)$$
$$T_x = NK_2(V_x + V_0) \qquad (1)$$
$$T_{off} = NK_2V_0$$

where C_x or V_x is the sensor signal to be measured, C_{ref} or V_{ref} the reference signal, C_0 or V_0 a constant part (including offset voltages etc.) and K_1 or K_2 the gain. The factor N represents the number of internal oscillator periods in one phase. In slow mode N=1024, and in fast mode N=128. The voltages V_x and V_{ref} are, for instance, the voltage across the sensor resistor and the reference resistor or V_x and V_{ref} represent the bridge output voltage and the voltage across the bridge respectively. The microcontroller samples the output signal of the UTI by counting the number of internal clock cycles that fit in each phase. This results in the digital numbers N_{off}, N_{ref} and N_x. The ratio C_x/C_{ref} or V_x/V_{ref} can now be calculated by the microcontroller:

$$M = \frac{N_x - N_{off}}{N_{ref} - N_{off}} = \frac{C_x}{C_{ref}} \quad or \quad M = \frac{N_x - N_{off}}{N_{ref} - N_{off}} = \frac{V_x}{V_{ref}} \qquad (2)$$

This ratio does not depend on the constant part and the gain. In fact, the system is calibrated for offset and gain. Even in the case of drift or other slow variations of offset and gain, these effects are eliminated and (2) gives the right answer.
The three phases are time multiplexed, as depicted in Figure 1. The offset phase is labeled, because it consists of two short intervals: the output frequency is temporarily doubled. This is recognized by the microcontroller, which guarantees that the correct calculation, as depicted in (2), is made. The number of phases in a complete cycle varies between 3 and 5, depending on the mode.
A program for the microcontroller is available to handle the output signal of the UTI.

2. Pin-out and ratings

The interface is mounted in a 16-pins package. The function of the pins is listed in Table 1.

Name	Function of pin
V_{DD}, V_{ss}	Power supply
A, B, C, D, E, F	Sensor connections
SEL1..SEL4	Mode selection (see Table 2)
Out	Output for microcontroller
SF	Slow/fast mode selection
TEST	Normal/test mode selection
PD	Power down (three-state)

D	1	16	V_{DD}
C	2	15	E
B	3	14	F
SEL 1	4	13	TEST
SEL 2	5	12	OUT
SEL 3	6	11	PD
SEL 4	7	10	SF
V_{SS}	8	9	A

Table 1. Function of the 16 pins.

The selection pins SEL1, SEL2, SEL3, SEL4 define the UTI mode, as listed in Table 2. Here, a '1' corresponds to V_{DD} and '0' to GND. All sensor elements are connected to the UTI via pins A, B, C, D, E and F. Also available are some special functions like slow/fast selection, power-down and testing. These modes are set by SF, PD and TEST respectively.
SF=1: fast mode, N=128. SF=0: slow mode, N=1024.
PD=0: power-down, output node is high impedant, so several UTI can be used in parallel.
TEST=1: Testing mode. In this mode, the nonlinearity is measured.
All digital and analog inputs are protected for ESD.
No inputs may be floating, unless otherwise stated.

SEL1	SEL2	SEL3	SEL4	Mode	Number of phases	name	Mode number
0	0	0	0	5 Capacitors, 0-2pF	5	C25	0
0	0	0	1	3 Capacitors, 0-2pF	3	C23	1
0	0	1	0	5 Capacitors, 0-12pF	5	C12	2
0	0	1	1	Capacitors, 0-2pF/0-12pF, external MUX	-	CMUX	3
0	1	0	0	3 Capacitors, variable range to 300pF	3	C300	4
0	1	0	1	Platinum resistor Pt100-Pt1000, 4-wire	4	Pt	5
0	1	1	0	Thermistor 1kΩ-25kΩ, 4-wire	4	Ther	6
0	1	1	1	2 or 3 platinum resistors Pt100-Pt1000	5	Pt2	7
1	0	0	0	2 or 3 thermistors, 1kΩ-25kΩ,	5	Ther2	8
1	0	0	1	Resistive bridge, ref. is V_{bridge}, +/- 200mV	3	Ub2	9
1	0	1	0	Resistive bridge, ref. is V_{bridge}, +/- 12.5mV	3	Ub1	10
1	0	1	1	Resistive bridge, ref. is I_{bridge}, +/- 200mV	3	Ib2	11
1	1	0	0	Resistive bridge, ref. is I_{bridge}, +/- 12.5mV	3	Ib1	12
1	1	0	1	Res. bridge and two resistors, +/- 200mV	5	Brg2	13
1	1	1	0	Res. bridge and two resistors, +/- 12.5mV	5	Brg1	14
1	1	1	1	3 Potentiometers 1kΩ-50kΩ	5	Potm	15

Table 2. Different modes of the UTI , including the name of the modes and the number of phases within 1 cycle.

Some specifications and maximum ratings are listed in Table 3.

Parameter	min	typ.	max	unit
Power supply	3.3		5.5	V
Operating temperature	-30		80	°C
Supply current of interface:				
C25, C23, C12, CMUX, C300		1.5		mA
Pt, Pt2, Potm, Ib2		1		mA
Ub2, Brg2		1.1		mA
Ther, Ther2, Ub1, Ib1, Brg1		2.4		mA
power down mode			1	µA
Output impedance		60		Ω

Table 3. Some specifications and maximum ratings.

3. Some theory

Here, the following aspects are discussed:

- Internal oscillator frequency
- Chopping
- Resolution
- Testing mode
- Measurement of sensor elements

3.1 Internal oscillator frequency

The data in this section yields for the measurement condition V_{DD}=5V and T_a=25°C.
The modulator period of the internal first order oscillator for capacitive ($T_{osc,C}$) and resistive ($T_{osc,R}$) measurement is given by:

$$T_{osc,C} = K_1(C + C_0)$$
$$T_{osc,R} = K_2(V + V_0) \qquad (3)$$

The constants K_1C_0 and K_2V_0 both equal 20µs, corresponding to a 50kHz offset frequency. The maximum oscillator periods are for both types of measurements approximately 40µs. The gains K_1 and K_2 depend on the mode and can be found in the specification list of each mode.

3.2 Chopping

The electrical drive signals for the sensing elements are chopped at 1/4 of the modulator frequency. This is to remove low-frequency disturbing signals coming from the mains supply. Also the effect of parasitic thermocouple junctions is eliminated. By using a second-order Switched-Capacitor filter, in combination with a differentiation during capacitive measurements, the 50/60Hz interfering signal is substantially reduced.

3.3 Resolution.

The output signal of the UTI is sampled by the microcontroller. This sampling introduces quantization noise, which also limits the resolution. The amount of quantization noise of a measurement phase is given by the relative standard deviation σ_q:

$$\sigma_q = \frac{1}{\sqrt{6}} \frac{t_s}{T_{phase}} \tag{4}$$

where t_s is the sampling time and T_{phase} the phase duration. When the sampling time is 1µs and the offset frequency is 50kHz, the standard deviation of the offset phase is 160ppm in the fast mode and 20ppm in the slow mode. Further improvement of the resolution can be obtained by taking into account several values of M. When P values $M_1..M_P$ are used to calculate M, the value of σ_q is $P^{1/2}$ times decreased.

In addition to quantization noise, another limitation of the resolution is the thermal noise of the oscillator itself. In the fast mode, quantization noise is found to be the main noise source. During our measurements, we used the Intel 87C51FA microcontroller with a 3MHz sampling frequency.

3.4 Test mode

In the test mode, the nonlinearity of the system is measured. This mode can be activated by selecting TEST=1. In the normal mode, the UTI measures according to the selected function in Table 2. During each phase, only one sensing element is measured. In the test mode however, the output is slightly different with respect to Figure 1. During two phases, two signals S_{x1} and S_{x2} are measured successively. During a third phase, $S_{x1}+S_{x2}$ is measured. Of course, the offset needs to be measured, so one cycle takes 4 phases. The sampling by the microcontroller of these four phases results in the digital numbers N_{x1}, N_{x2}, N_{x1+x2} and N_{off}. A measure of the nonlinearity is given by λ:

$$\lambda = \frac{N_{x1} + N_{x2} - 2N_{off}}{N_{x1+x2} - N_{off}} - 1 \tag{5}$$

If the modulator is perfectly linear, λ equals zero. In practical situations, λ has values between 100ppm and 500ppm, depending on the mode.

The nonlinearity can be measured in almost all modes. The signals which are measured during all measurement phases for TEST=1 are listed in Table 4.

Mode	Phases	Phase 1	Phase 2	Phase 3	Phase 4
0. C25	4	$C_{BA}+C_0$	$C_{CA}+C_0$	$C_{DA}+C_0$	$C_{CA}+C_{DA}+C_0$
1. C23	4	$C_{BA}+C_0$	$C_{CA}+C_0$	$C_{DA}+C_0$	$C_{CA}+C_{DA}+C_0$
2. C12	4	$C_{BA}+C_0$	$C_{CA}+C_0$	$C_{DA}+C_0$	$C_{CA}+C_{DA}+C_0$
3. CMUX	$C_{BA}+C_0$	-	-	-	-
4. C300	4	$C_{BA}+C_0$	$C_{CA}+C_0$	$C_{DA}+C_0$	$C_{CA}+C_{DA}+C_0$
5. Pt	4	V_0	$V_{AB}+V_0$	$V_{AD}+V_0$	$V_{BD}+V_0$
6. Ther	4	V_0	$V_{AB}+V_0$	$V_{AD}+V_0$	$V_{BD}+V_0$
7. Pt2	4	V_0	$V_{AB}+V_0$	$V_{AD}+V_0$	$V_{BD}+V_0$
8. Ther2	4	V_0	$V_{AB}+V_0$	$V_{AD}+V_0$	$V_{BD}+V_0$
9. Ub2	3	V_0	$V_{AB}^{I}+V_0$	$V_{CD}+V_0$	-
10. Ub1	3	V_0	$V_{AB}^{I}+V_0$	$V_{CD}^{II}+V_0$	-
11. Ib2	3	V_0	$V_{AB}+V_0$	$V_{CD}+V_0$	-
12. Ib1	3	V_0	$V_{AB}+V_0$	$V_{CD}^{II}+V_0$	-
13. Brg2	4	V_0	$V_{AB}+V_0$	$V_{AF}+V_0$	$V_{BF}+V_0$
14. Brg1	4	V_0	$V_{AB}+V_0$	$V_{AF}+V_0$	$V_{BF}+V_0$
15. Potm	4	V_0	$V_{EF}+V_0$	$V_{CF}+V_0$	$V_{EC}+V_0$

Table 4. Measured signals for TEST=1.

^{I}: A 32-times voltage divider is used. ^{II}: A 15-times voltage amplifier is used.

3.5 Introduction to measurement of sensor elements

The measurement setup for measuring capacitors is shown in Figure 2. All capacitors to be measured (C_x) are connected to node A, which is the input of an integrator during capacitive measurements. The DC voltage of this node is $V_{DD}/2$. The signal at the transmitting electrode V_{tr} is a square wave with an amplitude equal to V_{DD} and frequency between 20kHz and 50kHz (depending on C_x). The output voltage of the integrator is sampled and converted into a time signal. Only in the mode C300 is the amplitude of V_{tr} smaller than V_{DD}. The total capacitance at node A, including the parasitic capacitance C_{par}, should be limited to 500pF (except for mode CMUX). Calibration for C_{par} is not required, since the effect of C_{par} is eliminated by calculation (2). The integration capacitance C_{int} equals 7pF or42pF, depending on the mode.

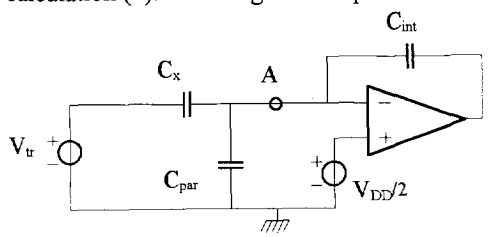


Figure 2. Measurement setup for measuring capacitors.

The measurement setup for measuring resistors and resistive bridges is shown in Figure 3. The electrical drive signals are chopped at 1/4 of the oscillator frequency. This is to suppress low-frequency disturbing signals. The voltage across the resistor to be measured (R_x), having maximum value of 0.4V, is sampled on C_s. The charge on C_s is transferred to C_{int}. The capacitor C_{par} is, for instance, the capacitance of the cables. The time constant consisting of R_1, R_x, C_{par} and C_s should be less than 250ns. The sampling capacitance C_s equals 2pF or 28pF, depending on the mode.

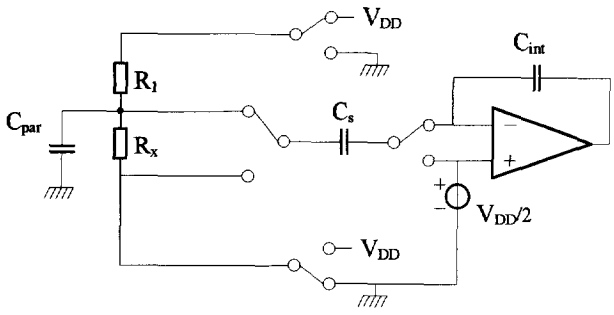


Figure 3. Measurement setup for measuring resistive sensor elements.

4. Different modes

Below, we give the connection of the sensors to the UTI for all the different modes. The names of these modes are the same as those used in Table 2. In this secton, TEST=0 and SF=0 unless otherwise stated. We also give important parameters, such as

- accuracy
- resolution
- number of phases
- signals during phases

We refer all phases to the labeled phase, which is phase 1. In this phase, the constant part (or offset) is measured. This phase contains the synchronization for the microcontroller, since the output frequency of the UTI is doubled. See also chapter 1.

Throughout the measurements, we used an Intel 87C51FA microcontroller with 3MHz sampling frequency.

4.1 Mode 0. C25: 5 capacitors 0-2pF

In this mode, 5 capacitors with one common electrode in the 0-2pF range can be measured. The connection of capacitors is depicted in Figure 4. All capacitors should have a common receiver electrode, connected to node A. The signal at the transmitting electrodes B to F is a square wave with amplitude V_{DD}. When a capacitor is not selected, the voltage is equal to GND. The value of C_{int} in Figure 2 is 7pF. Capacitor C_{par} is, for instance, the capacitance of the cables and does not affect the measurement result M for C_p<300pF.

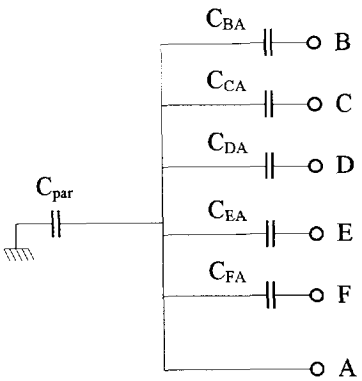


Figure 4. Connection of capacitors to the UTI.

In this mode, one cycle takes 5 measurement phases as depicted in Table 5.

Phase	Measured capacitors
1	$C_{BA}+C_0$
2	$C_{CA}+C_0$
3	$C_{DA}+C_0$
4	$C_{EA}+C_0$
5	$C_{FA}+C_0$

Table 5. Measured capacitors during each phase.

The specifications for the C25 mode are listed in Table 6.

Parameter	Value
K_1	10µs/pF
C_0	2pF
maximum capacitance C_{iA}	2pF
Max. value of C_{par}	300pF
Nonlinearity	250ppm
resolution SF=0, C_{par}=30pF	50aF
Resolution SF=0, C_{par}=300pF	200aF
Remaining offset	<15fF
Number of phases	5

Table 6. Specifications for the C25 mode.

The measured equivalent offset is the result of the parasitics between the bonding wires, the bonding pads and the IC pins. When this offset is considered to be too large, one should use the mode CMUX. In this mode, an external multiplexer is used and offset can be as low as 20aF.

4.2 Mode 1. C23: 3 capacitors 0-2pF

In this mode, 3 capacitors with one common electrode in the 0-2pF range can be measured. The difference between this mode and mode C25 is that in this mode one cycle consists of 3 phases. The connection of the capacitors is shown in Figure 4, where C_{EA} and C_{FA} are now

omitted. The measured capacitors during each phase are listed in Table 7. The specifications are listed in Table 6.

Phase	Measured capacitors
1	$C_{BA}+C_0$
2	$C_{CA}+C_0$
3	$C_{DA}+C_0$

Table 7. Measured capacitors during each phase for the mode C23.

4.3 Mode 2. C12: 5 capacitors 0-12pF

In this mode, 5 capacitors with one common electrode in the 0-12pF range can be measured. The connection of the capacitors to the UTI is shown in Figure 4. The maximum capacitance C_{iA} is 12pF. The number of phases is 5. The specifications are listed in Table 8. The value of C_{int} in Figure 2 is 42pF. The measured capacitors during each phase is listed in Table 5. The main difference between this mode and mode C25 is that the maximum capacitance that can be measured in this mode is 12pF.

The measured equivalent offset is the result of the parasitics between the bonding wires, the bonding pads and the IC pins. When this offset is considered to be too large, one should use the mode CMUX. In this mode, an external multiplexer is used and offset can be as low as 20aF.

Parameter	Value
K_1	1.7µs/pF
C_0	12pF
Maximum capacitance C_{iA}	12pF
Max. value of C_{par}	300pF
Nonlinearity	250ppm
Resolution SF=0, C_{par}=30pF	300aF
Remaining offset	<15fF
Number of phases	5

Table 8. Specifications for the C12 mode.

4.4 Mode 3. CMUX: capacitors 0-2pF/0-12pF, external MUX

In this mode an arbitrary number of capacitors with a common electrode in the 0-2pF range (TEST=0) or 0-12pF range (TEST=1) can be measured. The UTI does not perform a phase selection, so an external digital multiplexer should be used. The value of C_{int} in Figure 2 is 7pF (TEST=0) or 42pF (TEST=1).

The nonlinearity depends on the parasitic capacitance C_{par}, but is below 250 ppm for C_{par}<300pF. For larger values of C_{par}, the nonlinearity increases to 3000 ppm for C_{par}=1nF. Larger values of C_{par} are allowed, but the nonlinearity will be increased further.

The resolution also depends on C_{par}. The resolution in the small range (0-2pF) for a measurement time of 100ms equals 50aF for C_{par}<30pF and increases to 350aF for C_{par}=1nF.

The specifications for the CMUX mode are listed in Table 9.

Parameter	Value TEST=0	Value TEST=1
K_1	10µs/pF	1.7µs/pF
C_0	2pF	12pF
maximum capacitance C_{iA}	2 pF	12pF
max. value of C_{par}	10 nF	10nF
nonlinearity C_{par}<300pF	250 ppm	250ppm
Offset	20aF	20aF
resolution 100ms, C_{par}<30pF	50aF	300aF

Table 9. Specifications for the CMUX mode.

A possible measurement setup is depicted in Figure 5. An external multiplexer is controlled by the microcontroller (µC) and multiplexes the signal at node B to one (or more) of the capacitors. The oscillator output appears on the node "output". This is the signal for the microcontroller. This signal is a normal square wave with amplitude V_{DD} and frequency $f_{osc}/8$ (SF=1) or $f_{osc}/1024$ (SF=0). Nominal frequencies of the output signal during an offset measurement (none of the capacitors are selected) are 6kHz (SF=1) and 50Hz (SF=0).

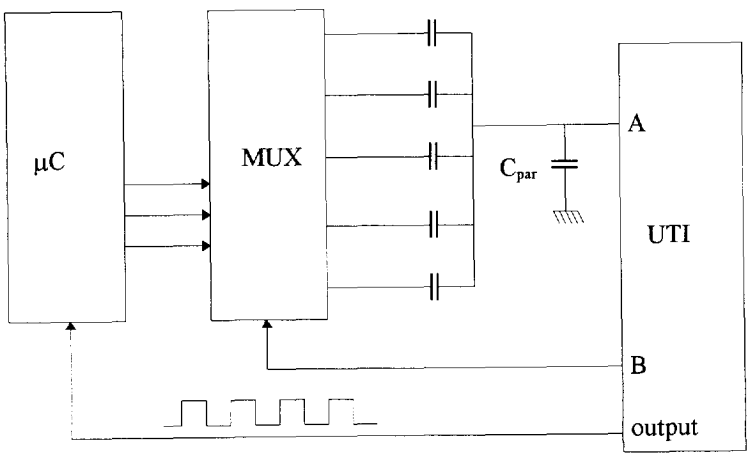


Figure 5. Possible measurement setup in the CMUX mode to measure more capacitors.

4.5 Mode 4. C300: 3 capacitors, range up to 300pF

In this mode, 3 capacitors with a common electrode with a variable range up to 300pF can be measured. The connection of sensors and external resistors is depicted in Figure 6. These resistors set the voltage swing at the transmitting electrode of C_{iA}. This voltage swing must be limited to keep the integrator in Figure 2 in its linear region. The value of C_{int} in Figure 2 is 42 pF.

The total capacitance at node A must be limited to 500pF in order to keep the nonlinearity below 10^{-3}. The voltage swing at the transmitting electrodes equals V_{EF} which is set externally by means of three inaccurate resistors R_1, R_2 and R_3, of which R_1 or R_3 may be zero. For the DC voltage V_{EF} holds:

$V_{EF} < 60/C_{max}$,

where C_{max} is the maximum of C_{BA}, C_{CA} and C_{DA} expressed in pF. The total time constant of all resistors and capacitors should be less than 500ns. This sets the values of the resistors.

Example: When C_{CA}=300pF, C_{DA}=200pF, C_{BA}=0 and V_{DD}=5V , practical values of the resistors are R_1=25kΩ, R_2=1kΩ and R_3=0. The voltage swing at the transmitting electrode V_{EF}=0.2V.
The value of K_1 depends on V_{EF}: the larger this voltage, the larger K_1. The value of K_1 is found from:
$K_1=0.33V_{EF}$ μs/pF·V.
For C_0 holds:
$C_0=20\mu s/K_1$.
The system contains two time constants $C_{tot}\cdot(R_3//(R_1+R_2))$ and $C_{tot}\cdot(R_1//(R_2+R_3))$, where $C_{tot}=C_{BA}+C_{CA}+C_{DA}+C_{par}$. Both time constants must be smaller than 500ns.

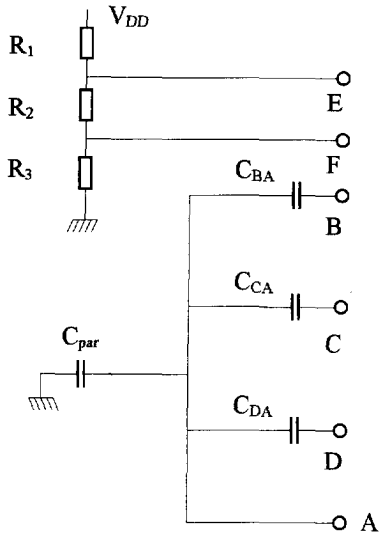


Figure 6. Connection of sensors to the UTI for the C300 mode.

The nonlinearity and resolution in the slow mode are depicted in Table 10. Here, the value of C_{DA}=0, C_{par}=30pF and V_{EF} has the maximum value $60/C_{max}$, as described before. The maximum measured capacitor during the measurement of the nonlinearity amounts to C_{BA}–C_{CA}.

Capacitors	Nonlinearity	Resolution (fF)
$C_{BA}=C_{CA}$=33pF	$1.4\cdot10^{-4}$	1.2
$C_{BA}=C_{CA}$=150pF	$1.9\cdot10^{-4}$	6.6
$C_{BA}=C_{CA}$=270pF	$9.0\cdot10^{-4}$	17
$C_{BA}=C_{CA}$=330pF	$2.6\cdot10^{-3}$	20
$C_{BA}=C_{CA}$=560pF	$6.3\cdot10^{-3}$	46

Table 10. Values of nonlinearity and resolution in C300 mode for different capacitor values.

The measured capacitors during each phase are listed in Table 11.

Phase	Capacitor
1	C_{BA} and C_0
2	C_{CA} and C_0
3	C_{DA} and C_0

Table 11. Measured capacitors during each phase for the mode C300.

4.6 Mode 5. Pt: 1 platinum resistor Pt100/ Pt1000, 4-wire

In this mode, one platinum resistor and one reference resistor can be measured.
The connection of the resistors to the UTI is depicted in Figure 7. Because of the ideal voltage measurement, both resistors R_x and R_{ref} are measured in a 4-wire setup, thereby completely eliminating the effect of lead resistances. The driving voltage V_{EF} is a square wave with amplitude V_{DD} at 1/4 of the oscillator frequency. Resistor R_1 sets the current through the chain.

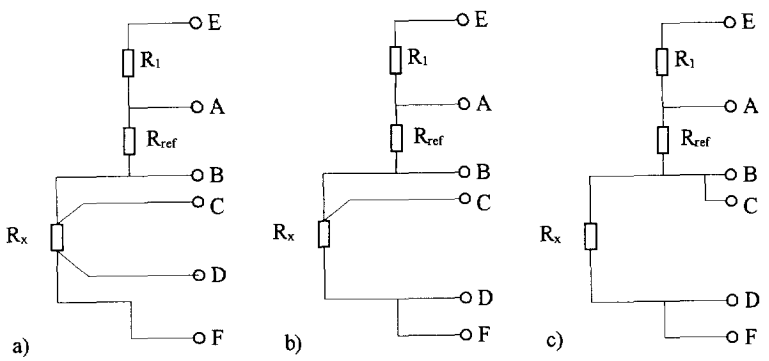


Figure 7. Connection of platinum resistors to the UTI in a 4-wire (a), 3-wire (b) and a 2-wire (c) connection.

One measurement cycle consists of 4 phases. These phase contain the information for a 2-, 3- and 4-wire measurement.

Phase	measured voltages
1	V_0
2	$V_{AB}+V_0$
3	$V_{CD}+V_0$
4	$V_{BC}+V_0$

Table 12. Measured node voltages during measurement of platinum resistors

To calculate the ratio as in (2), we have to make different calculations for the 2-, 3- and 4-wire measurement:

$$M_{2-,4-wire} = \frac{T_{phase3} - T_{phase1}}{T_{phase2} - T_{phase1}} = \frac{R_x}{R_{ref}}$$

$$M_{3-wire} = \frac{T_{phase3} - T_{phase4}}{T_{phase2} - T_{phase1}} = \frac{R_x}{R_{ref}} \quad (6)$$

The nonlinearity is better than 150 ppm when the amplitude of the voltages V_{AB} and V_{CD} is below 0.7V for V_{DD}=5V and 0.4V for V_{DD}=3.3V. This limits the current through the platinum resistor. Note that the temperature error of a Pt100 due to self-heating, for a thermal resistance of 200K/W (still air) at V_{CD}=0.7V and 0°C amounts to 1K. If this self-heating error is too large, R_1 must be increased to limit the current through the Pt100. The temperature error due to self-heating for the same thermal resistance amounts to 80mK for V_{CD}=0.2V. This is two times better than the initial inaccuracy of a class A Pt100. The current through the Pt100 then amounts to 2mA and this requires R_1=2.2kΩ.
The relative sensitivity of a Pt100 is $3.9 \cdot 10^{-3}$/K. When the current through the Pt100 is 2mA, this sensitivity corresponds to 780μV/K. The resolution in this mode of the UTI is 7μV, corresponding to 9mK. This holds for the slow mode.
Table 13 lists the UTI specifications in the Pt mode.

Parameter (V_{DD}=5V)	Value
K_2	56μs/V
V_0	0.36V
R_1 (Pt100, self-heating for 200K/W=80mK)	2.2kΩ (5%), I=2mA
R_1 (Pt1000, self-heating for 200K/W=80mK)	6.2kΩ (5%), I=600μA
Offset	10μV
Nonlinearity	150ppm
Resolution SF=0 (Pt100, 2mA)	7 μV (9mK)

Table 13. Specifications for the Pt mode.

Amplitudes of V_{CD} and V_{AB} up to 2.5V peak-to-peak are allowed, but self-heating effects have to be taken into account. Very good resolutions can be obtained in this case. The nonlinearity, however, is increased to 4000 ppm for peak-to-peak amplitudes in the range 0.7-2.5V.

The value of C_s in Figure 3 is 28pF. The time constant consisting of the resistors, C_s and the parasitics of the connecting cables must be less than 250ns.
Platinum resistors can also be measured using mode Ib2.

4.7 Mode 6. Ther: 1 thermistor, 4-wire

In this mode, one thermistor and one reference resistor can be measured. The connection of the thermistor and the reference resistor is shown in Figure 8. The driving voltage V_{EF} is a chopped voltage with an amplitude of V_{DD}/12.5. (0.4V at V_{DD}=5V) and DC value V_{DD}/2. The ratio of the thermistor and the reference resistor is also given by (6). The signals which are measured during the phases are listed in Table 12. The voltage V_{AB} is not constant, but has the same temperature information as V_{CD}.

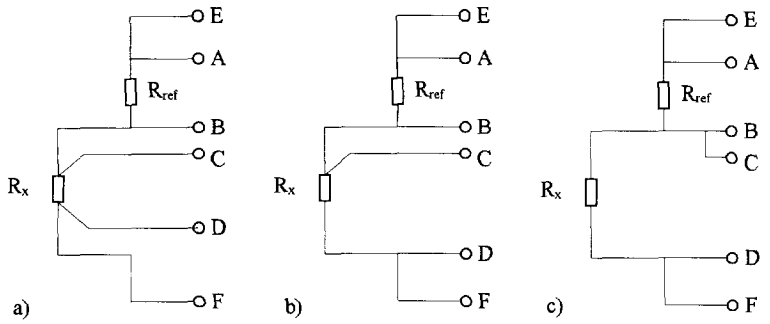


Figure 8. Connection of the thermistor to the UTI in a 4-wire (a), 3-wire (b) and 2-wire (c) connection.

Parameter (V_{DD}=5V)	Value
K_2	56µs/V
V_0	0.36V
$R_{ref}//R_x$	<5kΩ
$R_{ref}+R_x$	>1kΩ
Offset	10µV
Nonlinearity	150ppm
Resolution SF=0	7 µV (1mK)

Table 14. Specifications for the Ther mode.

For very large and very small values of R_x (10 times or 0.1 times R_{ref}), the resolution in voltage is still the same, but the resolution in temperature is decreased. This is due to the linearization method.

For a thermistor with a sensitivity of 4%/K, the resolution is 1mK for V_{DD}=5V.

4.8 Mode 7. Pt2: 2 or 3 platinum resistors

In this mode, 2 or 3 platinum resistors can be measured. The connection of the resistors to the UTI is shown in Figure 9. The voltage V_{EF} is the same as in the mode Pt.

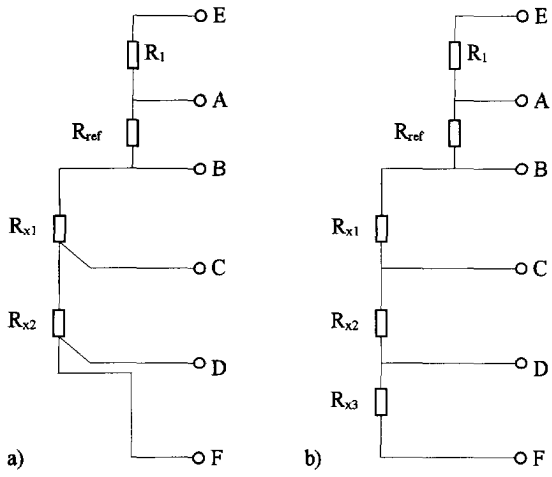


Figure 9. Connection of 2 (a) or 3 (b) platinum resistors for the Pt2 mode.

The same restrictions for the current through the resistors as in the pt mode holds here. The specifications are listed in Table 13. Note that R_{x2} can be measured with a 4-wire setup. Phase 5 can be used to measure just one lead resistance or to measure R_{x3}.
The main difference with the Pt mode is that one measurement cycle takes 5 phases, as listed in Table 15.

Phase	Measured voltages
1	V_0
2	$V_{AB}+V_0$
3	$V_{CD}+V_0$
4	$V_{BC}+V_0$
5	$V_{DF}+V_0$

Table 15. Measured voltages during the phases for the Pt2 mode.

4.9 Mode 8. Ther2: 2 or 3 thermistors

In this mode, 2 or 3 thermistors can be measured. The connection is depicted in Figure 10. The number of phases is also 5, as listed in Table 15. The specifications as listed in Table 14 hold for this mode.

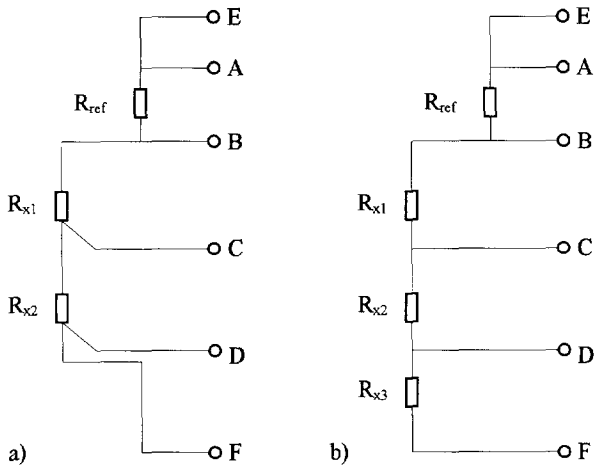


Figure 10. Connections of 2 (a) and 3 (b) thermistors to the UTI.

With the connection in Figure 10a, the effect of lead resistances can be eliminated, since the measurement of V_{DF} represents a lead resistance. With the connection shown in Figure 10b, the effect of lead resistances cannot be eliminated.

4.10 Mode 9. Ub2: resistive bridge, ref. is V_{bridge}, +/- 4% imbalance

In this mode, a resistive bridge can be measured where the ratio of the bridge supply voltage V_{AB} and the bridge output voltage V_{CD} represents the physical signal. The maximum bridge imbalance is +/-4%. The connection of the bridge to the UTI is shown in Figure 11. The driving voltage across the bridge V_{EF} is a square wave with amplitude V_{DD}. The frequency of this signal is 1/4 of the oscillator frequency.

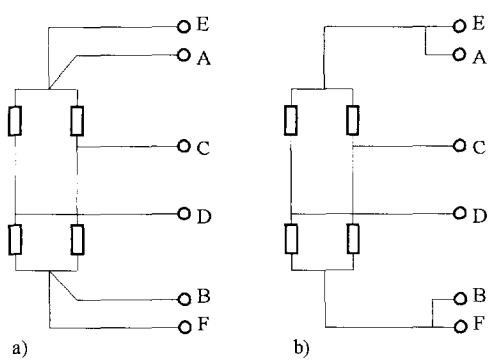


Figure 11. Connection of the resistive bridge to the UTI for the Ub2 mode in a 4-wire setup (a) and a 2-wire setup (b).

Because of the ideal voltage measurement, the bridge is measured in a 4-wire setup, as shown in Figure 11a. The signals which are measured in each phase are listed in Table 16.

Phase	Measured voltages
1	V_0
2	$V_{AB}/32 + V_0$
3	$V_{CD}+V_0$

Table 16. Measurement phases for the Ub2 mode.

During phase 2, the voltage across the bridge V_{AB} is measured. An on-chip voltage divider divides this voltage by 32. The divider does not have to be calibrated. After division, V_{AB} is processed in the same way as V_{CD}. To obtain the bridge imbalance, the microcontroller calculates:

$$M = \frac{1}{32}\,\frac{T_{phase3} - T_{phase1}}{T_{phase2} - T_{phase1}} = \frac{V_{CD}}{V_{AB}} \qquad (7)$$

The value of C_s in Figure 3 is 28pF. The time constant consisting of the bridge, the connecting cables and C_s should be limited to 250ns.
The specifications are listed in Table 17.

Parameter	Value
K_2	56µs/V
V_0	0.54V
Bridge excitation	AC V_{DD}
Bridge resistance R_b	$250\Omega < R_b < 10k\Omega$
Bridge output voltage	max +/- 0.2V
Accuracy of divider	$5 \cdot 10^{-4}$
Offset	10µV
Resolution SF=0	7µV

Table 17. Specifications for the Ub2 mode.

4.11 Mode 10. Ub1: res. bridge, ref. is V_{bridge}, +/- 0.25% imbalance

In this mode, a resistive bridge can be measured where the ratio of the bridge supply voltage and the output voltage of the bridge represents the physical signal. The main difference between this mode and mode Ub2 is that in the maximum bridge imbalance in this mod is 0.25%. (V_{CD}=12.5mV for V_{DD}=5V). The connection of the bridge to the UTI is the same as in the Ub2 mode. An on-chip 15-times voltage amplifier amplifies the small output voltage before it is processed in the same way as the divided voltage across the bridge. Both the amplifier and divider do not have to be calibrated. To calculate the bridge imbalance, (7) can be used, where 32 must be replaced by 480. Because of the ideal voltage measurement, the bridge is measured in a 4-wire setup. The specifications are listed in Table 18.

Parameter	Value
K_2	56µs/V
V_0	0.54V
Bridge excitation	AC V_{DD}
Bridge resistance R_b	$250\Omega < R_b < 10k\Omega$
Bridge output voltage	max +/- 12.5mV
Accuracy of divider and amplifier	10^{-3}
Offset	10µV
Resolution SF=0	700nV

Table 18. Specifications of the Ub1 mode.

The measured voltage during each phase is listed in Table 19.

Phase	Measured voltages
1	V_0
2	$V_{AB}/32 + V_0$
3	$15V_{CD} + V_0$

Table 19. Measured voltages during each phase for the Ub1 mode.

4.12 Mode 11. Ib2: resistive bridge, ref. is I_{bridge}, +/- 4% imbalance

In this mode, a resistive bridge can be measured where the physical signal is represented by the output voltage of the bridge and the current through the bridge. This current I is converted into a reference voltage. The connection of the bridge and the reference element is shown in Figure 12a. This mode can also be used for the measurement of platinum resistors, as shown in Figure 12b.

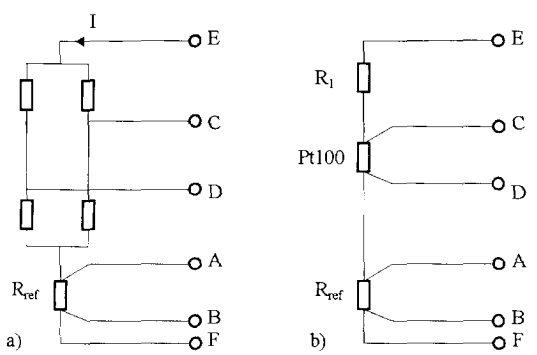


Figure 12. Connection of the resistive bridge and a reference resistor to the UTI (a) and connection of a platinum resistor in 4-wire setup (b).

The value of R_{ref} should be chosen such that V_{AB} is between 100mV and 200mV.

Phase	Measured voltages
1	V_0
2	$V_{AB}+V_0$
3	$V_{CD}+V_0$

Table 20. Measured voltages for the different phases for the Ib2 mode.

Parameter	Value
K_2	56µs/V
V_0	0.54V
Bridge excitation	AC V_{DD}
Bridge resistance R_b	250Ω < R_b < 10kΩ
Bridge output voltage	max +/- 0.2V
Accuracy	250ppm
Offset	10µV
Resolution SF=0	7µV

Table 21. Specifications for the Ib2 mode.

The sampling capacitance C_s in Figure 3 is 28pF. The time constant consisting of the bridge, R_{ref}, the cable capacitances and C_s should be less than 250 ns.

This mode can also be used to measure platinum resistors in a 4-wire setup. This is shown in Figure 12b. The advantage in comparison with mode Pt is that now only three phases have to be measured.

4.13 Mode 12. Ib1: resistive bridge, ref. is I_{bridge}, +/- 0.25% imbalance

This is almost the same mode as mode Ib2. The connection of the bridge and the resistor is shown in Figure 12. The difference is that the maximum bridge imbalance is +/- 0.25%. The voltage across the reference resistor should be between 0.1 and 0.2V, as mode Ib2. The bridge output voltage is amplified 15 times before it is processed in the same way as the reference voltage.
To obtain the bridge imbalance, the microcontroller calculates

$$M = \frac{1}{15}\frac{T_{phase3} - T_{phase1}}{T_{phase2} - T_{phase1}} = \frac{V_{CD}}{IR_{ref}} \tag{8}$$

The specifications for the Ib1 mode are listed in Table 22.

Parameter	Value
K_2	56µs/V
V_0	0.54V
Bridge excitation	AC V_{DD}
Bridge resistance R_b	250Ω < R_b < 10kΩ
Bridge output voltage	max. +/- 12.5mV
Accuracy	10^{-3}
Offset	10µV
Resolution SF=0	700nV

Table 22. Specifications for the Ib1 mode.

The voltage which are measured during each phase are listed in Table 23.

Phase	Measured voltages
1	V_0
2	$V_{AB} + V_0$
3	$15V_{CD} + V_0$

Table 23. Measured voltages during each phase for the Ib1 mode.

4.14 Mode 13. Brg2: resistive bridge +/- 4% and 2 resistors

In this mode, a resistive bridge with a maximum imbalance of +/-4% and 2 resistors can be measured. One of the resistors can be temperature dependent, so the bridge output can be digitally corrected for temperature effects.
Both the voltage across the bridge and the current through the bridge are measured. The connection of the elements to the UTI is shown in Figure 13.
The voltage V_{EF} is a square wave with amplitude V_{DD} at 1/4 of the oscillator frequency. The voltage across R_{ref} should be between 0.1 and 0.2V.

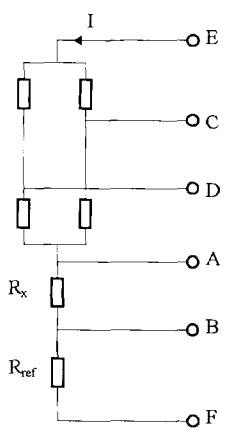


Figure 13. Connections of the sensors to the UTI.

The voltages to be measured are listed in Table 24.

Phase	Measured voltages
1	V_0
2	$V_{AB} + V_0$
3	$V_{CD} + V_0$
4	$V_{BF} + V_0$
5	$V_{EA}/32 + V_0$

Table 24. Signals during the different measurement phases for the mode: Brg2.

The voltage across the bridge V_{EA} is divided by 32 before it is processed in the same way as the other measured voltages. The bridge imbalance V_{CD}/V_{EA} is obtained from:

$$M = \frac{1}{32} \frac{T_{phase3} - T_{phase1}}{T_{phase5} - T_{phase1}} = \frac{V_{CD}}{V_{EA}} \quad (9)$$

The specifications for the Brg2 mode are listed in Table 25.

Parameter	Value
K_2	56µs/V
V_0	0.54V
Excitation V_{EF}	AC V_{DD}
Bridge resistance R_b	250Ω < R_b < 10kΩ
Bridge output voltage	max +/- 0.2V
Accuracy V_{CD}/V_{EA}	500 ppm
Accuracy V_{AB}/V_{BF}	200 ppm
Offset V_{CD} or V_{AB}	10µV
Resolution SF=0	7µV

Table 25. Specifications for the Brg2 mode.

4.15 Mode 14. Brg1: resistive bridge +/- 0.25% and 2 resistors

This mode is almost the same as mode Brg2. The connection is shown in Figure 13. The difference is that the maximum bridge imbalance is 0.25%. The bridge output voltage V_{CD} is amplified 15 times before it is processed further.
The specifications are listed in Table 26.

Parameter	Value
K_2	56µs/V
V_0	0.54V
Excitation V_{EF}	AC V_{DD}
Bridge resistance R_b	250Ω < R_b < 10kΩ
Bridge output voltage	max +/- 12.5mV
Accuracy V_{CD}/V_{EA}	10^{-3}
Accuracy V_{AB}/V_{BF}	$2 \cdot 10^{-4}$
Offset V_{CD}	10µV
Offset V_{AB}	10µV
Resolution V_{CD} SF=0	700nV
Resolution V_{AB} SF=0	7µV

Table 26. Specifications for the mode Brg1.

The measured voltages during each phase are listed in Table 27.

Phase	Measured voltages
1	V_0
2	$V_{AB} + V_0$
3	$15V_{CD} + V_0$
4	$V_{BF} + V_0$
5	$V_{EA}/32 + V_0$

Table 27. Measured voltages during each phase for the Brg1 mode.

4.16 Mode 15. Potm: 3 potentiometers, 1kΩ-25kΩ

In this mode, 3 potentiometers in the 1kΩ-50kΩ range can be measured. The connection of potentiometers is depicted in Figure 14. When two potentiometers are used, node D should be connected to F. The voltage across the potentiometers is a square wave with amplitude V_{DD} and frequency 1/4 of the oscillator frequency. The capacitors C_{pari} model the parasitics.

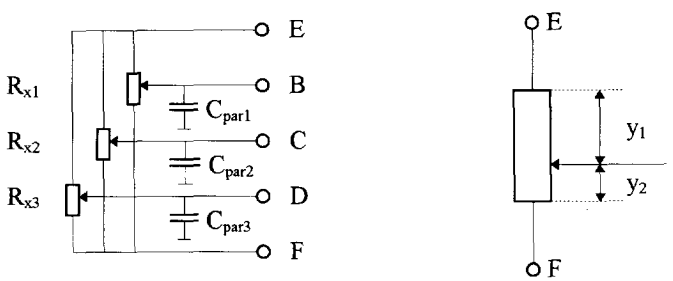


Figure 14. Connection of potentiometers to the UTI.

It is not possible to account for the influence of lead wires. Therefore, the use of low-ohmic potentiometers should be avoided.
The measured node voltages during each phase is listed in Table 28.

phase	measured voltages
1	V_0
2	$V_{EF}+V_0$
3	$V_{CF}+V_0$
4	$V_{BF}+V_0$
5	$V_{DF}+V_0$

Table 28. Measured node voltages for each phase during measuring of potentiometers.

The value of C_s in Figure 3 is 2pF. Every time constant consisting of one potentiometer, the sampling capacitance and the cable capacitance should be less than 250ns.
The calculation M for each potentiometer is given by:

$$M = \frac{T_{phase3,4,5} - T_{phase1}}{T_{phase2} - T_{phase1}} = \frac{y_2}{y_1 + y_2} \qquad (10)$$

Parameter	Value
K_2	4µs/V
V_0	5V
potentiometer value R_{xi}	$1k\Omega < R_{xi} < 25k\Omega$
Accuracy	10^{-3}
Resolution SF=0	50 ppm

Table 29. Specifications for the Potm mode.

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Biography

Frank van der Goes was born in Delft on the 21th February, 1966.
In 1984 he began his studies in Electrical Engineering at the Delft University of Technology. He graduated in 1990. For two years, he attended a designers course and started his Ph. D. research in 1992. His main scientific interest lies in the field of Analog-to-Digital conversion and low-cost sensor interfacing.

Samenvatting

Een groot probleem in huidige sensorsystemen is het ontbreken van goedkope en nauwkeurige sensor interfaces. Goedkope en nauwkeurige sensorsystemen zouden veel nieuwe toepassingen mogelijk maken en bestaande goedkoper en beter. Een goede manier om dergelijke systemen te realiseren is het combineren van interfaces en microcontrollers.
In dit proefschrift beperken we ons tot veelgebruikte sensorelementen zoals capaciteiten, platina weerstanden, thermistors, resistieve bruggen en potentiometers. Verder beperken we ons tot uitleessnelheden en nauwkeurigheden respektievelijk in het bereik 10-1000 metingen per seconde en 10-16 bits. We richten ons op een multi-purpose interface, aangezien dit type momenteel goedkoper kan zijn dan een applikatiespecifieke interface. Om zo eenvoudig en robuust mogelijke circuits te verkrijgen, proberen we de noodzakelijke functies zoveel mogelijk door de microcontroller te laten uitvoeren.
We moeten een aantal meettechnieken toepassen om een goedkope nauwkeurige multi-purpose interface te kunnen realiseren. Deze zijn continue autocalibratie technieken, tweepoort-meettechnieken, synchrone detectie en dynamic element matching.
Het blijkt dat de Analoog-naar-Digitaal omzetter in goedkope en nauwkeurige sensor systemen het best geïmplementeerd kan worden door een asynchrone oscillator in combinatie met een microcontroller. Dit volgt na de afweging van belangrijke aspecten zoals het aantal draden tussen de interface en de microcontroller, het formaat van het uitgangssignaal van de interface, de belasting van de microcontroller, de benodigde omzettingstijd en de onderdrukking van diverse stoorsignalen. De selectie van de referentie- en offsetmeting geschiedt door de interface zelf.
De relaxatieoscillator is gebaseerd op periode modulatie waarbij de spanningsslag over de integratiecapaciteit gemoduleerd wordt.
Laagfrequente stoorsignalen worden onderdrukt met synchrone detectie in combinatie met een tweede-orde switched-capacitor (SC) filter. Dit filter onderdrukt tevens laagfrequente 1/f ruis. Deze eigenschap maakt het mogelijk om goedkope CMOS processen te gebruiken, terwijl toch goede resultaten verkregen kunnen worden. Hoogfrequente stoorsignalen worden ook onderdrukt, onder andere door toepassing van dithertechnieken.
Het niet-lineare gedrag van de modulator is onderzocht. Het resultaat hiervan is dat aan de eisen die aan de modulator gesteld worden, gemakkelijk voldaan kan worden. Specifieke circuits zijn toegepast om sensor-specifieke meetproblemen op te lossen. Zo zijn bijvoorbeeld een calibratie-vrije spanningsdeler en spanningsversterker toegepast om de nauwkeurige uitlezing van brugsensoren mogelijk te maken.
De interface is gerealiseerd in een 0.7μm CMOS proces en is verpakt in een 16-pins DIL behuizing. Het aantal IC-pinnen, waaraan alle sensoren aangesloten worden, bedraagt slechts zes. Om de maximaal haalbare onderdrukking van laagfrequente stoorsignalen te verkrijgen, is de generatie van de integratiestroom gebaseerd of switched-current (SI) technieken. Een interne watch dog houdt het oscillatieproces scherp in de gaten en (her)start de oscillator indien nodig.
De gerealiseerde interface werkt op een enkelzijdige voedingsspanning tussen 3.3V en 5.5V. Het stroomverbruik bedraagt minder dan 2mA. In het algemeen bedraagt de resolutie 16 bits bij een meettijd van 100ms. De resolutie voor capacitieve metingen in het bereik 0-2pF bedraagt 50aF. De niet-lineariteit in het temperatuurbereik -40°C tot 80°C bedraagt 200 ppm.

Zowel resolutie als niet-lineariteit hangen af van de parasitaire capaciteit. De resolutie bij resistieve metingen bedraagt 7μV bij een meettijd van 100ms. Als bijvoorbeeld een Pt100 gemeten wordt, waardoor een stroom met een amplitude van 2mA vloeit, dan bedraagt de resolutie in temperatuur 9mK. Bij thermistors met een gevoeligheid van 4%/K is de resolutie beter dan 1mK bij gelijke meettijd. De niet-lineariteit in het genoemde temperatuur bereik bedraagt 150 ppm. De onnauwkeurigheid van de calibratie-vrije spanningsdeler en spanningsversterker bedragen respektievelijk 500 ppm en 1000 ppm. De onderdrukking van laagfrequente stoorsignalen is bijna gelijk aan het maximaal haalbare.