LOW-DISTORTION DELTA-SIGMA TOPOLOGIES FOR MASH ARCHITECTURES

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ABSTRACT

This paper describes low-distortion delta-sigma topologies with significant system and circuit-level advantages over traditional delta-sigma topologies, especially for wideband (low oversampling ratio) applications. A comparison between traditional and low-distortion MASH topologies shows how the latter can achieve higher performance while requiring smaller silicon area and power consumption.

1. INTRODUCTION

The recent growth in broadband communication applications has motivated the development of analog-to-digital converters capable of high resolution (above 14 bits) with increased signal bandwidth (several MHz). Often, converters which address these requirements use multi-stage delta-sigma (MASH) architectures operating with low oversampling ratios [1, 2].

Delta-sigma data converters rely on high oversampling ratios to obtain high resolutions and relaxed accuracy requirements for their analog components. However, at low oversampling ratios, these benefits should not be taken for granted. High resolutions can only be obtained by increasing other parameters, such as the noise-shaping order or the quantizer resolution. In addition, distortion components produced by nonlinear opamp gain and limited slew rate are not adequately attenuated by the delta-sigma loop, so careful opamp design is necessary to avoid those effects.

One way to deal with the issue of opamp distortion is to prevent the opamps from processing input signal. This can be achieved by making the modulator's signal transfer function *STF* equal to 1, which allows for the input signal and the quantization noise to be processed separately. This is not a new idea. Earlier applications were presented in [3, 4, 5]. However, its benefits have not been fully appreciated: in addition to low distortion, topologies using this technique have other advantages at system and circuit level, and are especially useful for MASH architectures. These benefits will be explored in this paper.

A low-distortion topology is described in Section 2. Its advantages are addressed in Section 3. Section 4 shows simulation results comparing a traditional topology (i.e., where *STF* is not 1) with the low-distortion topology in the context of MASH, and illustrates the specific gains that can be obtained from the novel structure.

2. THEORY OF LOW-DISTORTION OPERATION

Figure 1 shows a generic *L*-order cascade-of-integrators feedforward (CIFF) topology, as described in [9]. Consider the case when $b_1 = b_2 = \ldots = b_{L-1} = 0$ and $b_0 = b_L = 1$. It can be easily verified that, in this case, *STF(z)* = 1. For this condition, the input signal u is cancelled in e and the integrators process quantization noise only. Therefore, their nonlinearities do not affect the transmission of the input signal u. This concept can be applied to noise-shaping of any order or complexity [6].

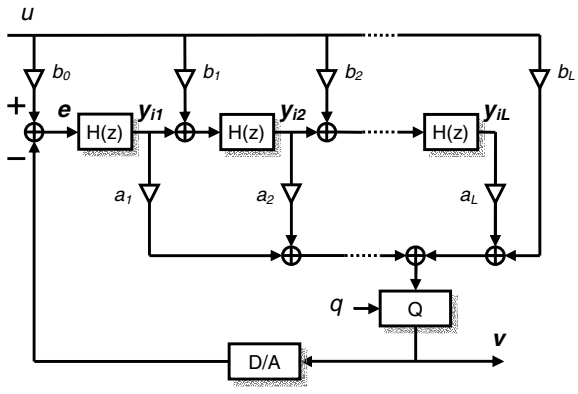

Figure 1: Generic *L*-order feedforward topology.

A particular case is the second-order topology shown in Figure 2, previously presented by the authors in [5]. Its main features are the feedforward path and the absence of DAC signal feedback to the second integrator.

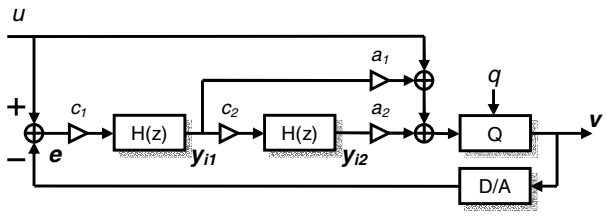

Figure 2: Low-distortion second-order topology.

3. ADVANTAGES OF THE LOW-DISTORTION TOPOLOGY

In addition to reduced sensitivity to opamp nonlinearities, the low-distortion topology has the following advantages:

3.1. Lower area and power consumption in multibit implementations

Since the integrators process quantization noise only, their coefficients can be scaled accordingly to the quantizer resolution. As an example, for the topology shown in Figure 2, it can be shown that the optimum coefficients for maximum opamp output swing under ideal conditions are

$$c_1 = 2^{N-1}, \quad c_2 = 2, \quad a_1 = \frac{2}{c_1} = \frac{1}{2^{N-2}}, \quad a_2 = \frac{1}{c_1 c_2} = \frac{1}{2^N} \qquad (1)$$

where N is the resolution of the quantizer in bits.

The integrator coefficients c_1 and c_2 can be larger than those of a traditional topology. Hence, for the same sampling capacitor sizes, constrained by kT/C noise considerations, the integrating capacitors can be smaller, resulting in area savings.

When designing the opamps, the bias currents are determined from bandwidth or slew rate requirements. In the latter case, the power consumption is proportional to $SR \cdot C_L$, where SR and C_L are the slew rate and load capacitance of each opamp, respectively. Depending on the choice of coefficients and targeted OSR, considerably lower power consumptions can be achieved.

In practice, there are reasons to make the integrator coefficients somewhat smaller than what is given by Eq. (1)—the opamp outputs include not only quantization noise, but also noise caused by circuit non-idealities (DAC errors, kT/C noise, etc). They may also include dither. If opamp bandwidth is an issue, the coefficient values can be lowered to increase the feedback factors and therefore reduce the unity-gain bandwidth requirements. Opamp slew-rate requirements can also be reduced. Also, it may be desirable to use less of the available dynamic range to reduce distortion—although opamp distortion does not affect the input signal u, it will modulate the quantization noise and may reduce the maximum achievable SNR.

3.2. Improved input signal range

The output swing of the opamps does not limit the input signal amplitude. In fact, the only elements that have to accommodate the full input signal swing are the switches and the quantizer. In traditional topologies, care must be taken to ensure that the opamp outputs do not saturate for the maximum signal amplitude, which is accomplished by designing the integrator coefficients for the worst case scenario. This is not necessary in the low-distortion topology.

3.3. Only one DAC in feedback path

Most delta-sigma A/D modulator topologies use distributed feedback and require two or more DACs in their implementation. Although not necessary for low-distortion operation, the presented topology has only one DAC is in the feedback loop, making it more convenient for circuit implementation. For multibit DACs, the savings in terms of area and complexity can be significant, especially if calibration is used for DAC linearization.

3.4. Simplified MASH architectures

MASH architectures require coupling the quantization noise of one stage to another, and this usually requires subtracting the quantizer output from its input. An example is the two-stage MASH shown in Figure 3, where the first stage uses a traditional topology. Extra circuitry is necessary to implement this operation. The low-distortion topology is especially useful for this application because the quantization noise is directly available at the output of the second integrator. With the integrator transfer function given by $H(z) = z^{-1}/(1 - z^{-1})$, this output can be written as

$$Y_{i2}(z) = \frac{H^2(z)}{[1+H(z)]^2} Q_1(z) = z^{-2} Q_1(z) \qquad (2)$$

Figure 4 illustrates this for the same two-stage MASH architecture, where the first stage uses a second-order low-distortion topology. The second stage uses a simple ADC, but there are also advantages in using this topology for subsequent MASH stages [10].

MASH architectures rely on accurate matching between analog and digital noise transfer functions for quantization noise cancellation. This matching is usually assured by making the analog NTF nearly ideal (by employing high-performance analog components). Another way is to match the digital NTF to the non-ideal analog NTF by using an adaptive compensation scheme [7, 8]. In the latter case, the adaptive filter can be simplified by using the low-distortion topology. The

details of the adaptive compensation scheme are omitted for brevity. For proper noise cancellation, the digital NTF needs to satisfy:

$$NTF_{1D}(z) = \frac{z^{-2}}{H^2(z)} = (1+n_0) - (2+n_1)z^{-1} + (1+n_2)z^{-2} \qquad (3)$$

where n_0, n_1 and n_2 are correction terms that compensate for circuit imperfections such as opamp finite gain and capacitor mismatch errors. For the same result, a traditional MASH architecture (shown in Figure 3) requires

$$NTF_{1D}(z) = \frac{1}{[1+H(z)]^2} = \frac{(1+n_0) - (2+n_1)z^{-1} + (1+n_2)z^{-2}}{d_0 + d_1 z^{-1} + d_2 z^{-2}} \qquad (4)$$

Note that coefficients d_1, d_2 and d_3 are now necessary for compensating circuit imperfections. Hence, Eq. (4) needs to be implemented as an IIR filter, or approximated by a higher-order FIR filter. Equation (3) requires only a 3-tap FIR filter, and therefore is simpler to implement.

4. SIMULATION RESULTS

To illustrate the advantages described in this paper, two MASH 2-0 structures were modeled and simulated in MATLAB. In the first structure (Figure 3), the first stage is implemented by a traditional modulator. In the second structure (Figure 4), the first stage is implemented by a low-distortion modulator. Both use a 5-bit quantizer in the first stage and a 6-bit quantizer in the second stage. Under ideal conditions, both structures offer the same SQNR performance.

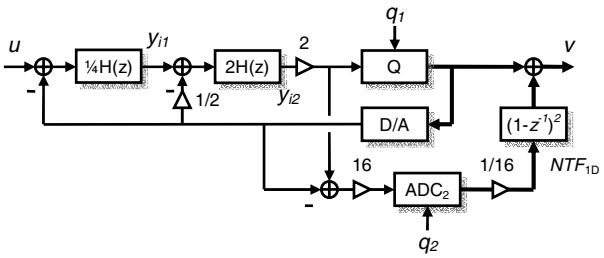

Figure 3: MASH 2-0 with traditional topology.

All integrator models include a nonlinear opamp input-output transfer curve, modeled as a hyperbolic tangent with a maximum gain of 60 dB. The coefficient values, shown in the Figures, were selected so that the integrator outputs y_{i1} and y_{i2} use half of the maximum range in both topologies. DAC nonlinearities were not included. In practice, a calibration method or a dynamic-element-matching algorithm are necessary to linearize the DAC operation.

In the following simulation results, the input signal u had a frequency of $f_s/64$, and the oversampling ratio was 16. Figure 5 shows the SNDR versus input amplitude curves for both topologies.

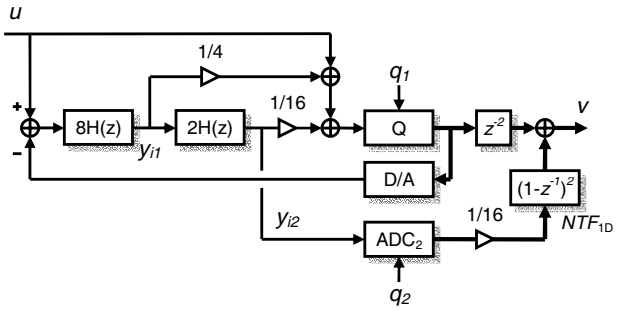

Figure 4: MASH 2-0 with low-distortion topology.

As shown in the Figure, both topologies have similar results for input signal amplitudes below -3 dB (in relation to V_{REF}). Above that, the traditional topology exhibits SNDR degradations due to the increased harmonic distortion. The maximum SNDR for the traditional topology is 97.4 dB. The proposed low-distortion topology does not show SNDR degradations until the input amplitude of -0.5 dB, and can achieve a maximum SNDR of 101.8 dB.

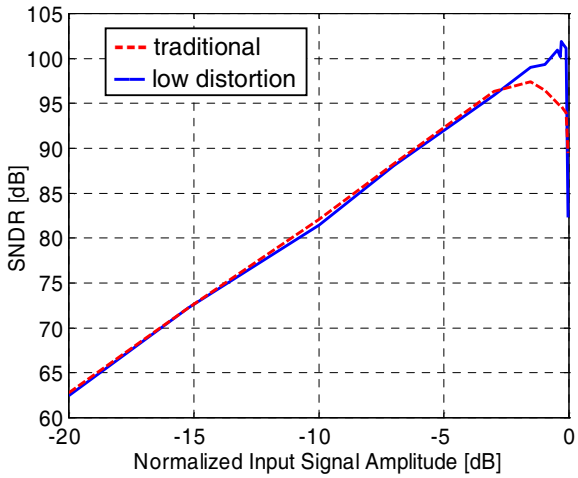

Figure 5: SNDR versus input amplitude.

Further advantages are observed when capacitor sizing is taken into consideration. The input sampling capacitor in the first integrator (C_{s1}) has the same noise contribution in both topologies. However, the sampling capacitor in the second integrator (C_{s2}) needs to be larger for the traditional topology because its noise is multiplied by a larger gain, as required by proper coefficient scaling. The size of this capacitor is more significant for low oversampling ratios. The choice of sampling capacitor sizes shown in Table 1 would generate the same total kT/C noise needed for 16-bit performance. The total capacitance for each topology, also shown in the Table, is calculated as

$$C_{TOTAL} = C_{s1} + C_{i1} + C_{s2} + C_{i2} = C_{s1}\left(1+\frac{1}{c_1}\right) + C_{s2}\left(1+\frac{1}{c_2}\right) \qquad (5)$$

where C_{i1} and C_{i2} are integrating capacitors.

Table 1: Capacitor sizes for same *kT/C* noise.

Topology	C_{s1} [pF]	C_{s2} [pF]	C_{TOTAL} [pF]
Traditional	15	4	81.0
Low-distortion	8.5	0.5	10.3

This translates into considerable area and power consumption savings for the low-distortion topology. Capacitance area is 7.9 times smaller. The total opamp power consumption for this example is 60% lower than that of the traditional topology. These savings are more pronounced for lower OSR values.

5. CONCLUSIONS

Low-distortion delta-sigma topologies have important system and circuit-level advantages over traditional topologies. These advantages were described in this paper and illustrated by comparing the requirements of traditional and low-distortion MASH topologies.

ACKNOWLEDGMENTS

The authors would like to thank the NSF Center for the Design of Analog and Digital Integrated Circuits for support. The authors are also grateful to Mr. Anas Hamoui of the University of Toronto, and Dr. Jesper Steensgaard for useful discussions.

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