Low-Energy CMOS Common-Drain Power Amplifier for Short-Range Applications

Parvaneh Saffari[1], Mohammad Taherzadeh-Sani[1], Ali Basaligheh[1], Frederic Nabki[2], Mohamad Sawan[3]

[1]Department of Electrical Engineering, Ferdowsi University of Mashhad, Mashhad, Iran
[2]CoFaMic Research Center, Université du Québec à Montréal, Montreal, Canada
[3]Department of Electrical Engineering, Polytechnique Montreal, Quebec, Montreal, Canada

***Abstract*— In this paper, a power amplifier implemented with a common-drain structure is introduced. With proper input matching, this structure is shown to provide a reasonable power gain and superior linearity and efficiency in comparison to other low-power topologies. This is shown to be due to the low dependency of the power gain to the transistor transconductance and the low-voltage variations across the gate-source capacitance. This power amplifier is suitable for low-power and short-range applications such as Bluetooth Low Energy (BLE). Based on the calculated *S*-parameters, the operation frequency of this amplifier and its design trade-offs are presented, along with a comparison with competitive topologies. The design is simulated in a 0.13 µm CMOS technology, operates with a 1.2 V supply, and provides a power gain of 8.5 dB with a DC power consumption of 3.6 mW. The input 1-dB compression point is 2.2 dBm, yielding a power added efficiency of 43%.**

Keywords*— *Power amplifier, Common-drain, High linearity and efficiency.

I. Introduction

Low-power, short-range and low-data rate radio frequency (RF) communication standards such as Bluetooth Low Energy (BLE) are becoming prevalent in today's handsets and consumer electronics. Typical applications of these standards include wireless sensor networks and wirelessly connected electronics running on cell batteries offering tight energy budgets [1-3]. As a result, highly power efficient circuitry must be designed in order to attain the power budgets required by the RF transceivers for use in these applications. CMOS technology is a natural fit to implement these circuits because of its low cost, and attainable performance that is well-suited to the relaxed output power requirements of such applications. Accordingly, this work addresses the design of a CMOS power amplifier having a medium gain and output power that are suited to these applications, and that can provide superior efficiency than typical power amplifier (PA) structures. For this purpose, an efficient and highly linear common-drain PA is presented.

Typically, the main nonlinearity in CMOS PAs results from the intrinsic nonlinear transconductance and the nonlinear gate-source capacitance C_{gs}, while other nonlinearities from the drain-junction capacitor C_{gd} and the output conductance $1/r_{ds}$ are negligible [4-6]. Most PAs utilize the common-source structure, whereas in [7-9] a common-drain structure is used. Although there are several designs and analyses of common-source PAs, the common-drain PA is rarely analyzed. In this paper, it is shown analytically for the first time that the common-drain PA has the potential to provide good performance (power gain, stability and efficiency) as well as a high linearity. The resulting design limitations and trade-offs are presented and discussed. Works such as the one presented in [7] operate a common-drain with a resistive network at the transistor gate for input bandpass filtering and stability, which limits the amount of gain achievable by such structures. In addition, in the high voltage transistors often used in common-drain topologies, large parasitic capacitances are present, which deteriorates the stability preventing larger gains to be attained. Particularities of the CMOS design presented here are that it utilizes standard transistors and voltage amplification from its input matching network to provide its power gain and bandpass filtering of the input. This allows the common-drain topology presented here to provide relatively large gain.

This paper is organized as follows. In section II, the operating principle of the proposed PA is described. In section III, equations for the operation frequency of the amplifier and its *S*-parameters are derived. By analyzing these *S*-parameters, it is shown that the PA can provide a reasonable gain and high linearity. Moreover, the design trade-offs and the performance limitations / conditions of the proposed structure are discussed. In section IV, the simulation results of the common-drain PA implemented in a 0.13 µm CMOS technology are presented and compared with other PAs for low-power applications. The results are discussed in section V and are compared to other works. This comparison is followed by a conclusion. The presented simulation results show that the proposed common-drain PA offers better linearity and efficiency than other PA structures for low-power and short-range applications.

II. Operating Principle

The proposed PA structure is shown in Fig. 1. Note that packaging parasitics (QFN package) used in simulations are not shown in Fig. 1 for simplicity. The circuit operates as

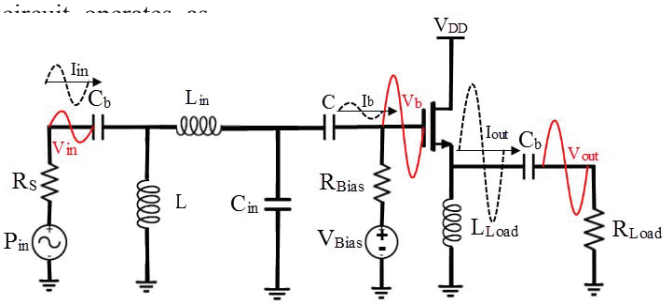

Fig 1. Common-drain PA structure with input matching network.

follows. Firstly, the input voltage amplitude is increased at the gate of the transistor by the Π input matching network. This voltage is then DC shifted to the source of the transistor with an attenuation of ~0.9. Accordingly, the role of transistor is to buffer its gate voltage to its source, and generate the required current to drive the load with sufficient power. The input matching network matches the input of the PA, and increases the input voltage amplitude at the gate of the transistor in order to provide the power gain. As such, the power gain results from the increased voltage at the gate buffered to the source, and from the associated drain current.

This operating principle is illustrated in Fig. 1 through the overlaid current and voltage conceptual waveforms. Across the matching network, the voltage signal is increased at the gate while the current is reduced, as the matching network is passive. At the source, the voltage is slightly attenuated, but the current is increased as a result of the transistor drive. Therefore, the power gain is not only a result of the high output current, but also of the effective voltage amplification due to the input matching network. Notably, the low dependency of the power gain to the transistor transconductance and the smaller voltage variations across the gate-source capacitance allow for the good linearity of this structure.

III. S-Parameter Analysis and Design Considerations

As shown in Fig. 1, L_{in}, C_{in}, L, and C implement the input matching network, while the input biasing voltage, V_{Bias}, is applied through R_{Bias}. L_{load} is the load inductor and R_{load} is the output load of the PA, which is considered to be a 50 Ω antenna. C_b is a large decoupling capacitor. The small-signal model of this PA is shown in Fig. 2. Through nodal analysis, the Y-parameters can be derived, and can be readily converted to S-parameters [10]. Simplifying the S-parameters, the operation frequency of the proposed common-drain PA, which is the frequency that $|S_{21}|$ is maximum, is derived to be:

$$\omega_{op} = \sqrt{\frac{1}{C_{in}\left(L + L_{in}\right)}} \tag{1}$$

Note that to simplify these equations, the parasitic elements R_{ds} and C_{ds} are neglected along with the parasitics of the package. The *S*-parameters at the operating frequency are derived to be:

$$|S_{21}| = \frac{2g_m\sqrt{R_{o1}R_{o2}\left(L^2\omega_{op}^2 + R^2\right)}}{Z_{02}g_m + 1} \times \frac{1}{\sqrt{\left(-\frac{R_{in}L}{L+L_{in}} + \frac{RL}{L+L_{in}}\right)^2 + \left(\frac{L^2}{L+L_{in}} + Z_{o1}C_{in}\left(R+R_{in}\right)^2\omega_{op}^2\right)^2}}, \tag{2}$$

$$|S_{22}| = \left|\frac{g_m Z_{o2}^* - 1}{g_m Z_{o2} + 1}\right|, \quad \text{and} \tag{3}$$

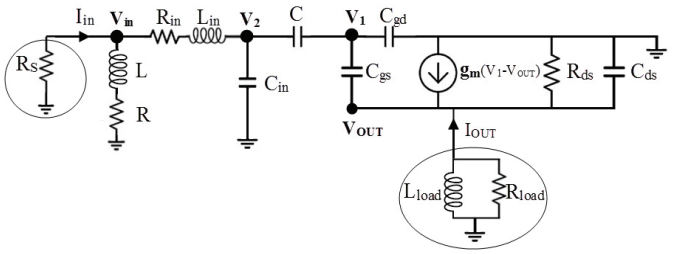

Fig 2. Small-signal model of the common-drain PA structure with input matching network.

$$|S_{12}| = \frac{2C_{gs}\sqrt{R_{o1}R_{o2}}\sqrt{L^2\omega_{op}^2 + R^2}.\omega_{op}}{(Z_{o2}g_m + 1)} \times \frac{1}{\sqrt{\left(-\frac{R_{in}L}{L+L_{in}} + \frac{RL}{L+L_{in}}\right)^2 + \left(\frac{L^2}{L+L_{in}} + Z_{o1}C_{in}(R+R_{in})^2\omega_{op}^2\right)^2}}. \tag{4}$$

where Z_{01} is the impedance of the PA input, Z_{02} is the impedance of its output, and R_{01}, R_{02} are their real parts, respectively.

According to (2), if $Z_{02}g_m >> 1$, $(1+Z_{02}g_m)$ can be simplified to $(Z_{02}g_m)$ and, hence, $|S_{21}|$ is independent of g_m, which results in a highly-linear power gain for the amplifier. Therefore, to achieve a good linearity, the value of g_m must be designed to be as large as possible. Moreover, according to (1) and (2), by selecting a small value for capacitor C_{in}, the gain of the PA can be increased.

Note that, as shown in (4), choosing a large g_m seems to result in a reduced $|S_{12}|$, and improved output-input isolation. However, $|S_{12}|$ is also directly proportional to C_{gs} which increases if a larger transistor is used to boost g_m. Therefore, increasing g_m by increasing the transistor's size does not improve $|S_{12}|$. Another important design consideration of this amplifier structure is the direct relation between $|S_{12}|$ and $|S_{21}|$. Using (2) and (4), it can be shown that $|S_{12}|$ can be written as a function of $|S_{21}|$ such that:

$$|S_{12}| = \frac{|S_{21}|}{g_m} \cdot C_{gs} \cdot \omega_{op} \tag{5}$$

Therefore, by increasing $|S_{21}|$, $|S_{12}|$ also increases. If the gain (i.e., $|S_{21}|$) is designed to be high, the amplifier can thus become unstable. This is an important trade-off of this PA structure which limits the maximum achievable gain. However, this amplifier is well-suited to applications such as BLE where lower output powers are required. Moreover, the reduction of C_{gs} in submicron technologies helps mitigate this stability gain trade-off for this PA structure.

Figs. 3 and 4 show the operation frequency and gain of the PA vs. key design parameters, valid for P_{in} below the 1-dB compression point. Simulation results were obtained through parametric simulations involving the design presented in section IV. Fig. 3 shows the operation frequency of the amplifier vs. (a) g_m, (b) L_{in}, and (c) C_{in}, obtained with the proposed equation (1), the simplified circuit level model in Fig. 2 and transistor level simulations. Fig. 4 shows the gain ($|S_{21}|$)

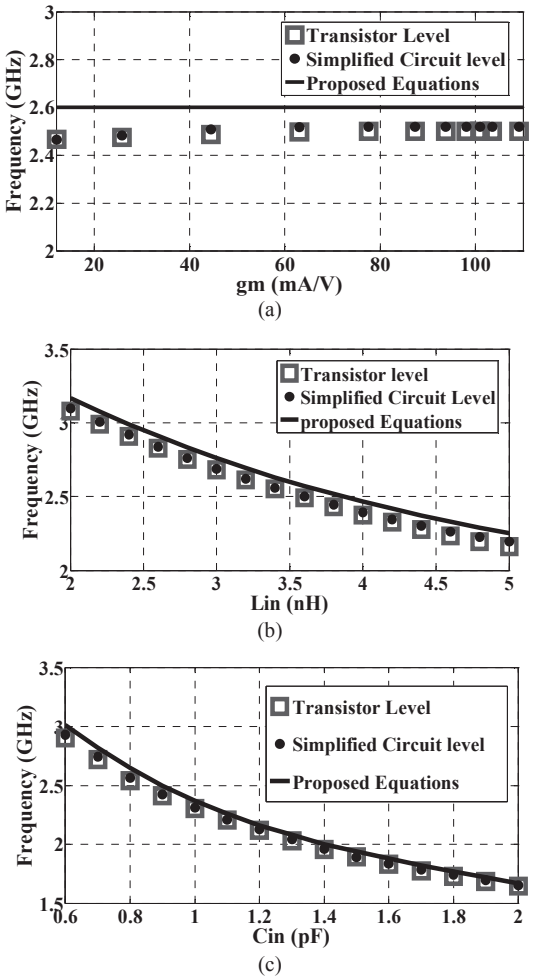

Fig. 3. Operation frequency versus: (a) g_m, (b) L_{in}, and (c) C_{in} using the proposed equation in (1), simplified circuit level model in Fig. 2 and transistor level simulations.

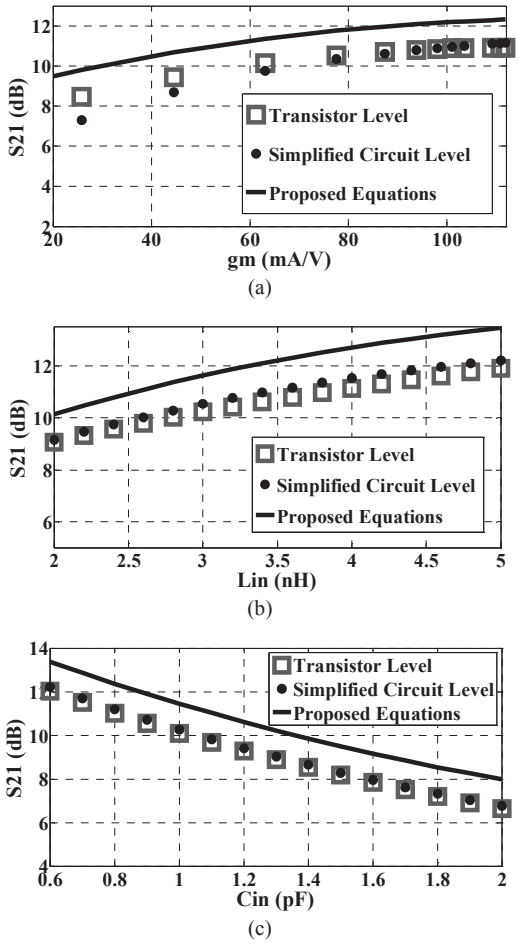

Fig. 4. S_{21} at the operation frequency versus **(a)** g_m, **(b)** L_{in}, and **(c)** C_{in} using the proposed equation in (2), simplified circuit level model in Fig. 2, and transistor level simulations.

at the operation frequency of the amplifier vs. (a) g_m, (b) L_{in}, and (c) C_{in}, using proposed equation (2), the simplified circuit level model in Fig. 2 and transistor level simulations. Figs. 3 and 4 show a very good agreement between the simulation results and the proposed analytical derivations. As such, these equations can be used to ease the design such a common-drain PA structure.

IV. Simulation Results

This section verifies the proposed *S*-parameter derivations by designing a common-drain PA using a 1.2 V supply in 0.13 µm CMOS technology. The inductor models used have a Q-factor of ~12. The PA is biased in class B operation. Here, a moderate gain of 8.5 dB was designed for at a center frequency of 2.45 GHz. In addition, a maximum output power of ~12 dBm was targeted such that the proposed circuit is suitable to short-range, low-power applications such as BLE. The stability of the amplifier was investigated through simulations of the stability factor, K_f, and S-parameter matrix determinant, $|\Delta|$. As shown in Fig. 5, this indicated unconditional stability as K_f was higher than 1.2 (i.e., larger than 1), and $|\Delta|$ (not shown in Fig. 5) was less than 1 in the frequency band of 0 -10 GHz.

Fig. 6 shows the simulated output power (P_{OUT}) and power added efficiency (PAE) versus the input power (P_{IN}) for the proposed PA. The simulation results show that the designed circuit delivers a maximum output power of more than 12 dBm with a gain of 8.5 dB and peak PAE of 47 %. The total power consumption is 3.6 mW from a 1.2V supply voltage. Moreover, its output power and PAE are, respectively, 9.7 dBm and 43 % at its input 1-dB compression point (P_{1dB}). This simulated performance makes the PA well-suited to low-power and short-range applications that require good linearity.

V. Discussion and Performance Comparison

The proposed PA structure has many advantages in comparison to other structures such as the common-source. As

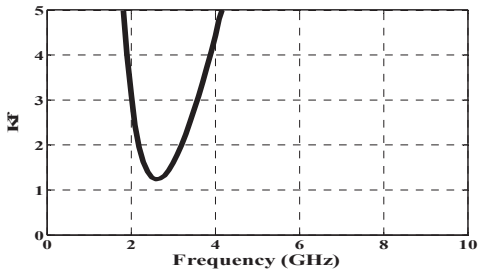

Fig. 5. Stability factor, K_f, for the designed common-drain amplifier.

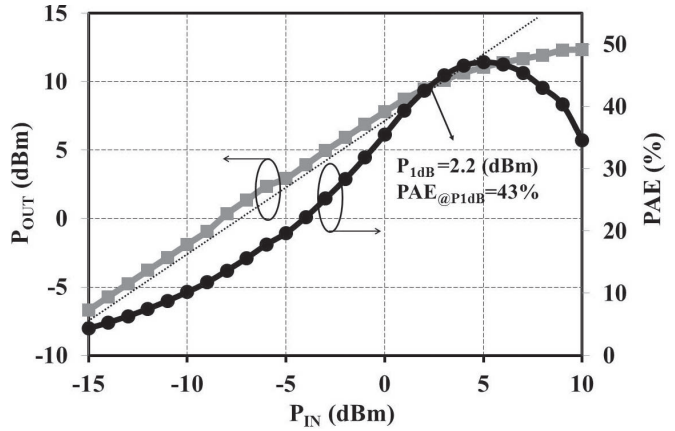

Fig. 6. Simulated output power, P_{OUT}, and power added efficiency, PAE, versus input power, P_{IN}.

the output is taken at the source, it is simple to adequately match the PA to the load by sizing and biasing the transistor such that its transconductance is appropriate.

As was previously described, because of the low dependency of the power gain to the transistor's transconductance, and the small variation of voltage across the gate-source capacitance, in comparison to a common-source for instance, this PA structure is more linear. Moreover, as the structure is scaled down in deeper submicron technologies, its design for stability should be eased because of the expected lower gate-source capacitance as shown in (5).

While a common-drain structure has been reported in [7-9], design considerations and trade-offs were not specifically discussed. Moreover, these where not designed for short-range applications such as BLE, in the 2.4 GHz band, where output powers below 15 dBm are suitable. Accordingly, these works utilized supply voltages of 2.5 V or above.

Table I summarizes the proposed PA and compares it with other works. In comparison to other common-drain structures (e.g., [7, 8]), the circuit achieves larger gain due to its enhanced stability, as shown in the previous equations. The PA compares favorably to other PA structures such as [11, 12] operating at a similar frequency and output power. Although biased in class B with relatively low-supply voltage, it still exhibits high linearity, and offers a good PAE in comparison to other works.

In addition, the proposed PA provides relatively large output power with reasonable power consumption. Limitations of this common-drain structure in comparison to the common-source structure are the restricted output power caused by power supply limiting and the relatively lower achievable gain. However, advantages of the proposed PA with regards to efficiency and linearity make it well-suited to low-power short-range applications.

VI. Conclusion

The *S*-parameter analysis of a common-drain PA for low-power short-range applications was presented, and a benchmark design was simulated in 0.13µm CMOS technology to verify the design considerations and trade-offs stemming from the analysis. With an appropriate input matching network, the PA provides moderate power gain, good stability, as well as a high linearity, and represents a suitable option for applications such as BLE.

TABLE I. PA Performance Summary and Comparison

	[7]*	[8]*	[11]	[12]	This work*
CMOS Tech. (nm)	90	GaN	130	180	130
Frequency (GHz)	2.55	10	1.92	2.40	2.45
PA Class	B	B	AB	AB	B
Supply Voltage (V)	2.5	-	1.2	1.8	1.2
DC Power Cons. (mW)	N/A	N/A	2.4	32.4	3.6
Output Power (dBm)	27.2	28	4	9	12.5
Power Gain (dB)	6.1	8	6	19	8.5
Input P_{1dB} (dBm)	18	20	-3.5	-13	2.2
PAE (%) @ P_{1dB}	40	49	22	10	43
Peak PAE (%)	43	54	26	16	47

*Simulated results.

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