

Fig. 3. Typical  $I_{DS}-V_{DS}$  curves of the fabricated FET.

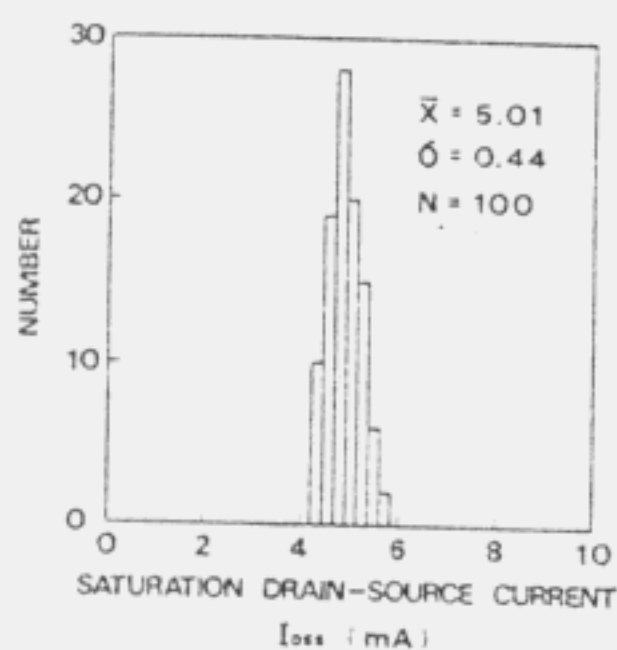


Fig. 4. Histogram of the saturation drain-source current of the experimental FET.  $L = 1.2 \mu\text{m}$ ,  $W = 20 \mu\text{m}$ .

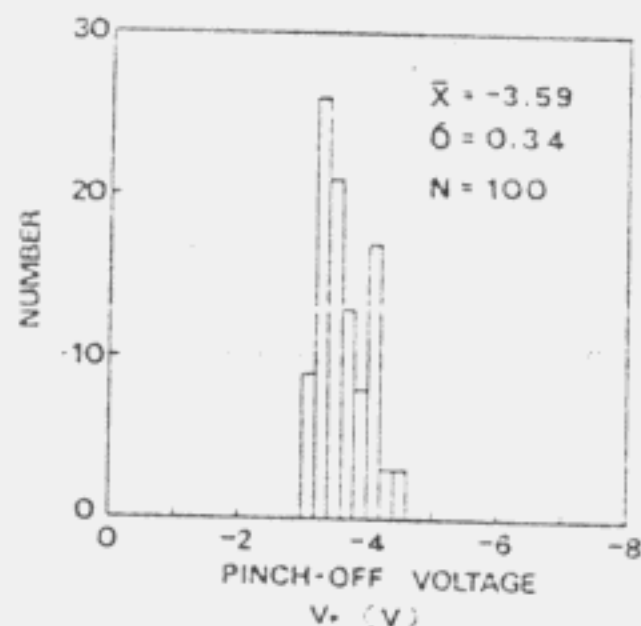


Fig. 5. Histogram of the pinch-off voltage of the experimental FET.  $L = 1.2 \mu\text{m}$ ,  $W = 20 \mu\text{m}$ .

new structure possesses the MBE as-grown uniformity of the active layer thickness even after the gate recesses are formed.

The source resistance of a present experimental device is  $56 \Omega$ , namely  $1.12 \Omega/\text{mm}$ , which is about 50 percent smaller than that of the conventional recessed gate MESFET fabricated with the same design. Because the  $\text{Ga}_{1-x}\text{Al}_x\text{As}$  layer remaining for the sources and drains is so heavily doped that the sheet resistance in the source-gate region as well as the source metal contact resistance has been effectively lowered. Further reduction of the source resistance will be obtainable by selective dry-etching of the  $\text{Ga}_{1-x}\text{Al}_x\text{As}$  layer, which can suppress the lateral etching.

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#### Low Field Mobility in GaAs Ion-Implanted FET's

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P. C. T. ROBERTS, AND M. J. HELIX

**Abstract**—We describe a new technique which allows one to deduce the mobility profiles under the gate of an ion-implanted GaAs MESFET. The technique is based on the measurements of the transconductance and the series resistance at very low drain-to-source voltages. The experimental results show that the mobility drops to about  $1000 \text{ cm}^2/\text{V}\cdot\text{s}$  at the channel interface from its maximum value of about  $2500 \text{ cm}^2/\text{V}\cdot\text{s}$ .

The parameters of GaAs MESFET's are strongly affected by low field mobility, especially in low pinchoff voltage devices [1].

In ion-implanted devices the low field mobility varies with the distance from the gate [2], [3]. *In situ* determination of the mobility profile is important for device modeling and improving MESFET fabrication procedures. Conventional methods [4]–[9] do not allow such *in situ* mobility profile measurements in  $1\text{-}\mu\text{m}$  ion-implanted GaAs FET's.

The technique proposed in this brief is based on the measurements of the transconductance and the series resistance at very low drain-to-source voltages when the Shockley model is applicable. It is a direct method which allows one to determine the mobility profile *in situ* for short gate devices.

We consider a case when the drain-to-source voltage  $V_{ds} \ll V_{Bi} - V_g$  where  $V_{Bi}$  is the built-in voltage and  $V_g$  is the voltage drop between the gate and the source side of the channel. Therefore the depletion region boundary is nearly parallel to the boundary between the active channel and the substrate. In effect, under such conditions a short-channel device behaves like a fat FET.

The equivalent circuit of the device between the source and drain may be then presented as a series connection of  $R_s$ ,  $R_{ch}$ , and  $R_d$ . Here  $R_s$ ,  $R_d$  are the source and drain series resistances, respectively. The reciprocal of the channel resistance  $R_{ch}$  for the channel with nonuniform mobility and doping profiles can

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be expressed as

$$R_{ch}^{-1} = \frac{qW}{L} \int_X^a \mu(X')N(X') dX' \quad (1)$$

where  $q$  is the electronic charge,  $a$  is the thickness of the channel,  $X$  is the depletion layer thickness, and  $L$  is the gate length. Again, (1) applies only at low  $V_{ds}$ .

For a given drain-to-source voltage  $V_{ds} = I_d (R_s + R_{ch} + R_d)$  and the device transconductance  $g_m$  is given by

$$g_m = \frac{\partial I_d}{\partial V_g} = - \frac{V_{ds}}{R_T^2} \frac{\partial R_{ch}}{\partial V_g} \quad (2)$$

where

$$R_T = R_s + R_{ch} + R_d$$

and

$$\frac{\partial R_{ch}}{\partial V_g} = R_{ch}^2 \left( \frac{qW\mu N}{L} \right) \frac{\partial X}{\partial V_g} \quad (3)$$

Here we may also neglect by the voltage drop across  $R_s$  compared to  $V_g$  so that  $V_g \approx V_{gs}$  (the voltage drop  $I_d R_s$  may, however, be comparable to  $V_{ds}$ ).

The relationship between  $V_g$  and depletion layer thickness is given by

$$V_g = V_{Bi} - \frac{q}{\epsilon} \int_0^X X' N(X') dX' \quad (4)$$

where  $V_{Bi} \approx 0.75$  V for our devices. From (4) we find

$$\frac{\partial X}{\partial V_g} = 1 / \left( \frac{\partial V_g}{\partial X} \right) = 1 / \left( - \frac{q}{\epsilon} \cdot N \cdot X \right) = - \frac{\epsilon}{qNX} \quad (5)$$

Substituting (5) into (3), we obtain

$$\frac{\partial R_{ch}}{\partial V_g} = - R_{ch}^2 \cdot \frac{W\mu\epsilon}{LX} \quad (6)$$

Combining (2) and (6), we get

$$\begin{aligned} g_m &= \frac{\partial I_d}{\partial V_g} = \frac{\epsilon W V_{ds}}{L} \cdot \frac{\mu}{X} \cdot \left( \frac{R_{ch}}{R_T} \right)^2 \\ &= \alpha \cdot \frac{\mu}{X} \cdot \left( \frac{R_{ch}}{R_T} \right)^2 \end{aligned} \quad (7)$$

where

$$\alpha = \frac{\epsilon \cdot W \cdot V_{ds}}{L}$$

In the case when  $R_s \ll R_{ch}$  and  $R_d \ll R_{ch}$  (which is typically not the case for 1- $\mu$ m GaAs MESFETs with nonself-aligned gates) (7) coincides with the equation for a fat FET derived by Pucel [8].

Our technique is based on the measurement of  $g_m(V_g)$  and  $R_T(V_g)$  ( $R_T = R_s + R_d + R_{ch}$ ), on the determination of  $R_s$  and  $R_d$  using the Hower method [12] or [10] (which we modified for the nonuniform doping profile) and on solving (7) numerically together with (4) for the given doping profile.

We start the determination of the series resistance using the Hower method, i.e., we plot the channel resistance  $R_T$  versus  $1/(1 - \sqrt{\eta})$  where  $\eta = (V_{Bi} - V_g)/(V_{Bi} - V_T)$  and crudely determine the sum of the series resistances, from the intercept

$$R_T = R_s^{(0)} + R_d^{(0)} + \frac{1}{G_0(1 - \sqrt{\eta})} \quad (8)$$

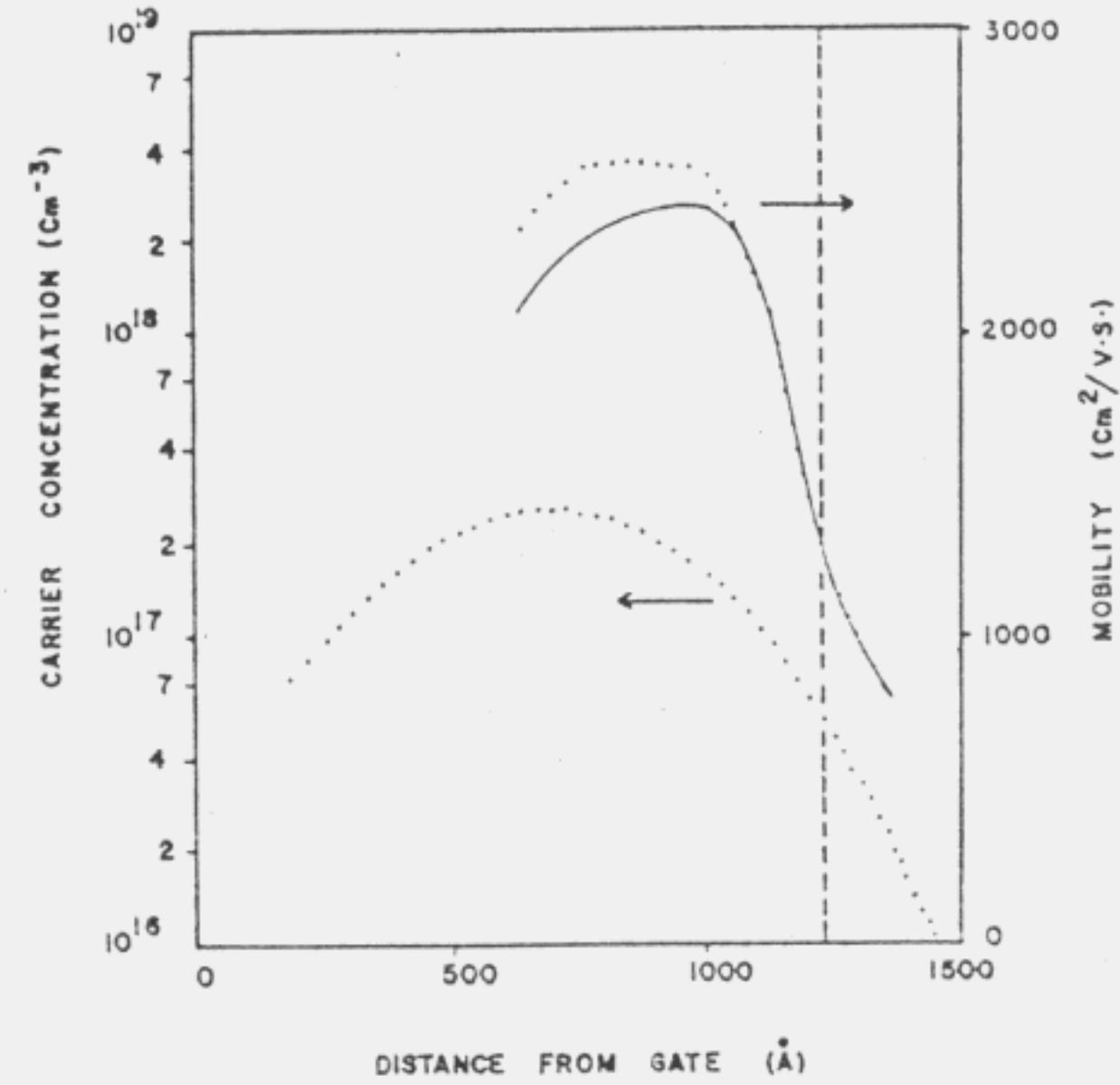


Fig. 1. Mobility and channel electron density versus distance from the gate for ion-implanted 1- $\mu$ m gate length MESFET. The dotted line is the zero approximation mobility profile and the solid line is the final mobility profile. In the region to the right of the vertical dashed line our technique does not apply because the Debye length becomes comparable with the characteristic length of the carrier profile variation.

The threshold voltage  $V_T$  is adjusted slightly to yield a linear plot.

The next step involves the calculation of the approximate mobility profile as described above. After that, we plot the channel resistance versus  $1/\sigma$  where,  $\sigma = L/(WR_{ch})$ . The intercept of this dependence yields  $R_s + R_d$  and the slope  $L/W$

$$R_T = R_s + R_d + \frac{L}{\sigma W} \quad (9)$$

Finally, we solve (4) and (7) again to determine the mobility profile using the new value of  $R_s + R_d$  and check for the convergence. Typically one iteration is all that is required for the accurate determination of the mobility profile.

GaAs MESFETs were fabricated using multiple selective ion implantation into undoped LEC semi-insulating GaAs. Selenium ions were implanted in the active channel and sulfur implantation was used for the  $n^+$  regions under the ohmic contacts. Ohmic contacts were made using AuGe/Ni metals and the Schottky barrier/first level metal was TiW/Au patterned using a dielectric assisted liftoff technique. The interlevel dielectric was plasma enhanced CVD silicon oxy-nitride, and the second level metal was TiW/Au patterned using ion-beam milling. The threshold voltage was close to -1 V. Doping profiles of the ion-implanted semiconductor can be fairly well approximated by Gaussian distribution [11]. The gate voltage  $V_g$  versus  $X$  given by (4) calculated for the doping profile shown in Fig. 1 is depicted in Fig. 2. This curve has been tabulated and used for the numerical solution of (7). The measured transconductance  $g_m$  versus  $V_g$  for  $V_{ds} = 20$  mV and  $V_{ds} = 40$  mV is shown in Fig. 3(a). As can be shown from (7) the value of  $(1/g_m) \cdot (\partial g_m / \partial V_g)$  is independent for  $V_{ds}$  for low values of  $V_{ds}$ . Indeed, the difference in this product measured at 20 and 40 mV was less than 3 percent.

The channel current  $I_d$  measured at low  $V_{ds}$  is shown in Fig. 3(b) as a function of the gate bias. From this measurement the total resistance was obtained as  $R_T = V_{ds}/I_d$ . The source and drain resistance  $R_s$  and  $R_d$  are determined as suggested in [10] or [12]. Plotting  $R_T$  as a function of  $(1 - \sqrt{\eta})^{-1}$  (see

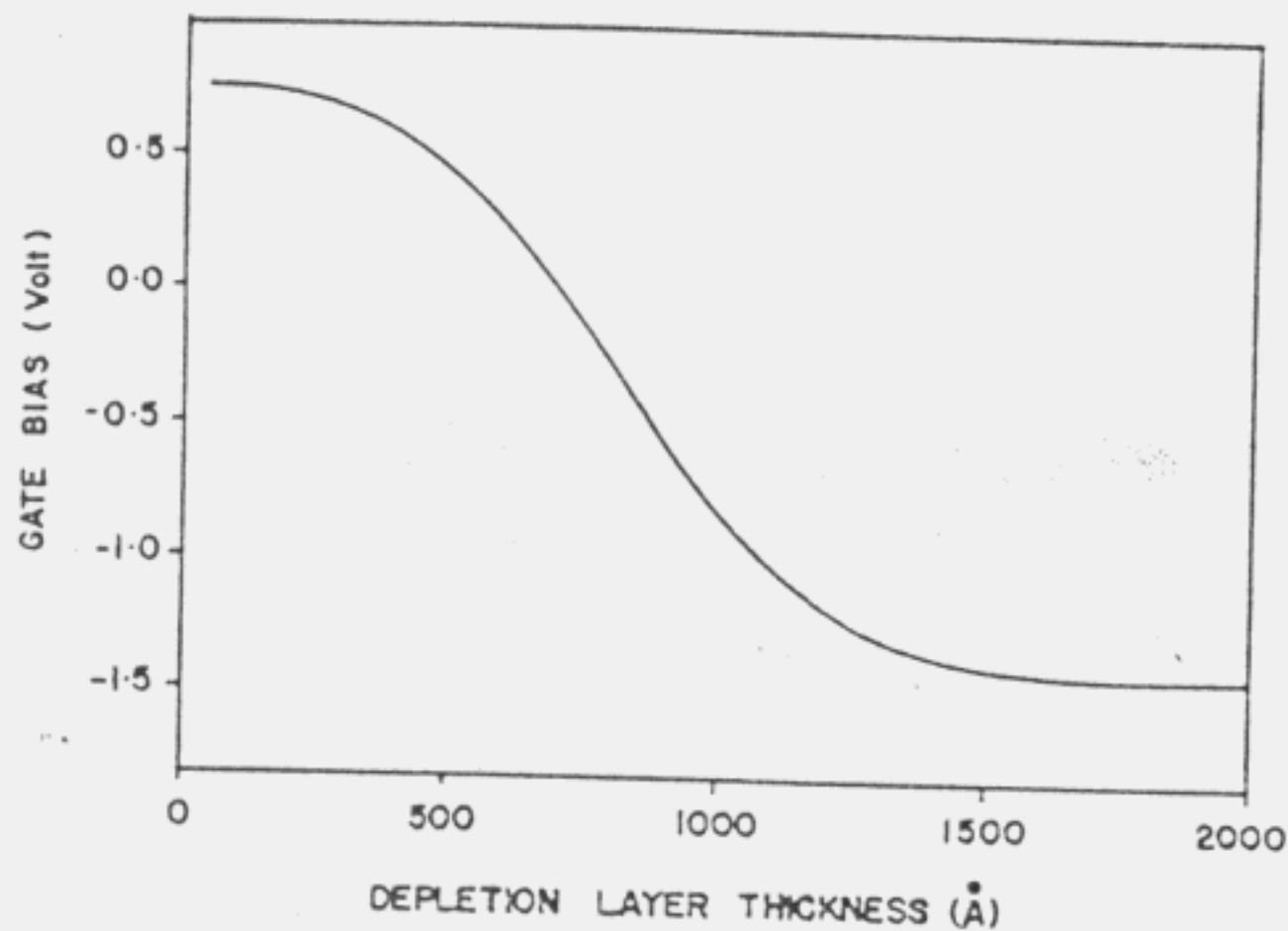
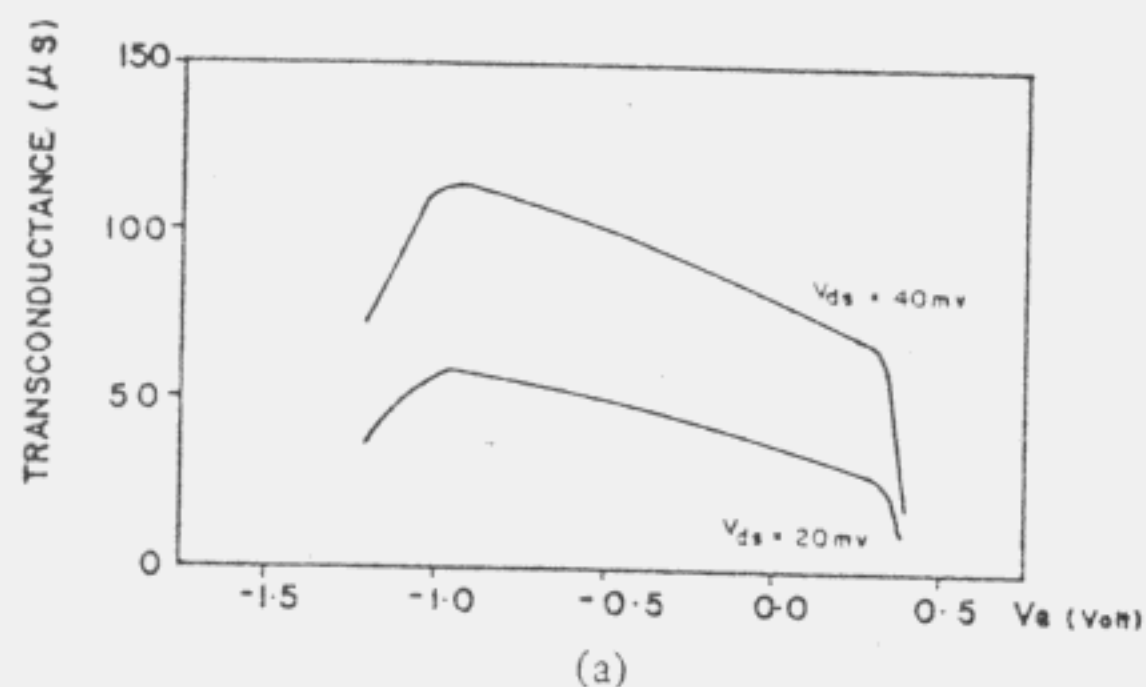
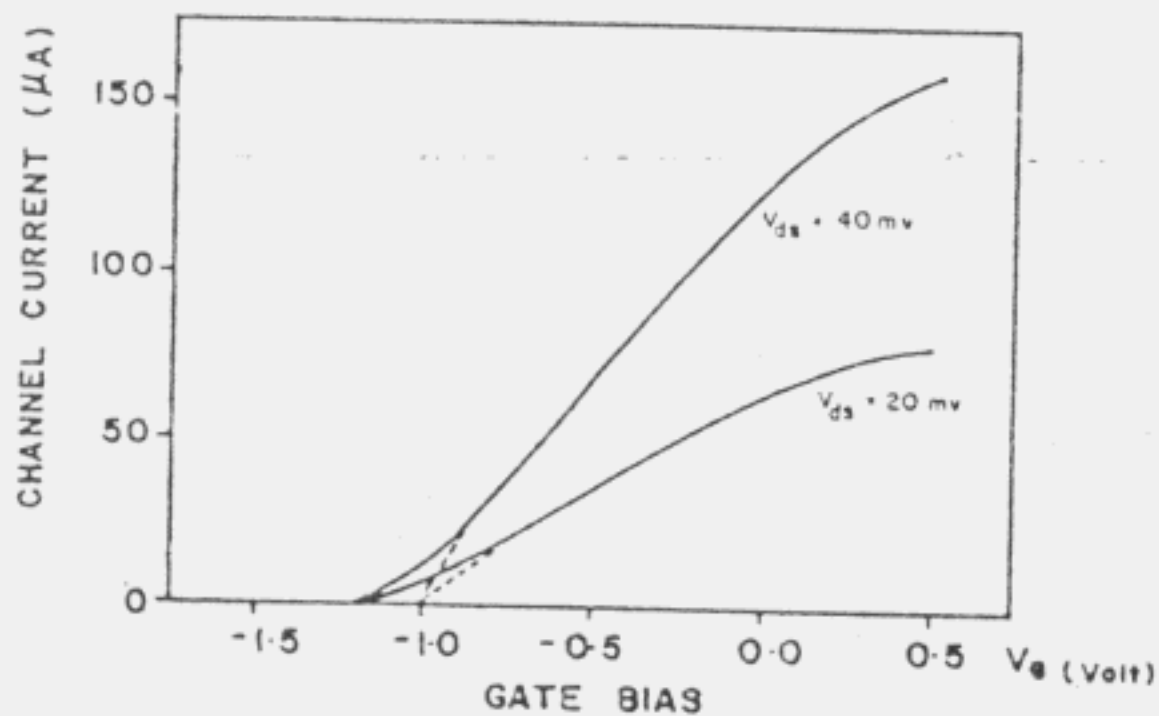


Fig. 2. The gate bias versus the depletion layer thickness (calculated from (4)).



(a)



(b)

Fig. 3. The transconductance (a) and the channel current (b) as functions of gate bias for low  $V_{ds}$  for 20- $\mu\text{m}$  wide devices.

(8)) and slightly adjusting  $V_T$  we obtain a linear plot for the data points. This yields both the value of  $R_s + R_d$  as the intercept and a more accurate value for  $V_T$  than the value obtained from the measurements of the FET characteristics at large  $V_{ds}$  ( $V_T = -0.995$  V).

Then we solve (7) together with (4). The resulting mobility profile is shown in Fig. 1 as a dotted line. Plotting  $R_T$  versus  $1/\sigma$  (see (9)) yields a more accurate value of  $R_s + R_d = 110 \Omega$  (as compared with an approximate value of  $120 \Omega$ ) (see Fig. 4) and the value of  $L/W = 0.066$  (the slope) in good agreement with the directly measured value  $L/W = 0.065$  (this value was determined optically).

Finally the mobility profile is recalculated again using the accurate value of  $R_s + R_d$ . The final profile is also shown in Fig. 1 as solid line. As can be seen from the figure the first iteration is not too far off from the zeroth approximation mobility curve. Our results indicate that the mobility may be quite low especially far from the gate. It is considerably

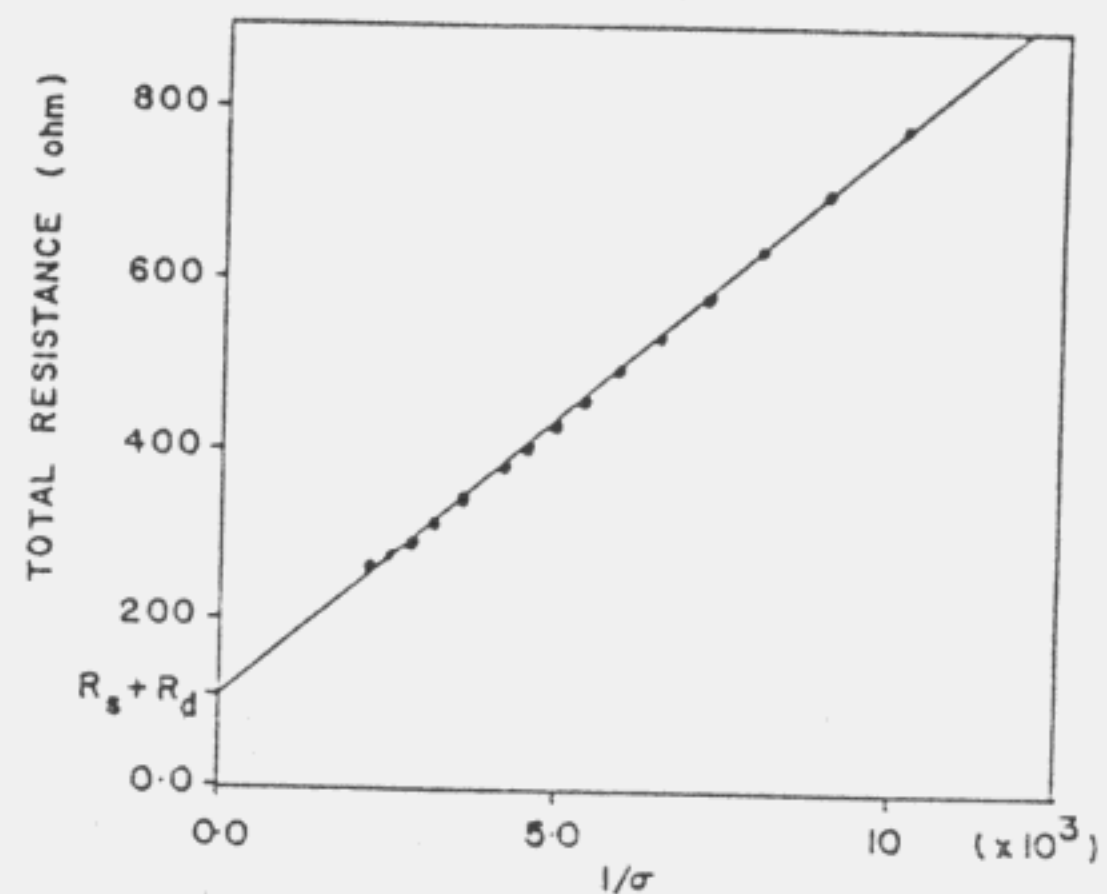


Fig. 4. Determination of  $R_s$  and  $R_d$ . The total resistance is plotted as a function of  $1/\sigma$  where  $\sigma = \int_{-\infty}^{\infty} \mu(X')N(X')dX'$ . This yields  $R_s + R_d$  ( $110 \Omega$ ) as the intercept and  $L/W$  ( $0.066$ ) as the slope.

smaller than the measured Hall mobility for the same wafers which is of the order of  $3000\text{--}4000 \text{ cm}^2/\text{V}\cdot\text{s}$ . A similar apparent decrease of the low field mobility in short devices has been noticed by Fukui [10]. The reasons for this decrease may be related to the device processing and are not clear at the present time. The nonuniform mobility profile has to be taken into account in modeling and characterization of ion-implanted GaAs devices, especially low pinchoff voltage devices where the low field mobility plays an important role in determining the device transconductance [1].

We should point out that the theory used in this brief may become inaccurate when the electron concentration drops below  $5 \cdot 10^{16} \text{ cm}^{-3}$  or so (i.e., at the distance farther from the gate than approximately  $1200 \text{ \AA}$ ) because in this region the Debye radius ( $190 \text{ \AA}$  at  $300 \text{ K}$ ) becomes comparable with the characteristic length of the carrier profile variation. A more elaborate analysis should be used in this region, as suggested in [13].

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