Low Field Vertical Charge Transport in the Channel and Buffer Layers of GaN-on-Si High Electron Mobility Transistors

Filip Wach, Michael J. Uren, *Senior Member IEEE*, Benoit Bakeroot, Ming Zhao, Stefaan Decoutere, Martin Kuball, *Fellow IEEE*

Abstract— **Substrate ramps and stepped stress transient measurements are applied to study vertical charge transport mechanisms in GaN-on-Si power HEMTs. By choosing appropriate bias points for substrate stress it is possible to single out the dominant charge transport mechanism: at low negative biases transport through carbon-doped GaN manifests itself in negative transients with apparent activation energy (E_A) = 0.29 eV, while at larger negative voltages transport through unintentionally doped GaN is characterized by positive transients (E_A = 0.38 eV). We present experimental evidence for 3D variable range hopping taking place in C-doped GaN and 1D hopping along the dislocations in unintentionally doped GaN. By investigating transients obtained from bidirectional voltage steps of 10 V potential difference in the range 0 to -140 V, we observe that hopping transport through dislocations shows non-Ohmic behavior at low substrate biases, which manifests itself in a time constant τ strongly dependent on bias. We propose that this can be explained by the existence of a diode junction between the dislocation core and the 2D electron gas (2DEG).**

Index Terms—**AlGaN/GaN HEMT, vertical leakage, vertical charge transport, dislocations, activation barrier.**

I. INTRODUCTION

GaN-on-Si High-Electron-Mobility Transistors (HEMTs) offer dramatic improvements in efficiency and power module volume [1], [2]. However, buffer trapping related dynamic R_{ON} still poses problems for full utilization.

Fig. 1a shows a schematic of an ungated HEMT and its basic epitaxial structure. At the vertical fields experienced in normal operation, buffer trapping is mainly dominated by the processes taking place in the unintentionally doped (UID) and carbon doped GaN (GaN:C) layers. However, separation of the individual contributions of each layer is not trivial and the previous attempt described in [3] has large error bars.

To suppress dynamic R_{ON}, Uren et al. [4] demonstrated the necessity for vertical leakage paths via a trap assisted band-to-band process across the UID GaN and extending into the resistive GaN:C layer. Measurements on vertical pn diodes in GaN LEDs have shown that the leakage is primarily associated with screw dislocations, and for vertical power pn diodes this has been shown to be consistent with hopping conduction [5].

The impact of leakage on dynamic R_{ON} in GaN-on-Si HEMTs is discussed in [6].
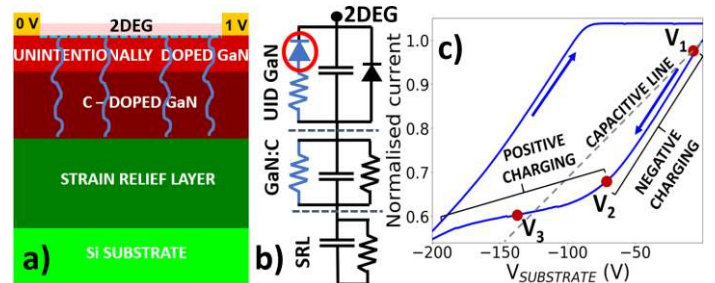

Figure 1. a) Diagram of the ungated HEMT used in this study with dislocations highlighted in blue. b) 1D lumped element diagram of the HEMT; proposed new diode barrier circled red; dislocations extending from GaN:C to the 2DEG have been shown in blue; c) substrate ramp experiment (ramp rate 1 V/s); the areas where negative and positive charging of the buffer takes place have been indicated on the diagram.

In the case of GaN:C, vertical charge transport involving C_N acceptors and activation of holes to the valence band (VB) can take place with a predicted and experimentally observed activation energy $E_A \sim 0.9$ eV [7], [8]. However, it has been shown that at carbon concentrations $\geq 10^{19}$ cm^{-3} vertical charge transport is dominated by defect band (DB) conduction with an apparent E_A that is temperature dependent and can vary between 0.05 and 0.8 eV [9].

In this letter we investigate vertical charge transport within a state-of-the-art 200mm GaN-on-Si HEMT epitaxial stack in the low-field regime most relevant to dynamic R_{ON}. We propose a new method for investigation of the vertical charge transport process in GaN layers and show that the transport is consistent with 3D variable range hopping in a DB in the carbon doped layer, and 1D hopping along dislocations in the critical undoped channel layer. The key novelty is the recognition that the leakage paths through the UID GaN are non-Ohmic and we propose that this can be explained by the presence of a previously unrecognised diode barrier between the dislocation core and the 2DEG.

II. EXPERIMENTAL DETAILS

This study was performed on ungated Ohmic structures consisting of a GaN–on–Si epitaxial architecture with >1 Ω.cm

p-type Si substrate, AlN/AlGaN superlattice strain relief layer (SRL), 1 µm carbon doped GaN buffer with concentration ~2×10^{19} cm^{-3} (measured by secondary ion mass spectrometry), 300 nm UID GaN channel, and AlGaN barrier (Fig. 1a).

Substrate ramps were performed to study charge transport through the stack. This technique involves applying a small bias difference to the top contacts to monitor the 2DEG conductivity, while slowly ramping substrate bias, acting as a back-gate. The changes in conductivity of the 2DEG reflect vertical electric fields in the buffer, whilst being insensitive to surface effects [3], [10]. This technique is most sensitive to vertical charge transport in the upper GaN layers due to their proximity to the 2DEG.

Substrate stress transient measurements were conducted, in which the substrate bias is switched rapidly (~10 µs) between two specific bias points (V_i, V_f). Time dependence of the 2DEG conductivity was measured and time constants (τ) were extracted using multiexponential fitting [11]. If the initial voltage $|V_i|$ was greater than 0V, then the substrate was biased for 1000 s at the voltage V_i, followed by a step to V_f after which a transient was recorded. The measurement timeline is shown in Fig. 2.
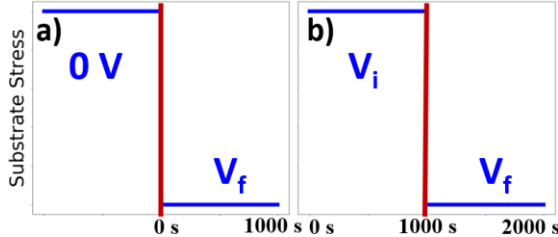

Figure 2: Measurement timeline showing: a) substrate transients – voltage is switched rapidly from 0V to a chosen value (V_f) then current measured for 1000 s; b) stepped substrate transients – the substrate is biased for 1000 s at the initial voltage V_i, then the voltage is rapidly stepped up (or down) to a value V_f and measured for 1000 s.

III. RESULT

Substrate ramps were performed on devices across the wafer and showed negligible device to device variation. There was also no significant variation for devices with different contact spacing indicating uniform vertical conductivity across the entire length of the device as described in [5]. Likewise, active area of the devices had little effect on the substrate ramp. All of this implies the transport through the stack can be approximated as being 1D and there are no significant leakage paths under the contacts or internal lateral leakage paths associated with 2D hole gases (2DHGs) or 2DEGs at heterojunctions [12][13].

Fig. 1c shows a substrate ramp for a contact spacing of 8 µm. Comparison with an ideal capacitive response (i.e. the entire epitaxy acting as a dielectric – any response below the line requires negative charge and above the line positive stored charge) reveals negative charging at V_1 and positive charging at V_3. These regimes were elucidated by substrate conductance transients performed at these bias points and show two distinct regimes: negative going transient with E_A = 0.29 eV and time constant τ_1 at V_1 transitioning to a positive going transient (E_A = 0.38 eV, τ_2) at V_3. Fig.3a shows an intermediate regime at V_2 where both are visible.

Fig. 3b shows the data from stepped stress transients for a range of (V_i, V_f) bias points. The time constant for negative transient (τ_1) is only weakly voltage dependent, while the positive transient shows a strong change in time constant (τ_2) with applied stress. For bidirectional voltage steps (in which the substrate stress transients are performed by first stepping the voltage from V_i to V_f and vice versa – see Fig. 3c), there is a strong asymmetry in τ_2, but not τ_1, at low voltage, with the ratio of τ_2 for reverse and forward voltage steps (τ'_2/τ_2 ratio) tending to unity at higher voltage as is shown in Fig. 3d.
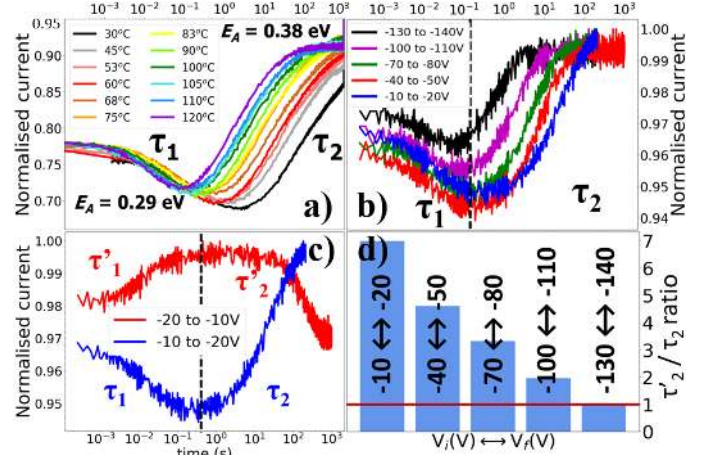

Figure 3: a) Temperature dependence of normalized drain current transients for V_i=0V, V_f=V_2 = -70 V. b) Transients for a range of (V_i, V_f) bias points of constant potential difference. c) Transients for bidirectional steps (V_i=-10↔V_f=-20) – τ' indicates equivalent reverse process to τ. d) UID GaN – ratio of time constants (τ'_2/τ_2) for bidirectional steps at different voltages.

Temperature and field dependence of τ_1 and τ_2 were measured and are plotted in Fig. 4. The dependence of τ_1 and τ_2 on substrate voltage can be approximated as $log(\tau^{-1}) \propto V_{SUB}$ for most of the range of τ_2 and the entire voltage range of τ_1 (Fig. 4b) with a much stronger dependence for τ_2.
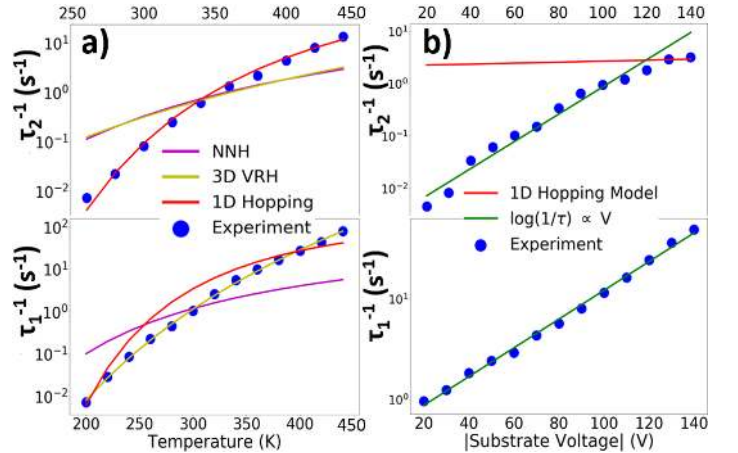

Figure 4. Inverse time constant as a function of a) temperature (at -10 V and −140 V for τ_1 and τ_2 respectively corresponding to the voltages where the transport for each is Ohmic) and b) field (at 300 and 380K for τ_1 and τ_2 respectively) with different theoretical transport mechanisms fitted to data. Top panel shows the data for UID GaN (τ_2); bottom panel represents the data for GaN:C (τ_1). Fitted lines were calculated from the equations described in Table 1 (NNH and 3D VRH stand for nearest neighbor and 3D variable range hopping respectively).

IV. DISCUSSION

The location of the charges responsible for the transient responses are discussed in [3][4][6]. It is important to note that significant charge only resides in narrow depletion regions at

the top and bottom of the heavily doped GaN:C layer. Charge redistribution and current flow within the GaN:C layer first leads to the negative going transient (τ_1) as a dipole forms under the action of the applied field with negative charge at the top and positive at the bottom. This is followed by band-to-band leakage from the 2DEG through the UID GaN which neutralizes the negatively charged depletion region at the top of the GaN:C and leads to the positive transient (τ_2). The impact of these processes on the shapes of substrate ramps and dynamic R_{ON} has been described in more detail in [6].

TABLE I
HOPPING CONDUCTIVITY MODELS

1D Hopping Conduction	$\tau^{-1} = \dfrac{v_0 N_{TD} e}{\varepsilon E}\left[1 + \dfrac{2exp\left(\frac{eE_\sigma}{kT}\right)^2}{exp\left(\frac{ebE}{kT}\right)-1}\right]^{-1}$
Variable Range Hopping 3D	$\tau^{-1} = A_{VRH}\exp\left(-\left[\frac{T_0}{T}\right]^{1/4}\right)$
Nearest Neighbour Hopping	$\tau^{-1} = A_{NNH}\exp\left(-\frac{E_A}{kT}\right)$

Time constant (τ) dependence on temperature (T) for charge transport mechanisms (fitting parameters give in brackets). A denotes pre-exponential factors (with $A_{VRH} = 1.68\times10^{20}$ s^{-1} and $A_{NNH} = 163.2$ s^{-1}), while T_0 (1.4×10^9 K) is the Mott Temperature. N_{TD} (6×10^8 cm^{-2}) denotes dislocation density, e electron charge, E electric field, b (0.1nm) trap separation along the dislocation, v_0 (1 GHz) is the hopping frequency and E_σ (60 meV) is the trap characteristic energy distribution [14], [15], [16], [17].

Temperature and field dependence of vertical leakage was compared with the most likely theoretical models (see Table I). The constants of proportionality were extracted from the line of best fit as dictated by each model. For the GaN:C layer (τ_1) the measured $E_A = 0.29$ eV indicates activation of holes to the VB from C_N acceptors was not the dominant process, as the signature E_A would be ~0.9 eV. The fit in Fig, 4c suggests that the charge redistribution within GaN:C is best described by 3D variable range hopping. This is consistent with [9] and defect band conduction; it might suggest primarily bulk hopping rather than dislocation transport which would be expected to be 1D in nature. The results obtained from stepped and bidirectional stress transients (Fig. 3b,c) show negligible change in time constants for small forward and reverse voltage steps, however there is clearly a gradual, but nevertheless significant, field dependence apparent in Fig. 4b which is not expected for hopping [16].

For the UID GaN layer (τ_2), the fits for the temperature dependence in Fig. 4a (which were measured at -140V where the asymmetry apparent in Fig. 3d was insignificant), are consistent with 1D nearest neighbor hopping along dislocations. However, at low fields there is a strong asymmetry in conduction (Fig, 3c,d) implying a very strongly non-Ohmic conduction process. 1D hopping is an Ohmic process (i.e. τ is expected to be field independent as shown in Fig. 4b) so cannot explain the strong dependence on field found in Fig, 4b, and especially not the dependence on voltage step sign at low bias.

A plausible origin for the non-Ohmic conduction is shown in Fig, 5. Fig. 5a shows a simulated vertical band diagram across the UID GaN and the upper part of the GaN:C buffer layer 10 s after the stress was applied. Charge redistribution within the GaN:C (τ_1 in Fig. 3a) has resulted in almost complete

suppression of the electric field across this layer. Charge transport across the UID GaN is then expected to be associated with the dislocations extending from the buffer to the 2DEG (as indicated by the arrows in Fig. 5a). However, where the dislocation passes through the 2DEG, there must be a depletion region surrounding the core if E_F is pinned to the DB at its core [18]. This results in a Schottky barrier as shown in Fig. 5b, which is in series with the 1D conduction along the dislocation (see diode in lumped element diagram in Fig. 1b; we believe that it is unlikely there is a significant diode barrier between the dislocation and GaN:C due to the p-type nature of the GaN and the band bending in the dislocation core of at least 2.5 eV [18]). The Schottky barrier is reverse biased for applied negative substrate bias, but increasing field will lead to current flow through the barrier by processes such as trap assisted tunneling or Fowler-Nordheim tunneling. Hence its differential resistance will fall with increasing negative bias until the leakage behavior is dominated by the Ohmic conduction along the dislocation. This provides an explanation for the strongly asymmetric behavior seen in Fig. 3d and at least partially for the strong electric field dependence. Interestingly and in support of this model, similar discrepancy between experimental data and the 1D hopping model at low voltages was observed by Moroz et al. in GaN p-n diodes, however no explanation was offered [5].
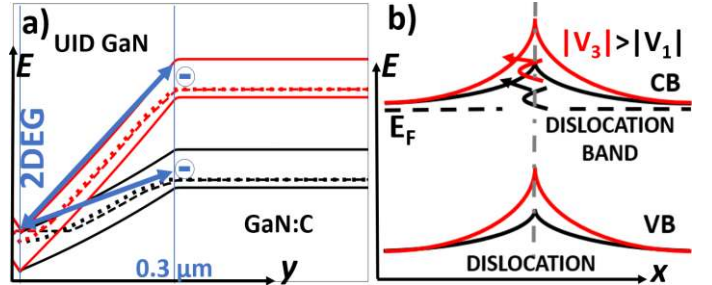

Figure 5: a) Simulated vertical band diagram of the device after 10 s of substrate stress for V_3 (red) and V_1 (black). Blue arrows indicate charge transport along the dislocations towards the 2DEG; dashed and dotted lines indicate position of the electron and hole quasi Fermi levels respectively. b) Schematic horizontal band diagram along the 2DEG – at higher substrate voltages electrons can enter the 2DEG more easily as the field thins the depletion region around the dislocation core. y and x axes indicate device depth and length.

Finally, we note that strong non-linearity can occur in the carbon doped GaN system under some circumstances. Negative differential resistance in the IV characteristics of GaN:C to Si doped GaN diodes [19], and relaxation oscillation behavior in substrate ramp experiments [20], suggest that the transport cannot always be described by band edge transport.

V. CONCLUSION

In summary, temperature and field dependent measurements of GaN-on-Si HEMTs were performed to investigate transport mechanisms through the epitaxy at fields significantly below breakdown. 1D hopping was identified as the dominant charge transport mechanism through UID GaN and was consistent with there being a series connected Schottky junction restricting charges from entering the 2DEG. Transport through GaN:C appears to involve 3D hopping conductivity likely via a defect band.

REFERENCES

[1] H. Amano, Y. Baines, E. Beam, M. Borga, T. Bouchet, P. R. Chalker, M. Charles, K. J. Chen, N. Chowdhury, R. Chu, C. De Santi, "The 2018 GaN power electronics roadmap." Journal of Physics D: Applied Physics vol. 51, no. 16, p.163001, Mar. 2018. DOI: 10.1088/1361-6463/aaaf9d

[2] K. J. Chen, O. Häberlen, A. Lidow, C. l. Tsai, T. Ueda, Y. Uemoto, and Y. Wu, "GaN-on-Si Power Technology: Devices and Applications," IEEE Transactions on Electron Devices, vol. 64, pp. 779-795, Feb. 2017. DOI: 10.1109/TED.2017.2657579

[3] M. J. Uren, M. Cäsar, M. A. Gajda, and M. Kuball, "Buffer Transport Mechanisms in Intentionally Carbon Doped GaN Heterojunction Field Effect Transistors " Applied Physics Letters, vol. 104, p. 263505, June 2014. DOI: 10.1063/1.4885695

[4] M. J. Uren, M. Silvestri, M. Cäsar, G. A. M. Hurkx, J. A. Croon, J. Šonský, M. Kuball, "Intentionally carbon-doped AlGaN/GaN HEMTs: Necessity for vertical leakage paths." IEEE Electron Device Letters vol. 35, no. 3, pp. 327-329, Jan. 2014. DOI: 10.1109/led.2013.2297626

[5] V. Moroz, H. Y. Wong, M. Choi, N. Braga, R. V. Mickevicius, Y. Zhang, and T. Palacios, "The impact of defects on GaN device behavior: Modeling dislocations, traps, and pits." ECS Journal of Solid State Science and Technology vol. 5, no. 4, pp. 3142-3148, Jan. 2016. DOI: 10.1149/2.0211604jss

[6] M. J. Uren, S. Karboyan, I. Chatterjee, A. Pooth, P. Moens, A. Banerjee, M. Kuball, ""Leaky Dielectric" Model for the Suppression of Dynamic RON in Carbon-Doped AlGaN/GaN HEMTs." IEEE Transactions on Electron Devices vol. 64, no. 7, pp. 2826-2834, June 2017. DOI: 10.1109/ted.2017.2706090

[7] J. L. Lyons, A. Janotti, and C. G. Van de Walle, "Carbon impurities and the yellow luminescence in GaN." Applied Physics Letters vol. 97, no. 15, p. 152108, Oct. 2010. DOI: 10.1063/1.3492841

[8] A. Y. Polyakov, and L. In-Hwan, "Deep traps in GaN-based structures as affecting the performance of GaN devices." Materials Science and Engineering: R: Reports vol. 94, pp. 1-56, Aug. 2015. DOI: 10.1016/j.mser.2015.05.001

[9] C. Koller, G. Pobegen, C. Ostermaier, and D. Pogany, "Effect of Carbon Doping on Charging/Discharging Dynamics and Leakage Behavior of Carbon-Doped GaN." IEEE Transactions on Electron Devices vol. 65, no. 12, pp. 5314-5321, Oct. 2018. DOI: 10.1109/ted.2018.2872552

[10] S. Yang, C. H. Zhou, Q. M. Jiang, J. B. Lu, B. L. Huang, and K. J. Chen, "Investigation of buffer traps in AlGaN/GaN-on-Si devices by thermally stimulated current spectroscopy and back-gating measurement," Applied Physics Letters, vol. 104, p.013504, Jan. 2014. DOI: 10.1063/1.4861116.

[11] D. Bisi, M. Meneghini, C. De Santi, A. Chini, M. Dammann, P. Brueckner, M. Mikulla, G. Meneghesso, and E. Zanoni, "Deep-level characterization in GaN HEMTs-Part I: Advantages and limitations of drain current transient measurements." IEEE Transactions on Electron Devices vol. 60, no. 10, pp. 3166-3175, Oct. 2013. DOI: 10.1109/ted.2013.2279021

[12] M .Singh, S. Karboyan, M. J. Uren, K. B. Lee, Z. Zaidi, P. A. Houston, and M. Kuball "Lateral charge spreading and device-to-device coupling in C-doped AlGaN/GaN-on-Si wafers." Microelectronics Reliability vol. 95, pp. 81-86, April 2019. DOI: 10.1016/j.microrel.2019.02.012

[13] I. Chatterjee, M. J. Uren, S. Karboyan, A. Pooth, P. Moens, A. Banerjee, and M. Kuball, "Lateral Charge Transport in the Carbon-Doped Buffer in AlGaN/GaN-on-Si HEMTs," IEEE Transactions on Electron Devices, vol. 64, pp. 977-983, March 2017. DOI: 10.1109/TED.2016.2645279

[14] N. F. Mott and E. A. Davis, Electronic Processes in Non-Crystalline Materials. Oxford, U.K.: Oxford Univ. Press, 2018.

[15] Mott, Nevill. Metal-insulator transitions. CRC Press, 2004.

[16] H. Cordes, S. D. Baranovskii, K. Kohary, P. Thomas, S. Yamasaki, F. Hensel, and J. H. Wendorff, "One-dimensional hopping transport in disordered organic solids. I. Analytic calculations." Physical Review B vol. 63, no. 9, p. 094201, Jan. 2001. DOI: 10.1103/physrevb.63.094201

[17] S. Dalcanale, M. J. Uren, M. Kuball "TCAD Simulation of Leakage Through Threading Dislocations in GaN-based pn-diodes" Simulation Standard 2018.

[18] D. Cherns and C. G. Jiao, "Electron holography studies of the charge on dislocations in GaN," Physical Review Letters, vol. 87, p. 205504, Nov 2001. DOI: 205504 10.1103/PhysRevLett.87.205504

[19] C. Koller, G. Pobegen, C. Ostermaier, G. Hecke, R. Neumann, M. Holzbauer, G. Strasser, and D. Pogany, "Trap-Related Breakdown and Filamentary Conduction in Carbon Doped GaN," Physica Status Solidi (b), vol. 256, no. 6, p. 1800527, Feb. 2019. DOI: 10.1002/pssb.201800527

[20] M. Singh, S. Karboyan, M. J. Uren, K. B. Lee, Z. Zaidi, P. A. Houston, and M. Kuball, "Lateral charge spreading and device-to-device coupling in C-doped AlGaN/GaN-on-Si wafers," Microelectronics Reliability, vol. 95, pp. 81-86, April 2019. DOI: 10.1016/j.microrel.2019.02.012