KTH Information and
Communication Technology

Low-frequency noise characterization, evaluation and modeling of advanced Si- and SiGe-based CMOS transistors

Doctoral Thesis

by

Martin von Haartman

Stockholm, Sweden
2006

Laboratory of Solid State Devices (SSD),
School of Information and Communication Technology (ICT),
Royal Institute of Technology (KTH)

Low-frequency noise characterization, evaluation and modeling of advanced Si- and SiGe-based CMOS transistors

A dissertation submitted to Kungliga Tekniska Högskolan (KTH), Stockholm, Sweden, in partial fulfillment of the requirements for the degree of Teknologie Doktor (Doctor of Philosophy)

ISRN KTH/EKT/FR-2006/2-SE

ISSN 1650-8599

TRITA-EKT

Forskningsrapport 2006:2

This thesis is available in electronic version at: http://media.lib.kth.se

Printed by Universitetsservice US-AB, Stockholm, 2006.

To Anne

von Haartman, Martin: Low-frequency noise characterization, evaluation and modeling of advanced Si- and SiGe-based CMOS transistors, ISRN KTH/EKT/FR-2006/2-SE, KTH, Royal Institute of Technology, School of Information and Communication Technology, Stockholm, 2006.

Abstract

A wide variety of novel complementary-metal-oxide-semiconductor (CMOS) devices that are strong contenders for future high-speed and low-noise RF circuits have been evaluated by means of static electrical measurements and low-frequency noise characterizations in this thesis. These novel field-effect transistors (FETs) include (i) compressively strained SiGe channel pMOSFETs, (ii) tensile strained Si nMOSFETs, (iii) MOSFETs with high-k gate dielectrics, (iv) metal gate and (v) silicon-on-insulator (SOI) devices. The low-frequency noise was comprehensively characterized for different types of operating conditions where the gate and bulk terminal voltages were varied. Detailed studies were made of the relationship between the 1/*f* noise and the device architecture, strain, device geometry, location of the conduction path, surface cleaning, gate oxide charges and traps, water vapour annealing, carrier mobility and other technological factors. The locations of the dominant noise sources as well as their physical mechanisms were investigated. Model parameters and physical properties were extracted and compared. Several important new insights and refinements of the existing 1/*f* noise theories and models were also suggested and analyzed. The continuing trend of miniaturizing device sizes and building devices with more advanced architectures and complex materials can lead to escalating 1/*f* noise levels, which degrades the signal-to-noise (SNR) ratio in electronic circuits. For example, the 1/*f* noise of some critical transistors in a radio receiver may ultimately limit the information capacity of the communication system. Therefore, analyzing electronic devices in order to control and find ways to diminish the 1/*f* noise is a very important and challenging research subject.

We present compelling evidence that the 1/*f* noise is affected by the distance of the conduction channel from the gate oxide/semiconductor substrate interface, or alternatively the vertical electric field pushing the carriers towards the gate oxide. The location of the conduction channel can be varied by the voltage on the bulk and gate terminals as well by device engineering. Devices with a buried channel architecture such as buried SiGe channel pMOSFETs and accumulation mode MOSFETs on SOI show significantly reduced 1/*f* noise. The same observation is made when the substrate/source junction is forward biased which decreases the vertical electric field in the channel and increases the inversion layer separation from the gate oxide interface. A 1/*f* noise model based on mobility fluctuations originating from the scattering of electrons with phonons or surface roughness was proposed.

Materials with a high dielectric constant (high-k) is necessary to replace the conventional SiO_2 as gate dielectrics in the future in order to maintain a low leakage current at the same time as the capacitance of the gate dielectrics is scaled up. In this work, we have made some of the very first examinations of 1/*f* noise in MOSFETs with high-k structures composed by layers of HfO_2, $HfAlO_x$ and Al_2O_3. The 1/*f* noise level was found to be elevated (up to 3 orders of magnitude) in the MOSFETs with high-k gate dielectrics compared to the reference devices with SiO_2. The reason behind the higher 1/*f* noise is a high density of traps in the high-k stacks and increased mobility fluctuation noise, the latter possibly due to noise generation in the electron-phonon scattering that originates from remote phonon modes in the high-k. The combination of a TiN metal gate, $HfAlO_x$ and a compressively strained surface SiGe channel was found to be superior in terms of both high mobility and low 1/*f* noise.

Keywords:

MOSFET, SOI, SiGe, strain, high-k, metal gate, 1/*f* noise, low-frequency noise, mobility fluctuations, phonons, number fluctuations, traps, buried channel, mobility, substrate bias.

Table of Contents

List of Appended Papers

I. **1/*f* noise in Si and $Si_{0.7}Ge_{0.3}$ pMOSFETs**
M. von Haartman, A.-C. Lindgren, P.-E. Hellström, B. G. Malm, S.-L. Zhang and M. Östling, *IEEE Trans. Electron Devices*, vol. 50, pp. 2513-2519, 2003.

II. **Influence of gate width on 50 nm gate length $Si_{0.7}Ge_{0.3}$ channel PMOSFETs**
M. von Haartman, A.-C. Lindgren, P.-E. Hellström, M. Östling, T. Ernst, L. Brévard and S. Deleonibus, in *Proc. 33rd ESSDERC*, 2003, pp. 529-532.

III. **Low-frequency noise in SiGe channel pMOSFETs on ultra-thin body SOI with Ni-silicided source/drain**
M. von Haartman, J. Hållstedt, J. Seger, B. G. Malm, P.-E. Hellström and M. Östling, in *Proc. 18th Int. Conf. Noise and Fluctuations (ICNF)*, 2005, pp. 307-310.

IV. **Comprehensive study on low-frequency noise and mobility in Si and SiGe pMOSFETs with high-κ gate dielectrics and TiN gate**
M. von Haartman, B. G. Malm and M. Östling, *accepted for publication in IEEE Trans. Electron Devices (in print April 2006).*

V. **Low-frequency noise in $Si_{0.7}Ge_{0.3}$ surface channel pMOSFETs with ALD HfO_2/Al_2O_3 gate dielectrics**
M. von Haartman, D. Wu, B. G. Malm, P.-E. Hellström, S.-L. Zhang and M. Östling, *Solid-State Electronics*, vol. 48, pp. 2271-2275, 2004.

VI. **Low-frequency noise and Coulomb scattering in $Si_{0.8}Ge_{0.2}$ surface channel pMOSFETs with ALD Al_2O_3 gate dielectrics**
M. von Haartman, J. Westlinder, D. Wu, B. G. Malm, P.-E. Hellström, J. Olsson and M. Östling, *Solid-State Electronics*, vol. 49, pp. 907-914, 2005.

VII. **Low-frequency noise in $Si_{0.7}Ge_{0.3}$ surface channel pMOSFETs with a metal/high-κ gate stack**
M. von Haartman, D. Wu, P.-E. Hellström, S.-L. Zhang and M. Östling, in *Proc. 17th Int. Conf. Noise and Fluctuations (ICNF)*, 2003, pp. 381-384.

VIII. **Noise in Si and SiGe MOSFETs with high-k gate dielectrics**
M. von Haartman, B. G. Malm, P.-E. Hellström and M. Östling, in *Proc. 18th Int. Conf. Noise and Fluctuations (ICNF)*, 2005, pp. 225-230. (Invited paper).

IX. **Random telegraph signal noise in SiGe heterojunction bipolar transistors**
M. von Haartman, M. Sandén, M. Östling and G. Bosman, *Journal of Applied Physics*, vol. 92, pp. 4414-4421, 2002.

Related work not included in the thesis

1. M. von Haartman, M. Östling and G. Bosman, "Temperature dependent RTS noise in SiGe HBTs", in *Proc 16th Int. Conf. Noise and Fluctuations (ICNF)*, 2001, pp. 383-386.

2. F. Jonsson, M. von Haartman, M. Sandén, M. Östling and M. Ismail, "A voltage controlled oscillator with automatic amplitude control in SiGe technology", in *Proc. 19th NORCHIP*, 2001, pp. 28-33.

3. A.-C. Lindgren, P.-E. Hellberg, M. von Haartman, D. Wu, C. Menon, S.-L. Zhang and M. Östling, "Enhanced intrinsic gain (g_m/g_d) of PMOSFETs with a $Si_{0.7}Ge_{0.3}$ channel", in *Proc. 32nd ESSDERC*, 2002, pp. 175-178.

4. M. von Haartman, T. Johansson, B. G. Malm and M. Östling, "Decreased low-frequency noise in polysilicon emitter bipolar transistors by epitaxial regrowth", in *Proc 17th Int. Conf. Noise and Fluctuations (ICNF)*, 2003, pp. 415-418. (oral presentation at conference)

5. D. Wu, A.-C. Lindgren, S. Persson, G. Sjöblom, M. von Haartman, J. Seger, P.-E. Hellström, J. Olsson, H.-O. Blom, S.-L Zhang, M. Östling, E. Vainonen-Ahlgren, W.-M. Li, E. Tois and M. Tuominen, "A novel strained $Si_{0.7}Ge_{0.3}$ surface-channel pMOSFET with an ALD $TiN/Al_2O_3/HfAlO_x/Al_2O_3$ gate stack", *IEEE Electron Device Lett*., vol. 24, pp. 171-173, 2003.

6. D. Wu, M. von Haartman, J. Seger, E. Tois, M. Tuominen, P.-E. Hellström, M. Östling and S.-L. Zhang, "Ni-salicided CMOS with a poly-SiGe/$Al_2O_3/HfO_2/Al_2O_3$ gate stack", *Microelectron. Eng.*, vol. 77, pp. 36-41, 2005.

7. J. Seger, P.-E. Hellström, J. Lu, B. G. Malm, M. von Haartman, M. Östling and S.-L. Zhang, "Lateral encroachment of Ni-silicides in the source/drain regions on ultrathin silicon-on-insulator", *Appl. Phys. Lett.*, vol. 86, 253507, 2005.

8. C. Isheden, P.-E. Hellström, M. von Haartman, H. H. Radamson and M. Östling, "pMOSFETs with recessed and selectively regrown $Si_{1-x}Ge_x$ source/drain junctions", *Mat. Sci. Sem. Proc.*, vol. 8, pp. 359-362, 2005.

9. J. Hållstedt, M. von Haartman, P.-E. Hellström, M. Östling and H. H. Radamson, "Hole mobility in ultra thin body SOI pMOSFETs with buried SiGe or SiGeC channels," *submitted to IEEE Electron Device Lett.*

Summary of Appended Papers

Paper I. This paper presented an in-depth low-frequency noise characterization of Si and SiGe pMOSFETs. A reduction of the 1/*f* noise by a factor of two was observed in the SiGe devices thanks to the buried channel conduction. The 1/*f* noise was evaluated for various thicknesses of the Si-cap, an optimum was found for a thickness in the middle of the studied interval 3-7 nm. The 1/*f* noise was also studied as a function of the substrate bias voltage, which translated to a variation in the effective vertical electric field in the channel. This was one of the first studies of this kind to be performed on Si and SiGe pMOSFETs. The source of the noise was investigated, and a modified 1/*f* noise model involving fluctuation in the surface roughness scattering was proposed.
The author of this thesis performed all low-frequency noise characterizations and most of the other electrical measurements, analyzed all the data, developed the model, performed all simulations and modeling, and wrote the whole manuscript. The author also established the CMOS low-frequency noise measurement setup.

Paper II. In this work, electrical evaluations of 50-nm gate length compressively strained $Si_{0.7}Ge_{0.3}$ channel pMOSFETs were performed. The influence of gate width was investigated, and it was shown that enhancements of the drain current and transconductance were achieved for 50-nm SiGe transistors compared to the Si ones at small gate widths ~0.25 μm. At the time of publication, this work showed the highest reported on-current for a SiGe channel pMOSFET so far.
The author performed 90% of the electrical measurements, analyzed all the data, suggested the gate width analysis and the interpretation, and wrote the major part of the manuscript. The author presented the paper with a poster at ESSEDERC 2003 in Estoril, Portugal.

Paper III. The mobility and low-frequency noise were investigated in fully-depleted (FD) SiGe channel pMOSFETs on ultra-thin SOI. Enhanced hole mobility was observed for SiGe channel transistors with a total body thickness of ~20 nm. Both the SiGe device and the reference FD SOI pMOSFET showed low 1/*f* noise thanks to buried channel conduction and negligible floating body effects. The effect of the Ni-silicide in S/D was also studied, especially for the case of a Schottky-Barrier (SB) MOSFET when the Ni-silicide is formed at the edges of the channel. This was the first study of SB MOSFETs from a low-frequency noise point of view.
The author performed all low-frequency noise and other electrical measurements, analyzed all the data, performed the Schred[1] simulations, and wrote the whole manuscript. The author presented the paper with a poster at ICNF 2005 in Salamanca, Spain.

Paper IV. A comprehensive study on low-frequency noise and mobility in pMOSFETs with high-k gate dielectrics was presented. The choice of channel material (Si or SiGe), gate dielectric material (Al_2O_3, $Al_2O_3/HfO_2/Al_2O_3$ or $Al_2O_3/HfAlO_x/Al_2O_3$) and gate electrode material (TiN or poly-SiGe) was investigated. The dominant sources of scattering as well as the origin of the low-frequency noise were studied. A new physical explanation of the increased 1/*f* noise in

[1] Simulation tool on the web, http://www.nanohub.org

high-k transistors based on remote phonon scattering was presented. This paper is a summary of the author's previous work on high-k MOSFETs (papers V-VIII) including additional measurements and an improved analysis. The authors were the first to present that a metal gate can give lower 1/*f* noise together with a physical explanation.
The author of this thesis performed all low-frequency noise and other electrical characterizations, analyzed all the data and made the interpretations, performed all simulations and modeling, and wrote the whole manuscript.

Paper V. Low-frequency noise was characterized in SiGe surface channel pMOSFETs with a gate stack in form of poly-SiGe on top of a $Al_2O_3/HfO_2/Al_2O_3$ high-k structure. The influence of surface treatment prior to ALD processing and the thickness of the bottom Al_2O_3 layer were studied in particular. The noise origin was interpreted both with the number and the mobility fluctuation noise models.
The author of this thesis performed all low-frequency noise measurements and the majority of the other electrical characterizations, analyzed all the data and performed all modeling, and wrote the whole manuscript. The author also developed the low-frequency noise measurement setup by implementing new equipment in form of a low-noise current amplifier.

Paper VI. This paper investigates low-frequency noise and hole mobility in SiGe surface channel pMOSFETs with a an ALD Al_2O_3 gate dielectrics. The devices were annealed in low-temperature H_2O vapour in order to modify the charge in the gate dielectrics and improve device performance. The scattering parameter that determines the strength of the Coulomb scattering was characterized both from I_D-V_{GS} and low-frequency noise measurements. A negative correlation between the number and mobility fluctuations was observed for devices containing a negative charge. For the 210 min annealed devices, on the other hand, a positive correlation was found. A model to explain the observed behaviour was presented.
The study, a collaboration between KTH and Uppsala University, was suggested and directed by the author. The water vapour annealing and the corresponding *I-V* characterizations were performed in Uppsala. The author performed all low-frequency noise characterizations, analyzed the noise data, made the interpretations and the modeling, and wrote the whole manuscript.

Paper VII. This was the first paper about low-frequency noise Si and SiGe pMOSFETs with HfO_2 based gate dielectrics. Low-frequency noise was measured in pMOSFETs with various high-k gate dielectrics and Ge concentrations in the channel. The 1/*f* noise was found to be significantly higher in the transistors with high-k gate dielectrics, which mainly was attributed to a high density of traps in the high-k materials. Oxide and interface trap densities were reported.
The author of this thesis performed all low-frequency noise measurements and the majority of the other electrical characterizations, analyzed all the data and performed all modeling, and wrote the whole manuscript. The author gave an oral presentation of the paper at ICNF 2003 in Prague, Czech Republic.

Paper VIII. This work was an invited paper to the 18th ICNF conference in Salamanca, Spain, 19-23 September 2005, which was later followed up in paper IV. An overview of previous work and new insights on noise in Si-based MOSFETs with high-k gate dielectrics were presented. The first measurements on buried SiGe

pMOSFETs with high-k were reported, not covered in paper IV. The effect of a substrate bias on the channel positioning and the 1/*f* noise was also studied.
The author performed all low-frequency noise and other electrical characterizations, analyzed all the data, performed the simulations, and wrote the whole manuscript. A comprehensive literature study was also carried out. The author gave an invited oral presentation of the paper at ICNF 2005.

Paper IX. In this work, random telegraph signal (RTS) noise was characterized as a function of bias voltage and temperature in SiGe heterojunction bipolar transistors. The RTS noise amplitudes as well as the trapping kinetics were studied, and a physical model was presented.
The author developed a setup and a method for measurements of RTS noise, wrote scripts controlling the measurement equipment as well as for automation of the heavy data processing, and established routines for the parameter extraction. Moreover, the author performed all noise measurements and data analysis, suggested and developed the physical model and wrote the manuscript.

Acknowledgments

I remember that I was fascinated by electronics, and in particular the tiny device called the transistor, already in elementary school (6^{th} or 7^{th} grade probably). I only had an old encyclopaedia at hand, and I wanted to know more. Roughly 18 years later I have written a Ph. D. thesis on this fascinating device, the MOS transistor. During this journey, there are many people I am deeply grateful to for their invaluable help. I would like to start in chronological order.

My parents, Gösta and Ann-Charlotte, have provided a good balance of support, high expectations and independence. I also wanted to be a good example for my younger sister, Marie, which motivated me to study hard. This gave me a good platform for my future career.

At the end of my undergraduate studies in electrical engineering at KTH, I came in contact with Prof. Mikael Östling and Prof. Carl-Mikael Zetterling at EKT. I had a wish to do my diploma work abroad as an exchange student and started to investigate possible international connections within the field of microelectronics at KTH. Mikael was enthusiastic about the idea, and he and Carl-Mikael helped and inspired me to set up a project together with Prof. Gijs Bosman at University of Florida, Gainesville, USA. I am deeply grateful to both of you for leading me into this path. In this MS thesis project, I made my first acquaintance with academic research and the low-frequency noise phenomenon. I am forever thankful for the excellent guidance and rich wisdoms I received from Gijs, which gave me a jump-start when I began my Ph. D. studies later.

Back in Sweden after the adventure in Florida I began my Ph. D. studies in the RFCMOS project. I would like to thank my supervisor Prof. Mikael Östling for giving me the opportunity to continue as a Ph. D. student in the RFCMOS project and the continuous inspiration he has given me with his optimistic attitude, always believing in my abilities, and never-ending idea-generation.

I am grateful to Dr. Martin Sandén for his guidance during the beginning of my studies. I wish to thank Dr. Gunnar Malm for the great support he has given in form of comments and ideas on my research work as well as numerous other things. I am also thankful to Docent Per-Erik Hellström for guiding me on MOSFET fundamentals and electrical measurements as well as being the brain behind much of the MOSFET fabrication process fuelling my research work with advanced devices. I appreciated the help I received from Prof. Carl-Mikael Zetterling on various matters regarding research, course work or practical issues. I am in debt to Docent Shi-Li Zhang for helping me with scientific writing and leading the high-k project to such a success, if this had not been the case this thesis would have been much different.

I have a deep gratitude for the friendship and collaboration with some of my closest colleagues at EKT, especially my former roommate Dr. Johan Seger, Dr. Christian Isheden, and Tekn. Lic. Julius Hållstedt. We have had some great times, sharing a beer after work sometimes or just chatting about research problems or life in general at lunches and coffee breaks. I am also grateful to Dr. Dongping Wu and Ann-Chatrin Lindgren for nice collaboration on various research projects.

Many thanks go to all of my present and former colleagues at KTH for friendship and scientific discussions: Dr. Erik Haralson, Dr. Martin Domeij, Zhen Zhang, Tekn. Lic. Hyung-Seok Lee, Docent Henry Radamson, Jonas Edholm, Christian Ridder, Timo Söderqvist, Dr. Stefan Persson, Dr. Erdal Suvar, Dr. Erik Danielsson, Dr. Johan Pejnefors, Dr. Zhibin Zhang, Dr. Wei Liu, Dr. Yong-Bin Wang, Dr. Uwe Zimmermann, Patrik Möller, Susanna Norell, Dr. Yohannes Assefaw-Redda, Emir Sakic, and friends in the 'Real KTH' football team.

I am also grateful to my external partners and research colleagues: Dr. Jörgen Westlinder and Docent Jörgen Olsson, Uppsala University, Dr. Ted Johansson, Infineon Technologies, Prof. Lode Vandamme, Eindhoven University of Technology, participants and partners in the 'high-frequency silicon' project and the European SIGMOS and SiNANO projects as well as other researchers I have met and discussed with at conferences etc.

Thank you Zandra Lundberg, our department administrator, for all your support and help with administrative details.

KTH, by granting me an 'excellenstjänst', and the Swedish Foundation for Strategic Research (SSF) are acknowledged for financial support.

Finally, and most important, I wish to express my deep love and gratitude to my wife, Anne, for her support, encouragement and kind love in everything that concerns my life. I dedicate this thesis to you. Du är viktigast för mig, jag älskar dig!

Stockholm, 2006-03-01

Martin von Haartman

List of Symbols and Acronyms

Symbol	Unit	Meaning
$c(s)$		Autocorrelation function
c_n		Fourier coefficients
C	F (F/cm^2)	Capacitance (per unit area)
C_{box}	F/cm^2	Capacitance per unit area of buried oxide (SOI)
C_d	F/cm^2	Depletion layer capacitance per unit area
C_{dm}	F/cm^2	Depletion layer capacitance per unit area when the depletion layer has its maximum width W_{dm}
C_{fb}	F/cm^2	Flat-band capacitance per unit area
C_{fox}	F/cm^2	Capacitance per unit area of front oxide (SOI)
C_G	F	Gate capacitance
C_{GB}	F	Gate-to-substrate capacitance
C_{gb}	F/cm^2	Gate-to-substrate capacitance per unit area
C_{GC}	F	Gate-to-channel capacitance
C_{gc}	F/cm^2	Gate-to-channel capacitance per unit area
C_{it}	F/cm^2	Interface trap capacitance per unit area
C_{ox}	F/cm^2	Gate oxide capacitance per unit area
d	cm	Lattice constant
D_{it}	cm^{-2}eV^{-1}	Density of interface states (traps)
E	J	Energy
E	V/cm	Electric field
E_{eff}	V/cm	Effective electric field (effective vertical field across gate oxide)
E_F	J	Fermi energy level
E_{fn}	J	Quasi-Fermi energy level for electrons
E_{fp}	J	Quasi-Fermi energy level for holes
E_g	J	Band gap energy
E_i	J	Intrinsic Fermi energy level
E_T	J	Trap energy level
E_C	J	Conduction band edge energy
E_V	J	Valence band edge energy
f	Hz	frequency
f(E)	-	Fermi-Dirac distribution function, gives the probability that an electronic state at energy E is occupied
$f(X)$	-	Probability density function of random variable X
f_0	Hz	Oscillation frequency of VCO
f_T	Hz	Transition frequency
F	-	Noise factor
g	-	Degeneracy factor
g_{ch}	S = A/V	Channel conductance
g_{ds}	S	Source-drain conductance
g_m	S	Transconductance
h	Js	Planck's constant (= 6.63×10^{-34} Js)
I	A	Current
I_{cp}	A	Charge-pumping current (through the bulk terminal)
I_D	A	Drain current
$I_{D,sat}$	A	Drain current in saturation
i_n	A	Noise current
J	A/cm^2	Current density
J	A/cm	1D current density (along width of inversion channel)
k	J/K	Boltzmann's constant (=1.38×10^{-23} J/K)
L	cm	Gate length (length)

$L(\Delta f)$	dB	Phase noise
m	-	MOSFET body-effect coefficient
m^*	kg	Electron effective mass
N	-	Number of carriers
n	cm^{-3}	Electron concentration (per unit volume)
N_a	cm^{-3}	Acceptor doping concentration
N_d	cm^{-3}	Donor doping concentration
n_i	cm^{-3}	Intrinsic carrier concentration
n_s	cm^{-3}	Surface carrier concentration
N_{sub}	cm^{-3}	Doping concentration in the substrate
N_t	$cm^{-3}eV^{-1}$	Oxide trap density (per unit volume)
NF	dB	Noise figure
p	cm^{-3}	Hole concentration (per unit volume)
q	C	Electronic charge (=1.602×10^{-19} C)
Q_d	C/cm^2	Depletion charge per unit area
Q_D	C	Depletion charge
Q_i	C/cm^2	Inversion charge per unit area
Q_I	C	Inversion charge
Q_m	C/cm^2	Charge on gate per unit area
$q_{\max}$	C	Maximum charge displacement of tank capacitor in VCO
Q_{ox}	C/cm^2	Oxide charge per unit area
R	Ω	Resistance
R_{ch}	Ω	Channel resistance
R_D	Ω	Drain series resistance
R_S	Ω	Source series resistance
R_{SD}	Ω	Source-drain series resistance ($R_S + R_D$)
S		Power spectral density
S_{I_D}	A^2/Hz	Power spectral density of the drain current noise
S_{V_G}	V^2/Hz	Power spectral density of the equivalent gate voltage noise
$S_{V_{fb}}$	V^2/Hz	Power spectral density of the flat-band voltage noise
$S_{Q_{ox}}$	C^2/cm^4Hz	Power spectral density of the oxide charge density fluctuations
S_I	A^2/Hz	Power spectral density of current fluctuations
S_J	A^2/cm^4Hz	Power spectral density of current density fluctuations
S_N	1/Hz	Power spectral density of carrier number fluctuations
S_R	Ω^2/Hz	Power spectral density of resistance fluctuations
S_V	V^2/Hz	Power spectral density of voltage fluctuations
SS	V/decade	Subthreshold slope
T	K	Absolute temperature
t	s	time
T_n	-	Normalized absolute temperature ($T_n = T$/300 K)
t_{ox}	cm	Gate oxide thickness
V	cm^3	Volume
V	V	Voltage
V_B	V	Substrate voltage (Bulk terminal voltage)
V_{BS}	V	Substrate-to-source voltage
V_{DD}	V	Power supply voltage
V_{DS}	V	Drain-to-source voltage
$V_{DS,sat}$	V	MOSFET drain-to-source saturation voltage
V_{fb}	V	Flat-band voltage
V_G	V	Gate voltage
V_{GS}	V	Gate-to-source voltage
V_{GT}	V	Gate voltage overdrive (= $\lvert V_{GS} - V_T \rvert$)

V_{max}	V	Maximum voltage swing over tank capacitor in VCO
v_n	V	Noise voltage
V_R	V	Reverse voltage
V_T	V	Threshold voltage
v_{th}	cm/s	Thermal velocity of electrons
W	cm	Gate width
W_d	cm	Depletion layer width
W_{dm}	cm	Maximum depletion layer width
W_{poly}	cm	Width of depletion layer in polysilicon gate
z	cm	Distance in a direction vertical to the channel
Δf	Hz	Frequency separation from the oscillating frequency of a VCO
Δx or δx		Fluctuation in x
Φ_B	J	Energy barrier height
α	Vs/C	Scattering parameter of the correlated mobility fluctuations
α_C	Vs/C	Coulomb scattering parameter
α_H	-	Hooge parameter
$\alpha_{H,a}$	-	Hooge parameter of $1/f$ noise generated in scattering processes other than surface roughness scattering.
$\alpha_{H,i}$	-	Hooge parameter for individual carrier
$\alpha_{H,ph}$	-	Hooge parameter of $1/f$ noise generated in the phonon scattering
$\alpha_{H,sr}$	-	Hooge parameter of $1/f$ noise generated in the surface roughness scattering
ε_{ox}	F/cm	Permittivity of SiO_2 ($=3.45\times10^{-13}$ F/cm)
ε_{Si}	F/cm	Silicon Permittivity ($=1.04\times10^{-12}$ F/cm)
ϕ_{ms}	V	Work-function difference between the gate material and the substrate material
γ	-	Frequency exponent
γ	-	MOSFET thermal noise coefficient
η	-	MOSFET parameter describing the relative degree of drain saturation
λ	cm	Tunneling attenuation length
λ_e	cm	Phonon mean free path
μ	cm^2/Vs	Carrier mobility
μ_a	cm^2/Vs	Carrier mobility limited by other mechanisms than surface roughness scattering
μ_{ac}	cm^2/Vs	Mobility limited by scattering with surface acoustic phonons
μ_b	cm^2/Vs	Mobility limited by scattering with bulk phonons
μ_C	cm^2/Vs	Mobility limited by Coulomb scattering
$\mu_{C,imp}$	cm^2/Vs	Mobility limited by Coulomb scattering from impurities
$\mu_{C,ox}$	cm^2/Vs	Mobility limited by Coulomb scattering from oxide charges
μ_{C0}	cm/Vs	Screened Coulomb scattering parameter
μ_{eff}	cm^2/Vs	Effective mobility
μ_i	cm^2/Vs	Individual carrier mobility
μ_n	cm^2/Vs	Electron mobility
μ_p	cm^2/Vs	Hole mobility
μ_{ph}	cm^2/Vs	Mobility limited by scattering with phonons, both bulk phonons and surface acoustic phonons.
μ_{sr}	cm^2/Vs	Mobility limited by surface roughness scattering
θ	rad	Phase
σ	$\Omega^{-1}cm^{-1}$	Conductivity
σ	cm^2	Capture cross section
σ_n	cm^2	Capture cross section for electrons
σ_p	cm^2	Capture cross section for holes

σ_{N_t}	$cm^{0.5}eV^{0.5}$	Relative standard deviation of the trap density
τ	s	CMOS inverter delay
τ	s	Time constant of the g-r noise
τ_0	s	Tunneling time constant
τ_1	s	Lower limit of the g-r noise time constant
τ_2	s	Upper limit of the g-r noise time constant
τ_c	s	Capture time for electrons (holes)
τ_e	s	Emission time for electrons (holes)
τ_f	s	Pulse fall time
τ_h	s	Time in high level of two-state RTS
τ_l	s	Time in low level of two-state RTS
τ_r	s	Pulse rise time
τ_{th}	s	Time constant of thermally activated traps
ω_0	rad/s	Angular frequency of oscillation
ψ_B	V	Difference between Fermi level and intrinsic level
ψ_s	V	Surface potential
$\psi_{s,inv}$	V	Surface potential in inversion

ALD	Atomic layer deposition
B	Bulk
CMOS	Complementary metal-oxide-semiconductor
C-V	Capacitance-voltage
CVD	Chemical vapour deposition
D	Drain
DC	Direct current
DCR	Direct conversion receiver
DI water	De-ionized water
DIBL	Drain-induced barrier lowering
DT	Dynamic threshold
DUT	Device-under-test
EOT	Equivalent oxide thickness
FD	Fully depleted
FFT	Fast Fourier Transform
FUSI	Fully silicided
G	Gate
g-r	Generation-recombination
HF-clean	Clean in Hydroflouric acid
HRTEM	High resolution transmission electron microscopy
ISF	Impulse sensitivity function
ITRS	International technology roadmap of semiconductors
I-V	Current-voltage
JFET	Junction field-effect transistor
LC	Inductance-capacitance
LNA	Low-noise amplifier
MBE	Molecular beam epitaxy
MOCVD	Metal-organic chemical vapour deposition
MOSFET	Metal-oxide-semiconductor field-effect transistor
nMOSFET	n-channel MOS transistor
PD	Partially depleted
pMOSFET	p-channel MOS transistor

PSD	Power spectral density
PVD	Physical vapour deposition
RF	Radio frequency
RTS	Random-telegraph-signal
S	Source
SCE	Short channel effect
SMU	Source-measure unit
SNR	Signal-to-noise ratio
SOI	Silicon-on-insulator
TCAD	Technology computer aided design
TEM	Transmission electron microscopy
VCO	Voltage controlled oscillator
WKB	Wentzel-Kramers-Brillouin

1. Introduction

Semiconductor devices are designed for higher and higher speeds, propelled by the electronics industry's pursuit and the consumer's demands in achieving faster computers that can perform heavier tasks, handheld wireless multimedia units, entertainment systems with advanced 3D graphics, realizing global high-speed communication systems etc. The metal-oxide-semiconductor field-effect transistor (MOSFET) is a key semiconductor component, the heart and brain in almost all electronic circuits, the evolution of which has stimulated the recent explosion in information and communication technology [1]. By downsizing the geometrical dimensions of the MOSFET and replacing established material combinations with new, improved ones, the performance and speed of the transistor are enhanced. However, several undesired effects emanate from the miniaturization of the device sizes. One such unwanted effect is a strong increase of the low-frequency noise generated in the transistor as the size of the device decrease. Moreover, there are many unexplored issues regarding the introduction of new materials in complementary-metal-oxide-semiconductor (CMOS) technology. Therefore, electrical evaluations of devices using new materials and architectures are highly desired.

Noise is a fundamental problem in science and engineering, recognized and underlined for a variety of fields such as telecommunication, nanoelectronics, and biological systems. The noise cannot be completely eliminated and will therefore ultimately limit the accuracy of measurements and set a lower limit on how small signals that can be detected and processed in an electronic circuit. The low-frequency noise, or 1/*f* noise, is the excess noise at low frequencies whose power spectral density (PSD) approximately depends inversely on the frequency and therefore escalates at low frequencies. The 1/*f* noise originating from the transistors is a severe obstacle in analog circuits. The 1/*f* noise is, for example, upconverted to undesired phase noise in voltage controlled oscillator (VCO) circuits, which can limit the information capacity of communication systems [2]. Moreover, the downscaling of the device dimensions entails a downscaling of the voltage levels too, which lowers the signal-to-noise ratio. In fact, with this progress, the 1/*f* noise may soon become a major concern not only in analog circuits but also in the digital ones [3]. Fig. 1.1 depicts a schematic diagram of

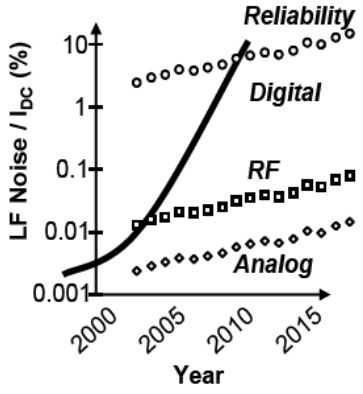

Fig. 1.1. Schematic graph showing the relative low-frequency noise magnitude and the reliability limits for different applications (after Deen and Marinov [3]).

the device reliability showing that the relative noise level already is a problem in RF and analog applications and soon exceeds the limits for a reliable device operation also in digital applications. This demonstrates that overcoming the 1/*f* noise in electronic circuits and devices is an extremely important challenge for the future. Low-frequency noise measurements are also an important tool for device diagnostics. The 1/*f* noise is very sensitive to trap and defects in the device and is strongly related to physical processes such as trapping and release phenomena, electron scattering mechanisms and phonon processes. The low-frequency noise can therefore be used as the information carrying signal to evaluate and get insight in the physics and properties of a particular system, and estimate the quality and reliability of a device [4-8].

The main topic of this thesis is the investigation of 1/*f* noise in advanced Si- and SiGe-based CMOS transistors. The thesis is based on comprehensive experimental results on a wide variety of different CMOS technologies that are attractive for future analog and digital applications. The experimental method used in this work is built on extensive electrical measurements of the low-frequency noise as well as of static device properties such as current-voltage characteristics, carrier mobility, and MOS capacitances. The devices used in the experiments are designed and fabricated at KTH, and are advanced in the sense that novel channel materials (compressively strained SiGe, strained Si), gate dielectric materials (various high-k oxides), gate electrode materials (TiN, poly-SiGe) and low-noise device architectures (buried channel devices) were explored. Common for all of them is that low-frequency noise results from these types of devices are very few in the literature. In some cases when previous studies were available, for example on buried SiGe channel pMOSFETs [9, 10] and SOI [11], we focused our efforts on optimizing the structures for low 1/*f* noise by elaborating with the formation and positioning of buried channels. The obtained results in this thesis are important in order to evaluate a technology from a noise and quality standpoint, and represent among the first or best 1/*f* noise results for the evaluated technologies. The 1/*f* noise in MOSFETs with high-k gate dielectrics has been studied with particular emphasis, the results obtained are in many respect highly original.

In order to minimize the device 1/*f* noise, an understanding of the noise mechanisms, the underlying physics and the location of the sources is necessary. Still today, after several decades of debate, the exact origin of the 1/*f* noise is in many aspects an open question [12]. In this work, the 1/*f* noise sources and their origin have been thoroughly studied for different bias conditions, device parameters, and technological factors. Especially the behaviour and physical properties of mobility fluctuation noise, a phenomenon that has caused tremendous controversy [13, 14], have been studied with particular emphasis. An improved analysis and modeling of the 1/*f* noise in terms of mobility fluctuations, substrate voltage effects, and correlated mobility fluctuations is presented in this thesis, which relies on an in-depth understanding of the device physics and in particular the properties of current transport and its inherent noise. Especially, the position of the channel for current conduction, varied both by device engineering and bias conditions, has been studied in relation to noise. The technique to extract information from traps by measurements in the time domain of random-telegraph-signal (RTS) noise is also explored in this work. The accumulated knowledge presented here can be used in designing devices and selecting materials

and architectures in order to optimize the 1/*f* noise performance or for building further improved 1/*f* noise models.

In chapter 2, the basics of the MOS transistor are reviewed. Especially the current transport in a MOS-structure is examined in detail as this is important in order to understand the fluctuations in the current. Furthermore, electrical characterizations are described and several advanced CMOS concepts are introduced and motivated. Chapter 3 deals with the fundamental noise mechanisms, the noise sources in the MOS transistor and their implications on some RF circuits. The origin and modeling of the 1/*f* noise in a MOSFET is discussed in chapter 4, which ends with an improved analysis derived from this work. Chapter 5 describes the measurement setup and the low-frequency noise characterization technique. The core of this work, chapter 6, presents an overview of the 1/*f* noise results extracted in this work for a variety of devices including Si MOSFETs, SiGe pMOSFETs, strained Si nMOSFETs, devices with high-k gate dielectrics, metal gate devices, along with comparisons with results in literature. The thesis ends with a summary and future perspective in chapter 7.

2. MOSFETs: device physics, electrical characterization & novel concepts

The metal-oxide-semiconductor field-effect transistor (MOSFET) is the building block in digital electronic applications such as microprocessors and memories. Bipolar transistors were for a long time the natural choice for analog applications, but CMOS-technology is making rapid progress replacing the bipolar transistors in the RF circuits of today [15, 16]. The CMOS-technology is very attractive since it combines low-cost, high performance, low standby power and superior integrated functions. The rapid development of CMOS is possible thanks to the unique ability to downscale the dimensions of the transistor which greatly has enhanced its speed and reduced the area it takes up on the chip. This chapter will discuss the basic principles behind the MOS transistor and review the device physics (section 2.1-2.2). Especially the carrier transport will be dealt with as the $1/f$ noise in the current is due to fluctuations in the number of carriers or the carrier mobility. In section 2.3, the electrical characterization of MOS transistors by means of *I-V*, *C-V*, and charge-pumping measurements is described. The urgent demand for novel materials and new device concepts in order to continue the downscaling of device dimensions and increase device performance will be discussed in section 2.4 and finally some advanced MOSFET concepts will be presented.

2.1 Fundamentals of MOSFETs

The MOS transistor can simply be described as a voltage controlled resistor. A MOS transistor has four terminals, see Fig. 2.1. A voltage on the gate terminal (input) controls the current flowing between the Source and Drain (output) terminals. The substrate terminal is usually connected to ground with only a small leakage current flowing through it. The source and drain regions are heavily doped and of opposite type than the substrate. For a p-channel MOSFET, which is exemplified in Fig. 2.1, source/drain is p^+-doped and the substrate n-type. The gate electrode, usually made of metal or poly-silicon, is separated from the Si substrate by a thin insulating film (thickness t_{ox}) called the gate oxide or gate dielectrics. SiO_2 or nitrided SiO_2 is typically used as gate dielectrics in production today, but other materials with higher dielectric constant such as HfO_2 have been heavily researched and will likely replace SiO_2 in the future, as will be discussed later in this chapter.

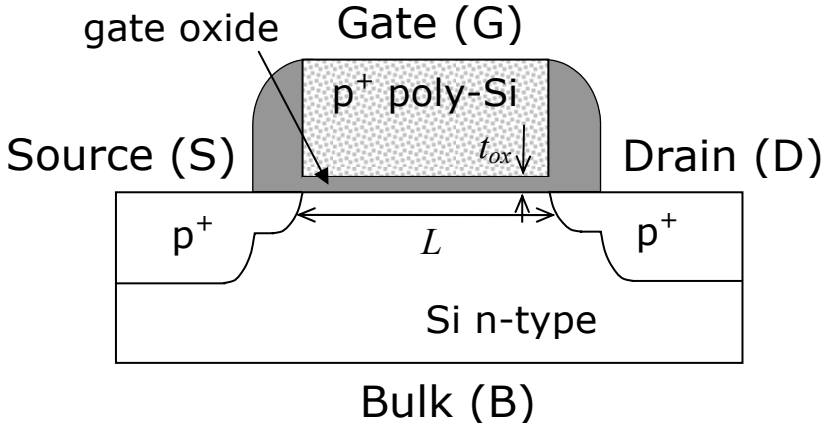

Fig. 2.1. A schematic cross section of a MOSFET.

When the gate voltage is higher (for pMOS, opposite for nMOS) than a voltage level called the threshold voltage, only a small leakage current can flow between source and drain. The p^+-n-p^+ structure consists of two p-n diodes connected front-to-front, preventing a current to flow except a small diffusion current. Biasing the gate with a negative voltage will decrease the surface potential and repel electrons from the surface leaving a positive charge of depleted ionized dopants. Decreasing the gate voltage below the threshold voltage will *invert* the substrate and a channel of carriers of the opposite type (holes in this case) is formed at the interface between the SiO_2 and Si substrate. The formation of the channel allows a large current to flow between source and drain, the device is switched on. Analytic expressions for the drain current are derived below for an nMOS transistor. Expressions for pMOS are obtained by exchanging polarity of voltages and reversing the direction of the currents.

First, we use the charge sheet approximation, which assumes that all the inversion charge is located at the Si surface and that there is no potential drop across the inversion layer. This is, however, not completely true. Quantum-mechanical calculations show that the inversion carrier density is zero at the interface and the peak is located a few nm below the interface (see chapters 4.3 and 6.4). Also, the inversion layer can be formed in a buried channel by device engineering. One such example is buried SiGe pMOSFETs, which is described later in this chapter. The approximation is still useful for the derivation of the drain current but some corrections for gate oxide capacitance and threshold voltage are necessary due to the quantum or buried channel effects. We also assume that the variation of the electric field is much weaker along the channel than perpendicular to the channel (gradual channel approximation) and that generation and recombination is negligible. Then the current per unit width at a position x along the channel can be written as:

$$J(x) = -\sigma(x)dV(x)/dx \tag{2.1}$$

where $\sigma(x) = \mu_{eff} Q_i(x)$ is the conductivity of a two-dimensional charge sheet with charge density Q_i (in C/cm^2) and V is the quasi-Fermi potential thus including both drift and diffusion current in Eq. (2.1). Since the DC current is constant at every point x due to continuity (no generation/recombination), integration of the current $I_D(x) = WJ(x)$ along the channel yields:

$$I_D L = -W\int_0^L \mu_{eff} Q_i(x)\frac{dV(x)}{dx}dx = -W\int_0^{V_{DS}} \mu_{eff} Q_i(V)dV \approx -W\mu_{eff}\int_0^{V_{DS}} Q_i(V)dV \tag{2.2}$$

In inversion, the inversion charge density can be approximated as

$$Q_i(V) = C_{ox}(V_{GS} - V_T - mV) \tag{2.3}$$

where V_T is the threshold voltage, m is a body-effect coefficient, and $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the oxide capacitance per unit area. Inserting Eq. (2.3) in Eq. (2.2), the following expression is obtained valid in the linear (triode) region where $V_{DS} < V_{DS,sat}$

$$I_D = \frac{W}{L}\mu_{eff} C_{ox}\left[(V_{GS} - V_T)V_{DS} - mV_{DS}^2/2\right] \tag{2.4}$$

The threshold voltage is given by:

$$V_T = V_{fb} \pm 2\psi_B \pm \frac{\sqrt{4\varepsilon_{si} q N_{sub} \psi_B}}{C_{ox}} \tag{2.5}$$

where N_{sub} is the doping concentration in the substrate, $2\psi_B = \psi_{s,inv} = 2kT/q \cdot \ln(N_{sub}/n_i)$ is the surface potential at the onset of strong inversion. The plus signs in Eq. (2.5) apply for nMOS and the minus signs for pMOS, respectively. The first term is the voltage drop required to achieve flat-band, i.e. no potential drop in the oxide and the Si substrate. The second term is the voltage required to invert the substrate in such a way that the inversion charge concentration has the same absolute value as in the substrate below the depletion region but with different polarity, or in other words bring the Fermi-level above or below the intrinsic level but with the same absolute separation E_F - E_i as in the substrate far below the surface (see Fig. 2.2). The third term is the voltage required to build up the depletion charge. The flat-band voltage depends on the work function difference between the gate material and the substrate material and the equivalent (trapped or fixed) charge density at the oxide-silicon interface

$$V_{fb} = \phi_{ms} - Q_{ox}/C_{ox} \tag{2.6}$$

For n^+ or p^+ doped poly-Si gate and p-type or n-type Si substrate the work function difference is calculated to be

$$\phi_{ms} = \pm 0.56 \pm kT/q \cdot \ln(N_{sub}/n_i) \tag{2.7}$$

where the plus or minus sign in front of the first term is for p-type or n-type gate material, respectively. For the second term, the plus sign applies for n-type substrate and the minus sign for p-type.

The factor m in Eqs. (2.3) and (2.4), called the body-effect coefficient, has been inserted to account for corrections to the simple theory. The value of m is typically between 1-1.4 and is calculated as follows [17]:

$$m = 1 + \frac{\sqrt{\varepsilon_{si} q N_{sub} / 4\psi_B}}{C_{ox}} \tag{2.8}$$

The drain current in Eq. (2.4) increase with the drain voltage until a maximum is reached and saturation occurs. The drain voltage at saturation is

$$dI_D / dV_{DS} = 0 \Rightarrow V_{DS,sat} = (V_{GS} - V_T)/m \tag{2.9}$$

At that point, called pinch-off, the channel at the drain end vanishes. The electric field along the channel between source and the pinch-off point stays constant with increasing $V_{DS} > V_{DS,sat}$ resulting in essentially the same current $I_{DS,sat}$. By inserting Eq. (2.9) in Eq. (2.4) the drain current in the saturation region can be written as

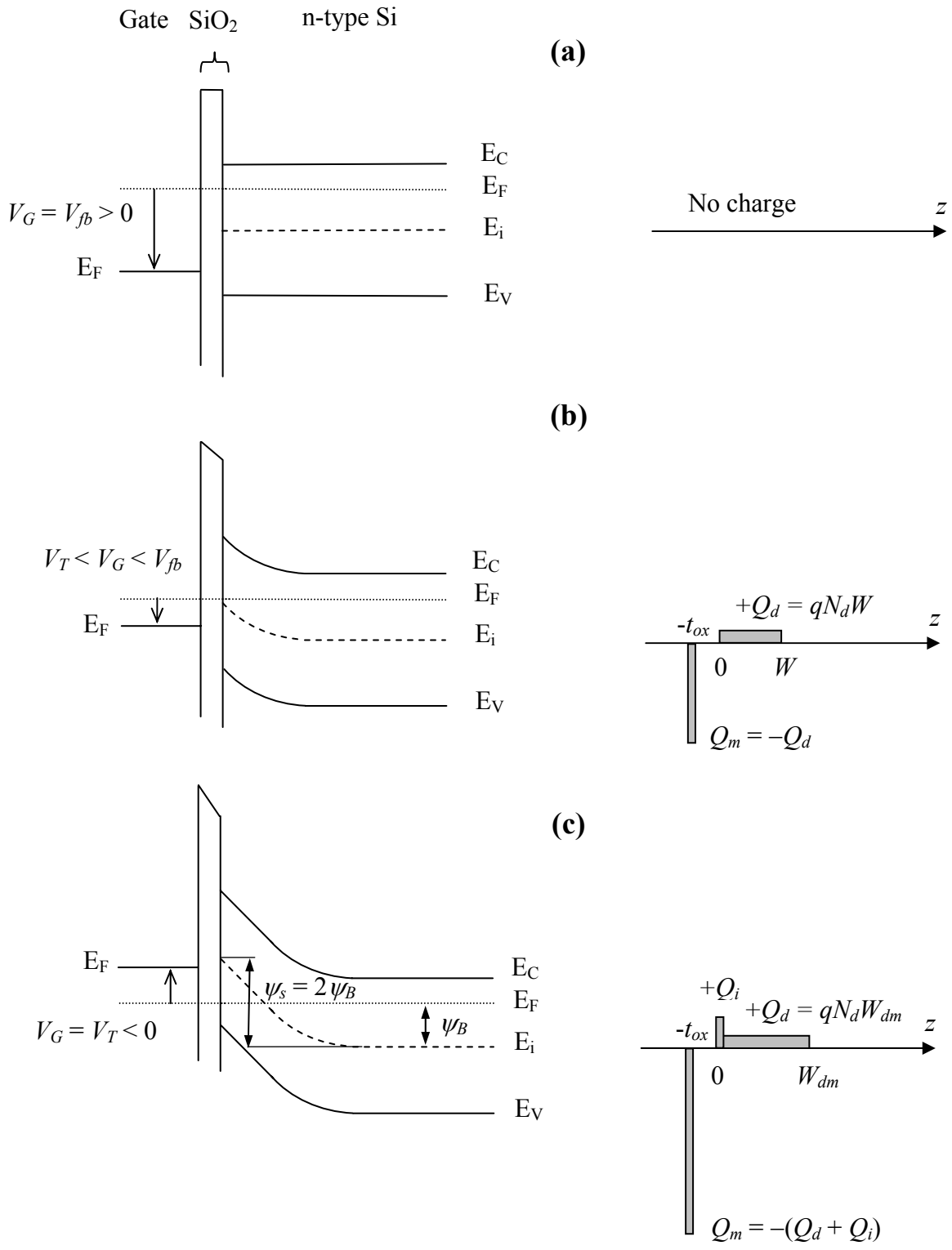

Fig. 2.2. Energy band diagram illustrations of a pMOSFET biased (a) at flat-band, (b) in depletion and (c) in strong inversion. The pictures to the right show the charge distributions in the MOS structure under these bias conditions.

$$I_D = \frac{W}{L}\mu_{eff} C_{ox} \frac{(V_{GS} - V_T)^2}{2m} \tag{2.10}$$

The pinch-off point moves slightly towards the source side for $V_{DS} > V_{DS,sat}$, which decreases the effective channel length somewhat. This effect is called channel length modulation and results in a weak increase of I_{DS} with V_{DS} in saturation.

The current will not go to zero when biased below threshold, $V_{GS} < V_T$, called the subthreshold region. A small diffusion current will remain

$$I_D = \mu_{eff} C_{ox} \frac{W}{L}(m-1)\left(\frac{kT}{q}\right)^2 e^{q(V_{GS}-V_T)/mkT}\left(1 - e^{-qV_{DS}/kT}\right) \tag{2.11}$$

The ability to turn off a device is described by the subthreshold slope

$$SS = \left(\frac{d(\log_{10} I_D)}{dV_{GS}}\right)^{-1} = \frac{mkT}{q\log_{10} e} \approx 2.3\frac{mkT}{q} = 2.3\frac{kT}{q}\left(1 + \frac{C_{dm}}{C_{ox}}\right) \tag{2.12}$$

A low subthreshold slope is desired since the current drops steeper with decreasing gate voltage, the device is easier to turn off. This allows a lower threshold voltage and consequently a higher on-current. An ideally low *SS* value of ~60 mV/dec can be achieved in SOI-technology whereas *SS* typically is between 60-100 mV/dec in bulk Si MOSFETs. The subthreshold slope is sensitive to the presence of traps at the SiO_2/Si interface since the capacitance associated with the interface states will act in parallel with the (maximum) depletion-layer capacitance C_{dm} and thus increase *SS*. At last, the drain current characteristics are shown for different regions of operation in Fig. 2.3, where the I_D-V_{GS} characteristics are displayed in (a) and the I_D-V_{DS} characteristics in (b).

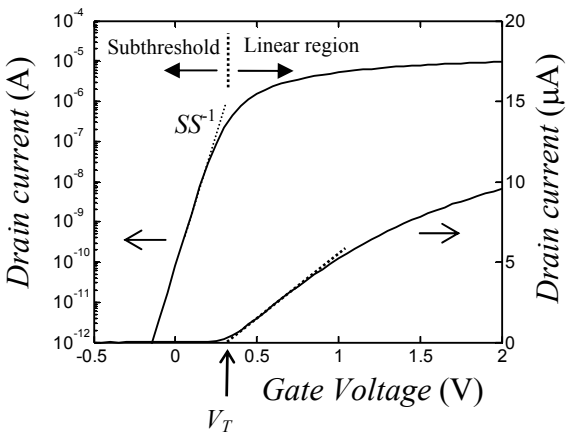

Fig. 2.3(a). I_D-V_{GS} characteristics in both logarithmic (left) and linear (right) scales.

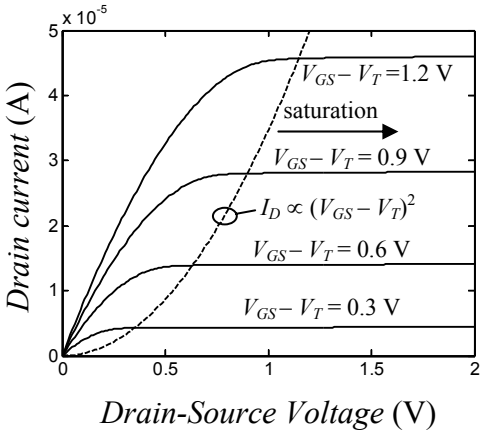

Fig. 2.3(b). I_D-V_{DS} characteristics for four different gate voltage overdrives.

2.2 Carrier mobility

The carriers in a semiconductor, which is placed under thermal equilibrium and with no electric field applied, move rapidly with the thermal velocity ~ 10^7 cm/s in random directions with no net current flow. The carriers are scattered by lattice vibrations (phonons) and impurities (dopants or defects) whereby their velocities are abruptly changed, under conservation of energy and momentum. The time between scattering events, the collision time τ_c, is typically on the order of 0.1 ps [17]. Carriers under influence of an electric field are accelerated between the collisions. The carriers are assumed to immediately relax upon a collision and emerge at a random direction and a speed corresponding to the local temperature. Therefore, at a certain point of time, the carriers will on average have been accelerated by the force qE during the time τ_c and gained a drift speed of $\tau_c qE/m^*$, where m^* is the effective mass. Holes move in the same direction as the field and electrons in the opposite direction. One defines the mobility according to $\mu = v_{drift}/E$, which thus equals $\mu = q\tau_c/m^*$. The carrier mobility in an inversion layer of a MOSFET is lower than in the bulk since the carriers are confined to a narrow region below the oxide/substrate interface and therefore suffer from scattering at the surface (roughness and surface phonons). By assuming that the different scattering mechanism act independently and have the same energy dependence, the effective mobility μ_{eff} in an inversion layer of a MOSFET can be computed using Matthiessen's rule from the individual mobilities according to [18-21]

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_b} + \frac{1}{\mu_{ac}} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_C} \tag{2.13}$$

where μ_b is the bulk phonon mobility, μ_{ac} the mobility limited by surface acoustic phonon scattering, μ_{sr} the mobility due to surface roughness scattering and μ_C the mobility limited by Coulomb scattering mainly from ionized impurities and fixed/trapped charge in the gate oxide (its bulk and surfaces) or, if a very thin gate oxide is used, also from depleted charge in the poly-Si gate [22]. Although the conditions for using Matthiessen's rule seldom are fulfilled in practice, the formula still serves as a good approximation for the effective mobility. The phonon scattering is only weakly dependent on technology for a semiconductor material of good crystalline quality. The surface roughness scattering due to the micro roughness at the substrate/gate oxide interface and the Coulomb scattering, on the other hand, are sensitive to technology factors such as doping concentration ($\mu_C \propto 1/N_{doping}$) and surface cleaning and gate oxidation process ($\mu_{sr} \propto 1/\Delta^2\Lambda^2$, where Δ is the RMS value of the roughness and Λ is the correlation length) [23]. The manufacturing technology of planar Si MOSFETs on (100) surface using SiO_2 as gate dielectrics has reached a mature level. The Si inversion layer electron and hole mobility can actually be well described by universal relations [24]:

$$\mu_{eff,n} = \frac{638}{1 + (E_{eff}/7 \cdot 10^5)^{1.69}} \tag{2.14}$$

for the electron mobility, and

$$\mu_{eff,p} = \frac{240}{1 + (E_{eff} / 2.7 \cdot 10^5)} \tag{2.15}$$

for the hole mobility, where E_{eff} is the effective electric field perpendicular to the channel direction. The universal mobility curves are plotted in Fig. 2.4. Deviations from the universal behaviour are observed for advanced MOSFETs with channels in different crystal planes or orientations other than (100) and <110>, strained channels, or devices with high-k gate dielectrics. Techniques to enhance the mobility by strain engineering or locating the channel in a more favourable direction are currently intensively studied, see chapter 2.4 for further discussion.

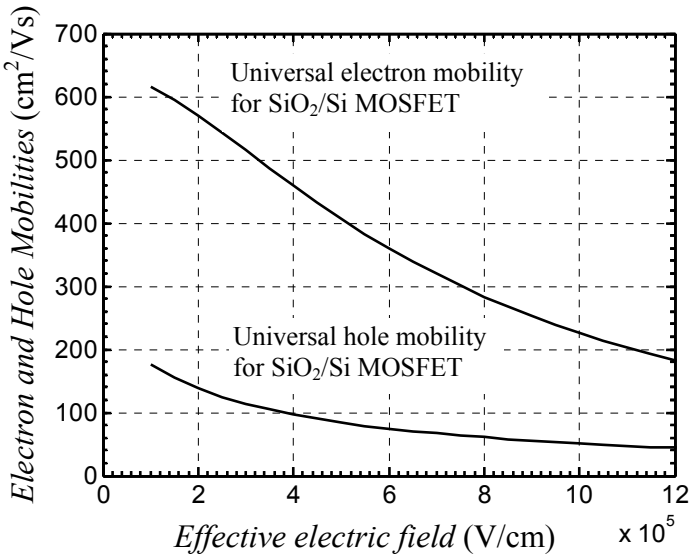

Fig. 2.4. Universal electron and hole mobilities vs. effective electric field.

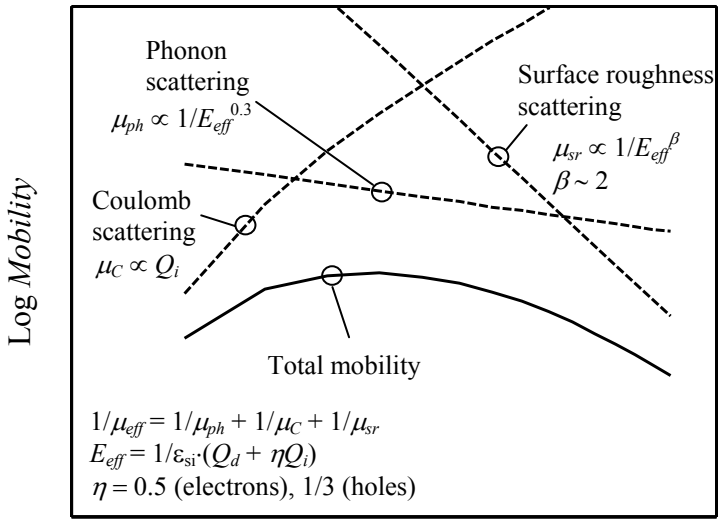

Fig. 2.5. Schematic description of the E_{eff} and Q_i dependence of the mobility in an inversion layer of a MOSFET and how different scattering mechanisms affect the mobility.

The mobility in Si MOSFETs has been investigated extensively and the different scattering sources are well understood. The different scattering mechanisms depend in different ways on the effective electric field and temperature. Fig. 2.5 shows a schematic diagram of the E_{eff} dependencies and describes how the different scattering mechanisms generally affect the mobility [19].

Phonon scattering and Coulomb scattering are both strongly temperature dependent, whereas surface roughness scattering has a weaker dependence on temperature. Since the lattice vibrations increase with increasing temperature (more phonons are excited), the phonon limited mobility decreases. The thermal velocity of the carriers increases by increasing temperature. The carriers will then have a shorter interaction with the charged impurities resulting in reduced Coulomb scattering. For bulk semiconductors, temperature relation $\mu_b \propto T^{-3/2}$ and $\mu_C \propto T^{3/2}$ have been observed [25].

2.3 Electrical characterization

2.3.1 I-V characterization

The first step in the device evaluation process is to perform *I-V* characterization and measure the terminal currents versus applied voltage. A parameter analyzer, connected to Source-Measure Units (SMUs) on a shielded probe-station with triax cables, is typically used for sensitive and disturbance free *I-V* measurements. Several device properties and parameters can be deduced from the *I-V* characterization. The threshold voltage is extracted from I_D-V_{GS} measurements at low V_{DS} where the extrapolated maximum tangent on the I_D-V_{GS} curve intersects with the voltage axis. The extracted voltage is then reduced by $V_{DS}/2$. Another method outlined by Ghibuado uses the intercept of the $I_D / g_m^{1/2}$ function to derive the threshold voltage [26]. However, the extracted threshold voltage is not exactly the same as the theoretical threshold voltage in Eq. (2.5) but somewhat higher. Thus, the threshold voltage is not uniquely defined. The transconductance, defined as

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{2.16}$$

is an important parameter for analog circuit designers and can easily be extracted from I_D-V_{GS} curves. The low-field transconductance, measured at low V_{DS}, is also useful to study in order to estimate the carrier mobility. I_D-V_{GS} measurements at different gate lengths are used to extract the source/drain series resistances R_{SD} and the electrical channel length $L_{mask} - \Delta L$. A simple method to extract these parameters is to plot the total resistance R_{tot} versus the written channel length L_{mask}.

$$R_{tot} = \frac{V_{DS}}{I_D} = R_{SD} + R_{ch} \approx R_{SD} + \frac{L_{mask} - \Delta L}{\mu_{eff} C_{ox} W (V_{GS} - V_T)} \tag{2.17}$$

The point where the curves intersect gives R_{SD} and ΔL directly. An improved approach to the one outlined above, also somewhat more cumbersome, is the shift-and-ratio method [17]. These two methods typically give $R_{SD} \cdot W$ values in the range 1-3 kΩ·μm for most of the pMOS transistors used in this work.

2.3.2 C-V characterization

The gate oxide capacitance is typically measured in two configurations shown in Fig. 2.6(a). The gate-to-channel configuration measures the change in inversion charge with applied voltage

$$C_{GC} = \frac{dQ_I}{dV_{GS}} \tag{2.18}$$

Capital letters in the subscript of C and Q is used when normalization to gate area is not done. An accumulation charge or depletion charge cannot communicate with the S/D terminals. In strong inversion, $C_{GC} = WLC_{ox,eff}$, whereas C_{GC} approaches zero below threshold as Q_I decrease exponentially. Poly-depletion and inversion layer quantization effects reduce the effective oxide capacitance, $C_{ox,eff} < C_{ox} = \varepsilon_{ox}/t_{ox}$.

$$\frac{1}{C_{ox,eff}} = \frac{1}{C_{ox}} + \frac{z_{av}}{\varepsilon_{si}} + \frac{W_{poly}}{\varepsilon_{si}} \tag{2.19}$$

The second term is due to the quantization effect locating the inversion charge on average a distance z_{av} from the interface and the last term is the capacitance of a depletion layer W_{poly} in the poly-silicon gate. Scaling the oxide capacitance will become an important problem in the future due to the limitations caused by the quantization and the poly-depletion effects. A stretch-out of the C_{GC} curve is sometimes observed, which is due to interface states acting in parallel with the inversion charge. The charge in the interface states is unable to follow a fast switching ac signal; the measurement frequency should be sufficiently high, typically between 100 kHz - 1 MHz, to mitigate the influence of the interface states on the capacitance.

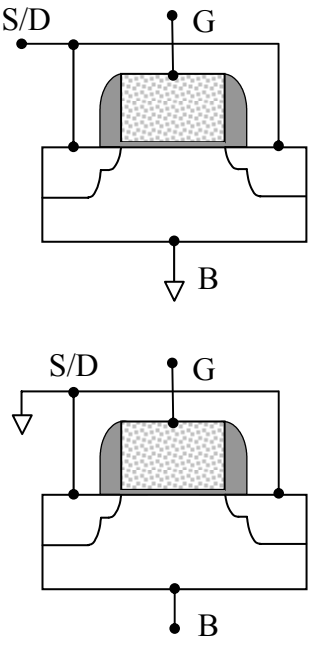

Fig. 2.6(a). Bias configurations to measure C_{GC} (top) and C_{GB} (bottom).

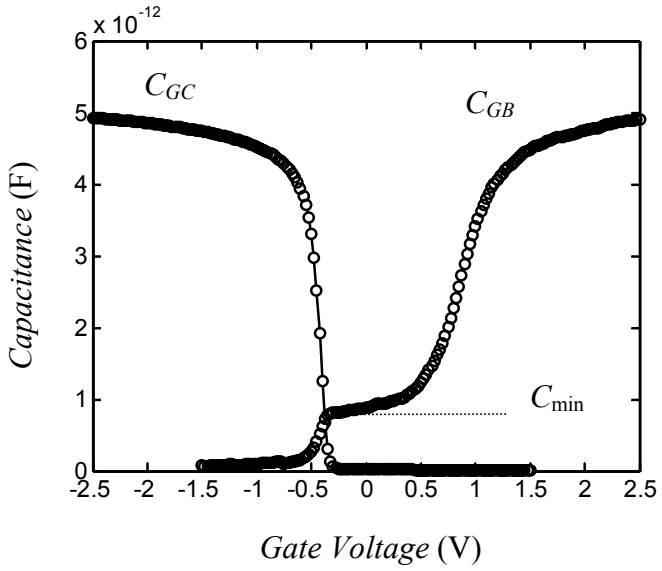

Fig. 2.6(b). C_{GC} and C_{GB} characteristics taken from a Si pMOSFET with high-k gate dielectrics.

The gate-to-substrate capacitance is measured with S/D grounded and therefore approach C_{ox} in accumulation and the series combination of C_{ox} and $C_d = \varepsilon_{si}/W_d$ in depletion. At the onset of strong inversion, the depletion layer reaches its maximum width. The depletion charge does not change with bias in strong inversion and C_{GB} goes to zero. The flat-band capacitance can be calculated from the C_{GB} curve as

$$\frac{1}{C_{fb}} = \frac{1}{C_{ox}} + \sqrt{\frac{kT}{\varepsilon_{si} q^2 N_{sub}}} \tag{2.20}$$

where the substrate doping concentration can be determined by solving

$$N_{sub} = \frac{4kT \ln(N_{sub}/n_i)}{\varepsilon_{si} q^2 (1/C_{\min} - 1/C_{ox})^2} \tag{2.21}$$

An analytic solution is not available so one has to resort to numerical procedures, e.g. iteration techniques. $C_{\min}$ is the capacitance value at the onset of strong inversion and is defined in Fig. 2.6(b). The flat-band voltage can be obtained from the graph as the voltage where $C_{GB} = C_{FB}$. The flat-band voltage can be shifted if the oxide contains charge. The oxide charge at flat-band can be calculated as follows

$$Q_{ox} = -C_{ox}\Delta V_{fb} = -C_{ox}(V_{fb} - \phi_{ms}) \tag{2.22}$$

Thus, a negative charge increases the flat-band voltage and vice versa.

2.3.3 Mobility extraction

The mobility can be obtained from *I-V* measurements in the linear regime at small V_{DS} by rearranging Eq. (2.4)

$$\mu_{eff} = \frac{I_D L}{W C_{ox}(V_{GS} - V_T) V_{DS}} \tag{2.23}$$

However, the mobility is not accurately determined close to threshold. The reason is twofold. First, the threshold voltage is not well-known, and second, Eq. (2.4) is based on the approximation $Q_i = C_{ox}(V_{GS} - V_T)$ that is not correct close to threshold.

The "split-CV" technique [24] uses the gate-to-channel capacitance to determine Q_i

$$Q_i = \int_{-\infty}^{V_{GS}} C_{gc} dV'_{GS} \tag{2.24}$$

The mobility is then calculated from

$$\mu_{eff} = \frac{g_{ds} L}{W Q_i} \tag{2.25}$$

where the source-drain conductance is defined by

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} \tag{2.26}$$

To obtain the best results, g_{ds} should be measured at low drain bias (~20-50 mV). An improved split-CV technique has also been proposed, which allows Q_i to be measured under a finite V_{DS} which gives the correct Q_i to be used in Eq. (2.25) as g_{ds} is obtained from a nonzero V_{DS}. The electric field is computed as

$$E_{eff} = \frac{1}{\varepsilon_{si}}\left(Q_d + \eta Q_i\right) \tag{2.27}$$

with η usually taken as 1/2 for electrons and 1/3 for holes, respectively. The effective field is the average field on the carriers, therefore the factor 1/2, $\eta = 1$ would be used to calculate the field right below the oxide interface. However, the factor 1/3 for holes is empirical; the physical reason has not been clarified yet. The depletion charge Q_d is obtained from the following integration

$$Q_d = \int_{V_{fb}}^{V_{GS}} C_{gb}\, dV'_{GS} \tag{2.28}$$

The split-CV method, as described above, has been employed to extract the carrier mobility throughout this work. However, Eq. (2.23) has sometimes been used for mobility estimations in transistors with gate lengths ≤ 1 μm.

2.3.4 Charge-pumping measurements

The oxide/channel interface contains electronic states with energies within the forbidden bandgap (see e.g. ref. [27] for a review). These interface states act as carrier traps and cause increased subthreshold slope and degradation of the mobility through Coulomb scattering. Traps within the gate oxide is also one of the two major sources behind the low-frequency noise in MOS transistors. The density of the interface states can be measured using the charge pumping technique [28]. Fig. 2.7(a) depicts the measurements setup. The source and drain are tied together and slightly reverse biased. A time varying rectangular pulse is applied on the gate. The charge pumping current I_{cp} is measured as function of V_B at the bulk terminal. A typical I_{cp} waveform is shown in Fig. 2.7(b). The current consists of carriers supplied by the substrate to recombine with carriers trapped in the interface states. Only carriers with the density $D_{it}\Delta E$ in the energy interval ΔE are available for recombination, the rest has been emitted. The density of interface states is given from the plateau value of the charge pumping current as

$$D_{it} = \frac{I_{cp}}{WLfq\Delta E} \quad [\mathrm{cm^{-2}eV^{-1}}] \tag{2.29}$$

where f is the frequency of the rectangular gate pulse. The energy interval was derived by Groeseneken *et al*. to be [28]

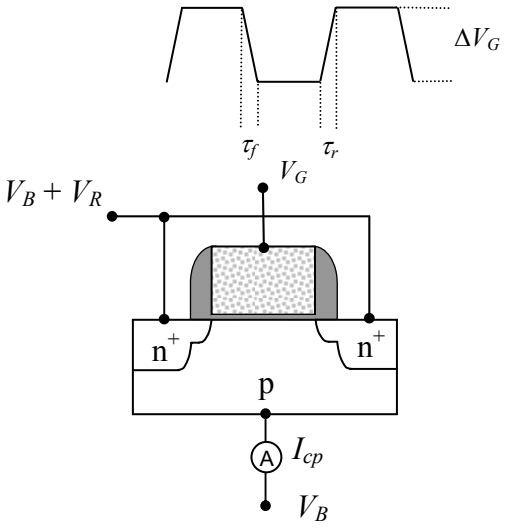

Fig. 2.7(a). Setup for charge-pumping measurement.

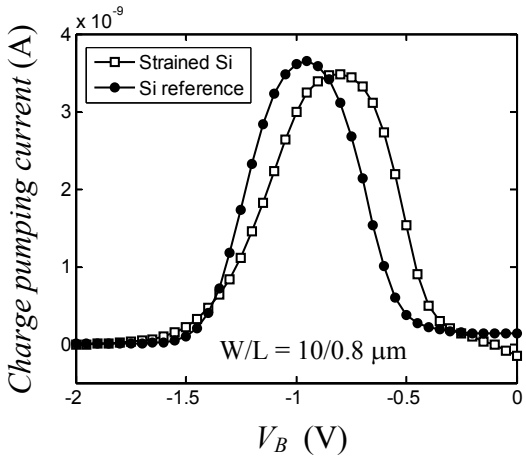

Fig. 2.7(b) Charge pumping currents for strained and unstrained Si nMOSFETs.

$$\Delta \mathrm{E} = 2kT \ln\left(v_{th} n_i \sqrt{\sigma_n \sigma_p} \frac{\left|V_{fb} - V_T\right|}{\left|\Delta V_G\right|} \sqrt{\tau_r \tau_f} \right) \tag{2.30}$$

where ΔV_G is the top-to-top amplitude of the pulse on the gate and $\tau_{r,f}$ are the respective rise and fall times. Using Eq. (2.29) gives an average value of D_{it} in the energy interval ΔE. Thermal SiO_2 of good quality demonstrate D_{it} values ~10^{10} $cm^{-2}eV^{-1}$. The energy distribution of D_{it} in the bandgap can be determined for example by employing a three-level charge pumping method or varying the rise and fall times of the gate pulse (see Eq. (2.30)). The capture cross section for electrons and holes, σ_n and σ_p, was reported for Si by Saks and Ancona to be 1×10^{-13} to 3×10^{-15} and 2-4 $\times10^{-16}$ cm^2, respectively [29]. Similar values were reported by Siergiej *et al*: $\sigma_n \approx 1\times10^{-13}$ and $\sigma_p \approx 1\times10^{-16}$ cm^2 [30]. Using $\tau_f = \tau_r = 100$ ns gives ΔE between 0.5-0.6 eV. Thus, the traps accessible for charge pumping measurement are located in the middle of the bandgap and spatially very close to the channel interface. Traps located deeper inside the oxide, typically within 3 nm from the channel interface, and near the Fermi level energy can be probed by low-frequency measurements, the topic of the coming chapters. These two measurement techniques complement each other for evaluation of traps in the gate oxide and at the gate oxide/channel interface.

2.4 Advanced MOSFET concepts

The main driver of the enhanced performance of CMOS devices has, up to now, been the downscaling of device dimensions. Fig. 2.8 shows how the MOS transistor gate length in Intel® Processors has evolved from 1971, when the first processor was presented, to 2004 [31]. Tremendous advances in fabrication technology, especially lithography techniques, have made the rapid downscaling possible. The maximum clock frequency that can be used in a circuit is ultimately restricted by the delay of its building blocks, the transistors. A commonly used figure of merit for the internal delay of a MOS transistor is the CMOS inverter delay given below

$$\tau = \frac{C_G V_{DD}}{I_{D,sat}} \tag{2.31}$$

where C_G is the gate capacitance (not per unit area) and V_{DD} is the circuit supply voltage. Inserting Eq. (2.10) for $I_{D,sat}$ and assuming $V_{DD} >> V_T$ gives $\tau \propto L^2/\mu_{eff}V_{DD}$. As can be seen, the speed increases quadratically with decreasing gate length. For analog applications, which this thesis mainly deals with, the transition frequency f_T is of utmost importance. The transition frequency is defined as the frequency where the current gain of the transistor has dropped to one. Thus,

$$f_T = \frac{g_m}{2\pi C_{GS}} = \{\text{using Eq.}(2.10)\} = \frac{3\mu_{eff}(V_{GS} - V_T)}{4\pi m L^2} \tag{2.32}$$

Obviously, improved mobility and decreased gate length give enhanced device speed. However, several unwanted effects degrading the device operation and performance come into play when the device dimensions are reduced. These limitations and the demand for novel materials and device concepts are discussed in the next section.

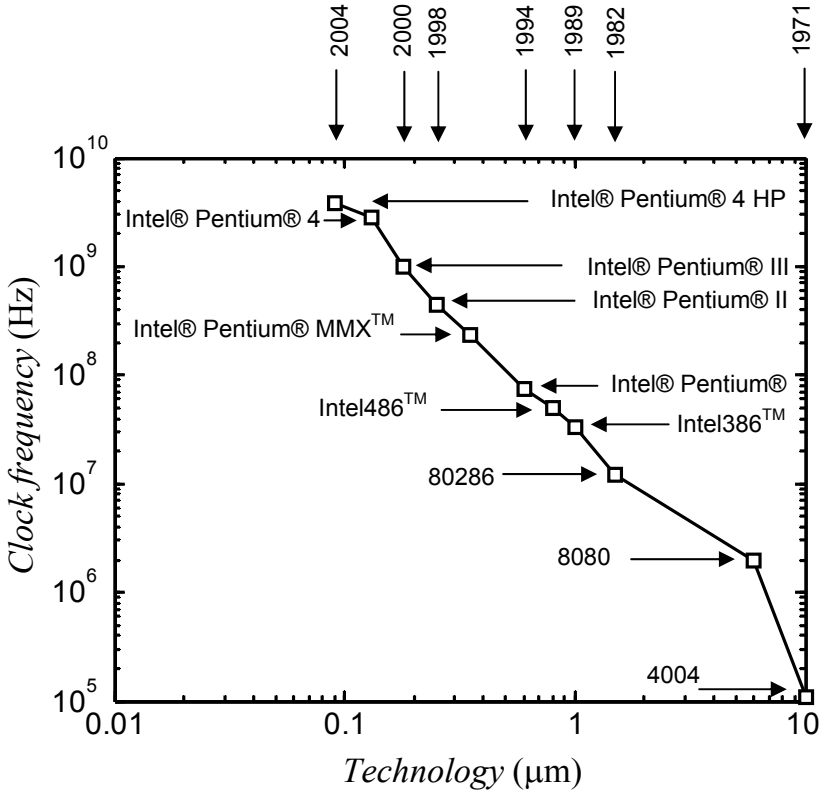

Fig. 2.8. Evolution of the clock frequency for different processor technologies. The MOSFET gate length is related to the technology dimension, but somewhat smaller.

2.4.1 Demand for novel materials and advanced device concepts

The short-channel effect (SCE) became a problem already in the early 1970-ties when the shortest gate length was around 1-μm [32]. The gate loses control over the channel as the gate length is scaled down, which leads to a reduced threshold voltage and

increased off-current for short channel lengths. Another related effect is the Drain-Induced-Barrier-Lowering (DIBL), causing a further reduction in the threshold voltage and the off-current when a high drain voltage is applied. One can illustrate this as the source and drain depletion regions take up a larger share of the total depletion region under the channel, less charge is controlled by the gate (charge-sharing model) [33]. Three simple remedies to control the SCE and the DIBL are consequently decreased S/D junction depth, increased channel doping and decreased oxide thickness. Decreasing the supply voltage will also alleviate the problem with DIBL. To keep control of the SCE and DIBL, rules involving scaling of several device and circuit parameters with a common multiplicative factor were proposed [34]. The device dimensions t_{ox}, L, W, x_j are scaled with a factor $1/\kappa$, where $\kappa > 1$. The channel doping concentration is scaled with κ, and the supply voltages with $1/\kappa$. Scaling according to these rules will keep the electric field constant (constant-field scaling). Later a generalized scaling scheme intended to preserve the shape of the electric field was introduced, involving two scaling factors [35]. The scaling predictions for an nMOS analog speed device according to the ITRS roadmap are summarized in Table I. The shaded areas point out problems for which manufacturable solutions are not known.

Table I. Scaling of NMOS analog speed device according to the ITRS roadmap[1]

Year	2004	2007	2010	2013	2016
Technology node (nm)	90	65	45	32	22
Physical gate length[2] (nm)	65	37	25	18	13
Supply voltage (V)	1.2	1.1	1.0	0.9	0.8
EOT (physical) (nm)	2.1	1.6	1.3	1.1	0.9
g_m/g_{ds} @ $5 \cdot L_{min}$[3]	100	100	100	100	100
$1/f$ noise[4] ($\mu V^2 \cdot \mu m^2$/Hz)	200	150	150	100	75

(1) 2004 update, see http://public.itrs.net/
(2) Low Standby Power (LSTP) technology
(3) Measure of amplification of a 5×min gate length of a LSTP CMOS transistor. V_{GS}-V_T = 0.1 V.
(4) Input gate voltage $1/f$ noise spectral density at 1 Hz. V_{GS}-V_T = 0.1 V.

Unfortunately, several unwanted effects arise from the scaling. The mobility is degraded as the doping concentration is increased due to higher effective field. Moreover, the source and drain resistance must be scaled down in relation to the channel resistance, which is increasingly difficult as the junction depth decreases. Reliability and power, which are associated with higher field intensity, become serious problems in the generalized scaling scheme. The tunneling current through the gate oxide increases exponentially with decreasing thickness. Eventually, for physical oxide thicknesses around 1-1.5 nm the gate leakage current become unacceptably high [1]. Poly-depletion effects will limit the effective oxide capacitance as mentioned before. All these effects mentioned above demonstrate the need to find alternative materials and device concepts to enhance mobility, control the short channel effects, limit the gate leakage current etc. Some non-classical CMOS concepts investigated in this thesis are described in the following sections. Finally, as mentioned in the introduction, the downscaling of the supply voltage and the device dimensions cause a degradation of the signal-to-noise ratio. It has been suggested that the low-frequency noise, which depend inversely on the gate area, can be a showstopper for CMOS scaling in certain applications [5]. The main topic of this thesis is to investigate the low-frequency noise properties of advanced CMOS devices that may reside in future analog and digital applications and improve the understanding of the physical

mechanisms causing the low-frequency noise. This work can serve as a guideline how to design a device for low noise and which materials and structures that should be avoided.

2.4.2 SiGe channel pMOSFETs

Compressively strained SiGe channel pMOSFETs exhibit enhanced hole mobility compared to their Si counterparts, as demonstrated in Fig. 2.9(a), which makes them attractive for future CMOS applications. A schematic structure and a band diagram of a pMOSFET with a buried SiGe channel is illustrated in Figs. 2.9(b) and 2.9(c), respectively. $Si_{1-x}Ge_x$ has a larger lattice constant than Si, varying with Ge composition x between 5.43 Å (Si) to 5.66 Å (Ge). When SiGe is epitaxially grown on Si, the larger lattice constant of the former results in a biaxial compression of the SiGe layer for it to fit with the Si lattice. There is a critical thickness of the layer and maximum Ge concentration, which depend on each other, for the strain in the SiGe layer to remain [36]. Beyond this limit, undesired relaxation occurs. The compressive strain introduce splits and distortion in the energy band spectrum, which result in

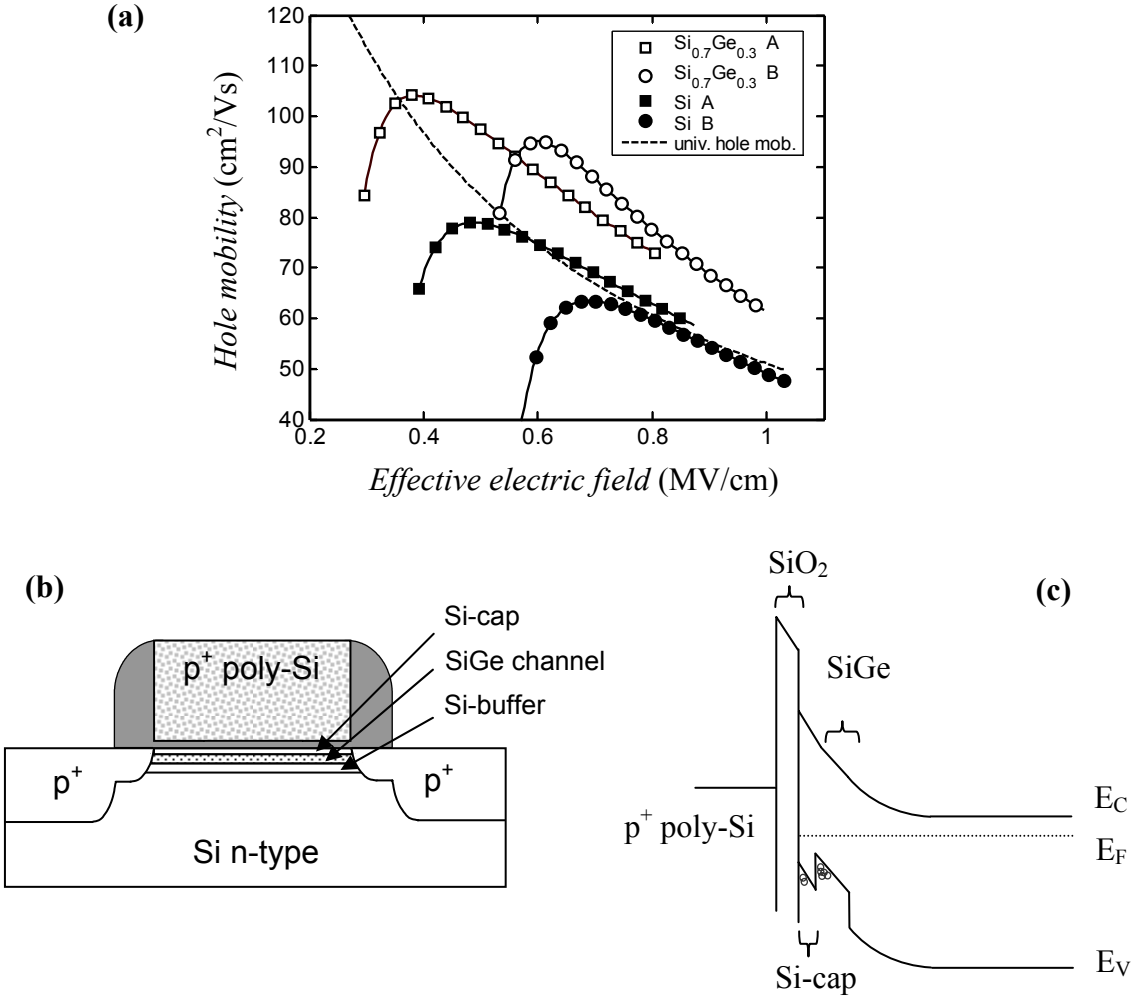

Fig. 2.9. (a) Hole mobility vs. effective electric field for $Si_{0.7}Ge_{0.3}$ and Si pMOSFETs, data from papers I and II. (b) Schematic cross section of a buried SiGe channel pMOSFET. (c) Energy band diagram of a MOS structure with a buried SiGe layer.

lower effective hole mass in the valence band of the SiGe and therefore enhanced hole mobility [37, 38]. The bandgap of the compressively strained $Si_{1-x}Ge_x$ also varies with x according to [39]

$$E_g(x) = 1.12 - 0.896x + 0.396x^2 \ \text{[eV]} \quad (x < 0.3) \tag{2.33}$$

Some additional physical properties of $Si_{1-x}Ge_x$ are summarized in appendix I. Around 97% of the bandgap offset is situated in the valence band [40]. This property can be exploited in a buried SiGe channel pMOSFET, confining holes in a quantum well away from the Si/SiO_2 interface, see Fig 2.9(c). This further enhances the hole mobility due to lower surface scattering. Lower $1/f$ noise has also been observed for buried SiGe pMOSFETs, which is an additional benefit of this type of device. It should be mentioned that the Si-cap on top of the SiGe channel is necessary also to maintain a low interface state density, since oxidation of SiGe introduce traps that deteriorate the interface [41, 42].

However, several reports have shown that the hole mobility enhancement in the SiGe channel is reduced when the channel length is decreased, which is a key problem that remains to be solved. Several reasons have been suggested: velocity saturation [43, 44], more pronounced effects of pocket implantations for SiGe [44-46], longer electrical channel length for SiGe due to reduced boron diffusion [47], and strain relaxation effects for shorter channels [45, 48]. Paper II in this thesis demonstrates drive current and transconductance enhancements down to 50-nm gate length by using SiGe. It was found that the transconductance increased with decreasing width of the SiGe channel, suggesting strain improvements from the field oxide or local loading effects altering the thickness and/or composition of the Si-cap/SiGe/Si-buffer stack in such a way that it improves the hole confinement in the SiGe channel. Integration of SiGe with SOI technology has shown very promising results down to 50 nm channel length [49]. In paper III, the low-frequency noise and mobility in SiGe channel fully-depleted SOI MOSFETs were investigated, promising results were obtained demonstrating the usefulness of this technology for future analog applications. The utilization of multiple SiGe well structures [48], a narrow channel width, or SiGe on SOI are alternative ways forward to achieve enhanced performance also at sub-100 nm gate lengths. Optimizing the Si-cap thickness is also important, both for drive current and noise performance. The Si-cap degrades the gate control of the SiGe channel; the effective gate oxide capacitance is lower as the capacitance of the Si-cap, ε_{si}/t_{cap}, acts in series with the oxide capacitance. Furthermore, a parasitic low-mobility channel is formed in the Si-cap, lowering the overall mobility of the transistor at high gate voltage overdrives [40]. For high drive current the Si-cap should be as thin as possible without causing degradation of the interface by a high density of traps. However, for low $1/f$ noise other considerations prevail, which is discussed in paper I.

2.4.3 Strained Si nMOSFETs

Enhancements of electron and hole mobilities in Si inversion layers from their universal values are possible by strain engineering [50]. Strain enhanced Si-channel mobility in MOSFETs can be realized by local strain techniques such as using silicon nitride capping layer (nMOS) or compressively strained SiGe films in the source/drain regions (pMOS) [51] as well as global techniques such as strained Si on relaxed SiGe virtual substrates (mainly nMOS) [52, 53] or strained Si on SiGe-on-insulator [54]. Techniques to obtain improved MOSFET channel mobility is currently a hot research

subject; there are several degrees of freedom and options in the type of strain, channel direction and crystal direction to achieve enhanced performance both for nMOS and pMOS devices [55]. In the following, we will concentrate our efforts on nMOSFETs with a strained Si-channel. The electron mobility is enhanced by tensile strain, which is induced in the thin epitaxial Si layer grown on a relaxed SiGe virtual substrate. The tensile strain causes an energy splitting of the 6-fold degenerate conduction band, resulting in a repopulation of the energy bands that preferentially fills the 2-fold band with lower energy and reduced effective mass. The strain-induced electron mobility enhancement is stronger for long channel lengths, as was the case for compressively strained SiGe channel pMOSFETs, but drive current improvements even in sub-50 nm gate length MOSFETs have recently been observed [56]. Strained-Si technology is under development at KTH in collaboration with European partners in the SiNano project, fabricating devices on a 200-nm thin relaxed $Si_{0.8}Ge_{0.2}$ virtual substrate. Fig. 2.10 shows the first results; the maximum low-field transconductance is enhanced by 50 % compared to the reference Si device. The low-frequency noise results from these devices are presented in chapter 6.

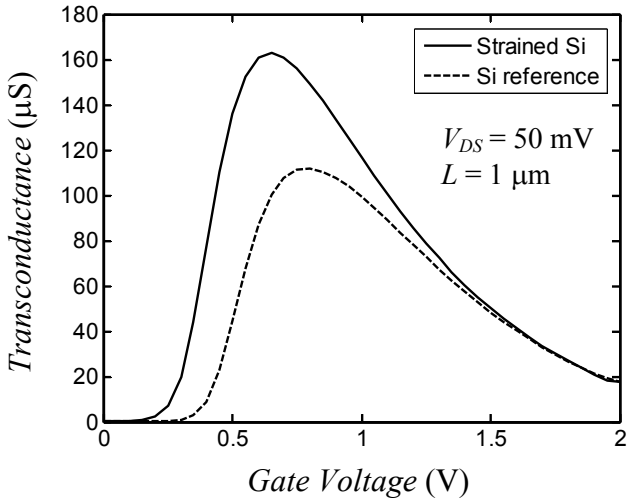

Fig 2.10. Low-field transconductance plotted vs. gate voltage for a strained Si (20% Ge) and an unstrained Si nMOSFET.

2.4.4 High-k gate dielectrics

As the gate length is scaled down, the gate oxide needs to be thinned in order to control the short channel effects. Unfortunately, the gate tunneling current increases exponentially with decreasing thickness [57]. For oxide thicknesses around 1-1.5 nm, depending on application, the gate leakage current become intolerable high [1]. A high gate leakage current causes problems such as increased standby power consumption, deteriorated reliability and lifetime, and can ruin the whole device operation. By replacing the SiO_2, which has a dielectric constant k of 3.9, with a material with higher dielectric constant, a so called high-k material, a physically thicker gate dielectric is allowed to achieve the same capacitance [58, 59]. The equivalent oxide thickness (EOT) is defined as

$$EOT = \frac{k_{SiO_2}}{k_{high-k}} t_{high-k} \tag{2.34}$$

which corresponds to the thickness of SiO_2 giving the same capacitance as of the high-k gate dielectric with thickness $t_{high\text{-}k}$ and dielectric constant $k_{high\text{-}k}$.

The dielectric constant is a measure of the material's polarization. The forces acting on the atom cores and the electrons in an insulator that is placed in an electric field will move them from their equilibrium positions; the moved distance is determined by the softness of the bonds. The electrons are attracted by the electric field and the positively charged atom cores are pushed in the direction of the field. Thus, the centre of the negative charge is moved towards the electric field and the positive charge with the field, creating an internal electric field opposite to the applied field. The voltage drop in the material, given by the electric field integrated over the distance, is reduced in proportion to the dielectric constant for a certain applied field. Thus, a lower voltage is required to control the charge giving rise to the applied field, which in turn implies a larger capacitance.

One of the reasons for the big success with CMOS technology is that an excellent insulator, SiO_2, has been available. To replace the silicon dioxide is therefore an enormous challenge. The high-k materials that are to replace the SiO_2 must satisfy various requirements namely: (i) thermodynamically stable together with Si, (ii) process compatible with CMOS, (iii) negligible interface layer formation, (iv) sufficient band offsets to act as tunnelling barriers for electrons and holes, (v) high quality interface with Si and (vi) low defect densities [60]. A large number of high-k materials, listed in Appendix II, have been researched in combination with CMOS and several difficulties have been encountered. From noise performance point of view it is worrying with the reports about degraded mobility [paper IV][59, 61-64] and high density of traps and fixed charges [papers IV and VII][58, 59, 65, 66]. Not surprising, most reports so far indicate 1-3 orders of magnitude higher $1/f$ noise compared to CMOS devices with thermal SiO_2 [papers IV-VIII][67-74]. The low-frequency noise properties of MOSFETs with high-k gate dielectrics have been comprehensively studied in this thesis; papers IV to VIII deal with this topic. Other problems that has been frequently observed include threshold voltage instabilities [75, 76], dopant penetration, crystallization upon heating, as well as points (i) to (vi) above. Due to these problems, the semiconductor industry has postponed the introduction of high-k materials and instead used existing technology with some modifications. By adding nitrogen to silicon dioxide, forming so called oxynitrides (SiO_xN_y), the dielectric constant is increased in proportion to the nitrogen content up to a value of 7. Oxynitrides also have the important advantage of suppressing boron penetration from a p^+ doped poly-Si gate and improving hot-carrier reliability [77, 78]. The use of oxynitride is a short term solution until some high-k gate dielectric integrated in CMOS technology is ready for mass production. Hafniumoxide (HfO_2) with a dielectric constant of 20-25, which is desired for scaling to the lowest EOTs, is the most studied high-k material and the leading contender to replace oxynitrides. Hafniumsilicates (HfSiON) might be an intermediate solution since they are more resistant to crystallization and presently have lower defect densities than HfO_2 [66].

Fig. 2.11(a) shows I_D-V_{GS} curves for surface Si and SiGe channel pMOSFETs with HfO_2 based high-k gate dielectrics. The Si device shows a low subthreshold slope of ~75 mV/dec and an interface state density of around 5×10^{11} $cm^{-2}eV^{-1}$. The hole mobility is slightly reduced compared to the universal mobility curve, as seen in Fig. 2.11(b). The origin of the lower mobility is ascribed to remote phonon scattering. The "soft" bonds in a highly polarizable material are associated with low-energy ("soft") optical phonons giving rise to additional scattering of the carriers in the remote inversion layer [79]. This scattering source does not play a major role in SiO_2 due to the stiff bond and low dielectric constant, but reduces the mobility in devices with high-k gate dielectrics roughly in proportion the value of the dielectric constant. The hole mobility in the surface SiGe channel devices is enhanced compared to Si, but suffers from Coulomb scattering from fixed charges at low electric fields. A further discussion of the hole mobility in these devices is presented in paper IV.

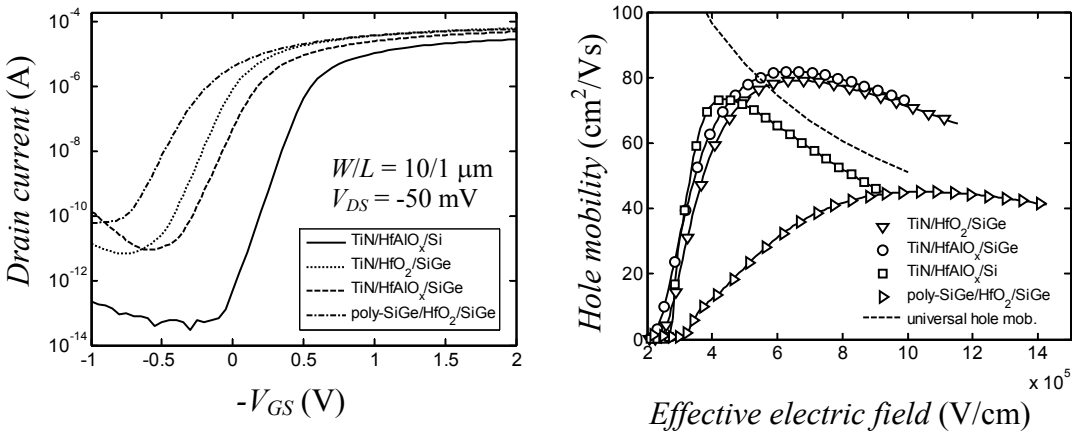

Fig. 2.11 (a). I_D-V_{GS} characteristics and (b) hole mobility for Si and $Si_{0.7}Ge_{0.3}$ pMOSFETs with HfO_2 based high-k gate dielectrics and a TiN or poly-SiGe gate (from paper IV).

2.4.5 Metal gate

The use of a metal gate instead of the poly-Si eliminates the problem with dopant penetration through the gate dielectric, Fermi-level pinning that can raise the threshold voltage of transistors with poly-Si/high-k gate stack, and poly-depletion that reduces the effective oxide capacitance [80-82]. The sheet resistance, which is important for the high-frequency properties of the device, can potentially be lower in a metal gate technology. Furthermore, if a mid-gap metal gate is used in combination with high-k gate dielectrics, the mobility degradation due to remote phonons has been reported to diminish due to more effective screening of the soft phonon modes from coupling to the channel [83]. However, the work function of the metal gate electrode material must be appropriate to give the correct threshold voltage; thermal stability and process integration are other issues. Several metal gate candidates has been investigated such as TaN, TaSiN, Mo, Ru, TiAlN (see [82] and references therein), TiN [80, 84] and fully silicided (FUSI) gates using for example NiSi [81]. We have studied TiN in combination with high-k in this work. TiN was found to be attractive both due to a higher hole mobility in the devices in comparison with the poly-SiGe gated ones, as shown in Fig. 2.11(b), and lower 1/*f* noise. The low-frequency noise properties are presented in chapter 6 as well as in paper IV.

2.4.6 Silicon-On-Insulator (SOI)

Fully depleted (FD) silicon-on-insulator (SOI) technology is very attractive for future generations of ultra-scaled CMOS devices thanks to enhanced performance in terms of high speed and low power consumption as well as improved scalability [85-90]. The MOSFET is fabricated on a thin Si body on top of a buried oxide. Fig. 2.12(a) shows a schematic cross section of SOI MOSFETs fabricated at KTH. The short-channel effect can effectively be controlled by making the Si body ultra-thin, approximately less than 1/3 of the gate length [91]. The body can actually be left undoped if it is sufficiently thin, which eliminates the Coulomb scattering from ionized impurities and lowers the effective electric field hence resulting in improved mobility. The SOI MOSFET has a very small body effect coefficient m, around 1.05-1.1 in a FD device and equal to 1 in a partially depleted (PD) device. It is readily observed from Eqs. (2.10) and (2.12) that a small m translates to a high drive current, high transconductance and small subthreshold slope. In SOI devices with source/drain junctions reaching through the body, the parasitic source and drain capacitances are also decreased.

SOI devices were for a long time mainly used in harsh-environment electronics for military, space and high-energy physics applications which require high radiation hardness. The SOI substrates used to be expensive and of moderate quality, making it difficult for the SOI technology to compete with bulk Si. But the quality of the substrates has been improved, for example the revolutionary smart-cut technology [92] provides prime quality and relatively inexpensive UNIBOND substrates, at the same time as the CMOS-technology on bulk Si is facing a number of critical limitations. The performance benefits offered by the SOI technology have now made it very attractive for CMOS logic, memories and analog circuits [85, 86, 93].

Fig. 2.12(b) shows the I_D-V_{GS} characteristics of Si and a SiGe channel FD SOI pMOSFETs with a body thickness of ~20 nm. The subthreshold slope is almost ideal ~62 mV/dec. The hole mobility shows a peak value around 130 cm^2/Vs in the Si channel device, which is a significant improvement compared to the results on bulk Si pMOSFETs (see Fig. 2.9(a)). The hole mobility in the SiGe channel device is further enhanced by 25-50 %, see figure 1 in paper III. The low-frequency noise properties of these devices are further discussed in paper III and chapter 6.

Finally, note that SOI substrates are used as the starting material to fabricate multiple-gate devices such as double-gate SOI MOSFETs, FinFETs, Omega FETs and Gate-all-around MOSFETs. A multiple-gate architecture provides an even better electro-static control of the channel by the gate, and consequently even better scalability of the technology. The concept of volume inversion, i.e. the inversion channel is formed in the middle of the thin body, can be realized by a combination of a multiple-gate architecture and a thin body (below ~10 nm in thickness). By inverting the middle of the body, the scattering and the noise generation related to the gate dielectric interface are avoided. Higher mobilities have been reported in such devices [87, 94, 95] and there are indications that the 1/f noise can be lower as well [11]. Thus, multiple-gate MOSFETs have excellent potential and have therefore been suggested as an end-of-the roadmap solution. However, such devices have not been researched in this thesis and are therefore left for future work.

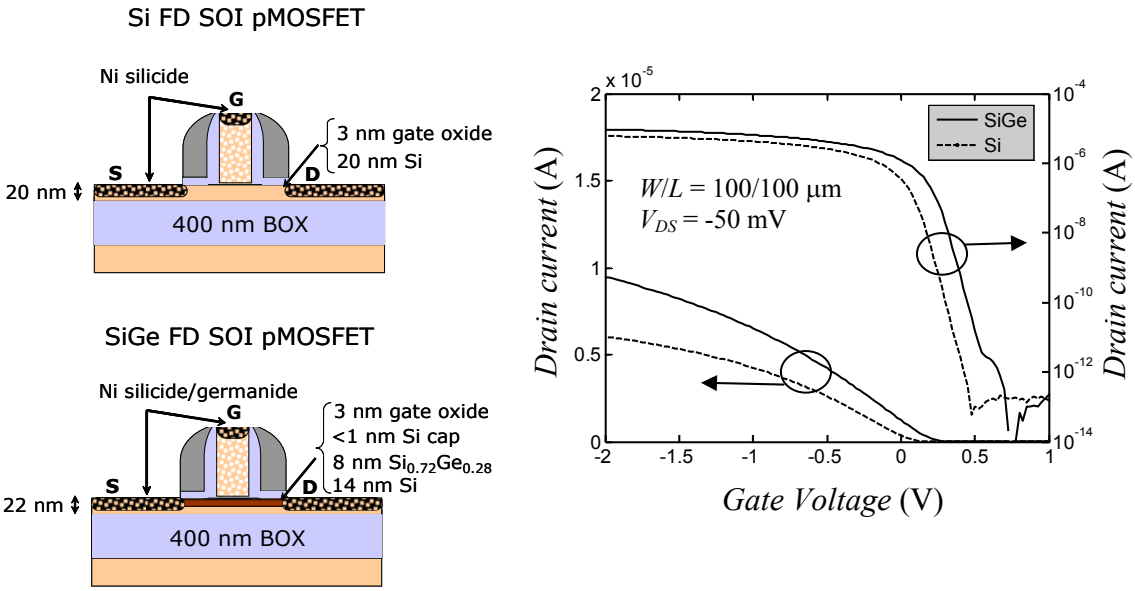

Fig. 2.12(a). Schematic cross sections and (b) I_D-V_{GS} characteristics of Si and SiGe pMOSFETs on SOI.

3. Noise mechanisms

Currents and voltages in an electronic circuit show random fluctuations around their DC bias values due to fluctuations in the physical processes governing the electronic transport. The wanted signal becomes difficult to distinguish from the background noise when the noise power is significant in relation to the signal power. Noise is a fundamental problem in science and engineering since it cannot be completely eliminated, therefore ultimately limiting the accuracy of measurements and setting a lower limit on how small signals that can be detected and processed in an electronic circuit. The importance of noise has been recognized and underlined in a variety of fields such as telecommunication, nanoelectronics, mesoscopic structures and biological systems. Noise is not only a problem that should be avoided as much as possible, the noise can actually be used as the signal to evaluate and get insight in the properties in a particular system [96]. Characterization of the low-frequency noise in electronic devices gives important information of the device physics and reliability such as scattering processes, traps and defects. This chapter begins with a background to noise, how it is defined and the mathematics involved. The fundamental noise mechanisms, thermal noise, generation-recombination noise, random-telegraph signal noise and 1/*f* noise, are discussed in section 3.2. The different noise sources in a MOSFET are analyzed in section 3.3. Finally, section 3.4 deals briefly with noise in RF circuits such as amplifiers, mixers and voltage-controlled oscillators (VCOs).

3.1 Background

True noise in an electronic device is a random, spontaneous perturbation of a deterministic signal inherent to the physics of the device. Disturbances in an electronic system originating from external sources, for example cross-talk between adjacent circuits, electrostatic and electromagnetic coupling from ac power lines, vibration, and light are not considered as noise in this work. These disturbances can often be eliminated by shielding, filtering and change of layout. True noise cannot be eliminated, but it is possible to reduce it by proper design of the devices and circuits.

Noise is a random phenomenon. At a certain location in the circuit at a certain point of time there is a probability dP that the wanted signal will be disturbed by noise with an amplitude in the interval [X, X+dX], where X is a random variable. One can define a probability density function $f(X)$ and write

$$\mathrm{d}P = f(X)\mathrm{d}X \tag{3.1}$$

The probability density function should be normalized (scaling of $f(X)$ with a constant) so that the integration over all allowed values of X yields 1. If $f(X)$ is independent of time the random process is said to be stationary, which always is assumed for the noise processes considered in this work. Practically all fluctuating currents and voltages in electrical devices are Gaussian processes due to the central limit theorem stating that the sum of a large number of independent random variables has a Gaussian distribution. One exception is the switching of the signal between two levels, random telegraph signal noise, which is a Poisson process.

For stochastic processes, several ensemble averages are defined; mean value, variance, autocorrelation function, power spectral density etc. For a stationary and

ergodic noise process, which is assumed here, the time averages equals the ensemble averages. Currents and voltages are readily measured over time and used to gain information about the noise. The time average of the noise voltage or noise current just equals zero if integrated long enough and provides no interesting information; instead square quantities are used to describe the noise. One such square quantity is the power spectral density $S(f)$ which is given from the autocorrelation function $c(s)$ according to the Wiener-Khintchine theorem

$$S_x(f) = 4\int_0^\infty c(s)\cos(2\pi fs)ds \quad [\mathrm{x}^2/\mathrm{Hz}] \tag{3.2}$$

S_x is a Fourier transformation of c, which is given by

$$c(s) = \overline{x(t)x(t+s)} = \lim_{T\to\infty}\frac{1}{2T}\int_{-T}^{T} x(t)x(t+s)dt \tag{3.3}$$

$$\text{or } c(s) = \int_0^\infty S_x(f)\cos(2\pi fs)df \tag{3.4}$$

Obviously, if $s = 0$ one obtains the variance or noise "power".

$$\overline{x(t)^2} = \int_0^\infty S_x(f)df \tag{3.5}$$

The power spectral density (PSD) is measured with a spectrum analyzer, which is discussed in chapter 5. Noise with a constant S for all frequencies is said to be white. It is usually observed that the noise spectral density is dependent on frequency at low frequencies, and becomes white thereafter. The corner frequency between frequency dependent noise and white noise is typically from a few Hz up to the MHz range and depends on the type and size of the device, bias conditions etc. The physical mechanisms behind the white noise sources are well known and the white noise level can be accurately predicted in electrical circuits. The excess noise at low frequencies, *low-frequency noise*, still raises questions and is important to study for many reasons that will be discussed shortly. In this thesis, only low-frequency noise has been studied in detail.

3.2 Fundamental noise sources

The total current at the output of a device can be written as $I(t) = I_{bias} + i_n(t)$, where I_{bias} is the bias current and $i_n(t)$ is a randomly fluctuating current. Remember that external sources that cause fluctuations in the current are not considered here. There are some fundamental physical processes that can generate the random fluctuations in the current (or voltage) in a device. These fundamental sources of noise are discussed below and described in terms of the PSD of the noise current.

3.2.1 Thermal noise

Thermal noise (Nyquist, Johnson, diffusion, velocity fluctuation noise) stems from the random thermal motion of electrons in a material. Each time an electron is scattered,

the velocity of the electron is randomized. Instantly, there could be more electrons moving in a certain direction than electrons moving in the other directions and a small net current is flowing. This current fluctuates in strength and direction, the average over (long) time is always zero. If a piece of material with resistance R and temperature T is considered, the PSD of the thermal noise current is found to be

$$S_I = 4kT/R \quad (\text{or } S_V = 4kTR), \tag{3.6}$$

where k is Boltzmann's constant [97, 98]. The thermal noise exists in every resistor and resistive part of a device and sets a lower limit on the noise in an electric circuit.

3.2.2 Shot noise

The current flowing across a potential barrier, like the pn-junction, is not continuous due to the discrete nature of the electronic charge (electrons). The current across a barrier is given by the number of carriers, each carrying the charge q, flowing through the barrier during a period of time. A shot noise current is generated when the electrons cross the barrier independently and at random. The current fluctuates with a PSD [99]

$$S_I = 2qI \tag{3.7}$$

The physics behind shot noise is closely related to the thermal noise phenomenon. A pn-junction has a non-linear resistance; the spectral density of the noise current is half the thermal noise for the dynamic resistance associated with the pn-junction. The reason behind the factor 1/2 is basically that the current is essentially flowing in one direction across the pn-junction.

3.2.3 Generation-recombination noise

Generation-recombination (g-r) noise in semiconductors originates from traps that randomly capture and emit carriers, thereby causing a fluctuation in the number of carriers available for current transport. If carriers are trapped at some critical spots, the trapped charge can also induce fluctuations in the mobility, diffusion coefficient, electric field, barrier height, space charge region width etc. Electronic states within the forbidden bandgap are referred to as traps, and exist due to the presence of various defects or impurities in the semiconductor or at its surfaces. Transitions of the following forms occur in a semiconductor

(i) free electron + free hole recombine
(ii) free electron + free hole generated
(iii) free electron + empty trap ⇆ electron bound to trap
(iv) free hole + empty trap ⇆ hole bound to trap

Note that a trap may be neutral or charged in its empty state. From the Langevin differential equation governing how the number of carriers N depend on time,

$$\frac{d\Delta N}{dt} = -\frac{\Delta N}{\tau} + H(t), \tag{3.8}$$

where $H(t)$ is a random noise term, ΔN is the fluctuation in the number of carriers and τ is the time constant, the PSD of the carrier fluctuation can be derived [100]

$$S_N(f) = 4\overline{\Delta N^2}\frac{\tau}{1+(2\pi f)^2\tau^2} \tag{3.9}$$

Here, f is the frequency. The shape of the spectrum given by Eq. (3.9) is called a Lorentzian. G-r noise is only significant when the Fermi-level is close, within a few kT in energy, to the trap level. Then the capture time τ_c and the emission time τ_e are almost equal. If the Fermi-level is far above or below the trap level, the trap will be filled or empty most of the time and few transitions occur that produce noise. The current density in n-type bulk semiconductor can be written as

$$J = \sigma E = (qn\mu_n + qp\mu_p)E \approx nq\mu_n E \tag{3.10}$$

If n fluctuates ($n = N/V$, where V is the volume), the current density fluctuates as

$$S_J(f) = \frac{S_N(f)}{N^2}J^2 \tag{3.11}$$

Thus, S_J decreases with increasing N as $1/N^2$. The variation of the PSD with the number of carriers is one way to distinguish noise originating from traps from noise related to fluctuations in the mobility, which will be described later.

3.2.4 Random-Telegraph-Signal (RTS) noise

A special case of g-r noise is the RTS noise, which is displayed as discrete switching events in the time domain, see Fig. 3.1. If only a few traps are involved, the current can switch between two or more states resembling a RTS waveform due to random trapping and detrapping of carriers. For two-level pulses with equal height ΔI and Poisson distributed time durations in the lower state τ_l and in the higher state τ_h the PSD of the current fluctuations is derived as [101].

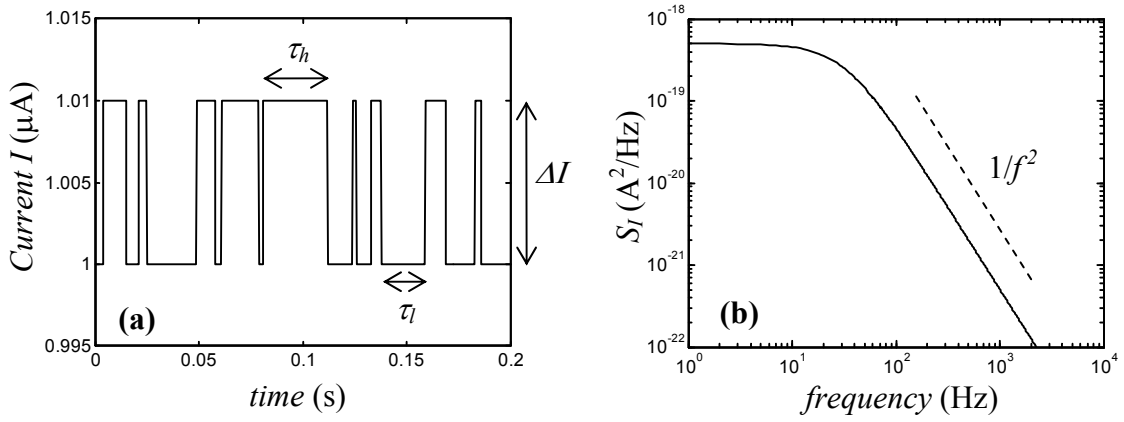

Fig. 3.1(a). RTS pulses in the time domain. (b) Lorentzian shaped power spectral density of the fluctuations in the time domain plotted vs. frequency.

$$S_I(f) = \frac{4(\Delta I)^2}{(\bar{\tau}_l + \bar{\tau}_h)\left[(1/\bar{\tau}_l + 1/\bar{\tau}_h)^2 + (2\pi f)^2\right]}, \tag{3.12}$$

The PSD for the RTS noise and the g-r noise are both of the Lorentzian type. G-r noise can be viewed as a sum of RTS noise processes from one or more traps with identical time constants, and is only displayed as RTS noise in the time domain if the number of traps involved is few. RTS noise is an interesting phenomenon from physics point of view since the random switching process from just one trap can be studied in the time domain. It is established that RTS noise is caused by a single carrier controlling the flow of a large number of carriers rather than a large number of carriers being involved in the trapping/detrapping process [8]. Interesting information about the trap energy, capture and emission kinetics and spatial location of the trap can be acquired from RTS noise characterizations. RTS noise is the topic of Paper IX where the capability of the technique is demonstrated for SiGe HBTs. RTS noise characterization can equally well be applied to study CMOS transistors, the method and theory are further discussed in chapter 5.

3.2.5 1/f noise

1/*f* noise, also called flicker noise, is the common name for fluctuations with a PSD proportional to $1/f^{\gamma}$ with γ close to 1, usually in the range 0.7-1.3. The PSD for 1/*f* noise takes the general form

$$S_I = \frac{KI^{\beta}}{f^{\gamma}}, \tag{3.13}$$

where *K* is a constant and β is a current exponent. 1/*f* fluctuations in the conductance have been observed in the low-frequency part of the spectrum (10^{-6} to 10^{6} Hz) in most conducting materials and a wide variety of semiconductor devices [14, 100, 102, 103]. Analysing Eq. (3.10) it is clear that there are essentially two physical mechanisms behind any fluctuations in the current: fluctuations in the mobility or fluctuations in the number of carriers (g-r noise). G-r noise from a large number of traps can produce 1/*f* noise if the time constants of the traps are distributed as [104]

$$g(\tau) = 1/\ln(\tau_2/\tau_1)\,\tau \quad \text{for } \tau_1 < \tau < \tau_2, \quad g(\tau) = 0 \text{ otherwise} \tag{3.14}$$

The factor $\ln(\tau_2/\tau_1)$ is for normalization purposes. The superposition of the g-r noise from many traps distributed according to $g(\tau)$ yields

$$S_{tot}(f) = \int_0^{\infty} g(\tau) S_{g-r}(\tau) d\tau = \frac{1}{\ln(\tau_2/\tau_1)} \int_{\tau_1}^{\tau_2} \frac{1}{\tau} \frac{K\tau}{1+(2\pi f\tau)^2} d\tau = \frac{1}{\ln(\tau_2/\tau_1)} \frac{K}{2\pi f} \left[\arctan(2\pi f\tau)\right]_{\tau_1}^{\tau_2}$$

$$S_{tot} \approx \frac{K}{4\ln(\tau_2/\tau_1) f} \quad \text{for } 1/2\pi\tau_2 << f << 1/2\pi\tau_1 \tag{3.15}$$

An example is given in Fig. 3.2 where g-r noise from four individual traps with different time constants adds up to a $1/f^{\gamma}$ spectrum with γ close to 1. Some remarks are necessary about the addition of g-r noise spectra. First, it is assumed that the g-r

noise from the traps can simply be added. This is true if the traps are isolated and do not interact. G-r noise is obtained with a time constant given by the reciprocal sum of all time constants if interaction occurs [105]. Secondly, the traps are assumed to couple in the same way to the output current (same K for all traps). Number fluctuation noise is discussed in more detail for the particular case of a MOSFET transistor in the next chapter.

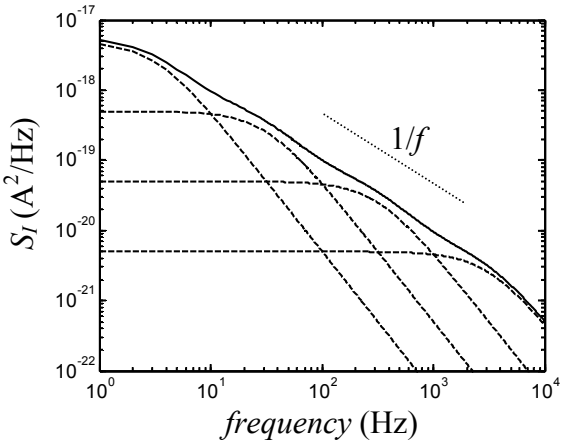

Fig. 3.2. Superposition of 4 Lorentzians that gives a total spectrum approximately showing a 1/f dependence over several decades of frequency.

The second mechanism that can give 1/*f* noise is mobility fluctuations. It was first described by Hooge with the following empirical formula for the resistance fluctuations [106]

$$\frac{S_R}{R^2} = \frac{\alpha_H}{fN} \tag{3.16}$$

The dimensionless parameter α_H, referred to as the Hooge parameter, was first suggested to be constant and equal to 2×10^{-3}. Later, it was found that α_H depends on the crystal quality; in perfect materials 2-3 order of magnitude lower values were observed. It was also proposed that only phonon scattering contributes to the mobility fluctuations (see next chapter). The factor 1/N results from independent mobility fluctuations by each of the N conducting carriers [107]. The conductivity σ is given as

$$\sigma = \frac{q}{V}\sum^{N}\mu_i = qN\overline{\mu_i}/V = qn\overline{\mu_i} \tag{3.17}$$

The conductivity fluctuates due to fluctuations in the individual carrier mobilities μ_i

$$\Delta\sigma = \frac{q}{V}\sum^{N}\Delta\mu_i \tag{3.18}$$

$$\text{independent fluctuations} \Rightarrow \overline{(\Delta\sigma)^2} = \frac{q^2}{V^2}\sum^{N}(\Delta\mu_i)^2 = \frac{q^2}{V^2}N\overline{(\Delta\mu_i)^2} \tag{3.19}$$

For the spectral density

$$\frac{S_\sigma}{\sigma^2} = \frac{S_\mu}{\mu^2} = \frac{1}{N}\frac{S_{\mu_i}}{\mu_i^2} = \frac{S_R}{R^2} \tag{3.20}$$

The PSD of the individual mobility fluctuations is then

$$S_{\mu_i} / \mu_i^2 = \alpha_H / f \,, \tag{3.21}$$

which means that α_H is proportional to the variance of the relative mobility fluctuation for each carrier, independent of the number of carriers.

The mobility fluctuation noise is always present and there is convincing evidence that the 1/*f* noise in metals and bulk semiconductors is dominated by mobility fluctuations [103]. In MOS-transistors, on the other hand, the current is flowing in a path confined close to the surface under the gate oxide. In such case, most evidence point to traps in the gate oxide as the dominant 1/*f* noise source. Nevertheless, the mobility fluctuation noise model tends to better explain the 1/*f* noise in p-channel MOSFETs [12, 108-110]. However, despite several good attempts there is still no widely accepted theoretical model for the mobility fluctuation noise. The disputed quantum noise theory of Handel explains the 1/*f* noise as fluctuations in the electron scattering due to infrared photon emission [111, 112]. An electron is decelerated when it is scattered, leading to electromagnetic field radiation, i.e. emission of photons. The photon energy, *hf*, depends on frequency, resulting in a probability of photon emission proportional to 1/*f* giving the 1/*f* fluctuations in the scattering cross section. The theory has, however, received criticism from both practical and theoretical viewpoints [113, 114]. The history of quantum 1/*f* noise research and a critical review of the theory can be found in a survey paper by Van Vliet [115]. The originally proposed model by Handel was fully confirmed by Van Vliet's quantum electrodynamical theory, but many of Handel's later additions were rejected. However, the predicted overall Hooge parameter value for Si is in the order of 10^{-8} [116], but reported values for Si MOSFETs range between 10^{-6} and 10^{-3}. Therefore, quantum 1/*f* noise may set a lower limit on the 1/*f* noise, but other sources are likely dominating the 1/*f* noise in the vast majority of devices. Furthermore, the quantum 1/*f* noise theory is difficult to reconcile with the impact of technology on the 1/*f* noise.

Another mobility fluctuation noise theory, proposed very recently by Musha and Tacano, suggests that energy partition among weakly coupled harmonic oscillators in an equilibrium system is subjected to 1/*f* fluctuations [117]. The authors derive the relationship $\alpha_H = d/\lambda_e$ where d is the lattice constant and λ_e is the mean free path of the electrons in the case of phonon scattering. It is also worth to mention the theory by Jindal and van der Ziel [118]. They propose that the phonon population exhibits g-r noise which is transferred to mobility fluctuation noise through a fluctuating phonon scattering. The idea is very interesting since it is possible that electrical g-r noise stems from g-r noise in the phonon population. The mobility and number fluctuations might even stem from the same physical mechanism. Mihaila plays with the idea that an inelastic tunneling process involving excitation of phonons is the origin of both the number and mobility fluctuation noise [119]. Next, noise modeling in MOSFETs is

discussed; the origin of the 1/*f* noise in MOSFETs is further treated in the next chapter.

3.3 Noise in MOSFETs

Electrical noise is small current or voltage fluctuations around a DC value. The small signal equivalent circuit is therefore appropriate to use for modeling. A noisy resistance is represented with a noiseless resistance in parallel with a noise current generator (Norton equivalent) or in series with a noise voltage generator (Thevenin equivalent), see Fig. 3.3. A resistance always generate thermal noise but may also exhibit superimposed 1/*f* noise. Similarly, other elements like p-n junctions and the channel of a MOS-transistor can be represented by a noiseless element in parallel or in series with a noise generator. A MOSFET is a complex device containing purely resistive parts and a channel which conductance is controlled by the gate voltage. Usually, the 1/*f* noise at the output is generated in the channel, but the 1/*f* noise originating from the S/D resistance contributes and may even take over as the dominant source at high drain currents. The low-frequency noise equivalent circuit of a MOSFET is shown in Fig. 3.4. For a short-circuited output, the total output drain current noise PSD from the uncorrelated noise sources in the channel and the S/D regions can be expressed as

$$S_{I_{D_{tot}}} = \frac{S_{I_{D,ch}} + g_{ch}^2 R_D^2 S_{I_{R_D}} + R_S^2 \left(g_m + g_{ch}\right)^2 S_{I_{R_S}}}{\left[1 + g_m R_S + g_{ch}(R_S + R_D)\right]^2} \tag{3.22}$$

For the general case with a load resistance R_L at the output, the output drain current noise is

$$S_{I_{D_{tot}}} = \frac{S_{I_{D,ch}} + g_{ch}^2 R_D^2 S_{I_{R_D}} + R_S^2 \left(g_m + g_{ch}\right)^2 S_{I_{R_S}} + S_{I_{R_L}} \left(1 + g_m R_S + g_{ch}(R_S + R_D)\right)^2}{\left[1 + g_m R_S + g_{ch}(R_S + R_D + R_L)\right]^2} \tag{3.23}$$

The drain current noise is the superposition of several noise sources with different spatial location and with different physical origins. The lower limit of the noise is always (white) thermal noise or shot noise. On top of the white noise, 1/*f* noise is

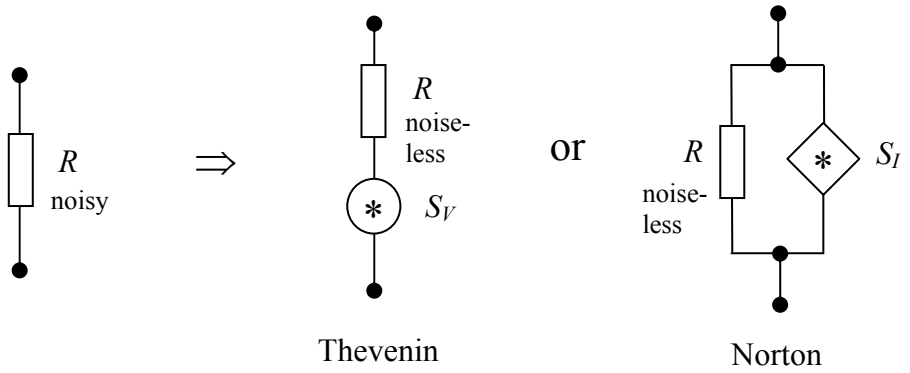

Fig. 3.3. Representation of a noisy resistor with Thevenin or Norton equivalent circuits.

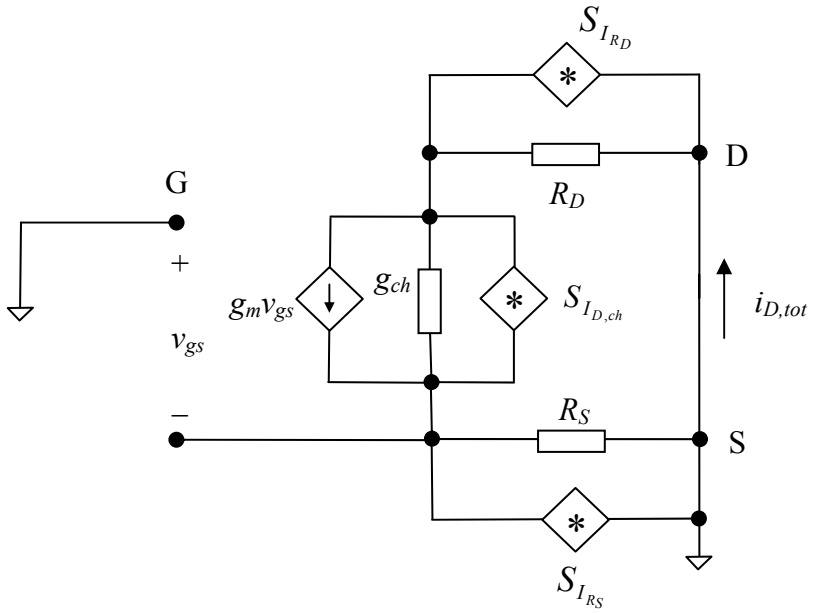

Fig. 3.4. Small-signal equivalent circuit of a MOSFET including noise sources.

usually present, and g-r noise can also be observed, especially in MOSFETs with a very small gate area (~0.1 μm^2). The total drain current noise has typically the appearance depicted in Fig. 3.5.

The noise originating from the S/D resistance can be modeled by a sum of thermal noise and mobility fluctuation 1/*f* noise

$$S_{I_{R_{S,D}}} = \frac{\alpha_{H,S/D} I_D^2}{fN} + 4kT / R_{S,D} \tag{3.24}$$

The thermal noise in the channel depends on the operating condition [120]

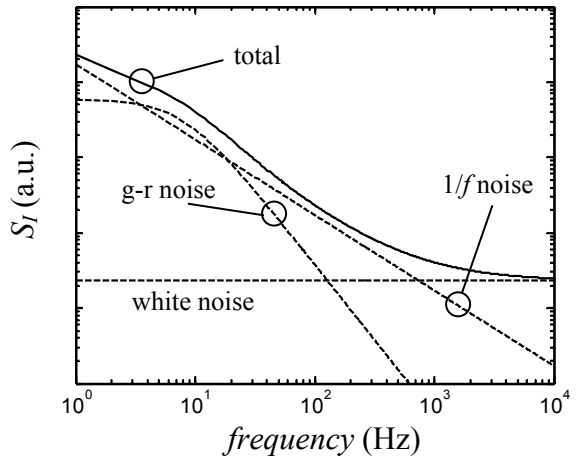

Fig. 3.5. The total noise is a superposition of 1/f noise, g-r noise and white noise. The thermal noise is always present, here 1/f noise and a g-r noise Lorentzian are also observed.

$$S_{I_{ch,thermal}} = 4kT\left[\frac{W}{L}\mu_{eff}C_{ox}(V_{GS}-V_T)\frac{2}{3}\frac{1+\eta+\eta^2}{1+\eta}\right], \tag{3.25}$$

where η is defined as

$$\eta = \begin{cases} 1-V_{DS}/V'_{DS}, & V_{DS} \le V'_{DS} = (V_{GS}-V_T)/m \\ 0, & V_{DS} > V'_{DS} \end{cases} \tag{3.26}$$

Thus, in the linear region at a small V_{DS}, $\eta \approx 1$

$$S_{I_{ch,thermal}} = 4kT\left[\frac{W}{L}\mu_{eff}C_{ox}(V_{GS}-V_T)\right] = 4kTg_{ch} \tag{3.27}$$

and in the saturation region where $\eta = 0$

$$S_{I_{ch,thermal}} = 4kT\left[\frac{W}{L}\mu_{eff}C_{ox}(V_{GS}-V_T)\frac{2}{3}\right] = 4kTg_m\gamma \tag{3.28}$$

From theory, the coefficient γ equals 2/3 if m = 1, but can be higher in short channel MOSFETs due to hot carrier effects for example. The channel 1/*f* noise is discussed in detail in chapter 4.

3.4 Noise in circuits

The design of RF and analog circuits involve several considerations and trade-offs such as gain, power dissipation, linearity, noise, speed, voltage swings, input/output impedance and supply voltage [121]. In contrast, digital circuits are primarily optimized by the trade-off between speed and power consumption. The complexity of the RF design entails specialized characterization and accurate modeling of the RF devices. Noise is one of the key difficulties in the RF and analog circuit design, it is therefore of utmost importance to have a good understanding of this phenomenon on transistor level and how it couples out to circuits. In this section, noise considerations for amplifiers, voltage controlled oscillators and mixers will be discussed. Note that "noise coupling" effects, for example the coupling of power supply and transistor switching disturbances through the substrate, are not treated here.

3.4.1 Low-Noise Amplifiers (LNAs)

A low-noise amplifier is used in the first stage of a receiver system to amplify the weak signal received from the antenna. The signal-to-noise level is inevitably degraded after amplification since the noise of the amplifier is added to the total noise power. Designing the LNA with low internal noise is therefore of enormous importance. A commonly used measure of the noise performance is the noise factor *F* or the noise figure NF = 10log*F*. The noise factor is defined in terms of the input and output signal-to-noise ratios (*SNR* = Signal power/Noise power) as

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{3.29}$$

The noise power is integrated over the bandwidth $\Delta f = f_2 - f_1$ of the amplifier

$$\overline{i_n^2} = \int_{f_1}^{f_2} S_I(f)df \quad \text{and} \quad \overline{v_n^2} = \int_{f_1}^{f_2} S_V(f)df \tag{3.30}$$

An RF amplifier is designed to work at frequencies in the GHz range, the contribution from the device $1/f$ noise is obviously negligible and only thermal noise is important for the total noise power. Even for an amplifier working in a small bandwidth at low frequencies down to DC, $1/f$ noise is not critical as the devices in such an amplifier can be designed to be large and therefore with low $1/f$ noise as the requirement on device speed is relaxed. Assuming only thermal noise, the noise power is equal to $S \cdot \Delta f$. The internal noise of the amplifier can be represented with two equivalent sources at the input according to Fig. 3.6. The noise factor can then be written as follows (assuming uncorrelated sources)

$$F = \frac{S_{V_{R_S}} + S_{V_n} + S_{I_n} R_S^2}{S_{V_{R_S}}} \tag{3.31}$$

The noise of the amplifier depends on the gain, thermal noise of the transistor(s) and on the impedance matching network. The minimum noise figure of the CMOS transistors is reduced as their cut-off frequency increase for smaller gate lengths [122, 123]. However, as scaling continues, increased gate leakage currents, greater impact of velocity saturation and increased importance of substrate resistance as well as higher $1/f$ noise due to miniaturization of device sizes will lead to higher RF noise [124].

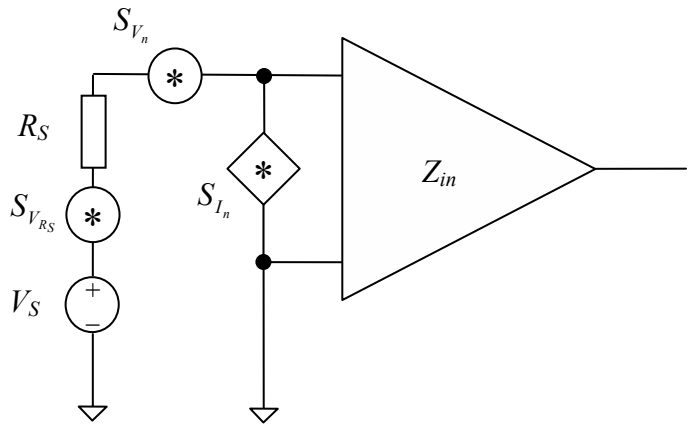

Fig. 3.6. Representation of the noise in the amplifier with equivalent sources at the input.

3.4.2 Voltage Controlled Oscillators (VCOs)

Voltage controlled oscillators are used to produce a periodic signal at a certain frequency that can be varied by an applied voltage. A typical LC oscillator consists of a passive LC-tank whose resonance frequency sets the frequency of oscillation. The

energy loss in the LC tank is precisely compensated by the energy supplied by an active device, typically a transistor. The VCO is a key building block in wireless transceivers, where it is used together with the mixer to perform frequency translation. The received RF signal (at 900 or 1800 MHz in the GSM, for example) is multiplied with the oscillator signal in the mixer to downconvert the RF signal to an intermediate frequency (heterodyne architecture) or directly to the baseband (homodyne). The VCO and the mixer is used in the opposite way to generate an RF signal from the baseband signal in the transmit path. An ideal oscillator generates a perfect sinusoidal signal, which corresponds to a pulse in the frequency spectrum, see Fig. 3.7(a). For an actual oscillator, however, the spectrum exhibits "skirts" around the centre frequency called phase noise [2], as shown in Fig. 3.7(b). Phase noise is a difficult problem in wireless transceivers; RF oscillators must therefore meet stringent phase noise requirements for these kinds of circuits. Fig. 3.7(c) describes how phase noise can be a problem in wireless communications. Both the desired signal and an unwanted, large interfering signal from an adjacent channel are downconverted by the oscillator which exhibits finite phase noise. The phase noise from the downconverted interfering signal is mixed with the downconverted desired signal at the output, the two spectra overlap corrupting the signal-to-noise ratio. The influence of the phase noise can be reduced by placing the channels further apart in frequency, which obviously limits the information capacity of the communication system.

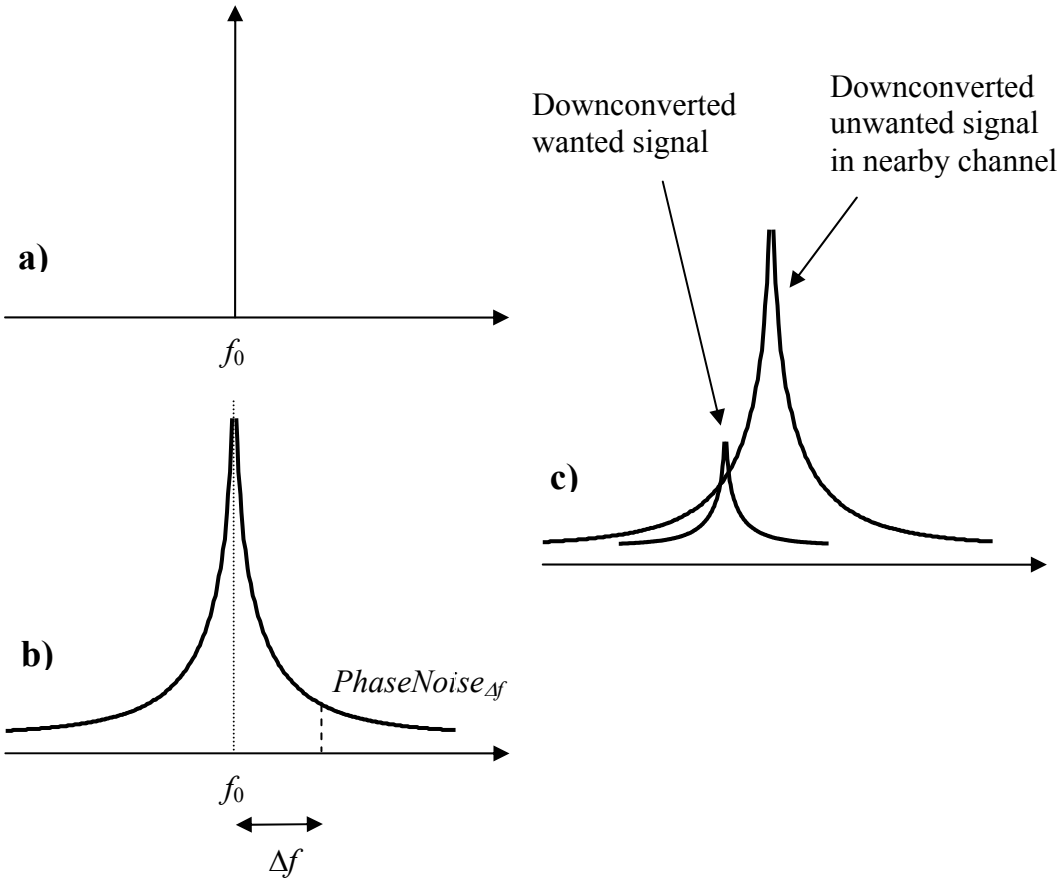

Fig. 3.7. (a) Ideal oscillator signal. (b) Actual oscillator signal with phase noise. (c) Effect of phase noise in a receiver. The phase noise from an interfering signal overlaps the wanted signal and degrades the SNR.

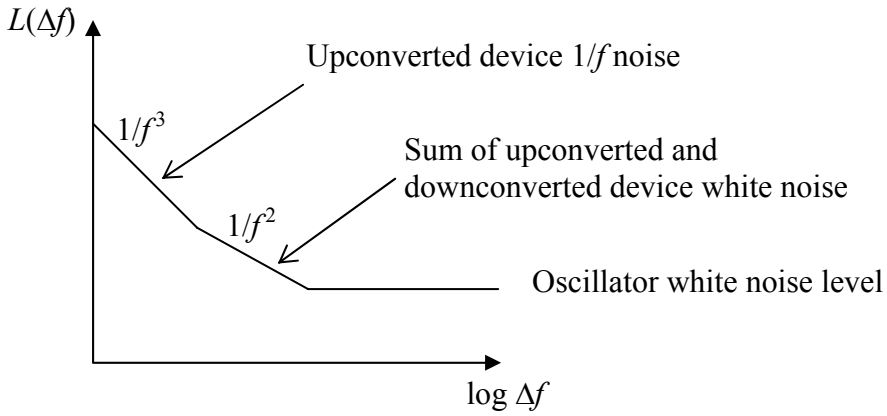

Fig. 3.8. Schematic illustration of the phase noise spectrum.

Device 1/*f* noise is a particular problem for VCOs since it is upconverted to phase noise at small frequency offsets from the carrier frequency and therefore sets the ultimate separation limit of two channels [2, 125-128]. Fig. 3.8 illustrates schematically the phase noise spectrum and the different physical origins. One drawback with oscillators implemented in CMOS compared to bipolar technology is the inferior 1/*f* noise performance in the former technology, which has been thought to exclude CMOS to be used high-performance oscillators [125]. This is a motivation to study how 1/*f* noise is upconverted to phase noise in oscillators and to understand the mechanisms behind the 1/*f* noise in CMOS transistors in order to be able to reduce the phase noise originating from device 1/*f* noise by proper design. The 1/*f* noise in each transistor in the oscillator can contribute to the phase noise, but the transistors used for the frequency control are particularly important [2]. The frequency of oscillation is a function of the current flowing through these devices. Low-frequency noise in the current is directly translated to low-frequency noise in the frequency of oscillation, to phase noise. A general theory of phase noise in electrical oscillators based on linearization of a time variant system was given by Hajimiri and Lee [125]. Noise located near integer multiples of the oscillation frequency contributes to the total phase noise, according to their approach. The upconversion of the 1/*f* noise is sensitive to symmetry properties of the oscillator waveform. The impulse sensitivity function (ISF) describes how much phase shift that results from an impulse at different position in the oscillation cycle. The ISF is periodic and can therefore be expanded in a Fourier series

$$ISF(\omega_0 t) = c_0 / 2 + \sum_{n=1}^{\infty} c_n \cos(n\omega_0 t + \theta_n) \tag{3.32}$$

Here, ω_0 is the frequency of oscillation, t is the time, c_n are Fourier coefficients. θ_n is the phase of the nth harmonic, which turns out to be unimportant. The phase noise resulting from the transistor drain current noise can then be written

$$L(\Delta f) = 10 \cdot \log\left(\frac{S_{I_{D,1/f}} \cdot c_0^2 + S_{I_{D,th}} \cdot \sum_{n=0}^{\infty} c_n^2}{32\pi^2 q_{\max}^2 \Delta f^2} \right) \tag{3.33}$$

where $q_{\max} = C \cdot V_{\max}$ is the maximum charge displacement across the tank capacitor C determined by the maximum voltage swing across the tank $V_{\max}$. $S_{I_{D,1/f}}$ and $S_{I_{D,th}}$ are the PSD of the $1/f$ noise and the thermal noise in the drain current, respectively. As seen in Eq. (3.33), the oscillator phase noise can be reduced by maximizing the voltage swing $V_{\max}$ and minimizing the coefficients c_n. Maximizing the quality factor (Q value) of the *LC*-tank will reduce the generated thermal noise and thereby lower the phase noise. The DC value of the *ISF*, c_0, can actually be minimized by symmetry considerations. An example of a simple symmetrical complementary negative resistance oscillator for low phase noise is shown in Fig. 3.9. The relative widths of the nMOS and pMOS transistors must be selected in an appropriate way in order to minimize c_0. In this way, it is possible to reduce the $1/f^3$ phase noise corner to a few kHz for a device with a $1/f$ noise corner of a few hundred kHz.

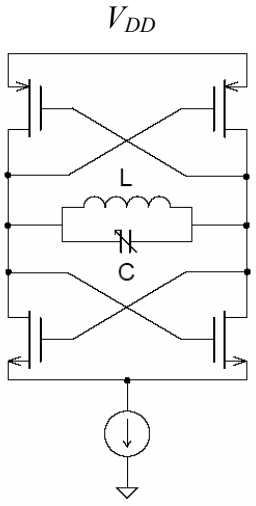

Fig. 3.9. Complementary oscillator topology for low phase noise.

Another type of oscillator, called the ring oscillator, can be realized by connecting an odd number of inverters in series forming a ring. The ring oscillator is easy to integrate and useful in digital circuits. However, its RF performance is poor due to high phase noise [126].

3.4.3 Mixers

The requirement on the noise figure is relaxed for the stages following the LNA in a receiver system. Therefore, the noise figure of the mixer in a heterodyne system, where the signal is translated to an intermediate frequency before baseband processing, is not very critical for the noise performance. In a homodyne system (or direct conversion receiver DCR), on the other hand, the signal is directly translated to

zero frequency by the mixer. Homodyne systems have advantages such as a simple architecture, easy integration with the baseband circuit and the elimination of the problem with the "image" signal. However, one disadvantage is that the 1/*f* noise in the mixer can severely degrade the signal-to-noise ratio [129, 130]. This can be understood if the signal is translated to very low frequencies where the 1/*f* noise of the devices contributes appreciable. The 1/*f* noise problem can be mitigated by employing long channel transistors in the mixer, which instead degrades the transconductance and the circuit speed. The solution to the problem from a circuit point of view is to adopt a passive mixer, which involves no DC biasing current [129]. However, passive mixers provide no gain and are usually less preferred in RF design.

In summary, the 1/*f* noise in MOS transistors is a problem for several analog and RF circuits, such as mixers and VCOs, which can limit the performance of a transceiver system for example. This imposes additional circuit design considerations and necessitates a good understanding of the noise mechanisms in order to reduce the noise by device design. In order to achieve a good understanding and description of the noise in circuit simulators, accurate characterization and modeling of the 1/*f* noise are extremely important.

4. 1/*f* noise in MOSFETs: origins and modeling

The origin of the 1/*f* noise in MOS transistors has been debated for several decades, whether number fluctuation noise due to traps in the gate oxide or bulk mobility fluctuations dominate the 1/*f* noise. The drain current in a MOSFET is constricted to a narrow surface channel under the gate oxide. The current transport is therefore sensitive to traps present at the interface. While a superposition of g-r noise spectra to produce 1/*f* noise is unlikely to occur for a homogenous bulk device since the required distribution of time constants is not possible to achieve without very special assumptions, this can easily be obtained for a surface channel. In 1957, McWorther presented a 1/*f* noise model based on quantum mechanical tunneling transitions of electrons between traps in the gate oxide and the channel [131]. The tunneling time varies exponentially with distance, thus the required distribution of time constants to produce 1/*f* noise is obtained for a trap density that is uniform in both energy and distance from the channel interface. The McWorther model is celebrated for its simplicity and excellent agreement with experiments, especially for nMOS transistors [109, 110]. However, the mobility fluctuation noise model tends to better explain the 1/*f* noise in pMOS transistors [12, 108]. It was later observed that a trapped carrier also affects the surface mobility through Coulomb interaction. The so-called correlated mobility fluctuations gave a correction to the number fluctuation noise model that was suggested to resolve the deviations found in pMOSFETs. However, the correction factor was criticized for being unphysically high since screening was not accounted for [13]. MOSFETs with a buried channel for the current transport as well as junction field-effect transistors (JFETs) can show significantly lower 1/*f* noise than that for surface channel device [132-138]. The current between source and drain in a JFET flows in the un-depleted part of the Si, the width of which is modulated by the gate voltage, far away from any oxide interface. These results are in favour of the number fluctuation theory that the 1/*f* noise in MOSFETs is due to traps in the gate oxide. However, the surface carrier mobility is reduced compared to the bulk value due to additional surface scattering (acoustic phonons and surface roughness), which has an impact on the mobility fluctuations. Moreover, the Hooge mobility noise is sensitive to the crystalline quality, which is deteriorated close to the interface. Therefore, another possibility to explain the higher 1/*f* noise when the carriers are in close proximity to the gate oxide surface is increased mobility fluctuation noise. In this chapter, the number fluctuation noise and mobility fluctuation noise theories and their models for 1/*f* noise in MOSFETs are presented in detail (section 4.1 and 4.2, respectively). In section 4.3, the 1/*f* noise dependence on the voltage on the bulk terminal (substrate bias), an effect that was recently discovered, is reported and discussed. The number and mobility fluctuation noise models are critically discussed in section 4.4. An improved model and description of the 1/*f* noise in MOSFETs based on the research performed in this thesis is presented, which takes the substrate effect into account.

4.1 Number fluctuations

The physical mechanism behind the number fluctuation noise is interaction between slow traps in the gate oxide and the carriers in the channel, which is schematically illustrated in Fig. 4.1. The oxide traps dynamically exchange carriers with the channel causing a fluctuation in the surface potential, giving rise to fluctuations in the inversion charge density. This in turn leads to noise in the drain current. The

fluctuation in the inversion charge density occurs without a current flowing in the device, the current is only needed to sense the fluctuations. The fluctuating oxide charge density δQ_{ox} is equivalent to a variation in the flat-band voltage, see Eq. (2.6).

$$\delta V_{fb} = -\delta Q_{ox} / C_{ox} \tag{4.1}$$

The fluctuation in the drain current $I_D = f(V_{fb}, \mu_{eff})$ then yields [139]

$$\delta I_D = \frac{\partial I_D}{\partial V_{fb}} \delta V_{fb} + \frac{\partial I_D}{\partial \mu_{eff}} \frac{\partial \mu_{eff}}{\partial Q_{ox}} \delta Q_{ox} \tag{4.2}$$

Since $\partial I_D / \partial V_{fb} = -\partial I_D / \partial V_{GS} = -g_m$ ($+g_m$ for pMOS) and $I_D \propto \mu_{eff}$

$$\delta I_D = -g_m \delta V_{fb} + \frac{I_D}{\mu_{eff}} \frac{\partial \mu_{eff}}{\partial Q_{ox}} \delta Q_{ox} \tag{4.3}$$

One can define a coupling parameter that reflects how a variation in the oxide charge couples to the mobility

$$\alpha = \frac{1}{\mu_{eff}^2} \frac{\partial \mu_{eff}}{\partial Q_{ox}} \quad \text{(valid for nMOS, minus sign for pMOS)} \tag{4.4}$$

Inserted in Eq. (4.3) this gives

$$\delta I_D = -g_m \delta V_{fb} - I_D \mu_{eff} \alpha C_{ox} \delta V_{fb} \tag{4.5}$$

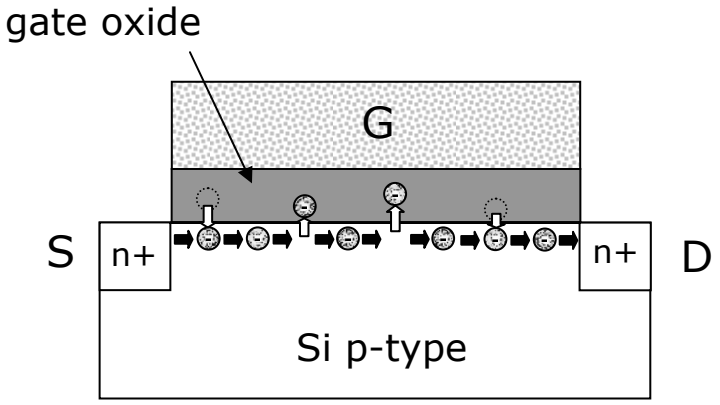

Fig. 4.1. Schematical illustration of electrons in the channel of a MOSFET moving in and out of traps, giving rise to fluctuations in the inversion charge density and thereby the drain current.

Calculating the power spectral density

$$S_{I_D} = S_{V_{fb}} \left(1 + \frac{\alpha \mu_{eff} C_{ox} I_D}{g_m} \right)^2 g_m^2 \tag{4.6}$$

The first term in the parentheses in Eq. (4.6) is due to fluctuating number of inversion carriers and the second term to mobility fluctuations correlated to the number fluctuations. Note that α can be negative or positive depending on if the mobility increases or decreases upon trapping a charge according to Eq. (4.4). The power spectral density of the flat-band voltage fluctuations is calculated by summing the contributions from all traps in the gate oxide [140, 141]:

$$S_{Q_{ox}} = S_{V_{fb}} C_{ox}^2 = \frac{q^2}{W^2 L^2} \int_{E_v}^{E_c} \int_0^W \int_0^L \int_0^{t_{ox}} 4 N_t f(\mathrm{E})(1 - f(\mathrm{E})) \frac{\tau}{1 + (2\pi f \tau)^2} dx dy dz d\mathrm{E} \tag{4.7}$$

where $f(\mathrm{E}) = \left[1 + e^{(\mathrm{E}-\mathrm{E}_{\mathrm{fn,p}})/kT} \right]^{-1}$ is the Fermi-function. The product f(E)(1-f(E)) = $-kT \cdot df(\mathrm{E})/d\mathrm{E}$ is sharply peaked around the quasi-Fermi level $\mathrm{E}_{\mathrm{fn,p}}$. Thus

$$S_{Q_{ox}} = \frac{q^2 kT}{WL} \int_0^{t_{ox}} 4 N_t \frac{\tau}{1 + (2\pi f \tau)^2} dz \tag{4.8}$$

where N_t is the density of traps in the gate dielectrics at the quasi-Fermi level (in $\mathrm{cm}^{-3}\mathrm{eV}^{-1}$) as these traps are the only ones that contribute to the $1/f$ noise. Other traps are permanently filled or permanently empty. In the McWorther model, assuming that trapping and detrapping occur through tunneling processes, the trapping time constant is given as

$$\tau = \tau_0(\mathrm{E}) \cdot e^{z/\lambda} \tag{4.9}$$

for tunneling from the interface to the trap located at z in the gate oxide. The tunneling attenuation length λ is predicted by the WKB theory to be

$$\lambda = \left[\frac{4\pi}{h} \sqrt{2 m^* \Phi_B} \right]^{-1} \tag{4.10}$$

where Φ_B is the tunneling barrier height seen by the carriers at the interface. The time constant τ_0 is often taken as 10^{-10} s, and $\lambda \approx 1$ Å for the Si/SiO_2 system. This yields z = 2.6 nm and 0.7 nm for a frequency of 0.01 Hz and 1 MHz, respectively. Thus, oxide traps located too close to the channel interface are too fast to give $1/f$ noise, and those located more than ~3 nm from the interface are too slow to contribute. By inserting Eq. (4.9), the integral in Eq. (4.8) can be evaluated as

$$S_{V_{fb}} = \frac{q^2 kT \lambda N_t}{f^\gamma WLC_{ox}^2} \tag{4.11}$$

The frequency exponent γ deviates from 1 if the trap density is not uniform in depth; $\gamma < 1$ is expected when the trap density is higher close to the gate oxide/channel interface than that in the interior of the gate oxide, and $\gamma > 1$ for the opposite case [7]. One example which is a good evidence of the McWorther model is the observation of $1/f^{1.7}$ noise [142]. These devices had a nitrided gate oxide, which contains a higher density of traps than pure thermally grown SiO_2. If the peak of the nitrogen profile is located away from the channel interface (due to re-oxidation for example), the observation of $\gamma = 1.7$ can be explained.

The bias dependence of the normalized drain current noise S_{I_D}/I_D^2 in the number fluctuation model is simulated for drain currents ranging from subthreshold to strong inversion regimes using Eq. (4.6) with $\alpha = 0$ and a constant arbitrary N_t, the result is shown in Fig. 4.2. S_{I_D}/I_D^2 varies approximately as $1/(V_{GS}-V_T)^2 \propto 1/Q_i^2$ in strong inversion, an even stronger fall off with drain current is observed at the highest currents in the graph due to the fact that g_m is reduced at high gate voltage overdrives. In subthreshold, on the other hand, S_{I_D}/I_D^2 is almost constant since $g_m = I_D q/mkT$ according to Eq. (2.11). The physical explanation is that $|\delta Q_i/\delta Q_{ox}| < 1$, the charge trapped in the oxide is not only supplied from the inversion charge but also from the depletion and interface trap charges. The normalized drain current noise can written as [143]

$$\frac{S_{I_D}}{I_D^2} = \frac{q^4 \lambda N_t}{kTf^{\gamma} WL(C_{ox}+C_d+C_{it})^2} \tag{4.12}$$

in the subthreshold region. The trap density can also vary in energy, which affects the bias and frequency dependence of the noise. The band diagram in Fig. 4.3 describes the tunneling transitions, directly (i) [140] or using interface traps as stepping stones (ii) [144], from the Si to the gate oxide, and the window (z,E) of traps seen at a

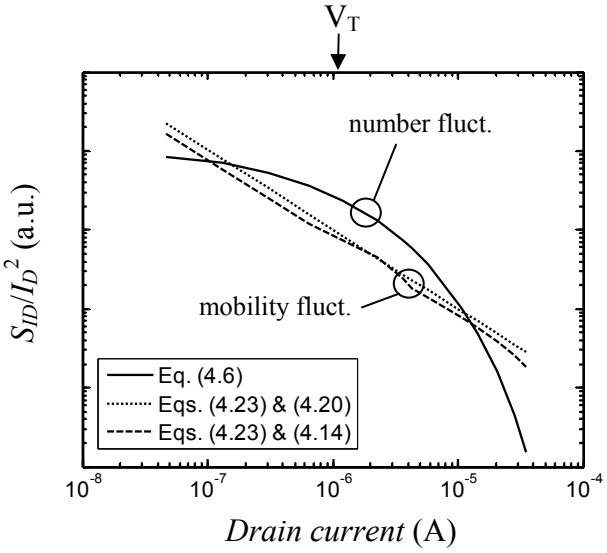

Fig. 4.2. Simulation of the drain current noise using both the number and the mobility fluctuation noise models. Eq. (4.6) with $\alpha = 0$ and constant N_t was used for the number fluctuations and Eqs. (4.14), (4.20) and (4.23) with constant α_H for the mobility fluctuations.

particular bias point (shaded area). A trap density that increases towards the conduction or valence band edges results in a weaker bias dependence of S_{I_D}/I_D^2 than $1/Q_i^2$. Due to the band bending of the gate oxide, traps in the oxide interior are swept "faster" in energy than the traps at the channel interface. Thus, it is expected that $\gamma > 1$ and increases with gate bias in the case of a trap density that increases towards the band edges. Another possibility instead of the tunneling model presented above is thermally activated traps [145]. Studies on RTS noise in MOSFETs show that thermally activated phonon-assisted capture and emission of carriers play an important role [8]. If the time constant of the trap is written as

$$\tau_{th} = \tau_{0,th} e^{\mathrm{E}/kT} \tag{4.13}$$

1/*f* noise is obtained for an even distribution of traps in energy. The problem with this theory is the difficulty to find a physical process with the property given by Eq. (4.13). The emission time for a thermally activated trap depends exponentially on the activation energy, but the capture time is normally independent on energy.

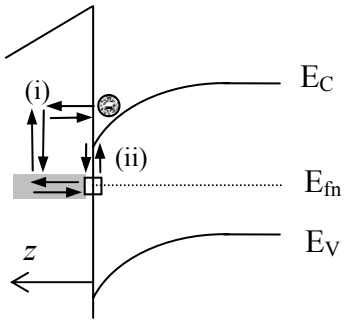

Fig. 4.3. Energy band diagram showing the tunneling transitions of electrons between the conduction band and traps in the gate oxide, (i) correspond to direct tunneling and (ii) to indirect tunneling via interface traps.

4.2 Mobility fluctuations

The drain current noise generated by fluctuations in the channel carrier mobility is given according to Hooge's empirical formula

$$\frac{S_{I_D}}{I_D^2} = \frac{q\alpha_H}{fWLQ_i}, \tag{4.14}$$

which is derived from Eq. (3.16) with the number of carriers N in channel replaced by WLQ_i/q. In the linear region, $Q_i = C_{ox}(V_{GS} - V_T)$, thus the normalized drain current noise depend inversely on the gate voltage overdrive. Typical values for α_H range between 10^{-3} and 10^{-6}. Values down to 10^{-7} have been observed for buried channel Si pMOSFETs [135] and in the order of 10^{-8} for JFETs [137, 138]. As mentioned in the previous chapter, the mobility 1/*f* noise is suggested to be primarily generated in the phonon scattering [146]. The different scattering mechanisms that limit the channel

mobility in MOSFETs vary in different ways with the effective (normal) electric field and density of inversion charge. Therefore, α_H is not only dependent on technology but also on the bias conditions as will be shown below. In the general case, each scattering process generates mobility fluctuation noise with the magnitude given by the Hooge parameter of the process $\alpha_{H,j}$. If the scattering processes are independent of one another Matthiessen's rule can be applied

$$\frac{1}{\mu_{eff}} = \sum_j \frac{1}{\mu_j} \tag{4.15}$$

The fluctuations in the different scattering processes are also assumed independent. Then we obtain

$$\frac{\Delta\mu_{eff}}{\mu_{eff}^2} = \sum_j \frac{\Delta\mu_j}{\mu_j^2} \tag{4.16}$$

and for the power spectral densities

$$\frac{S_{I_D}}{I_D^2} = \frac{S_{\mu_{eff}}}{\mu_{eff}^2} = \sum_j \left(\frac{\mu_{eff}}{\mu_j}\right)^2 \frac{S_{\mu_j}}{\mu_j^2} = \left\{\frac{S_{\mu_j}}{\mu_j^2} = \frac{q\alpha_{H,j}}{fWLQ_i}\right\} = \sum_j \left(\frac{\mu_{eff}}{\mu_j}\right)^2 \frac{q\alpha_{H,j}}{fWLQ_i} \tag{4.17}$$

Thus

$$\alpha_H = \sum_j \frac{\mu_{eff}^2}{\mu_j^2}\alpha_{H,j} \tag{4.18}$$

If only phonon scattering generates noise

$$\alpha_H = \frac{\mu_{eff}^2}{\mu_{ph}^2}\alpha_{H,ph} \tag{4.19}$$

Thus, α_H varies with gate bias due to the bias dependent factor μ_{eff}^2 / μ_{ph}^2. Moreover, $\alpha_{H,ph}$ is not necessarily constant but can depend on the conduction path. Both of theses issues are addressed in the next section.

The relation in Eq. (4.14) is only valid when the carrier density is uniform. In the saturation region, the carrier density varies parabolically along the channel and reaches zero at the drain. Then the total channel drain current noise is evaluated by adding the noise contribution from each channel segment

$$\begin{aligned}\frac{S_{I_D}}{I_D^2} &= \frac{q\alpha_H}{fWL^2}\int_0^L \frac{dx}{Q_i(x)} = \left\{I_D = W\mu_{eff}Q_i dV/dx\right\} = \\ &= \frac{q\alpha_H}{fWL^2}\int_0^{V_{DS}} \frac{W\mu_{eff}}{I_D}dV = \frac{q\alpha_H\mu_{eff}V_{DS}}{fL^2 I_D}\end{aligned} \tag{4.20}$$

This equation is valid for all regions of operation, but V_{DS} is replaced with $V_{DS,sat}$ for $V_{DS} > V_{DS,sat} = (V_{GS} - V_T)/m$. Using Eq. (2.10) for $V_{D,sat}$ the following expression is found for the saturated range

$$\frac{S_{I_D}}{I_D^2}\frac{q\alpha_H\sqrt{2\mu_{eff}}}{f\sqrt{WL^3C_{ox}mI_D}} \tag{4.21}$$

In the subthreshold region, the drain current is dominated by diffusion

$$I_{D,diff} = WkT\mu_{eff} / q \cdot dQ_i(x)/dx \tag{4.22}$$

Using the above expression in the integral to the left in Eq. (4.20), it is readily shown that the same final result appear. However, the drain current and the total charge density Q_i is independent on $V_{DS} >> mkT/q$. The mobility 1/*f* noise is also independent of V_{DS} in this case and can be written as [147]

$$\frac{S_{I_D}}{I_D^2} = \frac{\alpha_H\mu_{eff}2kT}{fL^2I_D} \tag{4.23}$$

The mobility 1/*f* noise is simulated from subthreshold to the strong inversion regime using Eqs. (4.14) or (4.20) in strong inversion and Eq. (4.23) in subthreshold, all with a constant arbitrary α_H, the results are shown in Fig. 4.2. The peak mobility was used in Eq. (4.20) as the effective mobility, which is a simplification since the effective mobility varies with gate bias. The mobility in subthreshold is not easily characterized; the value was estimated from the mobility value close to threshold. From the schematical bias dependencies in Fig. 4.2, it can be deduced that the number fluctuation noise is most important around threshold, whereas the mobility noise is prominent both at very low currents in the subthreshold region and at very high currents in the strong inversion region.

The 1/*f* noise can be significantly higher when the current density is inhomogeneous. In such case, Vandamme and Trefán have shown that the effective number of carriers is reduced and the 1/*f* noise is increased [148]

$$\frac{S_I}{I^2} = \frac{\alpha_H\int_\Omega J^4 d\Omega}{fN\left(\int_\Omega J^2 d\Omega\right)^2} \tag{4.24}$$

As an example, current crowding at contacts can lead to deteriorated 1/*f* noise performance due to inhomogeneous current flow. Inhomogeneous samples can also be shown to generate dramatically higher 1/*f* noise.

4.3 Impact of substrate bias and normal electric field

The 1/*f* noise is often shown to decrease when a voltage V_B is applied to the bulk (substrate) terminal forward biasing the substrate/source junction [149-151], which may be exploited in circuits to reduce the noise figure or phase noise. Conversely, the

1/*f* noise increases when the substrate/source junction is reverse biased. Another related observation is that dynamic threshold (DT) MOSFETs, where the bulk terminal is connected to the gate $V_B = V_G$, can present higher transconductance and significantly reduced 1/*f* noise than that when the device operated in the conventional mode with the bulk grounded [152-154]. Deen and Marinov found a reduction in the 1/*f* noise magnitude by 8 dB/V when a forward voltage was applied on the bulk [149]. In this work, a corresponding reduction around 5 dB/V has been observed. We will discuss our results below and compare them with results published in literature. First, we will explain the effect of V_{BS} on the static device parameters (body effect).

The width of the depletion region is changed due to the voltage V_{BS}. The depletion charge increases when the substrate is reverse biased (V_{BS} positive for pMOS, negative for nMOS), and decreases when the substrate is forward biased

$$Q_d = \sqrt{2\varepsilon_{si} q N_{sub} (2\psi_B + V_{BS})} \tag{4.25}$$

The threshold voltage depends on the depletion charge and is therefore shifted by the voltage on the bulk terminal, $|V_T|$ is increased by a reverse bias and decreased by a forward bias. Eq. (2.5) must be modified for a nonzero V_{BS} according to

$$V_T = V_{fb} \pm 2\psi_B \pm \frac{\sqrt{2\varepsilon_{si} q N_{sub} (2\psi_B + V_{BS})}}{C_{ox}} \tag{4.26}$$

The effective mobility varies with the effective electric field, given by Eq. (2.27), as was described in chapter 2.2. The effective electric field is increased by a reverse substrate bias, which results in a decrease in the mobility. The opposite occurs for a forward substrate bias. Fig. 4.4 shows g_m plotted versus V_{GS} for a Si pMOSFET with $HfAlO_x$ gate dielectrics which demonstrates both the effect on V_T and on μ_{eff}.

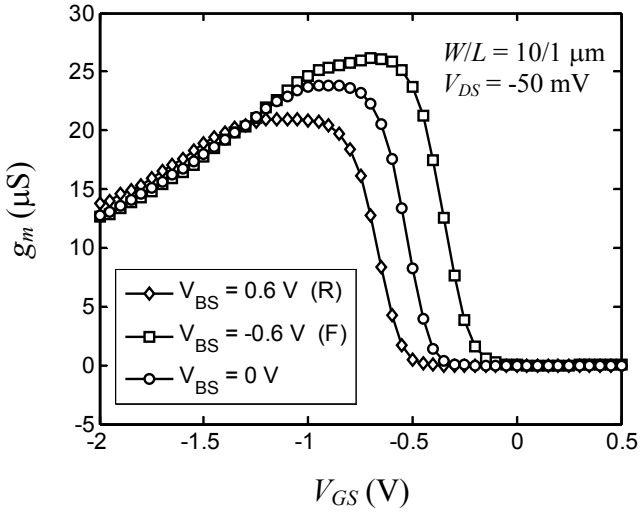

Fig. 4.4. Transconductance vs. gate voltage for three different V_{BS} on a TiN/$HfAlO_x$/Si pMOSFET.

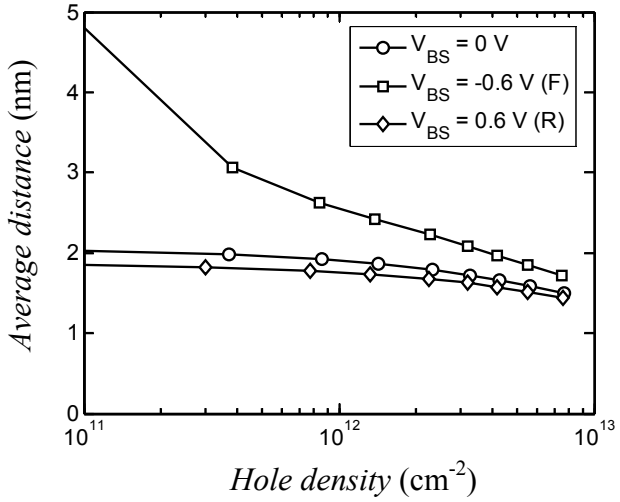

Fig. 4.5. Simulation of the average distance of the inversion charge from the oxide interface for different V_{BS}. t_{ox} = 2.8 nm and N_d =~5×10^{17} cm^{-3} were used in the simulations.

The average inversion carrier distance from the gate oxide interface increases for a forward substrate bias, vice versa for a reverse bias, as evidenced from the simulation in Fig. 4.5.

The 1/*f* noise has been found to decrease with forward substrate bias and increase with a reverse bias in a large number of studied devices including pMOSFETs with high-k gate dielectrics (Fig. 4.6(a)-(b)), Si pMOSFETs, and buried SiGe channel pMOSFETs (Fig. 4.6(c)). The influence on the substrate voltage is weak is some cases, but still discernable. However, the above mentioned dependence may not prevail in weak inversion as seen in Fig. 4.6(a).

The physical mechanism behind the noise lowering has been studied thoroughly. In the literature, several suggestions have been presented to explain the effect of the substrate bias. Park *et al*. examined nMOS transistors and found a noise reduction by one order of magnitude in weak inversion, but an almost independent behaviour in strong inversion [151]. A similar observation was made by Marin *et al*. on MOSFETs from a 130 nm CMOS technology, ~50% lower noise was found in weak inversion in their work [150]. These results can be explained by the fact that the depletion capacitance changes with the substrate voltage (increase with forward substrate bias, opposite for reverse voltage), which affects the number fluctuation noise according to Eq. (4.12).

However, we observe a strong(er) influence above threshold in our work. Ahsan *et al*. goes a step further and claims that the correlated mobility fluctuations also are affected by the substrate bias [155]. This is explained by the fact that the Coulomb interaction depends on the distance between the oxide charge and the channel carriers, which is modulated by the substrate bias as discussed above. According to the hole mobility model by Agostinelli, Jr. *et al*., the scattering parameter α can be modeled as [21]

$$\alpha = \frac{\alpha_0}{Q_i^{0.3} z^{0.7}} \tag{4.27}$$

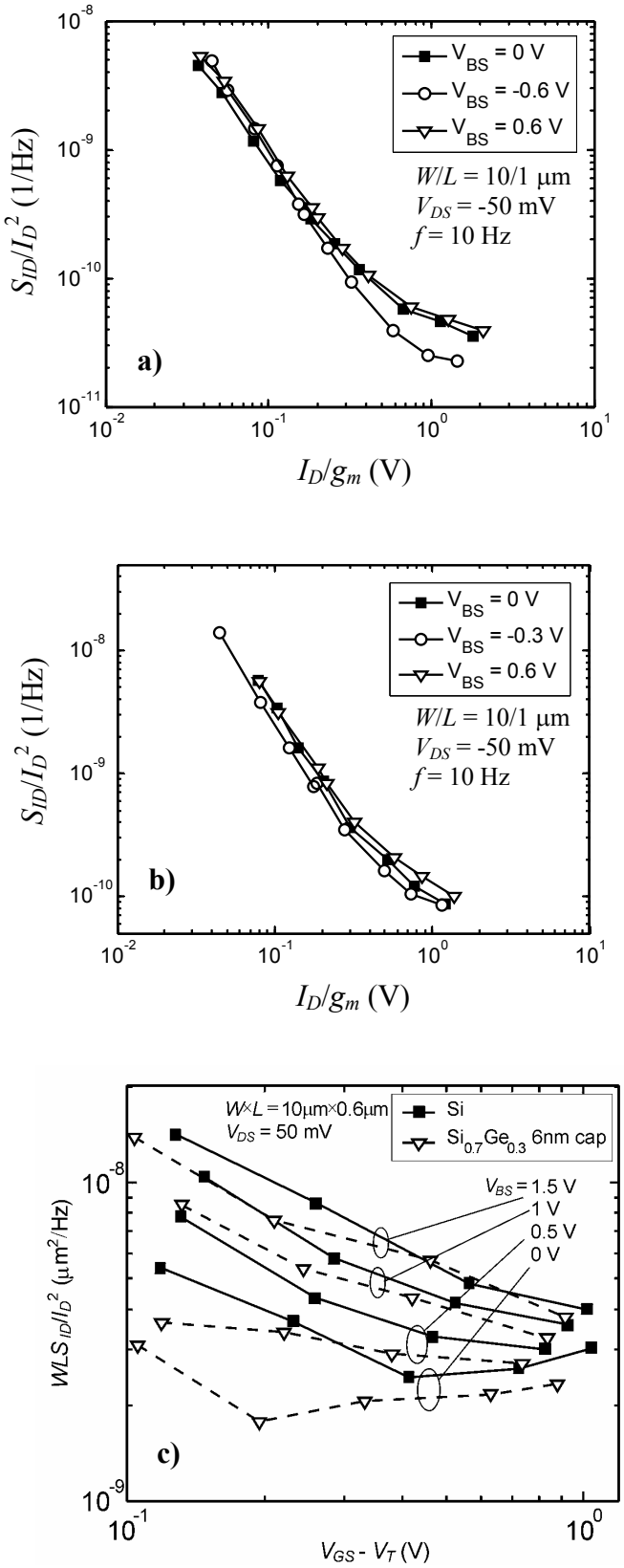

Fig. 4.6. Drain current noise measured at different V_{BS} on (a) a TiN/HfAlO$_x$/Si pMOSFET (paper VIII) (b) a poly-SiGe/HfO$_2$/Al$_2$O$_3$/SiGe pMOSFET (device C in paper V) (c) a Si and a buried SiGe (6-nm Si-cap) pMOSFET with poly-Si/SiO$_2$ gate stack (paper I).

where α_0 is temperature and material dependent parameter and z is the average inversion layer width given for holes as

$$z = 0.039 \cdot T_n / E_{eff} + 1.51 \cdot 10^{-5} / E_{eff}^{1/3} \quad \text{[cm]} \tag{4.28}$$

where T_n is the normalized temperature ($T_n = T/300$ K). However, the variation in the mobility with electric field must also be considered. The correlated mobility fluctuation noise, the second term in Eq. (4.6), is proportional to $\mu_{eff} \cdot \alpha$. The effects on the mobility and parameter α almost cancel out. A calculation using Eqs. (4.27) and (4.28) and the measured mobility vs. V_{BS} for the device in Fig. 4.6(a) shows that $\mu_{eff} \cdot \alpha$ decreases with increasing V_{BS}, as illustrated in Fig. 4.7. Thus, the observations in Fig. 4.6 cannot be explained with the model we have used. We therefore conclude that the correlated mobility fluctuation noise has a negligibly small influence on the 1/*f* noise variations with the substrate bias.

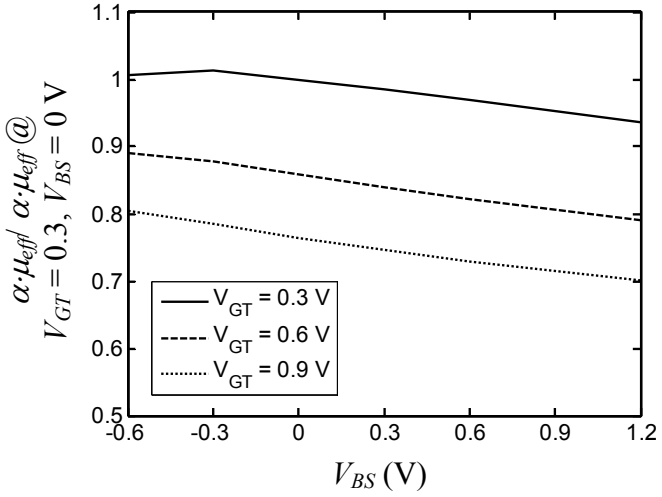

Fig. 4.7. Simulation of $\mu_{eff} \cdot \alpha$ (normalized with the value at $V_{GT} = 0.3$ V and $V_{BS} = 0$ V) using Eqs. (4.27) and (4.28) for α and the measured mobility for the pMOSFET in Fig. 4.6(a). $C_{ox} = 1.0 \times 10^{-6}$ F/cm^2.

In order to find the mechanism behind the substrate bias effects, we instead focus our efforts on the Hooge mobility fluctuation noise model. It was first suggested in paper I that the 1/*f* noise variations with the substrate bias can be explained by Hooge mobility fluctuation noise that depends on the position of the inversion channel or the effective electric field. According to the previous discussions in this chapter, the different scattering mechanisms can contribute with different magnitudes to the mobility fluctuation noise. The surface roughness can have a substantial impact on the 1/*f* noise [156]. The explanation could be that the scattering rate of the phonons is enhanced for a rougher surface which increases the fluctuations in the phonon population, or that the 1/*f* noise generated in the surface roughness scattering is dominant. In paper I, the influence of the surface roughness scattering was investigated. Simulations of the mobility fluctuation noise from different scattering mechanisms showed that the observed behaviour can be explained by 1/*f* noise

generated in the surface roughness scattering. The effective mobility μ_{eff} can be written as

$$\mu_{eff}^{-1} = \mu_{sr}^{-1} + \mu_a^{-1}, \tag{4.29}$$

where μ_{sr} is the mobility limited by surface roughness scattering, and μ_a here represents the mobility limited by scattering mechanisms other than surface roughness scattering. According to Eq. (4.18) the following relationship for the Hooge parameter can be derived

$$\alpha_H = \mu_{eff}^2 \left(\frac{\alpha_{H,sr}}{\mu_{sr}^2} + \frac{\alpha_{H,a}}{\mu_a^2} \right), \tag{4.30}$$

where $\alpha_{H,sr}$ and $\alpha_{H,a}$ are the Hooge parameters for the corresponding scattering processes, which were considered as constants in our experiments. The mobility was modeled using the model presented by Darwish *et al*. [157] with some modification for μ_{sr} which instead was extracted from measurements ($\mu_{sr} = 2.75\times10^{13} / E_{eff}^{1.87}$ cm^2/Vs). A simulation of the mobility 1/*f* noise using Eq. (4.30) with $\alpha_{H,sr} = 1.56\times10^{-3}$ and $\alpha_{H,a} = 1.1\times10^{-5}$ is shown in Fig. 4.8. As seen, the fit to the measured data is fairly good for both the V_{GT} and V_{BS} dependencies. The discrepancy at V_{GT} above 0.5 V is, at least partly, due to influence from noise generated in the source and drain resistances. This exercise shows that the substrate bias effects on the 1/*f* noise are possible to explain with changes in the individual mobilities related to different scattering mechanisms and that surface roughness scattering makes a dominant contribution to the 1/*f* noise. Another way to explain the 1/*f* noise behaviour is by considering the individual Hooge parameters $\alpha_{H,j}$, especially $\alpha_{H,ph}$, as bias dependent. This will be further discussed in the next section. An important observation from the simulation in Fig. 4.8 is that the weak decrease of the 1/*f* noise with increasing gate voltage overdrive can be explained by the fact that the effective electric field and the inversion carrier position are affected by the gate voltage overdrive as well.

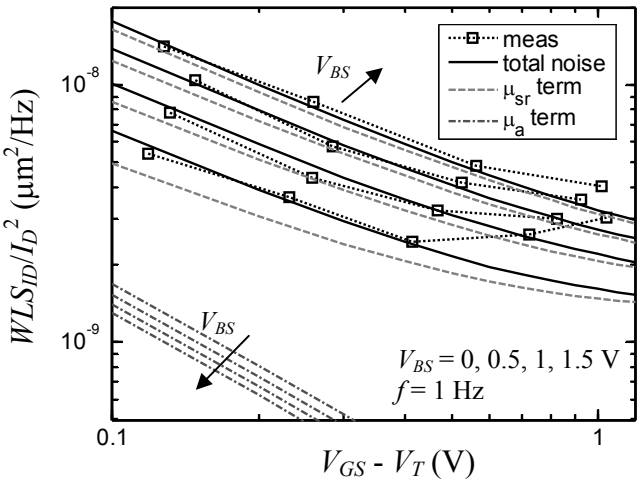

Fig. 4.8. Simulated (lines) and measured (open squares) drain current noise on a Si pMOSFET for different V_{BS} (from paper I). Eq. (4.30) was used to model α_H in the simulations. The first and second term in Eq. (4.30) are also plotted (denoted μ_{sr} and μ_a).

Finally, the quantum effects induced by the high effective electrical field have been investigated by Mercha *et al*. [158]. An empirical correction factor σ_{2D}/σ_{3D}, which increases exponentially with the effective electric field, was proposed and included in Eq. (4.11). This effect can also potentially explain the noise behaviour on V_{BS}.

4.4 Improved understanding & modeling of 1/*f* noise

This section critically discusses the mobility and number fluctuation noise models and presents new insights on 1/*f* noise in advanced CMOS transistors. The McWorther noise model is critically discussed for MOSFETs with ultrathin gate dielectrics in subsection 4.4.1. It is found that a correction to the originally proposed model is necessary. The mobility fluctuations correlated to the fluctuations in the number of carriers is one such correction. Subsection 4.4.2 deals with correlated mobility fluctuations and a new model is presented. Finally, subsection 4.4.3 critically reviews the Hooge noise model and discusses how the model can be improved to accommodate the effects of the substrate bias and resolve its shortcomings.

4.4.1 Critical discussion of the McWorther model

The McWorther number fluctuation noise model is, as explained earlier, based on tunneling transitions of electrons between traps in the gate oxide and the channel. The model often shows excellent agreement for nMOS transistors in the whole bias region from subhtreshold to strong inversion. However, deviations from the expected behaviour are observed for pMOSFETs. In the framework of the McWorther model, two different theories have been suggested and investigated to explain the 1/*f* noise in the pMOSFETs. One such theory is the correlated mobility fluctuations, which was implemented in the model given by Eq. (4.6). Values of the parameter α between 1-2 $\times 10^5$ Vs/C are often necessary to model the 1/*f* noise in pMOSFETs [110, 150, 159], which unfortunately are roughly an order of magnitude too high to be supported by the laws of physics. Moreover, screening from the inversion charge is not accounted for in the simple theory. By including screening and correct physical values [13], the model in Eq. (4.6) is not able to describe the observed 1/*f* noise in pMOSFETs, except if N_t is allowed to vary with energy. A possible, but controversial, idea how to explain the bias dependence for pMOSFETs is to make the assumption that $N_t \propto V_{GT}$. Scofield *et al*. studied the noise versus temperature (77-300 K) and gate voltage in nMOS and pMOS transistors and claim that the number fluctuation noise model can be used for both device types [160]. The reason, according to the authors, is that the trap density is constant near the conduction band edge (nMOS), while it increases with energy close to the valence band edge. Experiments probing the same traps but using another technique could falsify or verify this idea. The so-called U-shaped distribution where the trap density increases close to both the valence and conduction band edges is typically obtained from different types of measurements of traps at the Si/SiO_2 interface [28, 161, 162]. However, the oxide traps and interface traps do not necessarily have the same origin. A consequence of an energy dependent N_t in the McWorther model is that the frequency exponent should vary with gate bias too due to the band bending in the oxide. This is, however, seldom analyzed or reported in relation with N_t(E). Investigations of the gate voltage noise dependence on the oxide thickness in pMOSFETs by Knitel *et al*. showed that $S_{V_G} \propto t_{ox}^p$ with p ranging from 1.4-1.8 close to threshold and around 1 at high V_{GT} [163]. This strongly points to a mobility fluctuation origin (correlated to the number fluctuations or Hooge type) of the 1/*f* noise at high V_{GT}.

A type of noise experiment in favour of a number fluctuation origin is the occurrence of g-r noise in devices with small gate areas which adds up to 1/*f* noise in a large device. This has been shown by Brederlow *et al*. [164] and Scholten *et al*. [165]. It is, however, important to separate the 1/*f* noise and the g-r noise components, and make this study over a wide bias range in order to draw reliable conclusions. Another experiment pointing towards a trap origin of the 1/*f* noise is the switched bias experiments. When a rectangular pulse train is applied on the gate, a 5-8 dB reduction in the noise has been observed [166]. This can be explained by the number fluctuation noise model only if the trap densities differ at the two energetic levels given by the high and low gate voltage [167].

A serious problem with the McWorther noise model appears in devices with very thin gate oxides (t_{ox} < 2 nm). Then the tunneling time is too fast, even for traps situated close to the gate electrode/oxide interface, and no 1/*f* noise would be produced at the lowest frequencies. Instead, a roll-off in the spectrum is expected at a frequency corresponding to the tunneling time to the farthest situated traps. Low-frequency noise results have been reported for some 1.5 nm gate oxide MOSFETs, and only 1/*f* noise is observed, in contradiction with the McWorther model [159, 168]. This is an important problem that must be addressed in future noise research in ultra-scaled CMOS devices. Moreover, a trap situated in the middle of the gate oxide couples out to a flat-band voltage fluctuation with a strength given by ¼ of the value for a trap located at the gate oxide/channel interface. Eq. (4.7) should be modified by multiplying the integrand with $(1-z/t_{ox})^2$. The frequency exponent is then expected to be lower than 1.

4.4.2 Correlated mobility fluctuations

A trapped carrier will not only shift the flat-band voltage and thereby cause a fluctuation in the inversion charge density, the trapped carrier will also affect the mobility. These fluctuations in the mobility are correlated to the fluctuating inversion charge density, both related to the trapping and release of carriers in slow oxide traps. However, there is a disagreement in the literature regarding the strength of the correlated mobility fluctuations, which is usually modeled with a parameter α. A constant α is frequently used in the noise models, but this is not physically correct for several reasons such as the effect of screening which reduces the magnitude of α [13, 169, 170]. The parameter α can be estimated both from low-frequency noise and mobility characterizations. For nMOSFETs, the α values obtained using these methods are usually consistent around 1×10^4 Vs/C. For pMOSFETs, on the other hand, much larger α values are often reported from noise characterizations, in the range 3-20 $\times10^4$ Vs/C [110, 150, 159, 171-173], than expected from mobility models for pMOSFETs ($\alpha \sim 0.3\text{-}3\times10^4$ Vs/C) [21, 174]. This large discrepancy suggests that the correlated mobility fluctuations are mistaken for another noise mechanism in pMOSFETs. In the rest of this section, we will derive a new model for α based on existing mobility models and compare with experiments, the results from which were reported in detail in paper VI.

We start our analysis with the expression for α given in Eq. (4.4) and the mobility expression in Eq. (2.13). We do the derivation for pMOSFETs here, but the same final

expression is obtained for nMOSFETs. The Coulomb scattering is separated in a part caused by impurities and one part from charge in the oxide, $1/\mu_C = 1/\mu_{C,imp} + 1/\mu_{C,ox}$.

$$\alpha = -\frac{1}{\mu_{eff}^2}\frac{\partial \mu_{eff}}{\partial Q_{ox}} = \\ -\left(\frac{1}{\mu_{ac}^2}\frac{\partial \mu_{ac}}{\partial Q_i} + \frac{1}{\mu_b^2}\frac{\partial \mu_b}{\partial Q_i} + \frac{1}{\mu_{sr}^2}\frac{\partial \mu_{sr}}{\partial Q_i} + \frac{1}{\mu_{C,imp}^2}\frac{\partial \mu_{C,imp}}{\partial Q_i} + \frac{1}{\mu_{C,ox}^2}\frac{\partial \mu_{C,ox}}{\partial Q_i}\right)\frac{\partial Q_i}{\partial Q_{ox}} \tag{4.31}$$

The bulk phonon mobility μ_b is a constant and $\partial Q_i / \partial Q_{ox} = -1$ in strong inversion, which gives

$$\alpha = \frac{1}{\mu_{ac}^2}\frac{\partial \mu_{ac}}{\partial Q_i} + \frac{1}{\mu_{sr}^2}\frac{\partial \mu_{sr}}{\partial Q_i} + \frac{1}{\mu_{C,imp}^2}\frac{\partial \mu_{C,imp}}{\partial Q_i} + \frac{1}{\mu_{C,ox}^2}\frac{\partial \mu_{C,ox}}{\partial Q_i} \tag{4.32}$$

The first two terms will be negative since μ_{ac} and μ_{sr} fall off with increasing Q_i, whereas the third term will be positive. These terms are often neglected in the derivation of α. The last term will be positive or negative depending on the type of trap, channel type and the nature of the oxide charge; Table II summarizes the outcome for the different combinations.

Table II. Sign of last term in Eq. (4.32)

	Acceptor trap (–/0)	Donor trap (0/+)
pMOS	–	+
nMOS	+	–

A simple model for $\mu_{C,ox}$ is [175]

$$\mu_{C,ox} = 1/\alpha_C |Q_{ox}| \tag{4.33}$$

where α_C is a Coulomb scattering parameter. A common approximation is to set $\alpha = \alpha_C$, which leads to an overestimation of α at high gate voltage overdrives as shown below. The magnitude of α_C decreases with increasing Q_i since the inversion charge screens the Coulomb interaction between the oxide charge and the carrier in the inversion layer. According to Vandamme and Vandamme

$$\alpha_C = \left(\mu_{C0}\sqrt{C_{ox}(V_{GS} - V_T)/q}\right)^{-1}/q\,, \tag{4.34}$$

where μ_{C0} is a fitting parameter given as 5.9×10^8 cm/Vs [13]. Another model for α_C that has been used in the literature is $\alpha_C = \alpha_1 + \alpha_2 \ln(Q_i)$ where α_1 and α_2 are constants [141, 176], but we will concentrate our efforts on the models in Eqs. (4.34) and (4.27). The parameter α has been simulated using the Si inversion layer mobility model by Darwish *et al*. [157] and using the two aforementioned models for α_C to determine the last term in Eq. (4.32), the result is plotted for holes and electrons in Figs. 4.9 and 4.10 respectively. A donor trap was assumed for pMOS and an acceptor

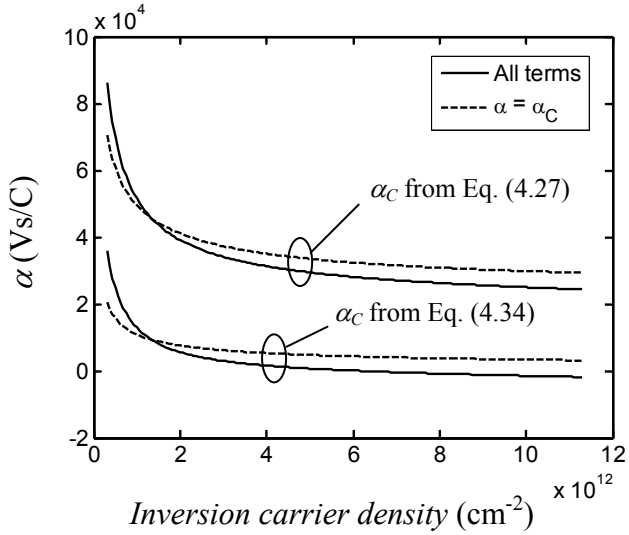

Fig. 4.9. Scattering parameter α simulated for holes in Si using Eq. (4.32).

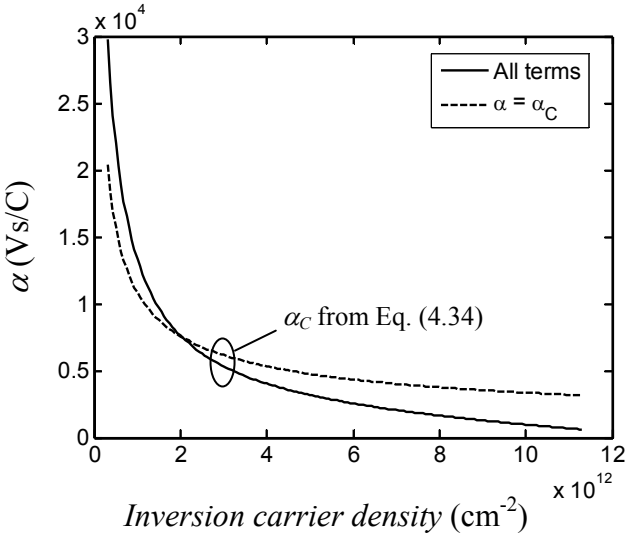

Fig. 4.10. Scattering parameter α simulated for electrons in Si using Eq. (4.32).

trap for nMOS, respectively. The difference between α values calculated by using all terms or only using α_C, i.e. the difference between the solid lines and the broken lines in Figs 4.9 and 4.10, is around 4×10^3 Vs/C for holes and 2×10^3 Vs/C for electrons at high inversion carrier densities. The two models used for the holes in Fig. 4.9 deliver different results. The model by Vandamme and Vandamme giving the lower α is supported by experimental results for a SiGe pMOSFETs with Al_2O_3 gate dielectrics as shown in Fig. 4.11. Of course, this can be a coincidence since the model is based on electron mobility measurements made by Koga *et al*. [170] on Si nMOSFETs with SiO_2 gate dielectrics. An additional important remark is necessary regarding the choice of model for α_C. The traps responsible for the 1/*f* noise are believed to be located 1-3 nm from the oxide/channel interface. The models used here are both valid for charge located at the interface. The Coulomb interaction between the traps and the channel carriers is weaker for traps located further from the interface. A safe choice would be to assume that $|\alpha|$ is below $\sim1\times10^4$ Vs/C, which means that the correlated

mobility fluctuations make a quite small correction to the number fluctuation noise. We have extracted reliable α values from noise measurements in the range 1-12 $\times 10^3$ Vs/C, see paper VI and chapter 6.5. In the cases when significantly higher α values are found, we find it very unlikely that they are physically correct.

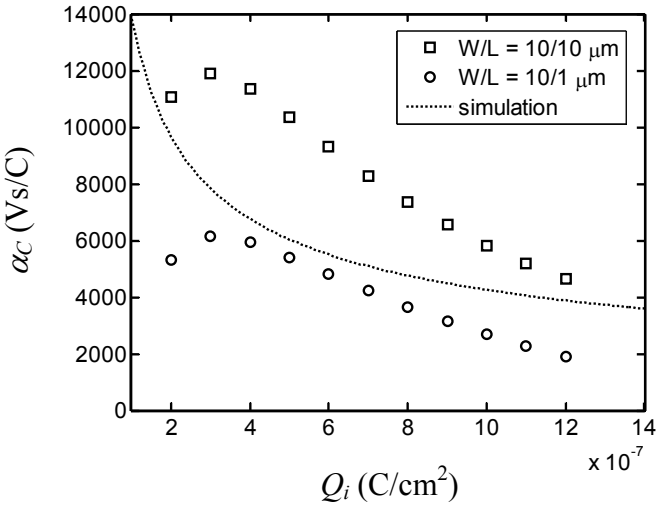

Fig. 4.11. Measured (paper VI) and simulated (Eq. (4.34)) Coulomb scattering parameter α_C.

4.4.3 Critical discussion & improved modeling with the Hooge model

While the Hooge noise model satisfactorily can describe the 1/*f* noise in pMOSFETs, a gate voltage dependent Hooge parameter, $\alpha_H \propto 1/V_{GT}$, must be assumed in the description of nMOSFETs. For both nMOSFETs and pMOSFETs, a roll-off in the S_{I_D} / I_D^2 curve at gate biases below the threshold voltage is often observed (see chapter 6), which means that the Hooge parameter reduces in subthreshold. From a modeling point of view, any bias dependence can be included in α_H, just like N_t was suggested to vary with energy in order to describe the 1/*f* noise in pMOSFETs. However, a good model should be physically based, be able to accurately model the observed behaviour and predict effects related to technology. Our approach in the following is to review and discuss improvements of the Hooge noise model starting from the basic assumptions of the model. We will also present new ideas on understanding the 1/*f* noise. This is valuable for improved 1/*f* noise modeling, and might eventually help and inspire the evolution of a theoretical, physics based 1/*f* noise model for mobility fluctuations.

One of the early improvements of the Hooge noise model was the finding that different scattering mechanisms contribute with different magnitudes to the fluctuations in the mobility (see Eq. (4.18)) and that the phonon scattering was proposed as the dominant source of the 1/*f* noise. A lower α_H in subthreshold can therefore be explained by an increasing influence of Coulomb scattering diluting the mobility noise. The mobility noise is also dependent on the effective electric field, as was elaborated in the previous section, which explains why α_H is lower in subthreshold than in strong inversion. Vandamme and Vandamme also proposed that the number of carriers taking place in the fluctuation process cannot go below a constant value determined by the thermal voltage [177]. Then *N* in Eq. (3.16) for a

MOSFET is replaced by $N + N_0$, where $N_0 = WLC_{ox}kT/q^2$. However, the theoretical basis for this assumption is still dubious. It is rather well established that the 1/*f* noise originate from traps in nMOS transistors, and here we agree with the majority. Most research groups use this model also for pMOS transistors, but invoke either an energy dependent trap density or correlated mobility fluctuations to explain the observed discrepancies from the standard number fluctuation noise model. In this case, we have a different opinion. We present good evidence in this thesis that Hooge mobility noise in many cases is the dominant noise source in pMOSFETs, but number fluctuation noise may make a significant contribution or dominate around threshold, as can be understood from Fig. 4.2. For a wide acceptance (or rejection) of the theory, a physically based mobility fluctuation noise model is highly desired. Detailed studies of how the Hooge parameter is affected by scattering mechanisms, carrier position, electric field, defect density etc would be an important future research topic, as well as an investigations of why number noise tends to dominate in nMOS and mobility noise in pMOS. The latter could be explained by an asymmetric trap distribution close to the band edges as well as the fact that holes suffer more from phonon scattering. The relative mobilites μ_{eff}^2/μ_{ph}^2, μ_{eff}^2/μ_{ac}^2, μ_{eff}^2/μ_{sr}^2 and $\mu_{eff}^2/\mu_{C,imp}^2$ were simulated for both electrons (open symbols) and holes (closed symbols) using the mobility model by Darwish *et al*. [157] and are displayed in Fig. 4.12. The phonon mobilities $\mu_{ph} = 1/(1/\mu_b+1/\mu_{ac})$ and μ_{ac} (acoustic phonons) are more dominant for the hole transport than that for the electrons. Thus, a larger Hooge parameter ($\alpha_H \propto \mu_{eff}^2/\mu_{ph}^2$ according to Eq. (4.19)) can be expected for the holes. Fig. 4.12 also shows that a decline of α_H is expected below threshold.

In this thesis, we have made thorough investigations of the 1/*f* noise dependence on gate voltage and substrate voltage. In the rest of this section, we will elaborate how α_H can depend on effective electric field and the inversion carrier position. The mechanism that is responsible for the 1/*f* noise variation with substrate bias is most

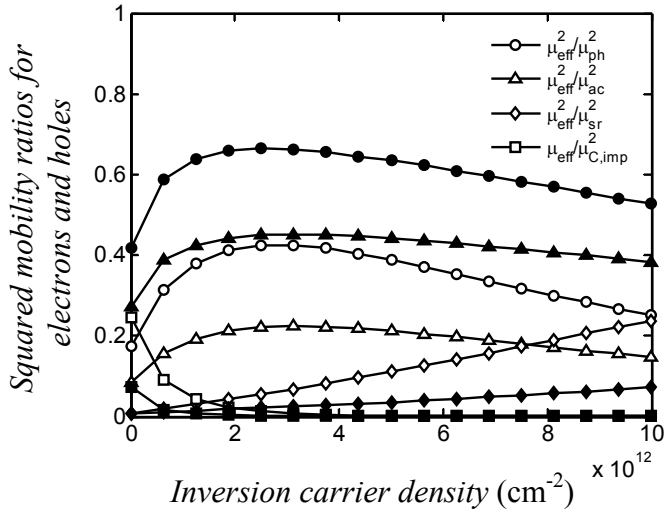

Fig. 4.12. Simulation of μ_{eff}^2/μ_{ph}^2, μ_{eff}^2/μ_{ac}^2, μ_{eff}^2/μ_{sr}^2 and $\mu_{eff}^2/\mu_{C,imp}^2$ for both electrons (open symbols) and holes (closed symbols) using the mobility model by Darwish et al.

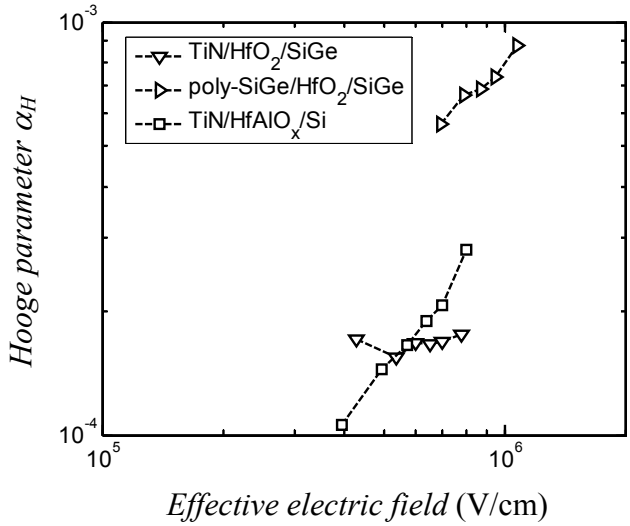

Fig. 4.13. Hooge parameter plotted vs. effective electric field for Si and SiGe pMOSFETs with high-k gate dielectrics (from paper IV). The electric field was varied by a voltage on the bulk terminal (substrate bias). V_{DS} = -50 mV.

likely that the vertical electric field or the channel position is affecting the 1/*f* noise. Fig. 4.13 illustrates how α_H varies with the effective electric field for a three different pMOSFETs with high-k gate dielectrics. The distance of the inversion carriers from the gate oxide interface depends on the effective electric field, which gives another way to explain the 1/*f* noise properties. Fig. 4.14 shows that the Hooge parameter is reduced when the carriers are located further away from the gate oxide interface, consistent with the fact that buried channel MOSFETs often exhibit reduced 1/*f* noise (see chapter 6). Furthermore, we have observed in many of our noise experiments (see paper I, IV and chapter 6) and from reported data in the literature that S_{I_D} / I_D^2 tends to flatten out and show a sublinear $1/I_D$ dependence at high gate voltage overdrives V_{GT}. In paper I, α_H for a Si pMOSFET was found to increase with V_{GT} as $\alpha_H \propto V_{GT}^{0.38}$. This phenomenon can be linked to the effects of the substrate bias as the electric field increases with increasing gate voltage overdrive. What can be the root cause of the inversion carrier position or E_{eff} dependence of α_H? We make two suggestions: (i) the variations in α_H originates from a non-constant $\alpha_{H,ph}$, (ii) surface roughness scattering dominates the mobility fluctuation noise, as was suggested in section 4.3 and paper I.

One important conclusion in this work is that the 1/*f* noise is sensitive to the gate oxide/channel interface properties and the current transport close to it. The 1/*f* noise dependence on electric field or channel positioning in pMOSFETs is not readily interpreted with the number fluctuation noise theory. A very interesting possibility, presented first in paper I, is that the surface roughness affects the 1/*f* noise. It was further on discovered by Gaubert *et al*. that the RMS value of the surface roughness could be related to the 1/*f* noise performance [156]. Two different explanations for how the surface roughness can influence the mobility fluctuation noise have been studied. The first one, that the fluctuations are generated in the carrier scattering

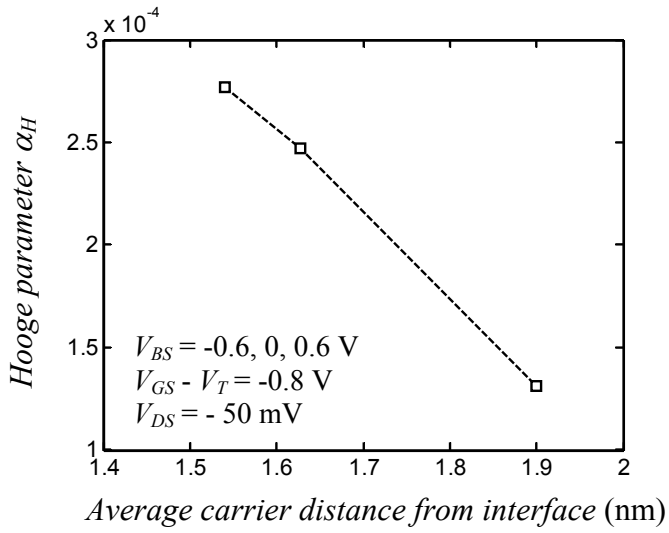

Fig. 4.14. Hooge parameter plotted vs. average distance of the inversion carriers from the gate oxide interface for TiN/HfAlO$_x$/Si pMOSFETs (from paper VIII). The inversion carrier distance was varied by V_{BS}.

against the rough surface, has been discussed in section 4.3. The second idea is that the mobility fluctuations are generated in the phonon scattering, but the fluctuations in the number of phonons are larger in magnitude closer to the surface. This can be modeled by using a bias dependent $\alpha_{H,ph}$. In fact, phonons are scattered against other phonons, defects, surfaces, electrons etc, which could be the origin of the fluctuations in the number of phonons and thereby the 1/*f* noise in the electron transport. The thermal conductivity is proportional to the phonon mean free path, which is strongly sensitive to crystal damage and defects etc [178]. An increase of the thermal conductivity by a factor of ~500 was observed by Takabatake *et al*. when a heavily ion implanted semiconductor specimen was annealed at 750 °C [179]. Interestingly, Vandamme and Oosterhoff found a 1/*f* noise reduction in ion implanted Si resistors by a factor of at least 50 after annealing at $T \geq 750$ °C [180]. The carrier mobility, on the other hand, only varied between 360 cm^2/Vs and 270 cm^2/Vs. This indicates that the 1/*f* noise due to mobility fluctuations may be related to the scattering of phonons, which causes fluctuations in the electron-phonon interaction and thereby the carrier transport. We therefore introduce the idea that $\alpha_{H,ph}$ is related to the rate at which the phonons are scattered. However, more research is needed to establish the connection.

In summary, the number and mobility fluctuation noise models were presented and critically discussed in this chapter. The effect of a substrate bias on the 1/*f* noise properties was demonstrated and discussed from a modeling point of view. It was shown that the effective electric field and/or position of the inversion carriers must be included in the noise 1/*f* models. New mobility fluctuation noise models were suggested regarding both the Hooge type 1/*f* noise and mobility fluctuations correlated to the number fluctuation noise.

5. Noise characterization

The measurement of noise is a complex task as the signal to be measured is very weak (down to ~1 pA). Moreover, a DC bias current is usually present as well as disturbances from electronic equipment, which complicates the task even more. The measurement setup must be designed carefully with appropriate shielding and preferably using batteries as power sources to avoid disturbances to be injected in the circuits. The typical low-frequency noise measurement setups used in this thesis are described in section 5.1. The measurements are usually performed in the frequency domain by measuring the power spectral density with a spectrum analyzer. If RTS noise is present, time domain analysis with the help of an oscilloscope is a valuable tool. These two analysis methods are described in section 5.2. The low-frequency noise in a device is sensitive to the device technology, especially the presence of traps, defects and crystal damage. Therefore, important information about reliability and sensitive areas for the current transport can be attained from noise studies. Section 5.3 discusses the low-frequency noise measurements as diagnostic tool.

5.1 Measurement setup

The low-frequency noise in this work was typically measured using the two configurations depicted in Figs. 5.1 and 5.2. The measurements were performed on-wafer by using a Cascade Microtech RF shielded probe station. Triax/BNC cables were connected to a custom built shielded bias box containing the bias circuit and the power supply. Lead cell batteries were used as power sources in order to minimize the disturbances in the measurement setup. Electrical equipment connected to the power mains give rise to disturbances at 50 Hz (60 Hz in some countries including USA), at multiples thereof, and usually at other frequencies as well. The weak noise from the device is amplified by a low-noise amplifier and then fed to the signal analyzer which measures the power spectral density. The output from the amplifier is also monitored by an oscilloscope, which is important in order to detect RTS noise and check that the amplifier is not saturated. Two types of amplifiers are frequently used in low-frequency noise measurement setups. Fig. 5.1 describes a setup with a low-noise voltage amplifier, which amplifies the voltage at its high impedance input and presents a voltage at the output amplified by a factor *A*.

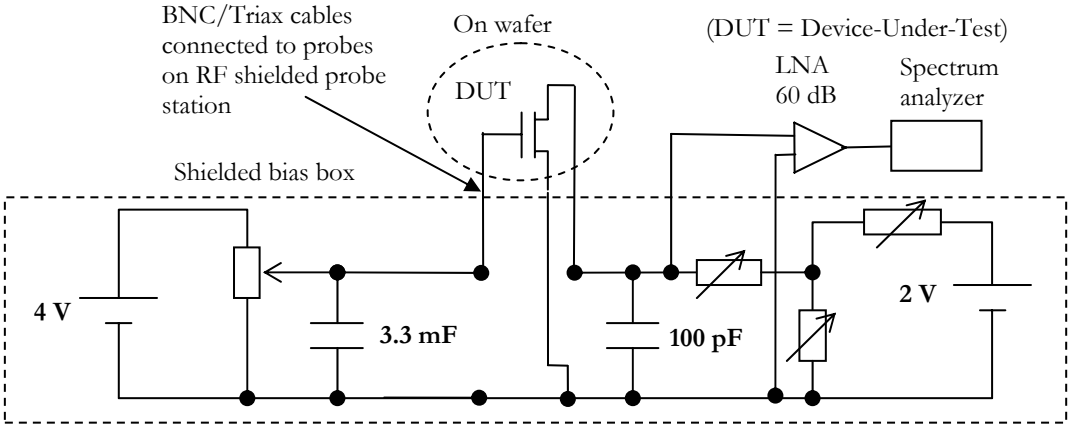

Fig. 5.1. Low-frequency noise measurement setup. The signal is amplified by a low-noise voltage amplifier.

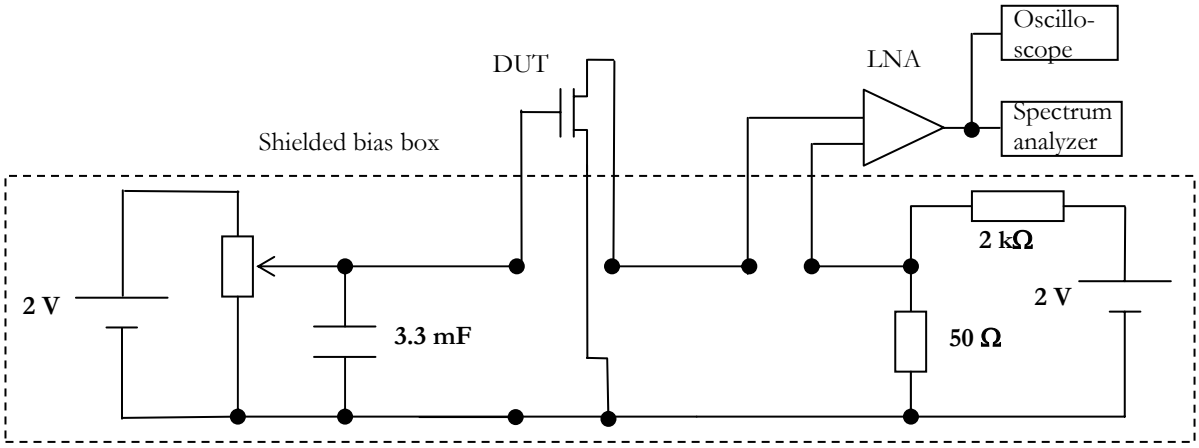

Fig. 5.2. Low-frequency noise measurement setup. The signal is amplified by a low-noise current amplifier.

The setup in Fig. 5.2 is operated with a low-noise current amplifier, which amplifies the current through its low-impedance input and gives a voltage at the output amplified by the transimpedance gain *G*. The amplifier inevitably adds noise to the circuit. Therefore, the internal noise of the amplifier sets the measurement limit of the system and must be minimized. The requirements on a good low-noise amplifier to be used for sensitive noise measurements include properties as ultra low internal noise, sufficient frequency range (DC to 100 kHz typically used in the measurements here), variable gain, and a wide dynamic range. A matched output (50 Ω) can also be desired. We have used a EG&G 5113 low-noise voltage amplifier and a Femto DLPCA-200 low-noise current amplifier for the setups in Figs. 5.1 and Fig. 5.2, respectively. Figure 5.3 displays an excerpt from the data sheet for the DLPCA-200 amplifier. The eqivalent input noise current sets the limit of the lowest noise current of the device that can be measured accurately. In addition, an equivalent noise voltage of 4 nV/Hz$^{0.5}$ @ 100 Hz needs to be considered when the impedance of the device is comparable or lower than the input impedance of the amplifier. The setup with the low-noise current amplifier outperforms the one with the voltage amplifier at ultra-small currents where the input impedance of the device is very large, for example a MOSFET biased in subthreshold. The voltage amplifier is often better to use at higher currents, such as a MOSFET biased in strong inversion.

Gain Setting (Low Noise) (V/A)	10^3	10^4	10^5	10^6	10^7	10^8	10^9
Upper Cut-Off Frequency (- 3 dB)	500 kHz	500 kHz	400 kHz	200 kHz	45 kHz	7 kHz	1.2 kHz
Rise / Fall Time (10% - 90%)	700 ns	700 ns	900 ns	1.8 µs	8 µs	50 µs	300 µs
Equ. Input Noise Current (/√Hz)	20 pA	2.3 pA	460 fA	130 fA	43 fA	13 fA	4.3 fA
Offset Current Drift (/°C)	30 nA	3 nA	0.3 nA	27 pA	2.5 pA	0.2 pA	60 fA
Gain Drift (/°C)	0.008%	0.008%	0.008%	0.01%	0.01%	0.01%	0.02%
Max. Input Current (±)	10 mA	1 mA	0.1 mA	10 µA	1 µA	0.1 µA	10 nA
Max. Input Offset Compensat. (±)	100 µA	10 µA	1 µA	0.1 µA	10 nA	1 nA	0.1 nA
DC Input Impedance (// 5 pF)	50 Ω	50 Ω	50 Ω	60 Ω	150 Ω	1 kΩ	10 kΩ

Fig. 5.3. Excerpt from data sheet for a Femto DLPCA-200 low-noise current amplifier.

A HP89410A vector signal analyzer was used in our experiments to analyze the output signal from the amplifier. The basic operating principle of the HP89410A analyzer is to collect the signal time data, digitize it and make a conversion to the frequency domain by discrete fast Fourier transformation (FFT). The analyzer presents (among other options) the power spectral density of the voltage noise at the analyzer input in V^2/Hz, averaged from several sweeps according to user settings.

5.2 Frequency and time domain analysis

Measurements performed in the frequency domain with the spectrum analyzer are performed by typically taking 100 averages. The data is collected for a number of transistor bias conditions which is set using the bias box, and then transferred to a PC for further processing and analysis. The power spectral density at the amplifier input is obtained by dividing with the gain squared. The drain current noise in a MOSFET is in most cases generated in the channel, except at high drain current where the contribution from noise originating from the S/D resistance may contribute appreciably. The noise generated in the channel is calculated with the help of Eqs. (3.22) or (3.23). A typical drain current noise spectrum is displayed in Fig. 5.4.

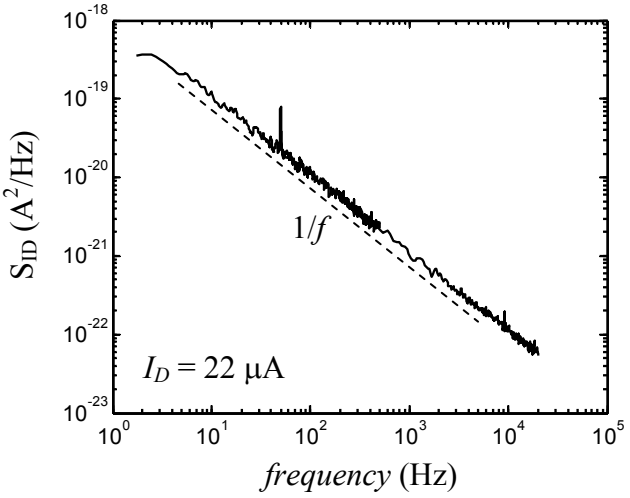

Fig. 5.4.Typical drain current noise spectra showing 1/f noise.

Time domain measurements are important in order to characterize RTS noise and are preferably performed with an oscilloscope. The Agilent 54621A digital oscilloscope used in our experiments has a sampling rate of $2 \cdot 10^6$ samples/s and a memory depth of 2 MB with a y-data resolution of 8 bits. This allows, for example, a collection of a 500 s long signal stream with a time resolution of 250 μs. In our RTS noise studies, pulse trains with around 100 transitions were recorded for each bias point. Ideally, an uninterrupted stream containing all the necessary transitions is preferred in order to reliably estimate the time constants. Data streams containing 20 transitions or more were typically used in the analysis. The data from the oscilloscope was stored in a PC and then low-pass filtered in order to remove high-frequency disturbances. A script was then used to find the location for the transition events between the different current levels in the noise data. Since the rise and fall times of the transitions are short, the time derivative at the transition is large. In this way, the transition events could be found and the time durations in the lower and higher RTS level and the pulse

amplitudes could be computed in an automatic procedure. The time constants $\tau_{l,h}$ for the RTS process can then be computed from a histogram analysis of number of pulses versus time. The relative occurrence of different time durations is given for Poisson distributed time durations as [8]

$$\text{Number of pulses between } t + \Delta t \propto \exp(-t / \tau_{l,h}) / \tau_{l,h} \tag{5.1}$$

An example of a time domain noise measurement showing random noise pulses is shown in Fig. 5.5. Estimations of the pulse amplitudes and the time constants can be used to extract information of the trap(s) that is causing the RTS noise. This is further described in the next section.

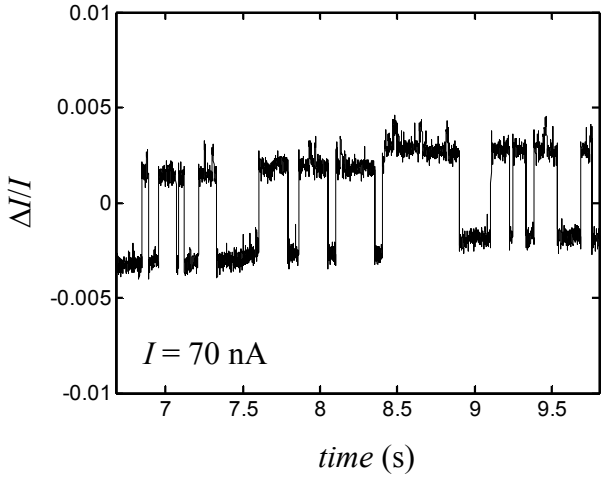

Fig. 5.5. Random telegraph signal noise in the base current of a bipolar transistor (from paper IX).

5.3 Noise measurements as a diagnostic tool

Low-frequency noise measurements can be used as a valuable tool for quality and reliability evaluations of electronic devices. First, from the observed low-frequency noise the noise mechanism and the spatial location of the noise source must be determined. The location of the dominant noise source is revealed by investigating the bias and geometry dependence of the noise. If the noise stemming from the S/D resistance is dominant, the drain current noise at constant drain current should be independent of the gate length. On the other hand, the noise originating from the channel increases with decreasing gate length. Having determined the dominant noise source, remedies to reduce the noise can be sought out. In this process, information about the dominant noise mechanism is highly desired.

The noise mechanism can be revealed by studying the bias dependence of the low-frequency noise. For a MOSFET the gate voltage is typically varied, which changes the inversion carrier density. The dominant source of the $1/f$ noise, mobility fluctuation or number fluctuation noise, can then be identified by analyzing the resemblance with Eqs. (4.6) or (4.14). In practice, this is not straightforward. Both number and mobility noise may contribute to the measured noise with similar magnitudes. There are usually deviations from the simple theory, the trap density can

vary with energy, mobility fluctuations correlated to the number fluctuations which roughly have the same gate voltage dependence as the Hooge noise can contribute, and the Hooge parameter can vary with inversion carrier density and electric field to mention some complicating effects. It is often necessary to measure the low-frequency noise over several decades of drain currents at a constant drain-source voltage. Investigating the substrate bias dependence of the low-frequency noise can provide additional information, as described in section 4.3. Correlating the noise level to other device parameters such as oxide charge density, interface state density, carrier mobility (especially phonon or Coulomb scattering limited mobility), oxide thickness (if varied in the experiments), etc, can help to establish the noise origin.

The information obtained about the location of the noise sources and the dominant noise mechanisms provides an understanding of the underlying physics and the possible measures that can be taken to improve the noise performance. The trap density and Hooge parameter can be used as figures-of-merit for a given technology or material system. In chapter 6, the $1/f$ noise results derived in this thesis are summarized and compared with other published results. If traps in the gate oxide are found to govern the $1/f$ noise, reducing the trap density by an improved gate oxidation process will reduce the noise. If mobility fluctuations prevail, reduced surface roughness, improved crystalline quality in the channel or using a strained channel can lower the $1/f$ noise. For both mechanisms, utilizing a buried channel potentially give improved noise performance. The level of noise from the S/D regions can be lowered by decreasing the S/D resistance, avoiding current crowding and improving the quality of the contacts.

G-r noise, RTS noise and number fluctuation $1/f$ noise in the MOSFET drain current originate from traps in the gate oxide. G-r noise and RTS noise can stem from traps at other locations also, for example the depletion region in the substrate, but it is rather rare. G-r and RTS noise are only important close to the Fermi-level energy, and are therefore very bias and temperature sensitive. For RTS noise, only one trap is active, while g-r noise can be generated from one or several traps with equal time constants. RTS noise is therefore only observed in small devices or/and devices with a low background noise. The total noise can be decomposed in a g-r and a $1/f^{\gamma}$ noise component when RTS noise is present in the time domain. RTS noise can be observed on top of the mobility $1/f$ noise in MOSFETs with small gate area (usually below 1 μm^2) if the following criterion on the number of carriers in the channel is fulfilled [181].

$$N < 1/4\pi\alpha_H \tag{5.2}$$

Obviously, the occurrence of RTS noise falls off with increasing N (increasing gate voltage overdrive). If the $1/f^{\gamma}$ noise and the RTS noise have the same origin, traps in the gate oxide, the occurrence of RTS noise depends on gate area but not bias (except if the trap density is bias dependent). The number of traps that can generate $1/f^{\gamma}$ noise can be estimated according to

$$\text{Number of traps} = 4kTWLN_t z\,, \tag{5.3}$$

where z is the tunneling distance of a carrier from the gate oxide/channel interface, maximum ~3 nm, and $4kT$ is the energy around the Fermi-level where the traps are distributed. RTS noise can be observed if the number of available traps is few. The relative drain current amplitude is related to the trap position z_t [182, 183]

$$\frac{\Delta I_D}{I_D} = \frac{q}{WL}\left[\frac{g_m}{I_D}\frac{1 - z_t / t_{ox}}{C_{ox}} + \alpha\mu_{eff}\right] \tag{5.4}$$

The trap depth can also be extracted from the variation of the emission time with gate voltage [110]

$$d\ln(\tau_e)/dV_G \approx qz_t / t_{ox}kT \tag{5.5}$$

The capture and emission times, τ_c and τ_e, are in general governed by from Shockley-Read-Hall statistics [184]

$$\tau_c = \frac{1}{\sigma n_s v_{th}} \text{ and } \tau_e = \frac{\tau_c}{g \cdot e^{(E_T - E_F)/kT}} \tag{5.6}$$

where n_s is the surface carrier concentration and g is the degeneracy factor usually taken as unity for electrons. It is usually observed that τ_c varies inversely with the gate voltage overdrive and τ_e is approximately constant. The trap position along the channel can be estimated from the variation of τ_c/τ_e with drain voltage [110]. Further RTS noise theory in terms of capture and emission kinetics and RTS amplitudes as well as an illustration of the RTS noise diagnostics for a SiGe heterojunction bipolar transistor are given in paper IX. The RTS amplitudes and emission and capture times were characterized for different bias voltages and temperatures. From the RTS noise characteristics, the location of the traps was determined and a physically based RTS noise model was developed.

While the energy level and spatial location of the trap can be determined from analysis of the RTS noise, the distribution of traps versus energy and oxide depth is characterized from the frequency and bias dependence of the number fluctuation $1/f^{\gamma}$ noise. The trap density as a function of gate bias, which can be related to the Fermi-level, can be evaluated by using Eq. (4.6). However, one must be cautious with this kind of analysis; the bias dependence could stem from a completely different mechanism.

The depth dependence of the trap density is calculated by using these relations

$$N_t = \frac{fWLC_{ox}^2 S_{V_G}}{q^2 kT\lambda\left(1 + \alpha\mu_{eff}C_{ox}I_D / g_m\right)^2} \text{ and } z = \lambda \cdot \ln(1/2\pi f\tau_0) \tag{5.7}$$

Fig. 5.6 illustrates the trap density profile for a pMOSFET with 5-nm ALD Al_2O_3 gate dielectrics. The low-frequency noise was measured between 1 – 20 kHz. A value of the time constant τ_0 equal to 10^{-10} s was used in Eq. (5.7). An interfacial oxide, around 1-nm thick, was found to be present between the Al_2O_3 and the channel.

As seen in Fig. 5.6, the trap density is higher in the bulk of the Al_2O_3 gate dielectrics than close to the SiO_2/Al_2O_3 interface. This exercise is an example of the usefulness of low-frequency noise measurements to characterize slow oxide traps. This type of traps is difficult to analyze with other methods. Standard charge-pumping techniques probe traps in the middle of the bandgap and situated very close to the oxide/channel interface. Therefore, low-frequency noise measurements fill an important purpose in the device evaluation process. Of course, the validity of the technique can be questioned if it is difficult to verify the results. Specialized charge-pumping techniques such as those described by Kerber *et al*. [75], Leroux *et al*. [185] (studies V_T shifts vs. time) and Jakschik *et al*. [186], also give information about the trap distribution versus depth; the results are in the same range as those given by noise measurements.

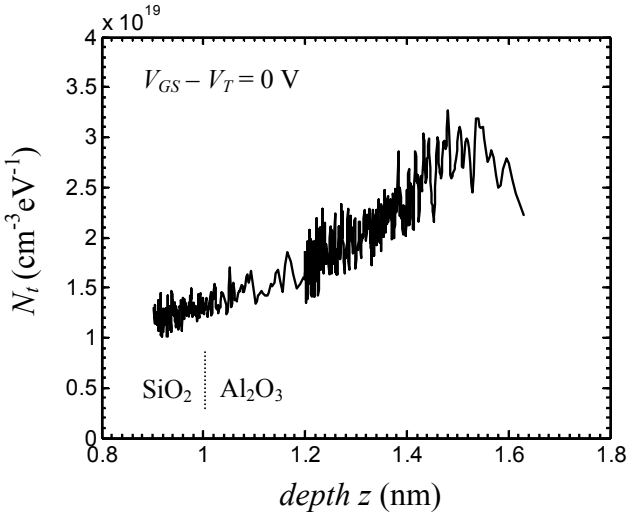

Fig. 5.6. Plot of N_t vs. depth in the gate oxide ($z = 0$ at the oxide/channel interface). N_t is extracted from low-frequency noise measurements on a $TiN/Al_2O_3/SiGe$ pMOSFET.

6. 1/*f* noise in advanced MOS transistors

MOS transistors generally show higher 1/*f* noise than bipolar transistors, and are therefore usually less preferred in low-noise applications. CMOS-technology, on the other hand, is superior in terms of low cost, scalability, and low power. CMOS-technology is now making inroads in the RF and analog domain, which also has inspired the evolution of new architectures [16]. However, the 1/*f* noise of the MOS transistors is a problem that must be tackled. Further downscaling of device dimensions will increase the 1/*f* noise, which makes it extremely important to understand the origin of the noise and reduce it by clever design. The 1/*f* noise is sensitive to technology; the choice of gate oxide material and oxidation/deposition process as well as channel type and material can have a large impact on the noise performance. The trap density and Hooge parameter can both be used as figures of merit for the 1/*f* noise performance, irrespective of the origin of the noise, and are frequently published in literature. Extracted values for the trap density and Hooge parameter are summarized in Figs. 6.1 and 6.2 for the devices investigated in this work (solid circles) and compared with relevant data published in the literature (other symbols) [9, 10, 43, 73, 74, 80, 108, 133, 135, 150, 158, 159, 171, 172, 187-199]. The requirements on N_t and α_H have been calculated from the ITRS roadmap by using the

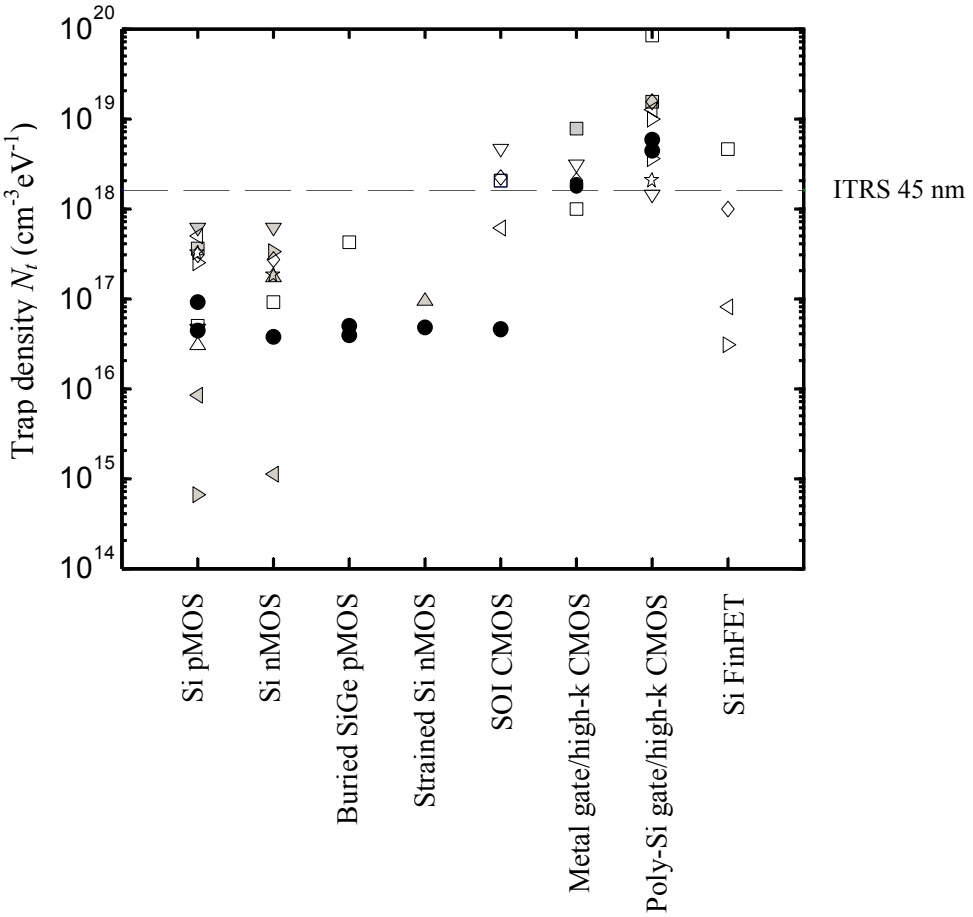

Fig. 6.1. Extracted values of N_t from this work (filled circles) for different CMOS technologies compared with results in literature (other symbols).

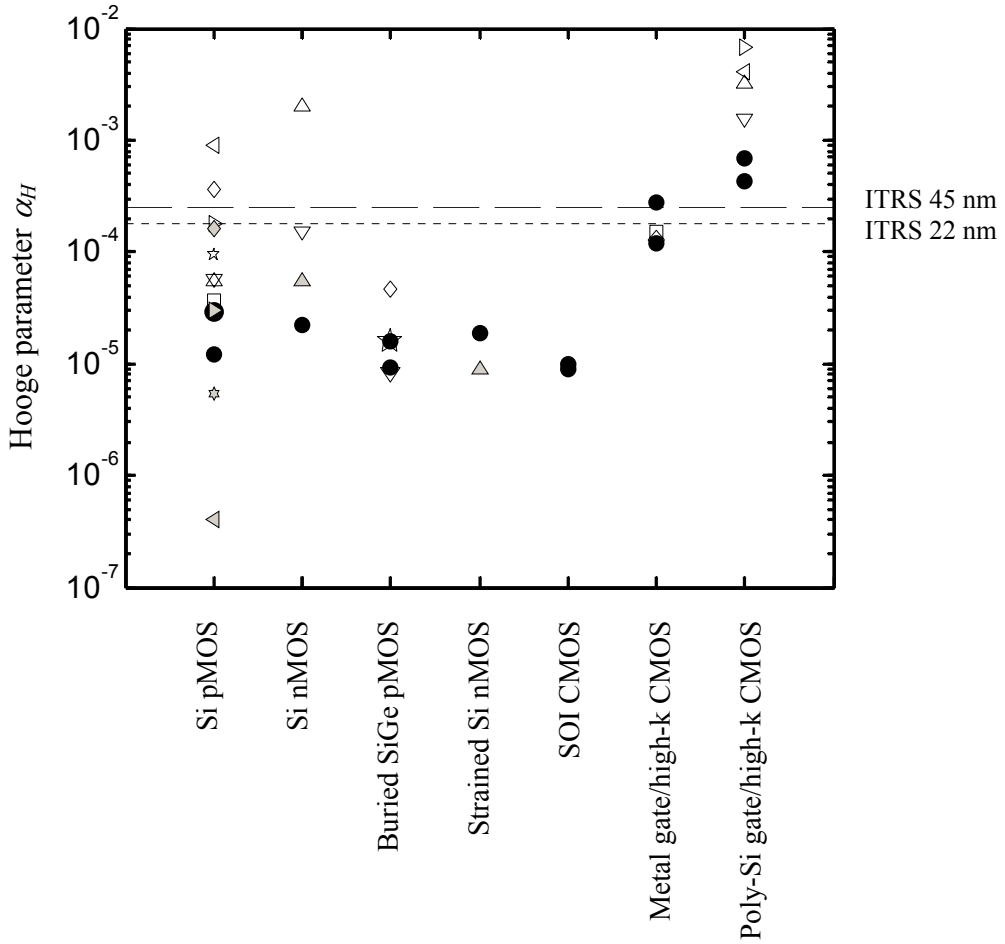

Fig. 6.2. Extracted values of α_H from this work (filled circles) for different CMOS technologies compared with results in literature (other symbols).

input gate voltage noise values given in Table I and are plotted as dotted or broken lines in Figs. 6.1 and 6.2. As seen, the 1/*f* noise performance of the devices fabricated by KTH is among the best reported for every category. Especially the SOI devices are outstanding compared to other recent published results. One reason behind the lower 1/*f* noise in our transistors is that we have used pure thermally grown SiO_2 as gate dielectrics (except in the high-k MOSFETs), whereas the semiconductor industry instead is using oxynitrides, known for their higher 1/*f* noise. Note that N_t is more commonly reported than α_H, especially for nMOS and SOI transistors. We have calculated N_t and α_H from noise results in the literature in some cases when these parameters were not reported. The N_t and α_H values reported in Fig. 6.1 and 6.2 are also listed in appendix III along with a brief description of the devices.

In the following sections, the 1/*f* noise performance of various CMOS technologies are discussed in more detail. Section 6.1 deals with scaled devices and explains why N_t and α_H tend to increase for smaller devices. Buried SiGe channel pMOSFETs have the potential of lower 1/*f* noise compared to surface Si channel pMOSFETs, which is discussed in section 6.2. The topics of section 6.3 and 6.4 are strained Si nMOSFETs and SOI MOSFETs, respectively. The 1/*f* noise is considerably higher in transistors

with high-k gate dielectrics, as evidenced in Fig. 6.1. MOSFETs with high-k gate dielectrics in form of HfO_2, Al_2O_3 and $HfAlO_x$ have been studied extensively in this work; the results are presented in section 6.5. The influence of metal gate on the 1/*f* noise performance is discussed in section 6.6. Finally, 1/*f* noise in FinFETs is reviewed in section 6.7.

6.1 Scaled devices

The normalized drain current noise PSD S_{I_D}/I_D^2 varies inversely with gate area for both number and mobility fluctuation noise according to Eqs. (4.6), (4.11) and (4.14). Further downscaling of the gate length therefore leads to increased noise. However, the oxide thickness is also downscaled, which either can worsen or improve the 1/*f* noise performance. For the number fluctuation noise model, $S_{V_G} \propto 1/C_{ox}^2 \propto t_{ox}^2$, while $S_{V_G} \propto 1/C_{ox} \propto t_{ox}$ in Hooge's model. Thus, lower noise is expected for MOSFETs with thinner oxides according to the models. On the other hand, nitridation of the SiO_2 gate oxide forming oxynitride (SiON) is necessary in order to scale down the oxide thickness for the technology nodes beyond 0.18 μm (t_{ox} ~ 3.5 nm). Further on, at the 65 nm node, the nitrided SiO_2 run out of steam and must be replaced with high-k gate dielectrics in order to control the gate leakage current. The advantages with oxynitrides are prevention of boron penetration through the gate oxide and improved hot carrier reliability. The dielectric constant is also slightly higher. The dielectric constant of Si_3N_4 and SiO_2 is 7 and 3.9, respectively. Oxynitrides will have a value in between those, depending on the nitrogen content. However, the nitrogen incorporation into the SiO_2 introduces charged traps in the oxide, which cause a reduction of the mobility due to Coulomb scattering as well as higher 1/*f* noise. The high-k gate dielectric MOSFETs show even worse noise performance, which will be addressed later in chapter 6.5.

In the following, we will review the properties of MOSFETs with oxynitrides. A small mobility reduction at low electric field is usually observed for both electrons and holes due to the increased oxide charge [77, 200]. At high electric fields, on the other hand, electrons and holes show different behaviours. It has been reported that the electron surface roughness mobility is increased in oxynitrides, whereas a reduction is found for holes, which was explained by a change in nature of the interface geometry by NO oxidation [201]. It is now well established that MOSFETs with nitrided gate oxide exhibit higher 1/*f* noise than that for devices with pure SiO_2. Morfouli *et al*. showed that N_t increases exponentially with the nitrogen content ranging between 0 – 11% [202]. P-channel MOS transistors are more affected by the nitrogen than the n-channel ones, Da Rold *et al*. reports a factor of 7-8 increase in 1/*f* noise for pMOS and 2-3 for nMOS with NO annealed oxides [203]. In the same study, a positive charge density equal to 8.7×10^{11} cm^{-2} was found to be introduced by the nitrogen in the pMOSFETs, whereas the nMOSFETs received an extra charge density of 2.9×10^{11} cm^{-2}. The correlation between the 1/*f* noise level and the oxide charge density indicates that oxide traps are responsible for the 1/*f* noise. However, some issues are still unexplored. As mentioned in chapter 4.4, the type of trap determines if the mobility fluctuations are negatively or positively correlated to the number fluctuations. A positive oxide charge indicates a negative correlation for nMOS and a positive correlation for pMOS, but a positive correlation is observed for both device types in the works by Morfouli *et al*. and Da Rold *et al*. The oxide/channel interface

properties and the mobility are also affected by the NO oxidations, which may increase the mobility fluctuation noise. This could be interesting topics for future work. Trap densities above 10^{18} $cm^{-3}eV^{-1}$ are often found in MOSFETs with nitrided gate oxides, which could disenable their use in analog applications. The 1/*f* noise can be reduced by locating the nitrogen peak away from the oxide/channel interface, which can be achieved by plasma nitridation [204] or O_2 re-oxidation [203].

Another problem related to the downscaling of the gate oxide thickness is the escalating gate leakage current, exponentially increasing with decreasing t_{ox}. A high gate leakage current is a problem for device reliability and also leads to higher power consumption. Moreover, 1/*f* noise and shot noise in the gate leakage current can dominate the output drain current noise under such conditions. Valenza *et al*. found that the 1/*f* noise in the gate current of a pMOSFET from a 90 nm CMOS technology with t_{ox} = 1.5 nm gave a significant contribution to the drain current noise [159]. Thus, noise stemming from the gate leakage current is expected to be a major problem in present and future CMOS technologies. Lee and Bosman have analyzed the gate leakage current noise in detail and developed a model, for further reading see [205-208].

An elevation of the average noise level is not the only concern for downscaled devices. The device-to-device variations in the 1/*f* noise performance increase when the gate area is reduced. Statistical fluctuations in the number of traps among an ensemble of devices will have a large impact on the 1/*f* noise level when the devices are so small that only a few traps are present. The relative standard deviation of the number of traps is given by Brederlow *et al*. as [164]

$$\sigma_{N_t} = 1/\sqrt{N_t \cdot W \cdot L} \tag{6.1}$$

Even if the average 1/*f* noise is below the required limit, some devices could display much higher noise. The modeling of the 1/*f* noise becomes more difficult; one has to include also the standard deviation in the models [209].

Further effects that come into play in aggressively scaled transistors are defects at the edges in narrow transistors leading to higher 1/*f* noise [210], hot carriers which may cause degradation of the gate oxide and increased noise [12], and field-dependence on the Hooge parameter [100]. One interesting phenomena in ultra short devices in the 10-nm range and below is the occurrence of ballistic transport; some carriers might traverse from source to drain without being scattered. 1/*f* noise generated from the involvement of phonons might decrease in such case.

6.2 SiGe channel pMOSFETs

A field-effect transistor in which the current flows in a buried channel separated from the oxide/semiconductor interface can exhibit much lower 1/*f* noise than that in surface channel transistors. This has been observed for JFETs [137, 138], buried Si channel MOSFETs fabricated by counter doping the surface of the substrate (n-type for nMOS and p-type for pMOS) [132, 133, 135] and buried SiGe channel pMOSFETs. Several groups have reported lower 1/*f* noise with a factor between 4 and 10 in buried SiGe channel pMOSFETs [9, 10, 43, 211, 212]. However, a reduction is not always observed [213]. In this work, lower 1/*f* noise by a factor of two was found

in SiGe devices with a "medium" thick Si-cap. Note that the 1/*f* noise performance of the best surface Si channel pMOSFETs is at the same level (or lower) as the buried SiGe channel pMOSFETs according to Fig. 6.2. One reason behind the significant reduction of the 1/*f* noise reported in some work for the SiGe devices in comparison with the Si references may actually be due to poor noise performance of the references. For Si pMOSFETs with $\alpha_H \sim 10^{-5}$ or $N_t \sim 5\times10^{16}$ $cm^{-3}eV^{-1}$ one can probably expect a less pronounced noise reduction.

Three different origins of the 1/*f* noise reduction in buried SiGe channel pMOSFETs have been suggested. Mathew *et al*. explain the lower noise in the buried channel devices with a lower trap density at the quasi-Fermi level [10]. The valence band offset between Si and SiGe leads to a lower surface potential at the oxide/Si interface than in a surface channel device biased at the same gate voltage overdrive. The interface traps are typically distributed with a higher density close to the valence and conduction band edges and lower density in the middle of the bandgap ("U-shaped"). The Ge-induced valence band offset increases the separation of the quasi-Fermi level from the valence band, which reduce the number of traps that are active in the noise generation if the oxide traps are assumed to be U-shaped in energy. This model has been adopted by other research groups as well, for example Prest *et al*. [43] to mention one. However, it has not been established that the oxide trap density varies appreciably with energy as the model by Mathew *et al*. requires. One consequence of the model is that decreasing the Si-cap thickness and increasing the Ge-content would result in stronger noise reduction. However, this is seldom observed. In this work we found the best 1/*f* noise performance for a Si-cap thickness around 5-6 nm, devices with both thicker and thinner cap showed higher 1/*f* noise. A similar conclusion was found by Prest *et al*. Ghibaudo and Chroboczek [213] as well as Tsuchiya *et al*. [211] report higher 1/*f* noise for the highest Ge-fractions used in their experiments compared to devices with a moderate Ge-fraction. It should be noted that the density of interface states increases for thin cap layers and high Ge-fractions, which could explain the observed behaviour. However, by biasing the surface Si and buried SiGe channel pMOSFETs in an appropriate way so that the quasi-Fermi levels in the two devices are equally distant from the valence band edges, the extracted trap densities would be roughly equal. In a recent publication Prest *et al*. [214] have been successful with this kind of exercise by including a Hooge mobility fluctuation noise term ($\alpha_H = 2\times10^{-5}$) also, which was not considered in earlier work.

Another model based on correlated mobility fluctuations was presented by Ghibaudo and Chroboczek. They assert that the correlated mobility fluctuations related to Coulomb interaction between the trapped carrier and the channel carriers diminish in the buried channel devices due to the large separation between the traps and the channel. The drain current noise PSD can then be written

$$S_{I_D} = S_{V_{fb}}\left[g_{m,cap}\left(1+\alpha C_{ox}\mu_{eff,cap}I_{D,cap}/g_{m,cap}\right)+g_{m,SiGe}\left(1+R\alpha C_{ox}\mu_{eff,SiGe}I_{D,SiGe}/g_{m,SiGe}\right)\right]^2 \tag{6.2}$$

where the subscripts 'cap' and 'SiGe' refer to the cap and the SiGe-channel, respectively. The parameter *R* is a reduction factor around 0.1-0.2. This model can successfully explain a 1/*f* noise reduction for a buried SiGe channel device biased in

strong inversion and is supported in the work by Myronov *et al*. [215], but fails below threshold since correlated mobility fluctuations are unimportant in this region of operation. In fact, the strength of the correlated mobility fluctuations is under debate; see our discussion in chapter 4.4. Moreover, Prest *et al*. could not explain their data using only correlated mobility fluctuations [214].

A third alternative to explain the lower 1/*f* noise in buried SiGe pMOSFETs was elaborated in paper I. The fact that Hooge mobility fluctuation noise often is found to be the dominant 1/*f* noise source in pMOSFETs was neglected in the previous models. The mobility fluctuation noise is sensitive to the "quality" of the semiconductor material. In chapter 4.4, we discussed the possibility that phonon interactions with defects, surfaces and other phonons cause a fluctuation in the phonon population which modulates the phonon-electron scattering, i.e. the mobility. If the carriers are in close proximity with the gate oxide, the dynamical fluctuation in the mobility is expected to be higher than in the bulk. A buried SiGe pMOSFET have two conducting channels; the high-mobility buried SiGe channel and a low-mobility parasitic channel in the Si-cap. A very simple approximation of the carrier distributions in the SiGe and Si channels is

For $V_T \le V_{GS} \le V_{T2}$

$$Q_{i,SiGe} = C_{ox,SiGe}(V_{GS} - V_T) \qquad (6.3)$$
$$Q_{i,cap} = 0$$

for $V_{GS} \ge V_{T2}$

$$Q_{i,SiGe} = C_{ox,SiGe}(V_{T2} - V_T) \qquad (6.4)$$
$$Q_{i,cap} = C_{ox}(V_{GS} - V_{T2})$$

where $1/C_{ox,SiGe} = 1/C_{ox} + t_{cap}/\varepsilon_{si}$

The Hooge mobility fluctuations can be described by different Hooge parameters for the two channels since uncorrelated noise currents can be assumed [213]

$$\frac{S_{I_D}}{I_D^2} = \frac{q\alpha_{H,cap}}{fWLQ_{i,cap}}\frac{I_{D,cap}^2}{I_D^2} + \frac{q\alpha_{H,SiGe}}{fWLQ_{i,SiGe}}\frac{I_{D,SiGe}^2}{I_D^2} \qquad (6.5)$$

The normalized drain current noise is plotted versus gate voltage overdrive V_{GT} for a buried SiGe channel pMOSFET in Fig. 6.3. As seen, S_{I_D}/I_D^2 flattens out at V_{GT} ~0.2 V, which is due to the onset of the parasitic channel. The solid line in Fig. 6.3 is a simulation using Eq. (6.5) with $\alpha_{H,cap} = 7\times10^{-5}$, $\alpha_{H,SiGe} = 1.5\times10^{-5}$ and $|V_{T2} - V_T| =$ 0.25 V. The 1/*f* noise generated in the parasitic current dominates in this case at a $V_{GT} \ge 0.4$ V. Reducing the Si-cap thickness will postpone the onset of the parasitic current to higher V_{GT}. A thin Si-cap would therefore be desired both to obtain a high drive current and low noise. However, as the SiGe channel moves closer to the gate oxide interface, the noise generated in the SiGe channel increases. In Fig. 6.4, the normalized drain current noise is plotted for SiGe pMOSFETs with different thicknesses of the Si-cap. The normalized drain current noise falls off roughly as $1/V_{GT}$ or weaker, which indicates that mobility fluctuation noise is the origin of the 1/*f*

noise. The device with a 3-nm thin Si-cap shows very similar 1/*f* noise level as the Si device, which indicates that a too thin Si-cap can deteriorate the noise performance of the SiGe channel. The device with a 7-nm thick Si-cap is likely dominated by the 1/*f* noise in the parasitic current at very low $V_{GT} \geq 0.1$ V since the S_{I_D} / I_D^2 curve closely follows the one for Si. A 1/*f* noise reduction with a factor of two was observed for the devices with a medium thick Si-cap (5-6 nm), which optimise the trade-off between distance from the notorious Si/SiO_2 interface and parasitic current. It is interesting to note that significantly lower 1/*f* noise was found in a SiGe pMOSFET, labelled with X in Fig. 6.4, fabricated on a low-doped substrate (~10^{14} cm^{-3}) without well or channel implantation. The other SiGe devices were implanted with As to a peak concentration of 2×10^{18} cm^{-3}. The lower doping results in a better hole confinement in

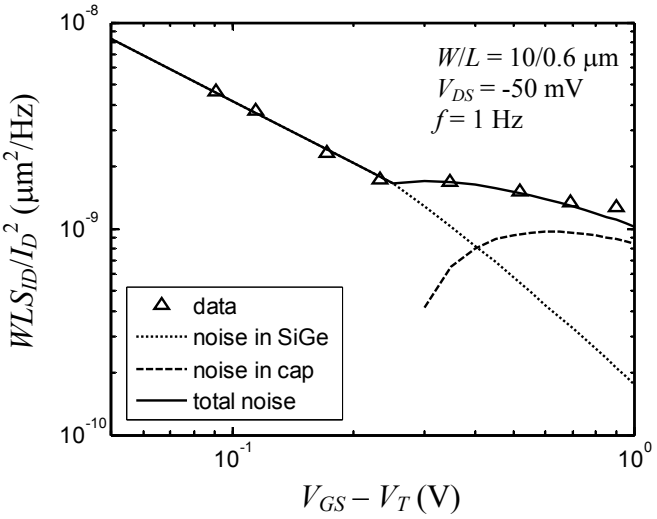

Fig. 6.3. Measured and simulated drain current noise for a buried SiGe channel pMOSFET with 5-nm Si-cap (data from paper I). Eq. (6.5) was used for the simulation.

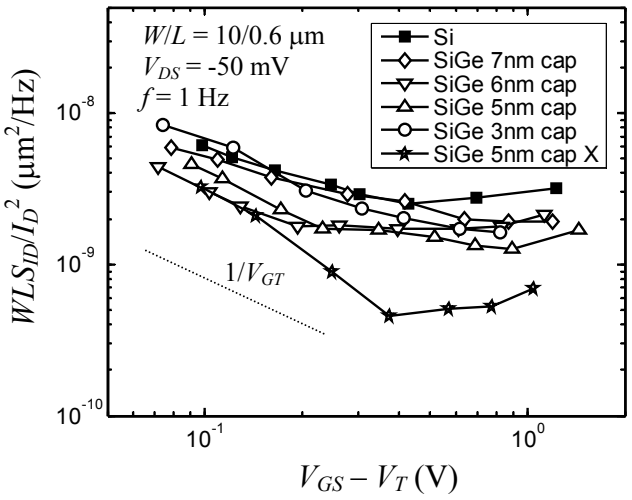

Fig. 6.4. Drain current noise measured in buried SiGe channel pMOSFETs with different Si-cap thickness (from paper I).

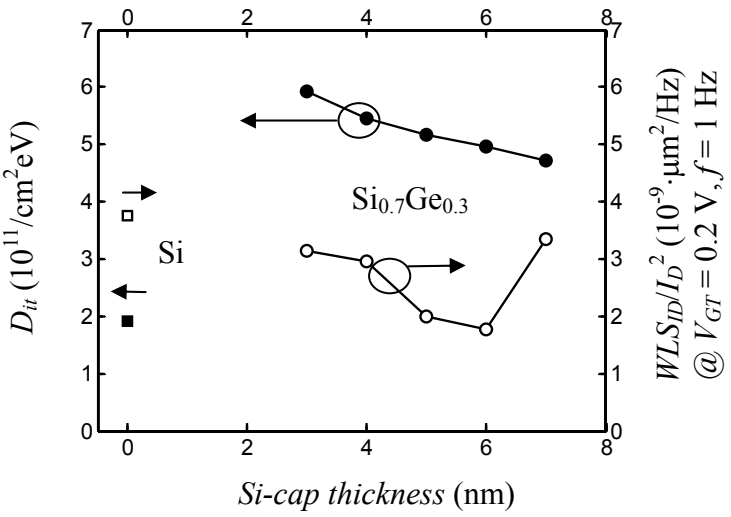

Fig. 6.5. Density of interface states and drain current noise extracted at V_{GT} = 0.2 V plotted vs. Si-cap thickness (estimated from TEM images) for SiGe pMOSFETs (from paper I).

the SiGe channel since the voltage drop in the Si-cap is reduced. As seen in Fig. 6.4, the parasitic channel turns on at a higher V_{GT} than in the other SiGe devices. Obviously, a too low doping leads to problems with short channel effects in a standard bulk MOSFET, but the concept can be employed in SOI MOSFETs.

The density of interface states and the normalized drain current noise extracted at V_{GT} = 0.2 V are plotted versus Si-cap thickness in Fig. 6.5. One possible origin behind the increased 1/*f* noise for the devices with thin Si-cap could be the degradation of the interface. Direct oxidation of SiGe results in the creation of interface traps [41, 42]. Ge atoms diffuse to the interface during the epitaxy step and preceding high-temperature steps, more Ge atoms will reach the interface as the distance is shortened. However, the density of interface states is always lower in the Si device than in the SiGe ones, which indicates that the interface traps are not likely the main origin of the 1/*f* noise.

Decisive arguments in favour of the mobility noise model were obtained from noise experiments where the substrate voltage was varied. As explained in chapter 4.3, the position of the inversion carriers depends on the surface electric field perpendicular to the channel direction, which is varied by the substrate voltage. The results strongly indicate that moving the carriers closer to the interface result in an increase of the 1/*f* noise, and vice versa, which is best explained within the framework of the Hooge mobility noise theory. A consequence of the *E*-field dependence of the 1/*f* noise is that the Hooge parameter is expected to increase with increasing V_{GT}. As a matter of fact, this has been observed in our experiments. The Hooge parameter for the Si pMOSFETs was found to vary as $\alpha_H = 2.9\cdot10^{-5}\cdot(V_{GT}/0.1)^{0.38}$. In other work, such behaviour has often been assumed to be due to a trap density that increases towards the valence band edge, but in our opinion it could be explained by a Hooge parameter that depends on the effective field.

In summary, buried SiGe channel pMOSFETs can exhibit lower 1/*f* noise than in Si pMOSFETs fabricated with the same technology. A moderate reduction by a factor of

two was obtained in this work, which likely can be improved by optimization of the SiGe channel and Si-cap thickness. There are two competing noise mechanisms in a buried SiGe channel pMOSFET: (i) the 1/*f* noise generated in the buried channel which decreases as the channel is positioned further from the SiO_2/Si interface, and (ii) the 1/*f* noise generated in the noisy Si-cap which decreases as the confinement in the SiGe channel is improved by, for example, lower doping and/or thinner Si-cap. Buried channel pMOSFETs are advantageous to use in low-power analog applications in view of the low noise at small V_{GT}, high mobility and enhanced intrinsic gain g_m/g_{ds} [43, 47]. Note that the α_H and N_t values (we find the former description more useful, but both parameters are reported for the sake of comparison with literature) are summarized in appendix III.

6.3 Strained Si nMOSFETs

Tensile strained Si nMOSFETs present increased electron mobility compared to unstrained Si references without degraded 1/*f* noise performance [216]. Simoen *et al*. even report reduced 1/*f* noise in strained Si devices fabricated on thin SiGe strained-relaxed buffer (SRB) layers [197]. One disadvantage by using global techniques with a relaxed SiGe buffer to induce the tensile strain in the Si channel is the presence of threading dislocations. It has been reported that large area devices (625 μm^2 in the particular case) have a higher probability of a threading dislocation penetrating in the channel and therefore also present degraded 1/*f* noise performance [216]. Ge outdiffusion from the Si/SiGe heterojunction can also lead to higher 1/*f* noise by the creation of traps at the oxide/Si interface [217]. High temperature steps in the fabrication process should therefore be avoided.

We have recently initiated 1/*f* noise investigations of strained Si nMOSFETs fabricated on 200-nm thin relaxed SiGe virtual substrates. The normalized drain current noise is plotted in Fig. 6.6 indicating similar 1/*f* noise performances of the strained and unstrained nMOSFETs. The normalized drain current noise follows a $1/I_D$ behaviour above threshold, which could indicate that Hooge mobility noise is the origin of the 1/*f* noise. However, the frequency exponent strongly deviates from unity in weak inversion and at low V_{GT}, and g-r noise bumps were frequently observed as well. Fig. 6.7 shows the variation of the frequency exponent γ with gate bias. These observations indicate that trapping/release phenomena are present (as well), since $\gamma \sim 1$ is expected for Hooge mobility noise. An analysis of the input gate voltage noise in Fig. 6.8 shows that it increases super-linearly with increasing I_D/g_m ($\sim V_{GT}$) above threshold. Extraction of the Coulomb scattering parameter α suggests that the 1/*f* noise can be satisfactorily described by correlated mobility fluctuations. The parameter α equals 2.3×10^4 and 1.7×10^4 Vs/C for the Si reference and the strained Si nMOSFETs, respectively. The values are somewhat higher than expected ($\sim1\times10^4$ Vs/C), which may indicate contributions from Hooge mobility fluctuations at high gate bias. The parameter α is proportional to the electron mass according to theoretical calculations [141], which explain the lower α for the strained nMOSFET. The scatter in the noise data is smaller at high V_{GT} at the same time as the frequency exponent stabilize at a value close to 1, which suggest that N_t is higher at elevated V_{GT} or that another noise source than traps contributes in this region of operation. This "other" noise source could be Hooge mobility fluctuations or noise contributions from the S/D resistance, further investigations are necessary to clarify which of the two possibilities that is more likely.

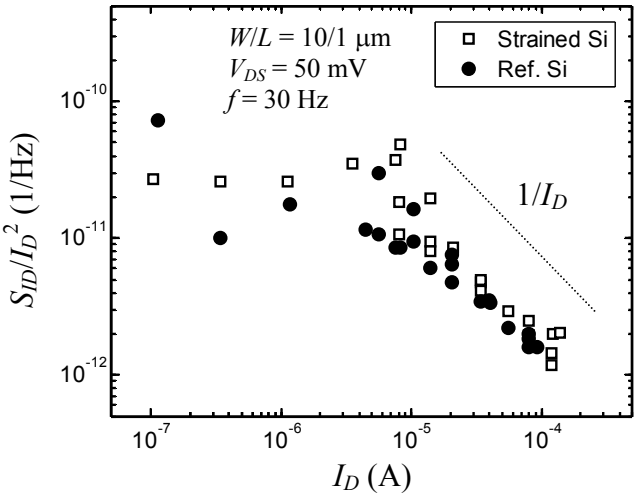

Fig. 6.6. Drain current noise of strained and unstrained Si nMOSFETs.

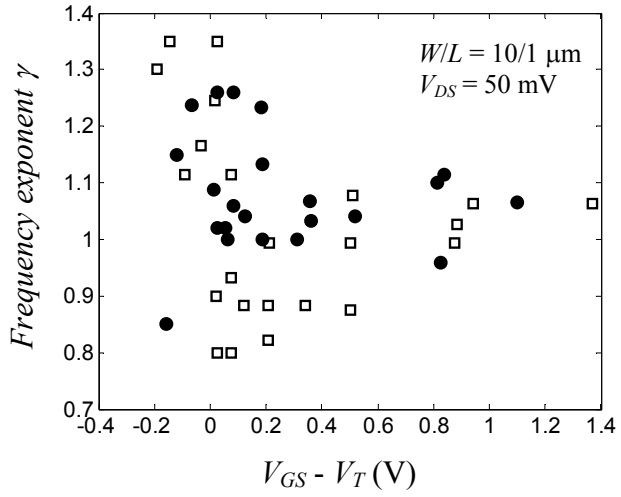

Fig. 6.7. Frequency exponent plotted vs. gate voltage overdrive for strained (open squares) and unstrained (closed circles) Si nMOSFETs.

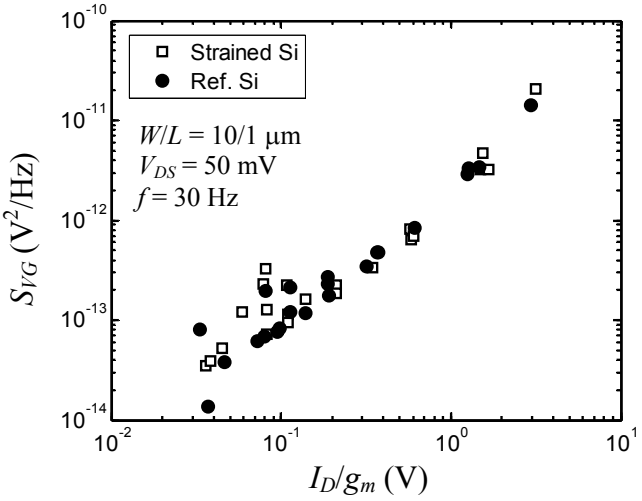

Fig. 6.8. Input gate voltage noise vs. I_D/g_m for strained and unstrained Si nMOSFETs.

In summary, 1/*f* noise investigations of strained and unstrained Si nMOSFETs show that both types of devices can be explained by number fluctuation noise with $N_t \sim 4\times10^{16}$ $cm^{-3}eV^{-1}$. The more complicated fabrication process for the strained Si nMOSFETs does not result in degraded 1/*f* noise performance. This type of device is therefore suitable for high-speed analog applications thanks to their high mobility and low noise. A more detailed analysis is needed to establish the exact mechanism behind the noise behaviour at high V_{GT}.

6.4 Silicon-On-Insulator (SOI) MOSFETs

In the past, MOS transistors fabricated on SOI-substrates were notorious for their poor low-frequency noise performance compared to bulk CMOS. There are several reasons why SOI MOSFETs were noisier; in addition to the noise generated at the front oxide interface, appreciable low-frequency noise can also be generated at the back interface, from defects in the Si-body, and due to floating body effects [11]. Naturally, the type of device (partially or fully depleted CMOS) and choice of SOI substrate (UNIBOND, SIMOX etc) can have a large impact on the low-frequency noise performance. Extensive advances have recently been made in improving the quality of the SOI substrates providing prime quality and relatively inexpensive UNIBOND substrates for example, which potentially can result in improved noise performance in SOI technologies. However, by comparing the recently reported trap densities for SOI MOSFETs, most of them fabricated on UNIBOND substrates, with those for standard bulk CMOS in Fig. 6.1, the values for SOI are still noticeable higher.

The other side of the coin is that SOI MOSFETs can be designed to produce very low noise under certain conditions [218, 219]. The position of the conduction channel can be varied from surface to bulk mode by the front and back gate voltage, which affects the noise properties. Ultimately, for sufficiently thin Si-body thickness (below ~10 nm) the interior of the body is inverted which separates the carriers from the noisy oxide interfaces. The concept of *volume inversion*, first invented by Balestra *et al*. [94], is very attractive to achieve high mobility, transconductance and low noise. In this work, we will demonstrate SOI pMOSFETs with improved low-frequency noise performance compared to similar bulk devices by exploiting the buried channel concept. First, we will describe the difference between fully depleted (FD) and partially depleted (PD) devices.

Partially depleted SOI

Partially depleted devices are fabricated on SOI substrates with a thick body ($t_{Si} > 2\sqrt{4\varepsilon_{Si}\psi_B / qN_{body}}$) so that only a part of the body is depleted and a neutral piece of Si exists. This type of device behaves exactly as a bulk MOS device with the exception of parasitic effects related to the electrically floating body. Charging of the body due to impact ionization effects in the high-field region near the drain or tunneling of carriers through the gate oxide will reduce the threshold voltage and cause a “kink” in the drain current at the output. Closely linked to the static behaviour is a noise overshoot occurring at the same bias conditions. The kink-related excess low-frequency noise appears as Lorentzian-like components in the spectra and arises from the shot noise in current that discharge the body through the S/B junction [220]. It is typical that the noise plateau ($\propto 1/I_{SB}$) and the corner frequency ($\propto I_{SB}$) of the Lorentzian-like excess noise shift with bias. The low-frequency noise observed at a certain frequency displays a sharp maximum for a particular V_{DS} (or V_{GS}) that can be

one or two orders of magnitude above the normal noise level. The kink-related excess noise can be almost eliminated by connecting the body to the ground [191, 220].

Fully depleted SOI

In fully depleted devices, the thin Si-body ($t_{Si} < \sqrt{4\varepsilon_{Si}\psi_B / qN_{body}}$) is fully depleted, the depletion region covers the whole body and does not extend with gate bias. Fully depleted SOI devices are normally free (or almost free) of floating body effects, but appear if the back interface is in accumulation [221]. Fully depleted MOSFETs are in theory dual-gate devices, the inversion channel can be controlled by both the front and back gate voltage. However, the buried oxide on a standard SOI wafer is usually much thicker than the front gate oxide. To obtain a symmetric behaviour, the back gate voltage must be much larger than the voltage on the front ($V_{BG} \sim t_{box}/t_{fox} \cdot V_{FG}$). This coupling between the front and back gate leads to increased noise as the noise generated from traps at the back interface then couples out to the output and adds to the drain current noise. The following equation describes the coupling effect on the drain current noise [192]

$$S_{I_D} \approx g_{m,f}^2 \left(S_{Vfb,f} + \frac{C_{Si}^2 \cdot C_{box}^2}{C_{fox}^2 (C_{box} + C_{Si})^2} S_{Vfb,b} \right) \tag{6.6}$$

where $g_{m,f}$ is the front-channel transconductance. $S_{Vfb,f}$ and $S_{Vfb,b}$ are the front and back gate flat-band voltage PSD, respectively. In the limit $C_{Si} >> C_{box}$

$$S_{I_D} \approx g_{m,f}^2 S_{Vfb,f} (1 + N_{t,b} / N_{t,f}) \tag{6.7}$$

Here, $N_{t,b}$ and $N_{t,f}$ are the oxide trap densities for the back and front oxide, respectively. Obviously, if the buried oxide is of poor quality ($N_{t,b} >> N_{t,f}$), the low-frequency noise performance is severely degraded. For the Hooge mobility fluctuations, the following relationship can be predicted (uncorrelated noise sources)

$$\frac{S_{I_D}}{I_D^2} = \frac{q\alpha_{H,f}}{fWLQ_{i,f}} \frac{I_{D,f}^2}{I_D^2} + \frac{q\alpha_{H,b}}{fWLQ_{i,b}} \frac{I_{D,b}^2}{I_D^2} \tag{6.8}$$

If little current is carried at the back interface, mobility fluctuation noise will mainly be generated in the front channel. The number fluctuation noise is more sensitive to coupling effects due to the $1/C_{ox}^2$ dependence compared to the $1/C_{ox}$ scaling for mobility fluctuations.

Accumulation-mode pMOSFETs

Buried channel devices are easily realized in SOI technology. A p-channel MOS transistor fabricated on a p-type SOI substrate work in the accumulation mode; the inversion charge is spread out in the body instead of piling up the front and back oxide interfaces [222], see the schematic band diagram in Fig. 6.9. By using a thin fully depleted Si-body, no current flows between source and drain in the off-state and the short-channel effects are well controlled even for a low-doped Si-body. In this work, FD pMOSFETs were fabricated on a 20 nm thin Si-body with a light p-type

doping (0.6-1 $\times 10^{15}$ cm^{-3}). The same type of wafers was used to fabricate SiGe pMOSFETs and partially depleted Si pMOSFETs as well, as described in chapter 2.6. The average distance of the inversion charge from the front oxide interface was simulated for the FD Si pMOSFETs (t_{ox} = 3 nm, t_{box} = 400 nm, $N_{A,body} = 1\times10^{15}$ cm^{-3}) and compared with the result for a bulk Si pMOSFET designed for ~0.1 μm gate length (t_{ox} = 3 nm, $N_{D,sub} = 7.7\times10^{17}$ cm^{-3}), the result is displayed in Fig. 6.10. Fig. 6.11 shows the hole density versus depth in the SOI device for two different gate voltages. The normalized drain current noise for these two devices, both fabricated at KTH using pure thermally grown oxide as gate dielectrics, is plotted in Fig. 6.12. A clear noise reduction is found for the SOI pMOSFETs and a low $\alpha_H \sim 9\times10^{-6}$ was extracted. This outcome is difficult to explain with the number fluctuation noise theory as an increase with the factor $(1 + N_{t,b} / N_{t,f})$ normally is expected for a FD

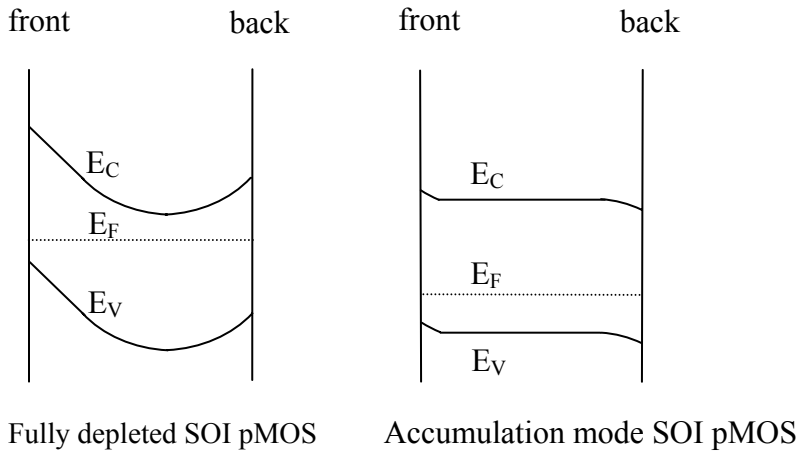

Fig. 6.9. Schematical band diagrams for a FD SOI and an accumulation mode SOI pMOSFET.

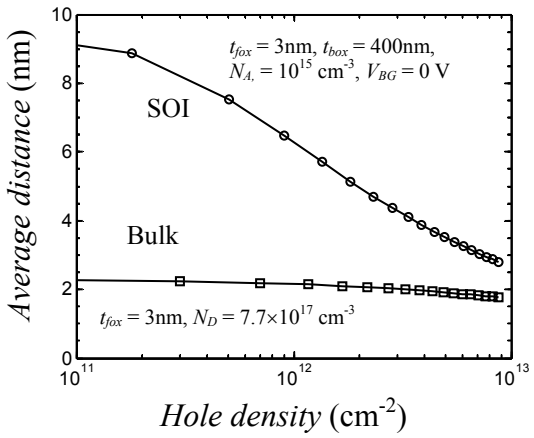

Fig. 6.10. Schred simulation [223] of the average distance of the inversion carriers from the front gate oxide interface in a SOI and a bulk Si pMOSFET.

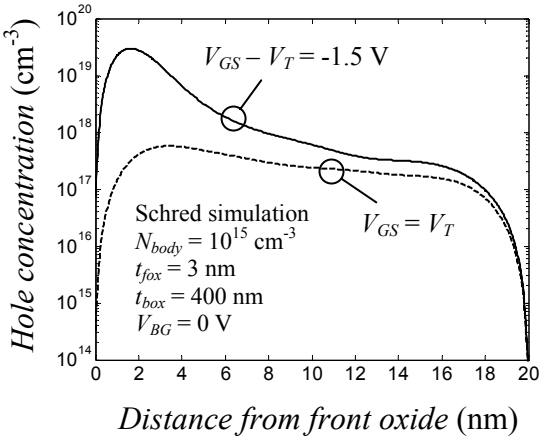

Fig. 6.11. Simulated distribution of holes in the 20-nm thin body of a SOI pMOSFET.

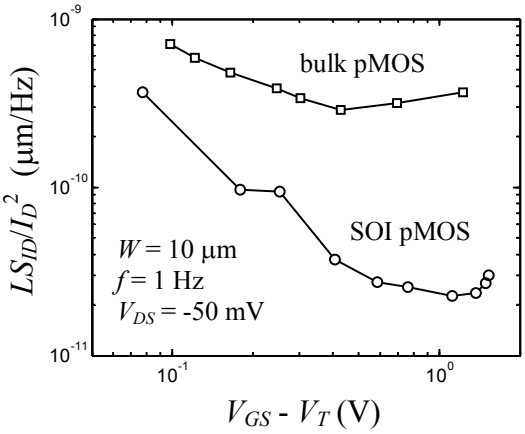

Fig. 6.12. Drain current noise measured in a bulk and a FD SOI pMOSFET (data from paper I and III).

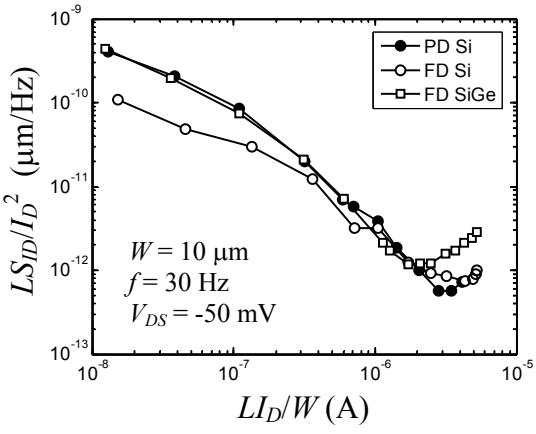

Fig. 6.13. Drain current noise measured in different SOI pMOSFETs (data from paper III).

SOI device. Invoking correlated mobility fluctuations and claiming that this effect is negligible in the SOI device due to the longer distance between the traps and the inversion charge is not a traversable way. Extraction of the parameter α gives the value 1.9×10^5 Vs/C for the bulk Si device, which is roughly an order of magnitude to high to be physically correct. For the FD device a more reasonable value was obtained, $\alpha \sim 1.5\times10^4$ Vs/C.

Utilizing a compressively strained SiGe channel on SOI gave ~50% enhanced hole mobility (see paper III, Fig. 1) and we was aiming for improved low-frequency noise performance as well. However, the low-frequency noise was not found to be lowered in the SiGe device compared to Si in this case, as seen in Fig. 6.13. The SiGe channel was intended to be buried, but the resulting Si-cap was too thin (< 1 nm) to effectively separate the inversion charge from the interface. Thus, optimization of the Si-cap thickness is necessary for improved low-frequency noise performance in buried SiGe channel pMOSFETs, in line with our conclusions in section 6.2. The PD device performs similarly as the FD device, which again indicates the absence of coupling effects. However, number fluctuation noise from the oxide interfaces is possibly contributing to the total output noise in the subthreshold regime and close to threshold in the SOI devices as the frequency exponent in several cases was significantly smaller than 1 ($\gamma \sim 0.5$-0.8) in this regime and g-r noise could be observed. The noise spectra for the PD SOI and bulk Si MOSFETs are plotted in Fig. 6.14, which highlights the different frequency dependencies. No evidence of kink-related excess noise was found either for the Si or the SiGe device in bias range studied as seen in Fig. 6.15, indicating that the problem with floating body is eliminated in the FD device architecture.

Finally, the S/D resistance is a difficult problem in devices fabricated on an ultra-thin Si body. A raised S/D structure is advantageous in order to reduce the S/D resistances to a tolerable level. Fig. 6.16 emphasizes the importance of a low S/D resistance also for the low-frequency noise performance. Schottky-Barrier (SB) pMOSFETs were fabricated where the Ni-silicide from the S/D regions penetrated into the channel and formed NiSi-Si Schottky junctions [224]. The I_D-V_{GS} characteristics of the SB

pMOSFET and a reference device where the Schottky barrier is formed in the extension region is compared in Fig. 6.17. The drain current in the SB device is limited by the reverse biased Schottky barrier at the source side at lower bias. The width of the barrier is decreased at higher gate bias, which enhances the tunneling current across the barrier and the S/D resistance reduces. As seen in Fig. 6.16, S_{I_D} / I_D^2 is independent of I_D, which indicates that the noise originates from the source side in both cases. This follows from Eq. (3.22) by setting $g_{ch} = 0$ (saturation). The fact that the contacts are poor and their area is small ($t_{si} \times W = 0.02 \times 10$ μm^2) make them very noisy. The normalized drain current noise starts to decrease and approach the reference device at $I_D \sim 10^{-5}$ A, which indicates that the noise properties of the contact improve as the contact resistance of the NiSi-Si junction starts to decrease.

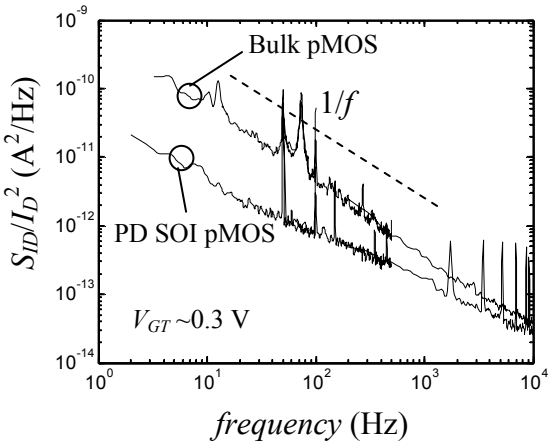

Fig. 6.14. Drain current noise vs. frequency for a PD SOI and a bulk Si pMOSFETs.

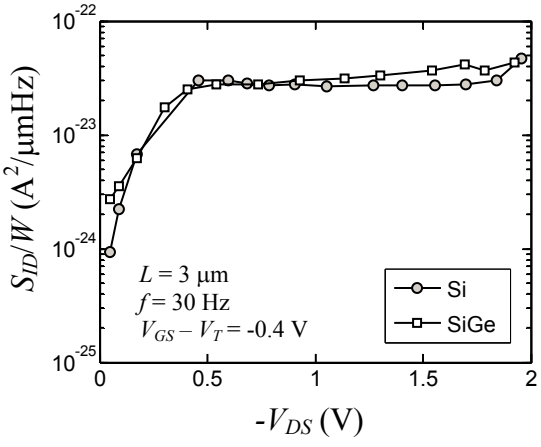

Fig. 6.15. Drain current noise vs. drain-source voltage for two FD SOI pMOSFETs.

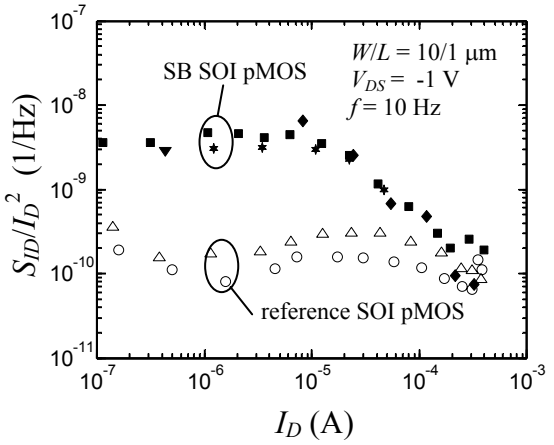

Fig. 6.16. Drain current noise for a Schottky-Barrier and a reference SOI pMOSFET.

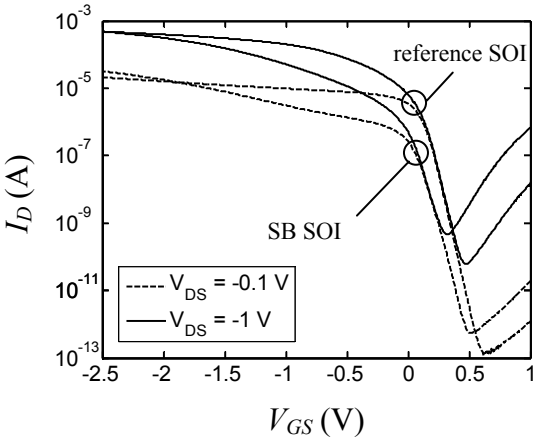

Fig. 6.17. I_D-V_{GS} characteristics for a Schottky-Barrier and a reference SOI pMOSFET.

In summary, the noise properties of SOI MOSFETs were reviewed in this section. SOI devices are more complicated from a noise perspective. It is common that the 1/*f* noise is generated by sources at the front and back oxide interfaces as well as from defects in the Si-body (at least for older SOI substrates of lower quality). Moreover,

floating body effects can give rise to a noise overshoot at higher drain biases and at a gate bias corresponding to the onset of electron valence band tunneling. The use of a FD body was found to eliminate this effect in our study. We also demonstrated that an accumulation mode SOI pMOSFET can exhibit lower 1/*f* noise than its bulk counterpart, which was attributed to buried channel conduction (see also paper III). Excellent 1/*f* noise performance was obtained for the SOI pMOSFETs in this work (FD Si, PD Si, FD SiGe). The devices showed a low $\alpha_H \sim 9\times10^{-6}$ (or $N_t \sim 4\times10^{16}$ $cm^{-3}eV^{-1}$), which is significantly lower in comparison with recent reported results in the literature [189, 191, 192]. The 1/*f* noise dependence on gate bias and the absence of coupling effects suggest that Hooge mobility fluctuations prevail.

6.5 MOSFETs with high-k gate dielectrics

The replacement of the SiO_xN_y gate dielectrics with materials having a higher dielectric constant *k* is required for future CMOS technologies beyond the 65 nm node, in order to maintain a low gate leakage current at the same time as the gate oxide capacitance is scaled up. From a noise perspective, this technology shift leads to orders of magnitude (1-3) higher 1/*f* noise compared to CMOS devices with thermal SiO_2. The higher 1/*f* noise is in most cases ascribed to a high density of traps in the high-k gate dielectrics. However, as will be shown in this work, Hooge mobility fluctuation noise is also important, especially in p-channel MOSFETs. Traps in the high-k material, located from near the channel interface to several nm inside the bulk of the material, can contribute to the 1/*f* noise. Interfaces between different materials are notorious for high trap densities and can cause g-r noise bumps. Simoen and co-workers have demonstrated that electrons tunneling to and from traps in an HfO_2 layer deposited on 2.1-nm SiO_2 is the origin of the $1/f^{\gamma}$ noise in their devices, which illustrates the McWorther type noise mechanisms [225]. This agrees with the observation of instabilities in the threshold voltage, which has been explained by charging and discharging of traps in the high-k material by tunneling [75]. From noise characterizations, trap densities N_t for the high-k materials in the range 1×10^{18} - 1×10^{20} $cm^{-3}eV^{-1}$ have been extracted (see ref. 4-20 in paper VIII). In Fig. 6.18, the different high-k materials are compared. Extracted trap densities for nitrided SiO_2

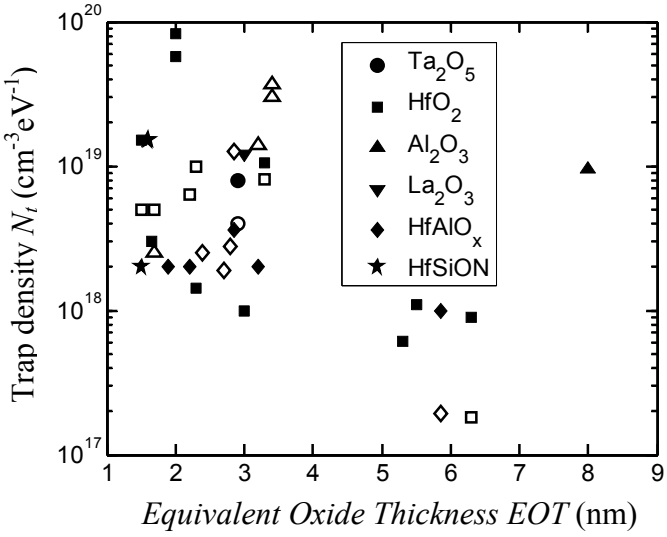

Fig. 6.18. A summary of reported trap densities in the literature (including our work) for different high-k materials plotted vs. EOT. Filled symbols denote nMOS, open symbols pMOS.

range between 1×10^{16} and 1×10^{18} $cm^{-3}eV^{-1}$, as shown in Fig. 6.1. Trap-density profiles in HfO_2 and Al_2O_3 gate dielectrics derived from various charge-pumping schemes are consistent with the results in Fig. 6.18 [65, 185, 186]. It has also been reported that the trap densities in SiO_2 increase when high-k materials are deposited on top [73, 74]. The values at large EOT in Fig. 6.18 are in most cases for devices with a thick layer of SiO_2 between the high-k layer and the substrate, which explains why these perform better. The Hooge parameter is found to be in the range 10^{-4} - 10^{-2} for the transistors with high-k gate dielectrics, which is higher than in conventional MOSFETs ($\alpha_H \sim 10^{-6}$ - 10^{-3}). For a comparison of α_H for different high-*k* materials, see figure 2 in paper VIII and appendix III. The main achievement in this thesis is the comprehensive and original studies of low-frequency noise in MOSFETs with high-k gate dielectrics. Papers IV to VIII are devoted to this topic. The key results are summarized below along with some additional remarks.

Experiment and theory

The high-k gate dielectric stacks in this work were, with one exception, deposited by means of Atomic Layer Deposition (ALD), performed at ASM Microchemistry Oy, Finland. Other techniques, such as Physical Vapour Deposition (PVD, for example sputtering and evaporation), molecular beam epitaxy (MBE), Metal Organic Chemical Vapour Deposition (MOCVD), are available as well. There exists no systematic study of the impact of the deposition methods in relation to noise, as far as we know. However, ALD is recognized for providing uniform layers with low defect densities, and is together with MOCVD the most frequently used deposition technique for high-performance transistors. Claeys *et al.* reported that N_t was found to be lower in ALD high-k layers than that for MOCVD [226].

P-channel transistors were fabricated with high-k stacks consisting of Al_2O_3 layers at top and bottom sandwiching an $HfAlO_x$, HfO_2 or Al_2O_3 layer in the middle. ALD TiN or *in-situ* p^+ doped poly-SiGe was used as gate electrode material. For further information about the device fabrication, please consult the appended papers (IV-VIII).

One particular problem with performing low-frequency noise measurements on transistors with high-k gate dielectrics is the threshold voltage instability. A low-frequency noise measurement from 1 Hz to 100 Hz typically takes several minutes. During this time period, the threshold voltage can shift a few tenths of volts, in the worst case. As the threshold voltage is not fixed, care must be taken when studying the noise variation with the gate voltage overdrive for example. In our measurements, the devices were given some time to settle after each bias point adjustment. The drain current was measured before and after the noise measurements at each bias point and the average current was used in the calculations. As it turned out, the drift and variations in the average drain current and transconductance were acceptably low (< 1%) in most cases, except at very low currents in the subthreshold region. For that reason, noise measurements below I_D =100 nA in an L = 1 μm MOSFET were not found to be useful, since I_D could vary with more than 10%.

From theoretical viewpoint, the difference between MOSFETs with high-k or SiO_2 gate dielectrics concerns the tunneling parameter λ. The barrier height and the effective mass of the carriers differ for the high-k materials and SiO_2, see appendix II for barrier heights of the most common high-k materials on Si. Min *et al.* [74]

calculated λ values equal to 2.10×10^{-8} cm and 1.10×10^{-8} cm for HfO_2 and Al_2O_3, respectively. Both these values are for electrons tunneling from the conduction band in Si to the high-k gate dielectrics. The corresponding value for SiO_2/Si is 1.0×10^{-8} cm. As noise magnitude differences of a factor of two are considered as small, the difference in λ can also be considered as small. A complicating circumstance is if the high-k stack is composed of several layers of different materials. Usually, a thin SiO_2 interfacial layer is present between the substrate and the high-k stack that may not be intentionally grown. In such cases, the calculation of λ is more complicated [227]. Our devices have gate stacks in form of two 5-Å Al_2O_3 layers sandwiching an HfO_2, $HfAlO_x$ or Al_2O_3 layer in the middle, a 0-10 Å thick interfacial layer is found to be present between the bottom Al_2O_3 layer and the substrate. For the sake of simplicity and the insignificant differences in the λ parameter values, we used the values calculated for the SiO_2/Si(Ge) system in our work. Therefore, for our pMOSFETs the following values were used

$$\lambda_{high-k/Si} = 0.81\times10^{-8}\ \text{cm},\ \lambda_{high-k/Si_{0.8}Ge_{0.2}} = 0.80\times10^{-8}\ \text{cm},\ \lambda_{high-k/Si_{0.7}Ge_{0.3}} = 0.79\times10^{-8}\ \text{cm}$$

Gate dielectric material (papers IV, VII, VIII)

Three different high-k materials were studied in this work: Al_2O_3, $HfAlO_x$ and HfO_2. As mentioned in chapter 2, HfO_2 is presently the main contender to replace oxynitrides in future CMOS devices. Fig. 6.19 illustrates typical normalized drain current noise power spectral density S_{I_D}/I_D^2 versus frequency for the TiN/$HfAlO_x$/Si pMOSFET biased at different gate voltages ranging from below threshold to strong inversion. The drain current noise was observed to be of the $1/f^{\gamma}$-type for several decades with the frequency exponent γ in the range 0.9-1.2 for almost all devices in this study. A γ value close to 1 was always observed in strong inversion, whereas some samples of the Al_2O_3 and the HfO_2 devices showed γ up to 1.2 when biased in the subthreshold regime.

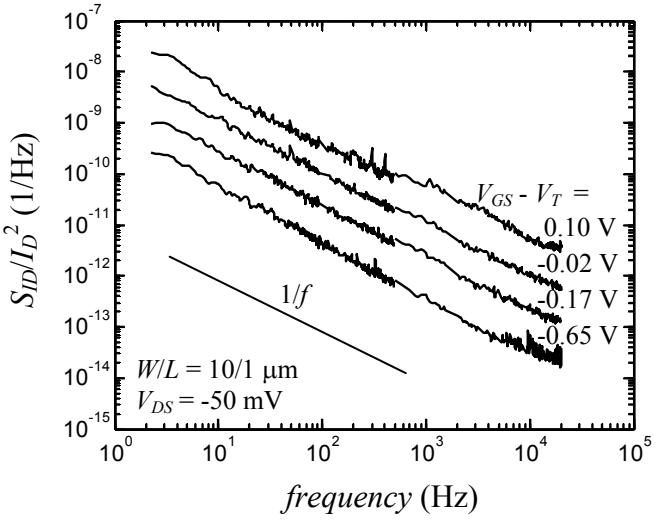

Fig. 6.19. Drain current noise vs. frequency for a TiN/$HfAlO_x$/Si pMOSFET.

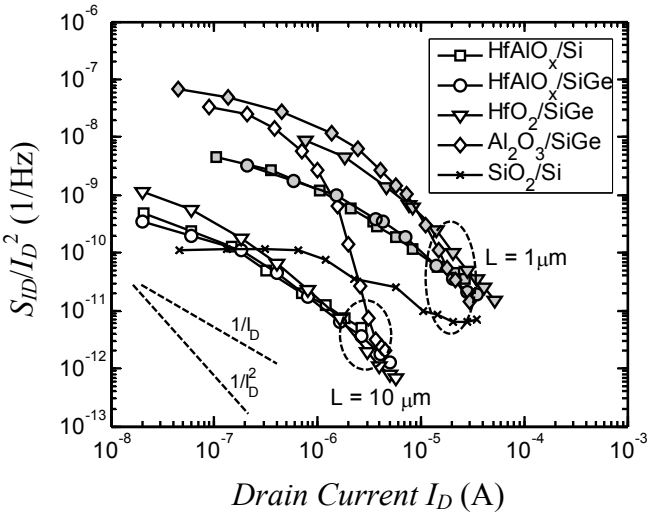

Fig. 6.20. Drain current noise at f = 10 Hz plotted for different high-k pMOSFETs with TiN gate along with a poly-Si/SiO_2/Si reference (from paper IV). V_{DS} = -50 mV, W = 10 μm.

Fig. 6.20 displays S_{I_D} / I_D^2 at 10 Hz versus I_D for various 10-μm and 1-μm TiN/high-k pMOSFETs along with a SiO_2/Si reference. The 1/*f* noise for the high-k pMOSFETs is 1-3 orders of magnitude higher than that for the SiO_2/Si reference. On the positive side, the difference decreases with increasing bias down to around a factor of two or three at I_D > 30 μA. At lower bias, $HfAlO_x$ gives the lowest 1/*f* noise among the high-k materials, whereas the difference between them is small at high bias. The differences in the bias dependencies indicate that different mechanisms govern the 1/*f* noise in different regions of operation and in different high-k materials. The device with 5-nm Al_2O_3 is noisiest, but in another experiment (see next subsection) a device with 2-nm thick Al_2O_3 at the bottom interface was somewhat less noisy than the devices with only 0.5-nm interfacial Al_2O_3. Therefore, it cannot be concluded that Al_2O_3 performs worse than the other materials. The 1/*f* noise for Al_2O_3 device in Fig. 6.20 does not scale with the gate length according the number or mobility fluctuation noise models. This indicates that the noise sources are not homogenously distributed under the gate, which could be attributed to process induced gate edge damage, a problem sometimes observed with high-k gate dielectrics [228]. An interesting observation, which is further elaborated shortly, is that the trap density extracted for HfO_2 is almost at the same level for devices processed in different batches, and with different interface properties and somewhat different deposited thicknesses. In the work by Simoen *et al.*, significant differences were observed among devices with 3-nm or 5-nm thick HfO_2 [188].

Influence of interfacial oxide layer (paper V)

The thickness of the interfacial SiO_2 layer between the high-k and the substrate has been found to be important [68, 72]. A large separation of the traps and defects in the high-k layer from the carriers in the channel reduces the 1/*f* noise as fewer carriers can tunnel the long distance and the Coulomb interaction between the charged trap and the channel carriers is weaker. But even for a thick SiO_2 interfacial layer (~ 4 nm), deposition of a high-k layer on top of it results in higher 1/*f* noise [73, 74]. This suggests that defects propagate from the high-k layer towards the bottom interface, as an exchange of carriers at 4-nm distance is highly unlikely.

We have studied the influence of the cleaning prior to ALD of the high-k layer. These devices used a surface $Si_{0.7}Ge_{0.3}$ channel and a gate stack consisting of p^+ poly-SiGe as gate material and $Al_2O_3/HfO_2/Al_2O_3$ as gate dielectrics. Prior to ALD, the $Si_{0.7}Ge_{0.3}$ surface was treated either with an HF-clean (i.e. 5-min in 0.5% dilute HF followed by N_2 blow-dry) or with an HF-clean followed by water-rinse (i.e. 5-min in 0.5% dilute HF followed by 30-s in de-ionized H_2O and then N_2 blow-dry). Fig. 6.21 shows three high-resolution transmission electron microscopy (HRTEM) images of the poly-SiGe/high-κ/SiGe structure of the pMOSFETs with $Al_2O_3/HfO_2/Al_2O_3$: (a) 0.5/3/0.5 nm, HF-clean followed by water rinse; (b) 0.5/3/0.5 nm, HF clean; and (c) 0.5/3/2 nm, HF-clean. The devices in Fig. 6.21(a)-(c) are labelled A1, B and C, respectively. Device A1 and A2 are from different batches but were otherwise processed almost identically (see refs. [229] and [230] for details) . Device A1 with the water-rinsed surface shows an amorphous interfacial layer, likely composed of Al_2O_3 and SiO_x with an average thickness of ~0.7 nm. In contrast, the bottom Al_2O_3 layer is not clearly observable for device B, which was not subjected to water rinsing after HF-cleaning.

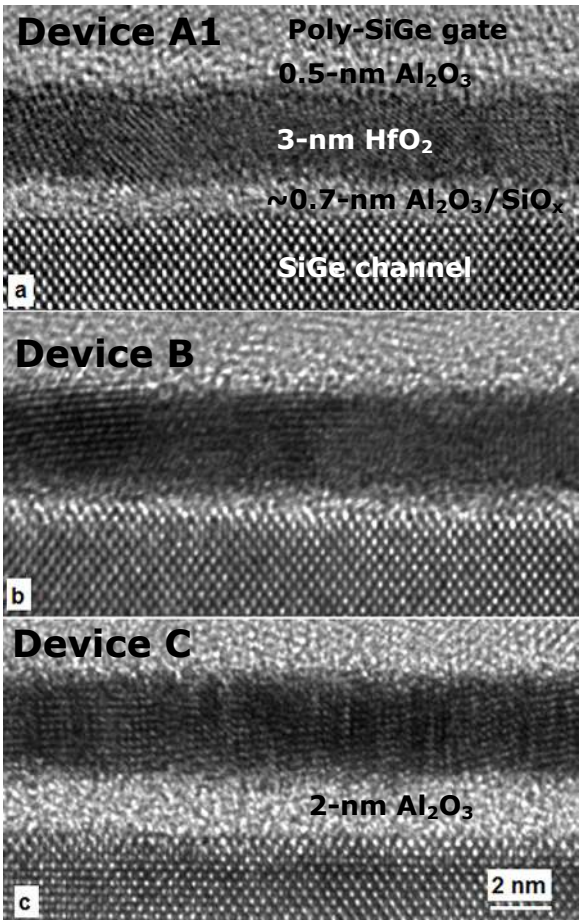

Fig. 6.21. High-resolution TEM images of the poly-SiGe/high-k gate stack and the underlying $Si_{0.7}Ge_{0.3}$ channel. The thickness of the $Al_2O_3/HfO_2/Al_2O_3$ structure and the surface treatment prior to deposition are as follows: (a) 0.5/3/0.5 nm, HF-clean followed by water rinse; (b) 0.5/3/0.5 nm, HF-clean; and (c) 0.5/3/2 nm, HF-clean.

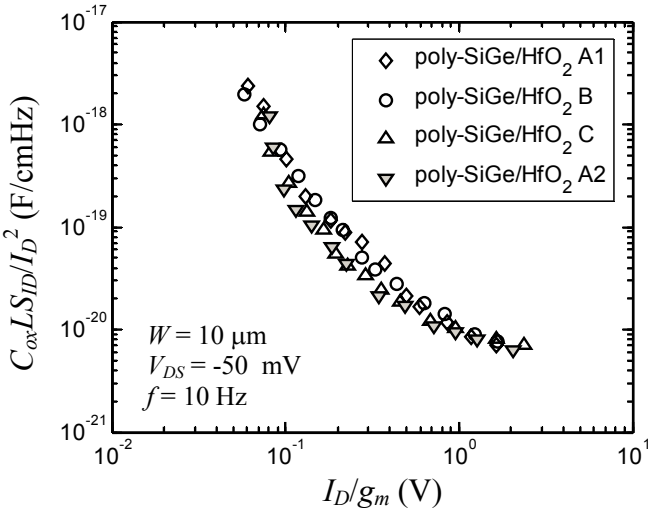

Fig. 6.22. Measured drain current noise of poly-SiGe gated pMOSFETs with high-k gate dielectrics in form of $Al_2O_3/HfO_2/Al_2O_3$ stacks and a surface $Si_{0.7}Ge_{0.3}$ channel.

The EOT values of the three dielectric structures A1, B and C are 1.5, 1.5 and 1.7 nm, respectively, as obtained from *C-V* measurements and after correcting for quantum mechanical and gate depletion effects. Device A2 has an EOT value of 1.9 nm, which indicates that the interfacial layer is thicker than in device A1. Comparing the 1/*f* noise characteristics in Fig. 6.22, no significant difference is found. The interval of interface layer thicknesses ranges from a few Å up to 1 nm in this study, which may be too narrow in order to observe significant differences. In any case, the 1/*f* noise is not sensitive to the cleaning prior to the ALD process step. A more careful analysis, which is given in paper V, reveals that device C shows a factor of two lower 1/*f* noise than that for devices A1 and B at low currents. This may be due to the fact that the traps in the HfO_2 layer are located too far from the channel to contribute to the 1/*f* noise, except at frequencies < 10 Hz, in case the bottom Al_2O_3 layer is 2-nm thick.

Influence of water vapour annealing (paper VI)

An important challenge for the future of high-k gate dielectrics is to reduce the density of traps and charges in their bulk and at the interfaces. The introduction of hydrogen annealing, now a standard process step in Si processing, resulted in lower density of interface states at the SiO_2/Si interface and reduced 1/*f* noise in bipolar and MOS transistors [193, 231]. A forming gas anneal, 10% H_2/90% N_2 at 400 °C, was employed in all devices and is not given particular attention here. Instead, in order to reduce the fixed charge and trap densities in the high-k material (even further), thereby possibly reducing the 1/*f* noise, a novel post-processing step in form of low-temperature water vapour annealing was performed. To the best of our knowledge, this type of anneal has not been studied previously in relation to 1/*f* noise in MOSFETs. The water vapour annealing was found to be effective in reducing the negative charge in the Al_2O_3. Fig. 6.23 displays the shift in threshold voltage with annealing time. The mobility increased as the oxide charge decreased at low effective field, as could be expected. However, as the annealing continued positive charge was added, and the mobility decreased again.

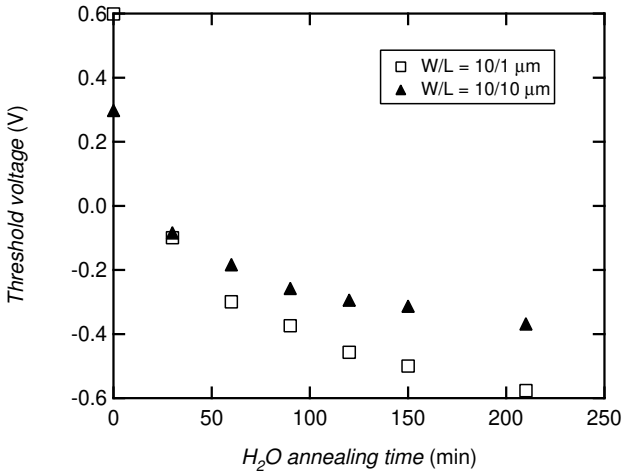

Fig. 6.23. Threshold voltage vs. annealing time for TiN/Al_2O_3/SiGe pMOSFETs (from paper VI). The H_2O annealing was carried out at 300 °C.

The effects on the 1/*f* noise characteristics were shown to be twofold. The H_2O annealing was not found to reduce the 1/*f* noise itself (at least when annealed at 210 min), but the combination of H_2O annealing and a subsequent bake in Argon resulted in improved noise performance, as seen in Fig. 6.24. The slope of the S_{I_D}/I_D^2 curve was found to change with annealing. The curve for the unannealed device follows a $1/I_D^{\beta}$ behavior in strong inversion with β around 2.8, whereas β in the range 1.8-2.2 holds for the H_2O annealed and Ar-treated devices. This difference was attributed to the influence of correlated mobility fluctuations. A negative correlation was found for the unannealed device, which leads to a steeper decrease of S_{I_D}/I_D^2 with drain current. The negative correlation is consistent with the fact that the gate dielectrics contain a negative charge. The negative charge is reduced upon trapping a hole, which

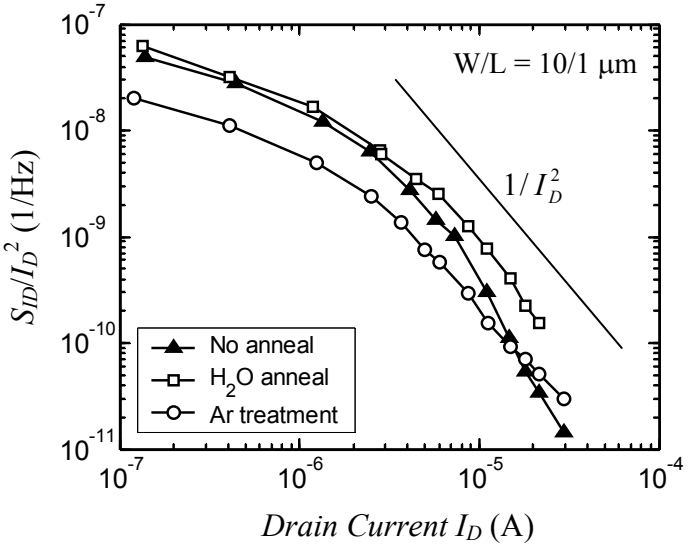

Fig. 6.24. Drain current noise at 10 Hz vs. drain current for the un-annealed, the 210 min H_2O annealed and the Ar-treated TiN/Al_2O_3/SiGe pMOSFETs (from paper VI). V_{DS} = -50 mV.

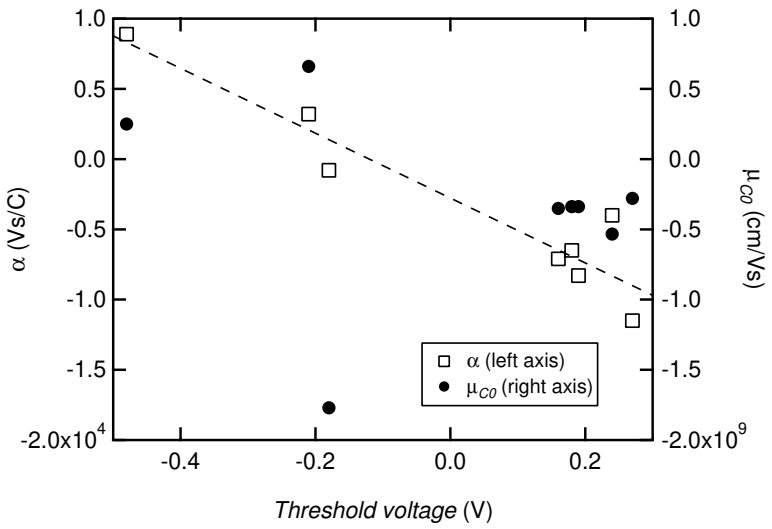

Fig. 6.25. Values of the scattering parameters α (left y-axis, denoted with open boxes) and μ_{C0} (right y-axis, denoted with filled circles) extracted from low-frequency noise measurements on TiN/Al_2O_3/SiGe pMOSFETs plotted vs. threshold voltage (from paper VI).

reduce the Coulomb scattering thus resulting in a negative correlation between the fluctuating inversion charge density and the fluctuating mobility. The 210 min annealed device, on the other hand, contains a positive charge. Then the mobility reduces upon trapping a hole, and the inversion charge and mobility fluctuations correlate positively. The parameter α was studied versus the threshold voltage of the devices ($\Delta V_T = -\Delta Q_{ox}/C_{ox}$) which is illustrated in Fig. 6.25. The maximum magnitude of α was found to be around 1×10^4 Vs/C. The magnitude and sign in front of α depend on the type of traps (acceptor or donor), see Table II in chapter 4.4.2, as well as the nature of the charge in the gate dielectrics. A model for α_C ($\approx\alpha$) in case two types of traps are present was developed and proposed in paper VI.

Channel type and material (papers IV, VIII)

A compressively strained SiGe channel is desired for its superior hole mobility compared to Si. Since no oxidation step is performed in the MOSFETs with high-k gate dielectrics, the Si-cap might no longer be necessary for maintaining a low interface state density. A surface channel is advantageous since the parasitic current limiting the drive current enhancement in a buried SiGe channel transistor is eliminated. However, the interface state density is almost one order of magnitude higher in the fabricated surface SiGe transistors, likely due to the formation of an interfacial oxide layer; see tables in paper IV and paper VII. Still, the 1/*f* noise performance is not deteriorated in the SiGe channel transistors. Comparing the two $HfAlO_x$ transistors in Fig. 6.20, no significant difference in noise level is found. In fact, by studying the drain current noise versus gate voltage overdrive, a noise reduction by a factor 2-4 is observed for the SiGe transistor. The Hooge parameter, extracted at V_{GT} = 1 V, was studied versus low-field mobility in Fig. 6.26 for the devices investigated in this work. As seen, lower values are obtained for the SiGe devices when compared with Si devices with the same gate stack. The dispersion in

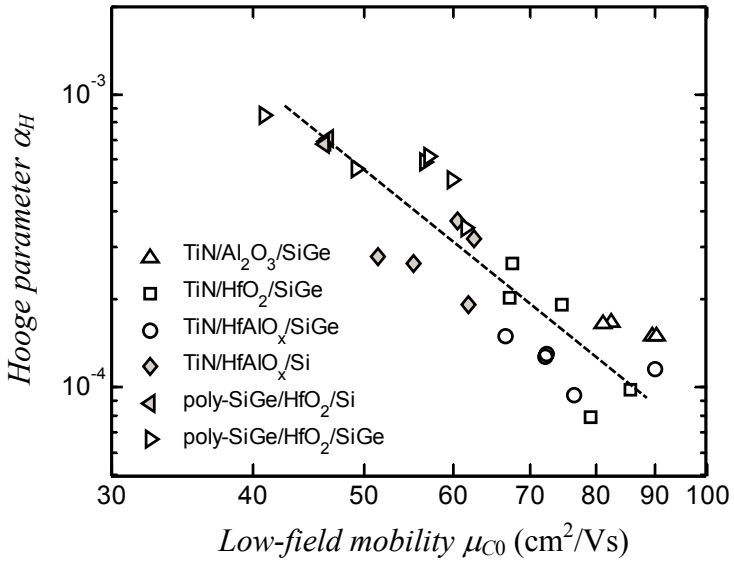

Fig. 6.26. Hooge parameter values extracted at $V_{GS} - V_T$ = -1 V are studied vs. low-field mobility for various pMOSFETs with high-k gate dielectrics (from paper IV).

α_H and μ_0 values is not dramatic, even though the some of the extracted values are from transistors with different gate lengths. The devices with poly-SiGe gate show lower mobility as well as higher noise compared to the devices with TiN gate. This will be addressed further in the next section. An interesting observation in Fig. 6.26 is that low noise is correlated to a high mobility and vice versa. This indicates that the 1/*f* noise mechanism is related to some scattering mechanism. A more detailed analysis carried out in paper IV demonstrates that the phonon scattering can explain the mobility differences among the devices with different gate stack and channel material, which suggests that mobility fluctuation noise prevail. The Coulomb scattering due to the oxide charge, which is related to the number fluctuation noise, cannot alone explain the mobility difference. The SiGe devices contain a higher density of oxide charge (see tables in paper IV and paper VII), but their hole mobility is also higher.

Buried SiGe channel pMOSFETs have been successful in lowering the 1/*f* noise in the past. The high 1/*f* noise level in the high-k transistors is a problem, which could disqualify them to be used in future analog circuits according to Fig. 6.1. A first attempt to fabricate buried SiGe channel transistors with HfO_2 gate dielectrics was made within the European SiNano-network. Figure 6.27 show $L \times S_{VG}$ vs. I_{DS} for pMOSFETs with HfO_2 gate dielectrics. The HfO_2 gate dielectrics in the SiNano devices were deposited by the MOCVD technique, while ALD was used for the $Al_2O_3/HfO_2/Al_2O_3$ structure (KTH). The devices have a poly-Si (SiNano) or poly-SiGe gate (KTH). As observed, the surface SiGe-channel yields some improvement in the noise level compared to Si also in the poly-SiGe gate devices. However, from our first attempt utilizing a buried SiGe channel in pMOSFETs with HfO_2 gate dielectrics no significant reduction in noise level compared to Si could be observed. According to Ghibaudo and Chroboczek [213], 1/*f* noise originating from trapping/release phenomena in the gate dielectrics is not necessarily reduced although most of the current flows in the buried SiGe channel. If the trap densities in the gate dielectrics

are similar one could also expect similar noise levels. Note that most of the SiNano devices showed $1/f^{\gamma}$-type noise with γ around 0.7 below ~1 kHz, and that high gate leakages were observed. Thus, noise generated in the gate current needs to be considered, especially at high gate bias. There were no positive effects on the mobility by using the buried SiGe channel in this study, which indicates that the quality of the compressively strained SiGe layers was imperfect. Therefore, more research is needed in order to draw any certain conclusions regarding the potential for a buried SiGe channel to reduce the $1/f$ noise in high-k devices.

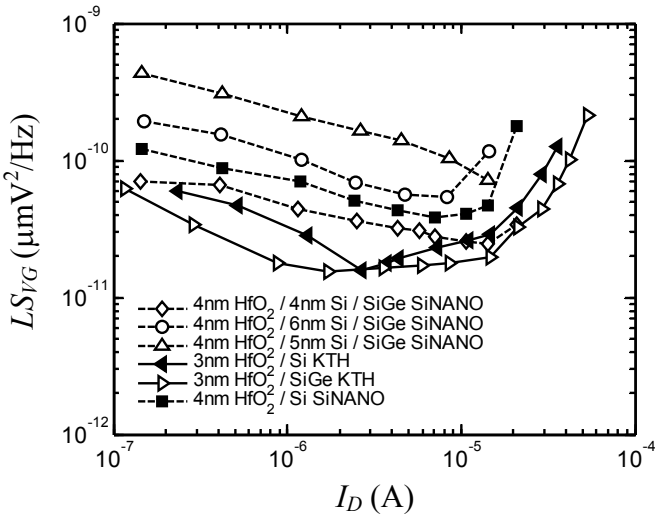

Fig. 6.27. Gate voltage noise at 10 Hz for Si and buried SiGe channel pMOSFETs with 4-nm HfO_2 (MOCVD) gate dielectrics and poly-Si gate compared with pMOSFETs fabricated at KTH with $Al_2O_3/HfO_2/Al_2O_3$ gate dielectrics (ALD, 0.5/3/0.5 nm) and poly-SiGe gate (from paper VIII). W = 10 μm, V_{DS} = -50 mV. L = 0.9 or 1 μm.

1/f noise modeling (papers IV - VIII)

Both the number fluctuation noise model including correlated mobility fluctuations and the Hooge mobility fluctuation noise model were used in our efforts to explain and model the measured low-frequency noise data. The devices with poly-SiGe gate or TiN gate and $HfAlO_x$ gate dielectrics are well modeled with Hooge's model in Eq. (4.20) since $S_{I_D}/I_D^2 \propto 1/I_D$ as demonstrated in Fig. 6.28. However, the devices with TiN gate and HfO_2 or Al_2O_3 gate dielectrics show a stronger I_D dependence and is better explained with the number fluctuation noise model. In Fig. 6.29, the gate voltage noise is plotted versus I_D/g_m for the TiN gated transistors. The solid lines are simulations using the model in Eq. (4.6), after division by g_m^2 to obtain S_{V_G}, with the following α values: 4×10^4 ($HfAlO_x$/Si), 1×10^4 ($HfAlO_x$/SiGe), -8×10^3 (Al_2O_3/SiGe), -1×10^3 or 6×10^3 Vs/C (HfO_2/SiGe). As shown, the combined number and mobility fluctuation noise model can also be used to describe the $HfAlO_x$ devices. However, the HfO_2 and Al_2O_3 devices are more difficult to model over the whole studied bias range due to the U-shaped S_{V_G} curve, which suggest that two different noise mechanisms are involved. The fact that the S_{V_G} curves for all the devices studied in

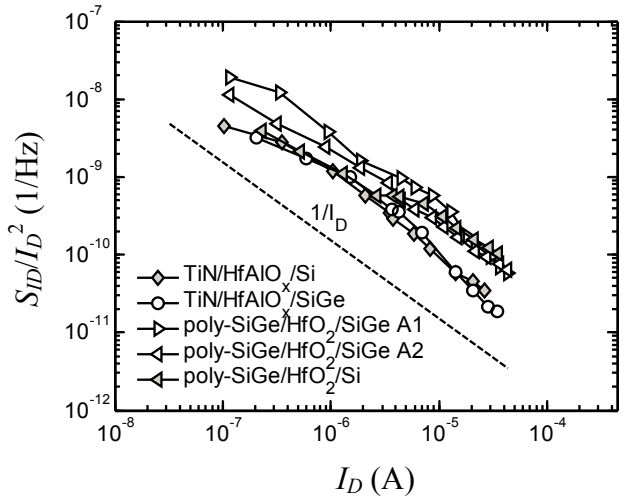

Fig. 6.28. Normalized drain current noise for various pMOSFETs with high-k gate dielectrics showing a $1/I_D$ dependence. f = 10 Hz, V_{DS} = -50 mV, W = 10 μm, L = 0.8-1 μm.

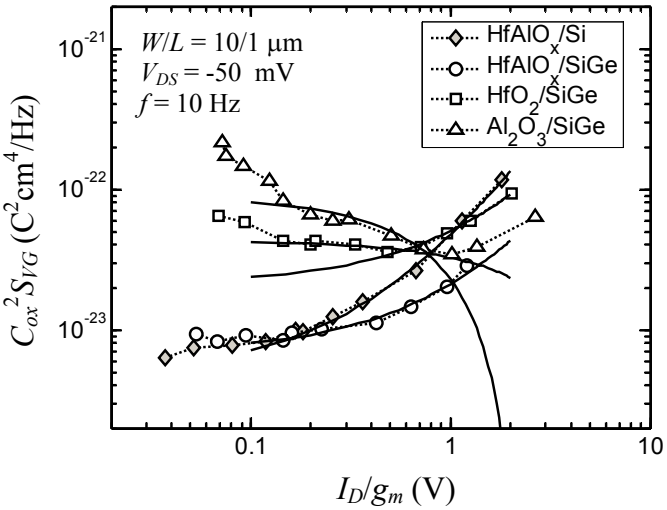

Fig. 6.29. Gate voltage noise multiplied with C_{ox}^2 plotted vs. I_D/g_m for TiN gated pMOSFETs with different high-k gate dielectrics. The solid lines are simulations using Eq. (4.6).

Fig. 6.29 approach each other in strong inversion makes it plausible that this "other" noise source is the origin of the increased S_{V_G} in the $HfAlO_x$ devices as well. Note that noise originating from the S/D resistance is most likely not the cause of this effect as was explained in paper IV and VIII. In this work we do not find it likely that the correlated mobility and number fluctuations is the dominant source of 1/*f* noise in strong inversion due to the aforementioned reason and due the problems to explain why the sign and magnitude of α vary substantially between the different high-k materials and channel types. From the 1/*f* noise analysis of the whole ensemble of high-k MOSFETs in this work, we conclude that Hooge mobility fluctuations dominate at high gate voltage overdrives in the vast majority of the devices. Number fluctuation noise due to traps in the gate dielectrics was found to be important below or close to threshold, especially for the devices using HfO_2 and 5-nm Al_2O_3. The

negative correlation between the number and mobility fluctuations causes the trap induced noise to decrease rapidly above threshold. Note that a positive correlation is almost always found in conventional MOSFETs. One reason why high-k devices show higher 1/*f* noise than devices with SiO_2, besides a higher density of traps, could be due to remote phonon scattering. We are the first to propose and investigate remote phonons as a possible source of 1/*f* noise in high-k transistors. If correct, this noise source could be a fundamental limitation of the noise performance in devices with high-k gate dielectrics.

Summary and future outlook

MOSFETs with high-k gate dielectric show increased 1/*f* noise compared to transistors using SiO_2 due to large defect densities originating from the high-k materials and possibly also due to mobility fluctuations originating from the remote phonon scattering. In terms of high-k materials, $HfAlO_x$ often contains lower trap densities N_t than HfO_2 and Al_2O_3 do (see Fig. 6.18). To reduce the 1/*f* noise, a TiN metal gate in combination with high-k gate dielectrics was shown to be advantageous compared to using poly-SiGe. The 1/*f* noise was only two to three times higher in the high-k devices with TiN gate than that in the reference SiO_2/Si device at gate voltage overdrives above 1 V, which is promising is view of previous work. Lower trap densities have been reported for materials such as $HfSi_xO_y$ [66, 185, 232] and Ta incorporated HfO_2 [233], possibly they exhibit lower 1/*f* noise as well. Srinivasan *et al*. report lower 1/*f* noise for HfSiON than that for HfO_2, although the dependence is not strong [195]. Still, the trap densities in HfSiON are an order of magnitude higher than in SiON [190, 195]. As with technology shifts, some time must be expended to learn the new materials and processing methods. In the future, we can expect that the 1/*f* noise is lower as the technology is more mature. Concepts to reduce the 1/*f* noise, such as using a buried channel, need to be explored more in high-k devices. In this context, it is encouraging with the results presented in this work where reduced 1/*f* noise was found in the devices at forward substrate bias (see chapter 4.3). In conclusion, based on our results the noise properties of high-k gate dielectrics seem promising for future generations of MOSFETs, yet some problems remains to be solved.

6.6 MOSFETs with metal gate

Replacing the poly-Si with a metal or silicide such as Mo, TiN, NiSi or TaN is highly desired as explained in chapter 2.4 and is currently a vivid research topic. As the gate dielectrics becomes thinner and thinner, the impact of the gate material on the device properties is expected to increase. The 1/*f* noise is very sensitive to traps, which might be introduced at the oxide/gate interface. So far, only a few reports are available in the literature about how a metal gate influences the 1/*f* noise performance. Lee *et al*. investigated pMOSFETs on SOI with a Mo gate [172]. The Mo film was deposited using dc magnetron sputtering and a 2.5-nm thick gate oxide was used. The results pointed to a relatively high noise level ($N_t \sim 1\times10^{18}$ $cm^{-3}eV^{-1}$), roughly one order of magnitude higher that that of conventional poly-Si gated MOSFETs. But as was shown in the previous section, the TiN gate was found to be favourable in comparison with the poly-SiGe gate in terms of both mobility and 1/*f* noise performance in the transistors with high-k gate dielectrics. Recent results by Srinivasan *et al*. confirm these exciting results for PVD TaN and NiSi [168]. The lowering of the 1/*f* noise is mainly observed in the strong inversion regime. In Fig. 6.30, the normalized drain current noise is plotted versus I_D/g_m for poly-SiGe and TiN gated transistors with

$Al_2O_3/HfO_2/Al_2O_3$ stacks as gate dielectrics. As observed, the normalized drain current noise is at the same level for all the HfO_2 gate dielectric pMOSFETs at low bias, whereas the TiN gated device shows significantly reduced noise in strong inversion. The metal gate is known to alleviate the effect of remote phonon scattering on the hole mobility, the same mechanism is proposed to explain the noise reduction.

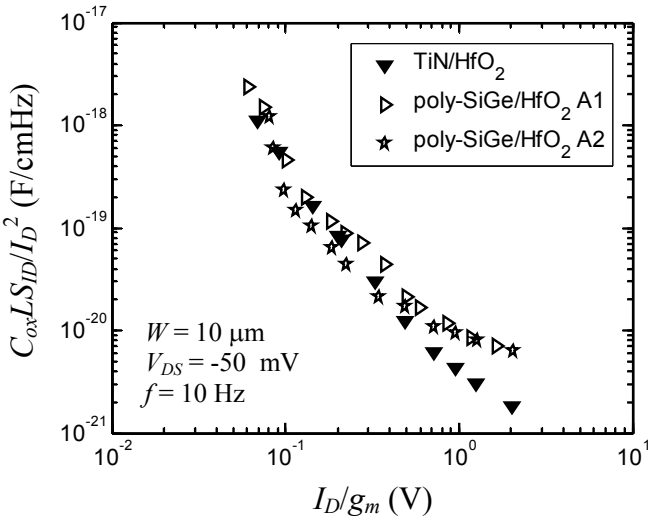

Fig. 6.30. The normalized drain current noise is compared for $Al_2O_3/HfO_2/Al_2O_3$ gate dielectric pMOSFETs with TiN and poly-SiGe gate. L = 0.8-1 μm.

The mobility fluctuation noise is assumed to be mainly generated in the phonon scattering. Therefore, a high-k device with a metal gate can be less noisy than the same device with a poly-Si gate. On the other hand, the traps and charges at the gate-dielectric interface might also be better screened by a metal gate, as indicated by Srinivasan *et al*. Further experiments are needed to pinpoint the exact origin of the lower 1/*f* noise in metal gate MOSFETs; the results on using metal gates in combination with high-k gate dielectrics are very promising so far.

6.7 Multiple gate MOSFETs

Multiple gate MOSFETs is a very attractive solution for ultra-scaled CMOS technologies at the 45 nm node and beyond. Several multiple-gate architectures have been proposed, such as back gated ultra-thin body SOI [87, 94, 234], gate-all-around MOSFETs [235], FinFETs [236], and Omega FETs [91]. FinFETs have received a lot of attention because of their excellent performance and the relatively simple fabrication. From a noise point of view, there are many unexplored issues. The FinFET conducts current in a vertical mode, which may lead to degraded 1/*f* noise performance according to recent reported results [156, 237]. The etching of the sidewalls of the fin could lead to higher micro-roughness and increased trap densities at the gate oxide/channel interface, which might be one explanation for the higher 1/*f* noise. Also, the gate area of FinFETs is very small, thus the devices might suffer form edge effects. On the other hand, by using a thin Si body (< ~10nm), the interior of the body is inverted (so-called volume inversion) which potentially can result in (much) lower 1/*f* noise. Significantly lower noise was reported for gate-all-around MOSFETs under some bias conditions [235], although the film thickness is too large (100 nm) to

produce volume inversion. In the few reports about the low-frequency noise characteristics of FinFETs so far [193, 198, 238], no evidence of lower noise due to volume inversion is observed. As seen in Fig. 6.1, low N_t values are found for some FinFETs which were annealed in hydrogen, but the values are not lower than that in bulk CMOS. Therefore, further development of the multiple-gate MOS-technology is necessary, and further noise investigations of multiple gate MOSFETs are urgently asked for.

7. Summary and future perspective

This thesis deals with low-frequency noise characterization and modeling of advanced Si- and SiGe-based CMOS transistors. Several novel device concepts including SiGe channel pMOSFETs, strained Si nMOSFETs, SOI technology, high-k gate dielectrics, metal gate, that all have great potential for future high-speed RF circuits, have been fabricated, characterized, and evaluated. The devices were characterized by static electrical measurements as well as low-frequency noise measurements, from which physical quantities and parameters have been extracted. Semiconductor device simulation tools such as ISE TCAD or Schred [223], where the device behaviour is obtained from solutions of partial differential equations that govern the device physics, have also been used as supplementary sources of information. The basis of our low-frequency noise modeling efforts is the existing number and mobility fluctuation noise theories, which are thoroughly described and analyzed in this work. However, the present models have failed in several instances; either the modeling parameters have been physically incorrect or the models have not been able to satisfactorily predict the noise behaviour. In order to circumvent these shortcomings, several attempts have been made in this work to develop the understanding of 1/*f* noise mechanisms and improve the modeling of 1/*f* noise in MOSFETs.

The major findings derived in this work are summarized below. A comprehensive evaluation of different CMOS technologies from a low-frequency noise point of view has been performed. This work is highly original in the respect that such a broad and detailed investigation and evaluation of a variety of state-of-the-art CMOS devices is unique in the literature.

1. Devices where the conduction path is buried under the gate oxide/channel interface have been shown to exhibit significantly lower 1/*f* noise than in devices with a surface channel. Examples of the former type of devices studied here are buried SiGe channel pMOSFETs as well as accumulation mode MOSFETs on SOI.

2. The 1/*f* noise performance is sensitive to the choice of gate dielectric material. Devices using gate dielectrics with a high dielectric constant (high-k) can exhibit up to three orders of magnitude higher 1/*f* noise than those with thermally grown SiO_2. In our work, ALD HfO_2, $HfAlO_x$ and Al_2O_3 gate dielectrics have been studied together with a TiN metal gate or poly-SiGe gate and a Si or SiGe surface channel. A strong correlation between carrier mobility and 1/*f* noise level was found; a high mobility resulted in low 1/*f* noise and vice versa. These results are best explained in terms of a phonon scattering origin of the 1/*f* noise. The combination of $HfAlO_x$, TiN gate and a compressively strained SiGe channel was found to be advantageous in terms of both mobility and 1/*f* noise performance. At high gate voltage overdrives the 1/*f* noise level was only a factor of three higher than that in the Si reference devices with SiO_2, which is a promising result in view of other work. The surface cleaning prior to deposition (ALD) of the high-k stack was not found to have any major impact on the 1/*f* noise performance. A novel post-processing step based on water vapour annealing reduced the negative oxide charge in the gate dielectrics and influenced the 1/*f* noise through the correlated mobility fluctuations. Our results on high-k gate dielectrics point out three important conclusions: (i) the 1/*f* noise in the high-k transistors must be decreased in order to meet the ITRS requirements; (ii) the 1/*f* noise level is closely

related to mobility degradation mechanisms; (iii) a TiN (metal) gate or a forward substrate bias can reduce the 1/*f* noise.

3. Tensile strained Si nMOSFETs showed enhanced mobility in comparison with unstrained references but the 1/*f* noise performance was not degraded although the device fabrication was more complex. These devices may therefore be suitable for high-speed low-noise applications.

4. We conclude that the 1/*f* noise is sensitive to traps and defects in the conduction path as well as the scattering processes that govern the carrier mobility. The traps are contained in the gate dielectrics and are responsible for fluctuations in the number of carriers that are available for current transport in the channel region of the device. High-k gate dielectrics contain a higher density of traps, partly due to immature technology, which translates to high 1/*f* noise. The other source of the 1/*f* noise is fluctuations in the carrier mobility, which has been shown to be the dominant mechanism in most of our pMOSFETs, both with high-k and SiO_2 gate dielectrics. Particularly, the scattering of electrons with phonons is on good grounds suspected to be the origin of the mobility 1/*f* noise. The carrier mobility in high-k devices is reduced due to remote phonon scattering originating from the soft phonon modes in the high-k material, which we propose as a reason for the higher 1/*f* noise in devices using these materials. Moreover, the question is raised if not the mere presence of a gate oxide interface close to the conduction path may lead to higher 1/*f* noise. Interfaces, surface roughness and crystalline defects have a detrimental impact on the charge transport as well as on the transport of phonons. The origin of the 1/*f* fluctuations in the mobility is not fully established, but is likely related the carrier and/or phonon transport properties.

5. Extensive experimental evidence in this work shows that the 1/*f* noise depends on the voltage on the bulk terminal. We discovered that this effect can be explained by the variation in the vertical electric field or the position of the inversion carriers with the substrate bias. The vertical electric field is lowered and the position of the channel is located further away from the interface when the substrate is forward biased. The 1/*f* noise in strong inversion is found to decrease for a forward bias on the substrate and increase for the opposite case, which correlates well with our conclusions on buried channel contra surface channel transport. The drain current noise spectral density S_{I_D} decreases as the number of channel carriers *N*, modulated by the gate voltage, increases. In the majority of our examined devices, S_{I_D} was found to decrease approximately as 1/*N* in strong inversion. In the subthreshold region, on the other hand, a weaker behaviour was often observed. We make the conclusion that Hooge mobility noise dominates in strong inversion but number fluctuation noise due to traps in the gate dielectrics may dominate around threshold. The relative importance of these two noise sources varies with bias conditions, technology and type of device. The n-channel MOSFETs and p-channel MOSFETs with high-k (especially HfO_2) are more strongly governed by number fluctuations noise than the pMOSFETs with SiO_2 or $HfAlO_x$ for example.

Finally, we believe that the results from the evaluation of different CMOS technologies and the new insights about 1/*f* noise mechanisms we have presented are of high importance for low-noise device design. The improved models can be adopted

in the device simulation tools used in circuit design. The accumulated knowledge is also important for the evolution of low-frequency noise measurements as a characterization tool to study traps, defects, surface properties and phonons as well as their interactions with carriers. The RTS noise measurement technique was examined and shown to be valuable in order to study traps and their kinetics.

The thesis has given some directions on future research and device concepts. Multiple gate devices fabricated on ultra-thin SOI substrates provides an excellent electrostatic control of the channel allowing extended scalability. From noise point of view, such devices have two gate oxide interfaces in the proximity of the current transport which may degrade the noise performance. On the other hand, the carriers are localized in the middle of the ultra-thin Si-body (for a thickness below ~10 nm) in such devices which have the potential of significantly reduced 1/*f* noise. Presently, strained channel devices are hot research topics. So far, no significant effects on the noise have been observed due to the incorporation of strain. Yet, 1/*f* noise reductions could be possible by utilizing smart engineering that reduces the impact of critical scattering processes. The strain seldom improves the device performance more than roughly a factor of two, as it seems, although a tenfold hole mobility enhancement recently was obtained in strained Ge-rich channels [239]. For further enhancement of device speed, continued downscaling of the device dimensions is necessary including the use of high-k gate dielectrics. Considering the results presented here, improved quality of the high-k materials is desired for good 1/*f* noise performance. Research on buried channel concepts together with high-k is also urgently needed. The 1/*f* noise increases as the number of channel carriers becomes fewer at smaller dimensions. However, as the channel length is reduced to the limit where ballistic transport becomes important, the 1/*f* noise may show a different behaviour. If phonons are considered as important for the 1/*f* noise generation, a reduction of the 1/*f* noise could be expected. This is an interesting and important subject for future noise research.

At last, a widely accepted physically based theory for mobility fluctuation 1/*f* noise is still not available. The ideas, results and improved models presented in this work on mobility fluctuations noise, both independent fluctuations (Hooge type) or correlated to the number fluctuations, can provide some important pieces in the development of such a theory. The prospects for future 1/*f* noise research look very promising.

Appendix I – properties of $Si_{1-x}Ge_x$

Property	Si	$Si_{1-x}Ge_x$
Dielectric constant ε_r	11.8	$11.4(1-x) + 15.6x$
Energy gap (eV) at 300K	1.12	$1.12 - 0.896x + 0.396x^2 \quad (x < 0.3)$
Effective Density of states N_C (cm^{-3})	3.2×10^{19}	$\frac{N_{V,Si}}{1+(18x)^{0.9}}$ $\quad \Delta E = 0.6x$ eV
N_V (cm^{-3})	1.8×10^{19}	$\frac{N_{C,Si}}{3}\left(\frac{3\exp(-\Delta E/kT)}{2+\exp(-\Delta E/kT)}+2\right)$
n_i (cm^{-3})	1.45×10^{10}	$\sqrt{N_V N_C} \times \exp(-E_g/2kT)$

The properties from $Si_{1-x}Ge_x$ were taken from [240] and [39].

Appendix II – high-k materials

Material	Dielectric constant *k*	Band gap	ΔE_C to Si	ΔE_V to Si
SiO_2	3.9	8.9	3.2	4.6
Si_3N_4	7	5.1	2	2
Al_2O_3	9	8.7	2.8	4.8
Y_2O_3	15	5.6	2.3	2.2
La_2O_3	30	4.3	2.3	0.9
Ta_2O_5	26	4.5	1-1.5	1.9-2.4
TiO_2	80	3.5	1.2	1.2
HfO_2	25	5.7	1.5	3.1
ZrO_2	25	7.8	1.4	5.3

Values from Wilk, Wallace and Anthony [58].

Note that the ΔE_V values were calculated from the Band gap and ΔE_C values in the table according to $\Delta E_V = E_{g,high\text{-}k} - \Delta E_C - E_{g,Si}$.

The properties of mixed materials such as $HfSiO_xN_y$ and $HfAlO_x$ depend on the content of the different atoms in the compound. The dielectric constants of $HfSiO_xN_y$ and $HfAlO_x$ are reported to range between 9-14 and 14-20, respectively.

Appendix III – table of 1/*f* noise results

Device description, (●) Fabricated at KTH	Paper	N_t ($cm^{-3}eV^{-1}$)	α_H
Si pMOS, t_{ox} = 3 nm, pure SiO_2, (15-nm Si epi).	I	9.1×10^{16}	2.9×10^{-5}
SiGe pMOS, t_{ox} = 3 nm, pure SiO_2, buried 10-nm $Si_{0.7}Ge_{0.3}$ channel, 6-nm Si-cap.	I	4.9×10^{16}	1.6×10^{-5}
Si pMOS, t_{ox} = 2.2 nm, pure SiO_2, 50-nm gate length process, (20-nm Si epi).	II	4.3×10^{16}	1.2×10^{-5}
SiGe pMOS, t_{ox} = 2.2 nm, pure SiO_2, buried 10-nm $Si_{0.7}Ge_{0.3}$ channel, 6-nm Si-cap, 50-nm gate length process.	II	3.9×10^{16}	9.4×10^{-6}
Si nMOS, t_{ox} = 2.8 nm, pure SiO_2.	[241]	3.7×10^{16}	2.2×10^{-5}
Strained Si nMOS, t_{ox} = 2.8 nm, pure SiO_2, 200-nm $Si_{0.8}Ge_{0.2}$ virtual substrate, 15-nm strained Si-channel.	[241]	4.8×10^{16}	1.9×10^{-5}
Si pMOS, EOT = 1.7 nm, $Al_2O_3/HfO_2/Al_2O_3$ (0.5/3/0.5 nm), poly-SiGe gate	[230]	5.9×10^{18}	6.9×10^{-4}
SiGe pMOS, EOT = 1.9 nm, $Al_2O_3/HfO_2/Al_2O_3$ (0.5/3/0.5 nm), poly-SiGe gate, surface $Si_{0.7}Ge_{0.3}$ channel.	[230]	4.4×10^{18}	4.3×10^{-4}
SiGe pMOS, EOT = 1.6 nm, $Al_2O_3/HfO_2/Al_2O_3$ (0.5/3/0.5 nm), poly-SiGe gate, surface $Si_{0.7}Ge_{0.3}$ channel.	V	9.0×10^{18}	6.5×10^{-4}
Si pMOS, EOT = 3.0 nm, $Al_2O_3/HfAlO_x/Al_2O_3$ (0.5/4/0.5 nm), TiN gate.	IV	1.9×10^{18}	2.8×10^{-4}
SiGe pMOS, EOT = 2.9 nm, $Al_2O_3/HfAlO_x/Al_2O_3$ (0.5/4/0.5 nm), TiN gate, surface $Si_{0.7}Ge_{0.3}$ channel.	IV	1.7×10^{18}	1.2×10^{-4}
SiGe pMOS, EOT = 2.3 nm, $Al_2O_3/HfO_2/Al_2O_3$ (0.5/4/0.5 nm), TiN gate, surface $Si_{0.7}Ge_{0.3}$ channel.	IV	6.5×10^{18}	-
SiGe pMOS, EOT = 3.7 nm, Al_2O_3 (5 nm), TiN gate, surface $Si_{0.8}Ge_{0.2}$ channel.	IV	2.4×10^{19}	-
Si FD SOI pMOS, t_{ox} = 3 nm, pure SiO_2, UNIBOND, 20-nm p-type Si body.	III	4.6×10^{16}	9.4×10^{-6}
Si PD SOI pMOS, t_{ox} = 3 nm, pure SiO_2, UNIBOND, 150-nm p-type Si body.	III	4.3×10^{16}	9.9×10^{-6}
SiGe FD SOI pMOS, t_{ox} = 3 nm, pure SiO_2, UNIBOND, 22-nm p-type Si body, $Si_{0.72}Ge_{0.28}$ channel, <1-nm Si-cap.	III	4.5×10^{16}	9.0×10^{-6}

N_t was extracted in the weak inversion region, α_H in the strong inversion region. The values were typically extracted on L = 0.6-1 μm devices. The shaded values were not plotted in Figs. 6.1 and 6.2.

References to the data points plotted in Fig. 6.1.

Si pMOS:	[171] (□ ▷), [187] (◁ ▷), [133] (▽ ■), [150] (▽), [158] (☆), [159](◇), [199] (△ ◁)
Si nMOS:	[133] (□), [187] (▷ ◁), [194] (◇), [197] (△), [150] (▽), [158] (☆)
Buried SiGe pMOS:	[10] (□)
Strained Si nMOS:	[197] (△)
SOI CMOS:	[191] (◁ □), [192] (◇), [189] (▽)
Metal gate/high-k CMOS:	[172] (□ ■), [195] (◇), [80] (▽)
Poly-Si gate/high-k CMOS:	[188] (■ □), [74] (△ ▷ ▽ ◁), [190] (◇), [73] (☆)
Si FinFET:	[193] (▷ ◁), [198] (□ ◇)

References to the data points plotted in Fig. 6.2.

Si pMOS:	[171] (□ ▷), [135] (▷ ◁), [10] (◇), [43] (☆), [9] (▽), [108] (✡), [159] (◇), [199] (◁ △)
Si nMOS:	[197] (△), [196] (△ ▽)
Buried SiGe pMOS:	[10] (◇), [43] (☆), [9] (▽)
Strained Si nMOS:	[197] (△)
SOI CMOS:	
Metal gate/high-k CMOS:	[195] (□ ◇)
Poly-Si gate/high-k CMOS:	[74] (◁ ▷ △ ▽)

References

[1] International Technology Roadmap for Semiconductors (ITRS), 2005 update, http://public.itrs.net/

[2] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 31, pp. 331-343, 1996.

[3] M. J. Deen and O. Marinov, "Noise in advanced electronic devices and circuits," in *Proc. Int. Conf. Noise and Fluctuations (ICNF)*, 2005, pp. 3-12.

[4] L. K. J. Vandamme, "Noise as a diagnostic tool for quality and reliability of electronic devices," *IEEE Trans. Electron Devices*, vol. 41, pp. 2176-2187, 1994.

[5] C. Claeys and E. Simoen, "Impact of advanced processing modules on the low-frequency noise performance of deep-submicron CMOS technologies," *Microelectron. Reliab.*, vol. 40, pp. 1815-1821, 2000.

[6] A. D. van Rheenen, G. Bosman, and R. J. J. Zijlstra, "Low frequency noise measurements as a tool to analyze deep-level impurities in semiconductor devices," *Solid-State Electron.*, vol. 30, pp. 259-265, 1987.

[7] R. Jayaraman and C. G. Sodini, "A 1/*f* noise technique to extract the oxide trap density near the conduction band edge of silicon," *IEEE Trans. Electron Devices*, vol. 36, pp. 1773-1782, 1989.

[8] M. J. Kirton and M. J. Uren, "Noise in solid-state microstructures: a new perspective on individual defects, interface states and low-frequency (1/*f*) noise," *Advances in Physics*, vol. 38, pp. 367-468, 1989.

[9] S. Okhonin, M. A. Py, B. Georgescu, H. Fischer, and L. Risch, "DC and low-frequency Noise Characteristics of SiGe P-Channel FET's Designed for 0.13-µm Technology," *IEEE Trans. Electron Devices*, vol. 46, pp. 1514-1517, 1999.

[10] S. J. Mathew, G. Niu, W. B. Dubbelday, and J. D. Cressler, "Characterization and Profile Optimization of SiGe pFET's on Silicon-on-Sapphire," *IEEE Trans. Electron Devices*, vol. 46, pp. 2323-2332, 1999.

[11] E. Simoen, and C. Claeys, "The low-frequency noise behaviour of silicon-on-insulator technologies," *Solid-State Electron.*, vol. 39, pp. 949-960, 1996.

[12] L. K. J. Vandamme, X. Li, and D. Rigaud, "1/*f* noise in MOS devices, mobility or number fluctuations?," *IEEE Trans. Electron Devices*, vol. 41, pp. 1936-1945, 1994.

[13] E. P. Vandamme and L. K. J. Vandamme, "Critical discussion on unified 1/*f* noise models for MOSFETs," *IEEE Trans. Electron Devices*, vol. 47, pp. 2146-2152, 2000.

[14] M. B. Weissman, "1/*f* noise and other slow, nonexponential kinetics in condensed matter," *Rev. Mod. Phys.*, vol. 60, pp. 537-571, 1988.

[15] J. L. Liou, and F. Schwierz, "RF MOSFET: recent advances, current status and future trends," *Solid-State Electron.*, vol. 47, pp. 1881-1895, 2003.

[16] A. A. Abidi, "RF CMOS comes of age," in *Proc. Symp. VLSI Circuits*, 2003, pp. 113-116.

[17] Y. Taur and T. H. Ning, *Fundamentals of modern VLSI devices*, Cambridge University Press, 1998.

[18] M. Lundstrom, *Fundamentals of carrier transport*, 2nd ed, Cambridge University Press, 2000.

[19] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universality of inversion layer mobility in Si MOSFET's: part I-effects of substrate impurity concentration," *IEEE Trans. Electron Devices*, vol. 41, pp. 2357-2362, 1994.

[20] S. A. Schwarz and S. E. Russek, "Semi-empirical equations for electron velocity in silicon: part II-MOS inversion layer," *IEEE Trans. Electron Devices*, vol. ED-30, pp. 1634-1639, 1983.

[21] V. M. Agostinelli, Jr., H. Shin, and A. F. Tasch, Jr., "A comprehensive model for inversion layer hole mobility for simulation of submicrometer MOSFET's," *IEEE Trans. Electron Devices*, vol. 38, pp. 151-159, 1991.

[22] F. Gámiz, J. B. Roldán J. E. Carceller, and P. Cartujo, "Monte Carlo simulation of remote-Coulomb-scattering-limited mobility in metal-oxide-semiconductor transistors," *Appl. Phys. Lett.*, vol. 82, pp. 3251-3253, 2003.

[23] G. Mazzoni, A. L. Lacaita, L. M. Perron, and A. Pirovano, "On surface roughness-limited mobility in highly doped n-MOSFET's," *IEEE Trans. Electron Devices*, vol. 46, pp. 1423-1428, 1999.

[24] D. K. Schroder, *Semiconductor material and device characterization*, 2nd ed., John Wiley & Sons, Inc., 1998.

[25] S. M. Sze, *Semiconductor devices, physics and technology*, John Wiley & Sons, 1985.

[26] G. Ghibaudo, "New method for the extraction of MOSFET parameters," *Electronics Letters*, vol. 24, pp. 543-545, 1988.

[27] N. Stojadinovic and S. Dimitrijev, "Instabilities in MOS transistors," *Microelectron. Reliab.*, vol. 29, pp. 371-380, 1989.

[28] G. Groeseneken, H. E. Maes, N. Beltrán, and R. F. De Keersmaecker, "A reliable approach to charge-pumping measurements in MOS transistors," *IEEE Trans. Electron Devices*, vol. ED-31, pp. 42-53, 1984.

[29] N. S. Saks and M. G. Ancona, "Determination of interface trap capture cross sections using three-level charge pumping," *IEEE Electron Device Lett.*, vol. 11, pp. 339-341, 1990.

[30] R. R. Siergiej, M. H. White, and N. S. Saks, "Theory and measurement of quantization effects on Si-SiO_2 interface trap modeling," *Solid-State Electron.*, vol. 35, pp. 843-854, 1992.

[31] Compiled from http://www.intel.com/pressroom/kits/quickref.htm

[32] R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous, and A. LeBlanc, "Ion implanted MOSFETs with very short channel lengths," in *IEDM Tech. Dig.*, 1973, pp. 152-155.

[33] L. D. Yau, "A simple theory to predict the threshold voltage of short-channel IGFETs," *Solid-State Electron.*, vol. 17, pp. 1059-1063, 1974.

[34] R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 256-268, 1974.

[35] G. Baccarani, M. R. Wordeman, and R. H. Dennard, "Generalized scaling theory and its application to a 1/4 micrometer MOSFET design," *IEEE Trans. Electron Devices*, vol. ED-31, pp. 452-462, 1984.

[36] R. People, "Physics and applications of Ge_xSi_{1-x}/Si strained-layer heterostructures," *IEEE J. Quantum Electronics*, vol. QE-22, pp. 1696-1710, 1986.

[37] T. Manku, J. M. McGregor, A. Nathan, D. J. Roulston, J.-P. Noel, and D. C. Houghton, "Drift hole mobility in strained and unstrained doped $Si_{1-x}Ge_x$ alloys," *IEEE Trans. Electron Devices*, vol. 40, pp. 1990-1996, 1993.

[38] T. Manku and A. Nathan, "Effective mass for strained p-type $Si_{1-x}Ge_x$," *J. Appl. Phys.*, vol. 69, pp. 8414-8416, 1991.

[39] D. J. Robbins, L. T. Canham, S. J. Barnett, A. D. Pitt, and P. Calcott, "Near-band-gap photoluminescence from pseudomorphic $Si_{1-x}Ge_x$ single layers on silicon," *J. Appl. Phys.*, vol. 71, pp. 1407-1414, 1992.

[40] S. Verdonckt-Vandebroek, E. F. Crabbé, B. S. Meyerson, D. L. Harame, P. J. Restle, J. M .C. Stork, and J. B. Johnson, "SiGe-Channel Heterojunction p-MOSFET's," *IEEE Trans. Electron Devices*, vol. 41, pp. 90-101, 1994.

[41] C.-G. Ahn, H.-S. Kang, Y.-K. Kwon, and B. Kang, "Effects of segregated Ge on electrical properties of SiO_2/SiGe interface," *Jpn. J. Appl. Phys.*, vol. 37, pp. 1316-1319, 1998.

[42] T. Ngai, X. Chen, J. Chen, and S. K. Banerjee, "Improving SiO_2/SiGe interface of SiGe *p*-metal-oxide-semiconductor field-effect transistors using water vapor annealing," *Appl. Phys. Lett.*, vol. 80, pp. 1773-1775, 2002.

[43] M. J. Prest, M. J. Palmer, G. Braithwaite, T. J. Grasby, P. J. Phillips, O. A. Mironov, E. H. C. Parker, and T. E. Whall, "Si/$Si_{0.64}Ge_{0.36}$/Si pMOSFETs with Enhanced Voltage Gain and low 1/*f* noise," in *Proc. ESSDERC*, 2001, pp. 179-182.

[44] N. Collaert, P. Verheyen, K. De Meyer, R. Loo, and M. Caymax, "High performance Si/SiGe pMOSFETs fabricated in a standard CMOS process technology," *Solid-State Electron.*, vol. 47, pp. 1173-1177, 2003.

[45] F. Andrieu, T. Ernst, K. Romanjek, O. Weber, C. Renard, J.-M. Hartmann, A. Toffoli, A.-M. Papon, R. Truche, P. Holliger, L. Brévard, G. Ghibaudo, and S. Deleonibus, "SiGe channel p-MOSFETs scaling-down," in *Proc. ESSDERC*, 2003, pp. 267-270.

[46] K. Romanjek, F. Andrieu, T. Ernst, and G. Ghibaudo, "Characterization of the effective mobility by split *C*(*V*) technique in sub 0.1 μm Si and SiGe PMOSFETs," *Solid-State Electron.*, vol. 49, pp. 721-726, 2005.

[47] A.-C. Lindgren, P.-E. Hellberg, M. von Haartman, D. Wu, C. Menon, S.-L. Zhang, and M. Östling, "Enhanced intrinsic gain (g_m/g_d) of PMOSFETs with a $Si_{0.7}Ge_{0.3}$ channel," in *Proc. ESSDERC*, 2002, pp. 175-178.

[48] J. Alieu, T. Skotnicki, E. Josse, J.-L. Regolini, and G. Bremond, "Multiple SiGe well: a new channel architecture for improving both NMOS and PMOS performances," in *Proc. Symp. VLSI Techology*, 2000, pp. 130-131.

[49] Y.-C. Yeo, V. Subramanian, J. Kedzierski, P. Xuan, T.-J. King, J. Bokor, and C. Hu, "Design and fabrication of 50-nm thin-body p-MOSFETs with a SiGe heterostructure channel," *IEEE Trans. Electron Devices*, vol. 49, pp. 279-286, 2002.

[50] M. V. Fischetti and S. E. Laux, "Band structure, deformation potentials, and carrier mobility in strained Si, Ge and SiGe alloys," *J. Appl. Phys.*, vol. 80, pp. 2234-2252, 1996.

[51] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, and M. Bohr, "A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors," in *IEDM Tech. Dig.*, 2003, pp. 978-980.

[52] J. L. Hoyt, H. M. Nayfeh, S. Eguchi, I. Aberg, G. Xia, T. Drake, E. A. Fitzgerald, and D. A. Antoniadis, "Strained silicon MOSFET technology," in *IEDM Tech. Dig.*, 2002, pp. 23-26.

[53] S. H. Olsen, K. S. K. Kwa, L. S. Driscoll, S. Chattopadhyay, and A. G. O'Neill, "Design, fabrication and characterisation of strained Si/SiGe MOS transistors," *IEE Proc.-Circuits Devices Syst.*, vol. 151, pp. 431-437, 2004.

[54] T. Tezuka, N. Sugiyama, and S. Takagi, "Fabrication of strained Si on an ultrathin SiGe-on-insulator virtual substrate with a high-Ge fraction," *Appl. Phys. Lett.*, vol. 79, pp. 1798-1800, 2001.

[55] Sessions about 'CMOS Devices – Strained Silicon' in *IEDM. Tech. Dig.*, 2004, pp. 157-184 and pp. 209-236.

[56] J.-S. Goo, Q. Xiang, Y. Takamura, H. Wang; J. Pan, F. Arasnia, E. N. Paton, P. Besser, M. V. Sidorov, E. Adem, A. Lochtefeld, G. Braithwaite, M .T. Currie, R.

Hammond, M. T. Bulsara, and M.-R. Lin, "Scalability of strained-Si nMOSFETs down to 25 nm gate length," *IEEE Electron Device Letters*, vol. 24, pp. 351-353, 2003.

[57] K. M. Cao, W.-C. Lee, W. Liu, X. Jin, P. Su, S. K. H. Fung, J. X. An, B. Yu, and C. Hu, "BSIM4 gate leakage model including source-drain partition," in *IEDM Tech. Dig.*, 2000, pp. 815-818.

[58] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-κ gate dielectrics: Current status and materials properties considerations," *J. Appl. Phys.*, vol. 89, pp. 5243-5275, 2001.

[59] E. P. Gusev, D. A. Buchanan, E. Cartier, A. Kumar, D. DiMaria, S. Guha, A. Callegari, S. Zafar, P. C. Jamison, D. A. Neumayer, M. Copel, M. A. Gribelyuk, H. Okron-Schmidt, C. D'Emic, P. Kozlowski, K. Chan, N. Bojarczuk, L.-Å. Ragnarsson, P. Ronsheim, K. Rim, R. J. Fleming, A. Mocuta, and A. Ajmera, "Ultrathin high-K gate stacks for advanced CMOS devices," in *IEDM Tech. Dig., 2001*, pp. 451-454.

[60] A. L. P. Rotondaro, M. R. Visokay, J. J. Chambers, A. Shanware, R. Khamankar, H. Bu, R. T. Laaksonen, L. Tsung, M. Douglas, R. Kuan, M. J. Bevan, T. Grider, J. McPherson, and L. Colombo, "Advanced CMOS transistors with a novel HfSiON gate dielectric," in *Proc. Symp. VLSI Technology*, 2002, pp. 148-149.

[61] W. J. Zhu and T. P. Ma, "Temperature Dependence of channel mobility in HfO_2-gated NMOSFETs," *IEEE Electron Device Lett.*, vol. 25, pp. 89-91, 2004.

[62] S. Saito, D. Hisamoto, S. Kimura, and M. Hiratani, "Unified mobility model for high-κ gate stacks," in *IEDM Tech. Dig.*, 2003, pp.797-800.

[63] Z. Ren, M. V. Fischetti, E. P. Gusev, E. A. Cartier, and M. Chudzik, "Inversion channel mobility in high-κ high performance MOSFETs," in *IEDM Tech Dig.*, 2003, pp. 793-796.

[64] L.-Å. Ragnarsson, L. Pantisano, V. Kaushik, S.-I. Saito, Y. Shimamoto, S. De Gendt, and M. Heyns, "The impact of sub monolayers of HfO_2 on the device performance of high-k based transistors," in *IEDM Tech. Dig.*, 2003, pp. 87-90.

[65] G.-W. Lee, J.-H. Lee, H.-W. Lee, M.-K. Park, D.-G. Kang, and H.-K. Youn, "Trap evolutions of metal/oxide/silicon field-effect transistors with high-*k* gate dielectric using charge pumping method," *Appl. Phys. Lett.*, vol. 81, pp. 2050-2052, 2002.

[66] J. Robertson, "Interfaces and defects of high-*K* oxides on silicon," *Solid-State Electron.*, vol. 49, pp. 283-293, 2005.

[67] M. Fadlallah, A. Szewczyk, C. Giannakopoulos, B. Cretu, F. Monsieur, T. Devoivre, J. Jomaah, and G. Ghibaudo, "Low-frequency noise and reliability properties of 0.12 μm CMOS devices with Ta_2O_5 as gate dielectrics," *Microelectron. Reliab.*, vol. 41, pp. 1361-1366, 2001.

[68] T. Ishikawa, S. Tsujikawa, S. Saito, D. Hisamoto, and S. Kimura, "Direct evaluation of an interfacial layer in high-κ gate dielectrics by 1/*f* noise measurements," in *Proc. Int. Conf. Solid State Devices and Materials (SSDM)*, 2003, pp. 14-15.

[69] E. Simoen, A. Mercha, L. Pantisano, C. Claeys, and E. Young, "Low-frequency noise study of n-MOSFETs with HfO_2 gate dielectric," in *Proc. Vol. 22 Electrochem Soc. Meeting*, 2003, pp. 319-331.

[70] H. Sauddin, Y. Yoshihara, S. Ohmi, K. Tsutsui, and H. Iwai, "Low-frequency noise characteristics of MISFETs with La_2O_3 gate dielectrics," in *Proc. Vol. 22 Electrochem Soc. Meeting*, 2003, pp. 415-423.

[71] H. D. Xiong, D. M. Fleetwood, J. A. Felix, E. P. Gusev, and C. D'Emic, "Low-frequency noise and radiation response of metal-oxide-semiconductor transistors with Al_2O_3/SiO_xN_y/Si(100) gate stacks," *Appl. Phys. Lett.*, vol. 83, pp. 5232-5234, 2003.

[72] E. Simoen, A. Mercha, L. Pantisano, C. Claeys, and E. Young, "Low-frequency noise behavior of SiO_2-HfO_2 dual-layer gate dielectric nMOSFETs with different interfacial oxide thickness," *IEEE Trans. Electron Devices*, vol. 51, pp. 780-784, 2004.

[73] T. Horikawa, N. Yasuda, W. Mizubayashi, K. Iwamoto, K. Tominaga, K. Akiyama, K. Yamamoto, H. Hisamatsu, H. Ota, T. Nabatame, and A. Toriumi, "Low frequency noise characteristics in $HfAlO_x/SiO_2$ n-MOSFETs," in *Proc. Vol. 1 Electrochem Soc. Meeting*, 2004, pp. 292-303.

[74] B. Min, S. P. Devireddy, Z. Çelik-Butler, F. Wang, A. Zlotnicka, H.-H. Tseng, and P. J. Tobin, "Low-frequency noise in submicrometer MOSFETs with HfO_2, HfO_2/Al_2O_3 and $HfAlO_x$ Gate Stacks," *IEEE Trans. Electron Devices*, vol. 51, pp. 1679-1687, 2004.

[75] A. Kerber, E. Cartier, L. Pantisano, R. Degraeve, T. Kauerauf, Y. Kim, A. Hou, G. Groeseneken, H. E. Maes, and U. Schwalke, "Origin of the threshold voltage instability in SiO_2/HfO_2 dual layer gate dielectrics," *IEEE Electron Device Lett.*, vol. 24, 87-89, 2003.

[76] S. Zafar, A. Callegari, E. Gusev, and M. V. Fischetti, "Charge trapping related threshold voltage instabilities in high permittivity gate dielectric stacks," *J. Appl. Phys.*, vol. 93, pp. 9298-9303, 2003.

[77] M. Bhat, D. J. Wristers, L.-K. Han, J. Yan, H. J. Fulford, and D.-L. Kwong, "Electrical properties and reliability of MOSFET's with rapid thermal NO-nitrided SiO_2 gate dielectrics," *IEEE Trans. Electron Devices*, vol. 42, pp. 907-914, 1995.

[78] J. S. Cable, R. A. Mann, and J. C. S. Woo, "Impurity barrier properties of reoxidized nitrided oxide films for use with P+-doped polysilicon gates," *IEEE Electron Device Lett.*, vol. 12, pp. 128-130, 1991.

[79] M. V. Fischetti, D. A. Neumayer, and E. A. Cartier, "Effective electron mobility in Si inversion layers in metal-oxide-semiconductor systems with a high-κ insulator: The role of remote phonon scattering," *J. Appl. Phys.*, pp. 4587-4608, 2001.

[80] B. Guillaumot, X. Garros, F. Lime, K. Oshima, B. Tavel, J. A. Chroboczek, P. Masson, R. Truche, A. M. Papon, F. Martin, J. F. Damlencourt, S. Maitrejean, M. Rivoire, C. Leroux, S. Christoloveanu, G. Ghibaudo, J. L. Autran, T. Skotnicki, and S. Deleonibus, "75nm damascene metal gate and high-k integration for advanced CMOS devices," in *IEDM Tech. Dig.*, 2002, pp. 355-358.

[81] P. Xuan and J. Bokor, "Investigation of NiSi and TiSi as CMOS gate materials," *IEEE Electron Device Lett.*, vol. 24, pp. 634-636, 2003.

[82] G. Sjöblom, J. Westlinder, and J. Olsson, "Investigation of the thermal stability of reactively sputter deposited TiN MOS gate electrodes," *IEEE Trans. Electron Devices*, vol. 52, pp. 2349-2352, 2005.

[83] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-κ/metal-gate stack and its MOSFETs characteristics," *IEEE Electron Device Lett.*, vol 25, pp. 408-410, 2004.

[84] D. Wu, A.-C. Lindgren, S. Persson, G. Sjöblom, M. von Haartman, J. Seger, P.-E. Hellström, J. Olsson, H.-O. Blom, S.-L. Zhang, M. Östling, E. Vainonen-Ahlgren, W.-M. Li, E. Tois, and M. Tuominen, "A novel strained $Si_{0.7}Ge_{0.3}$ surface-channel pMOSFET with an ALD $TiN/Al_2O_3/HfAlO_x/Al_2O_3$ gate stack," *IEEE Electron Device Lett.*, vol. 24, pp. 171-173, 2003.

[85] J.-P. Colinge, "Fully-depleted SOI CMOS for analog applications," *IEEE Trans. Electron Devices*, vol. 45, pp. 1010-1016, 1998.

[86] S. Cristoloveanu, "Silicon on insulator technologies and devices: from present to future," *Solid-State Electron.*, vol. 45, pp. 1403-1411, 2001.

[87] T. Ernst, S. Cristoloveanu, G. Ghibaudo, T. Ouisse, S. Horiguchi, Y. Ono, Y. Takahashi, and K. Murase, "Ultimately thin double-gate SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 50, pp. 830-838, 2003.

[88] S. Narasimha, A. Ajmera, H. Park, D. Schepis, N. Zamdmer, K. A. Jenkins, J.-O. Plouchart, W.-H. Lee, J. Mezzapelle, J. Bruley, B. Doris, J. W. Sleight, S. K. Fung, S. H. Ku, A. C. Mocuta, I. Yang, P. V. Gilbert, K. P. Muller, P. Agnello, and J. Welser, "High performance sub-40nm CMOS devices on SOI for the 70nm technology node," in *IEDM Tech. Dig.*, 2001, pp. 625-628.

[89] S. Monfray, T. Skotnicki, C. Fenouillet-Beranger, N. Carriere, D. Chanemougame, Y. Morand, S. Descombes, A. Talbot, D. Dutartre, C. Jenny, P. Mazoyer, R. Palla, F. Leverd, Y. Le Friec, R. Pantel, S. Borel, D. Louis, and N. Buffet, "Emerging silicon-on-nothing (SON) devices technology," *Solid-State Electron.*, vol. 48, pp. 887-895, 2004.

[90] B .Doris, M. Ieong, T. Kanarsky, Y. Zhang, R. A. Roy, O. Dokumaci, Z. Ren, F.-F. Jamin, L. Shi, W. Natzle, H.-J. Huang, J. Mezzapelle, A. Mocuta, S. Womack, M. Gribelyuk, E. C. Jones, R. J. Miller, H.-S. P. Wong, and W. Haensch, "Extreme scaling with ultra-thin Si channel MOSFETs," in *IEDM Tech. Dig.*, 2002, pp. 267-270.

[91] F.-L. Yang, H.-Y. Chen, F.-C. Chen, C.-C. Huang, C.-Y. Chang, H.-K. Chiu, C.-C. Lee, C.-C. Chen, H.-T. Huang, C.-J. Chen, H.-J. Yeo, M.-S. Liang, and C. Hu, "25 nm CMOS Omega FETs," in *IEDM Tech. Dig.*, 2002, pp. 255-258.

[92] M. Bruel, B. Aspar, B. Charlet, C. Maleville, T. Poumeyrol, A. Soubie, A. J. Auberton-Herve, J. M. Lamure, T. Barge, F. Metral, and S. Trucchi, "'Smart cut': a promising new SOI material technology," in *Proc. IEEE Int. SOI Conf.*, 1995, pp. 178-179.

[93] C. Claeys, E. Simoen, A. Efremov, V. G. Litovchenko, A. Evtukh, A. Kizjak, and Ju. Rassamakin, "γ-irridation hardness of short-channel nMOSFETs fabricated in a 0.5 μm SOI technology," *Nucl. Instr. and Meth. B*, vol. 186, pp. 429-434, 2002.

[94] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa, "Double-gate silicon-on-insulator transistor with volume inversion: a new device with greatly enhanced performance," *IEEE Electron. Device Lett.*, vol. EDL-8, pp. 410-412, 1987.

[95] D. Esseni, A. Abramo, L. Selmi, and E. Sangiorgi, "Physically based modeling of low field electron mobility in ultrathin single- and double-gate SOI nMOSFETs," *IEEE Trans. Electron Devices*, vol. 50, pp. 2445-2455, 2003.

[96] R. Landauer, "The noise is the signal," *Nature*, vol. 392, pp. 658-659, 1998.

[97] J. B. Johnson, "Thermal agitation of electricity in conductors," *Phys. Rev.*, vol. 32, pp. 97-109, 1928.

[98] H. Nyquist, "Thermal agitation of electric charge in conductors," *Phys. Rev.*, vol. 32, pp. 110-113, 1928.

[99] W. Schottky, "Über spontane Stromschwankungen in verschiedenen Elektrizitätsleitern," *Annalen der Physik*, vol. 57, pp. 541-567, 1918.

[100] A. van der Ziel, *Noise in solid state devices and circuits*, John Wiley & Sons, 1986.

[101] S. Machlup, "Noise in semiconductors: spectrum of a two-parameter random signal," *J. Appl. Phys.*, vol. 25, pp. 341-343, 1954.

[102] P. Dutta and P. M. Horn, "Low-frequency fluctuations in solids: 1/*f* noise," *Rev. Mod. Phys.*, vol. 53, pp. 497-516, 1981.

[103] F. N. Hooge, T. G. M. Kleinpenning, and L. K. J. Vandamme, "Experimental studies on 1/*f* noise," *Rep. Prog. Phys.*, vol. 44, pp. 479-531, 1981.

[104] M. Surdin, "Fluctuations in the thermionic current and the 'flicker effect'," *J. Phys. Radium*, vol. 10, pp. 188-189, 1939.

[105] F. N. Hooge, "1/*f* noise sources," *IEEE Trans. Electron Devices*, vol 41, pp. 1926-1935, 1994.

[106] F. N. Hooge, "1/*f* noise is no surface effect," *Phys. Lett. A*, vol. 29a, pp. 139-140, 1969.

[107] F. N. Hooge, "Discussion of recent experiments on 1/*f* noise," *Physica*, vol. 60, pp. 130-144, 1972.

[108] J. Chang, A. A. Abidi, and C. R. Viswanathan, "Flicker noise in CMOS transistors from subthreshold to strong inversion at various temperatures," *IEEE Trans. Electron Devices*, vol. 41, pp. 1965-1971, 1994.

[109] E. Simoen, and C. Claeys, "On the flicker noise in submicron silicon MOSFETs," *Solid-State Electron.*, vol. 43, pp. 865-882, 1999.

[110] G. Ghibaudo, and T. Boutchacha, "Electrical noise and RTS fluctuations in advanced CMOS devices," *Microelectron. Reliab.*, vol. 42, pp. 573-582, 2002.

[111] P. H. Handel, "Fundamental quantum 1/*f* noise in semiconductor devices," *IEEE Trans. Electron Devices*, vol. 41, pp. 2023-2033, 1994.

[112] P. H. Handel, "1/*f* noise-an 'infrared' phenomenon," *Phys. Rev. Lett.*, vol. 34, pp. 1492-1494, 1975.

[113] Th. M. Nieuwenhuizen, D. Frenkel, and N. G. van Kampen, "Objections to Handel's quantum theory of 1/*f* noise," *Phys. Rev. A*, vol. 35, pp. 2750-2753, 1987.

[114] L. B. Kiss and P. Heszler, "An exact proof of the invalidity of 'Handel's quantum 1/*f* noise model', based on quantum electrodynamics," *J. Phys. C: Solid State Phys.*, vol. 19, pp. L631-L633, 1986.

[115] C. M. Van Vliet, "A survey of results and future prospects on quantum 1/*f* noise and 1/*f* noise in general," *Solid-State Electron.*, vol. 34, pp. 1-21, 1991.

[116] G. S. Kousik, C. M. Van Vliet, G. Bosman, and P. H. Handel, "Quantum 1/*f* noise associated with ionized impurity scattering and electron-phonon scattering in condensed matter," *Advances in Physics*, vol. 34, pp. 663-702, 1985.

[117] T. Musha and M. Tacano, "Dynamics of energy partition among coupled harmonic oscillators in equilibrium," *Physica A*, vol. 346, pp. 339-346, 2005.

[118] R. P. Jindal and A. van der Ziel, "Phonon fluctuation model for flicker noise in elemental semiconductors," *J. Appl. Phys.*, vol. 52, pp. 2884-2888, 1981.

[119] M. N. Mihaila, "Phonon-induced 1/*f* noise in MOS transistors," *Fluctuation and Noise Letters*, vol. 4, pp. L329-L343, 2004.

[120] Y. Tsividis, *Operation and modeling of the MOS transistor*, 2nd ed., WCB McGraw-Hill, 1999.

[121] B. Razavi, "CMOS technology characterization for analog and RF design," *IEEE J. Solid-State Circuits*, vol. 34, pp. 268-276, 1999.

[122] K. Lee, I. Nam, I. Kwon, J. Gil, K. Han, S. Park, B.-I. Seo, "The impact of semiconductor technology scaling on CMOS RF and digital circuits for wireless application," *IEEE Trans. Electron Devices*, vol. 52, pp. 1415-1422, 2005.

[123] P. H. Woerlee, M. J. Knitel, R. van Langevelde, D. B. M. Klaassen, L. F. Tiemeijer, A. J. Scholten, and A. T. A. Zegers-van Duijnhoven, "RF-CMOS performance trends," *IEEE Trans. Electron Devices*, vol. 48, pp. 1776-1782, 2001.

[124] H. S. Bennett, R. Brederlow, J. C. Costa, P. E. Cottrell, W. M. Huang, A. A. Immorlica, J.-E. Mueller, M. Racanelli, H. Shichijo, C. E. Weitzel, and B. Zhao, "Device and technology evolution for Si-based RF integrated circuits," *IEEE Trans. Electron Devices*, vol. 52, pp. 1235-1258, 2005.

[125] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circ.*, vol. 33, pp. 179-194, 1998.

[126] T. H. Lee and A. Hajimiri, "Oscillator phase noise: a tutorial," *IEEE J. Solid-State Circuits*, vol. 35, pp. 326-336, 2000.

[127] M. Sandén, F. Jonsson, O. Marinov, M. J. Deen, and M. Östling, "Up-conversion of 1/*f* noise to phase noise in voltage controlled oscillators," in *Proc. 16th Int. Conf. Noise and Fluctuations (ICNF)*, 2001, pp. 499-502.

[128] F. Jonsson, M. von Haartman, M. Sandén, M. Östling, and M. Ismail, "A voltage controlled oscillator with automatic amplitude control in SiGe technology," in *Proc. 19th NORCHIP*, 2001, pp. 28-33.

[129] S. Zhou and M.-C. F. Chung, "A CMOS passive mixer with low flicker noise for low-power direct-conversion receiver," *IEEE J. Solid-State Circuits*, vol. 40, pp. 1084-1093, 2005.

[130] H. Darabi and A. A. Abidi, "Noise in RF-CMOS mixers: a simple physical model," *IEEE Trans. Solid State Circuits*, vol. 35, pp. 15-25, 2000.

[131] A. L. McWorther, *Semiconductor surface physics*, University of Pennsylvania Press, 1957.

[132] B. Cretu, M. Fadlallah, G. Ghibaudo, J. Jomaah, F. Balestra, and G. Guégan, "Thorough characterization of deep-submicron surface and buried channel pMOSFETs," *Solid-State Electron.*, pp. 971-975, 2002.

[133] M. Fadlallah, G. Ghibaudo, J. Jomaah, M. Zoaeter, and G. Guégan, "Static and low frequency noise characterization of surface- and buried-mode 0.1 μm P and NMOSFETS," *Microelectron. Reliab.*, vol. 42, 41-46, 2002.

[134] R. A. Wilcox, J. Chang, and C. R. Viswanathan, "Low-temperature characterization of buried-channel NMOST," *IEEE Trans. Electron Devices*, vol. 36, pp. 1440-1447, 1994.

[135] X. Li, C. Barros, E. P. Vandamme, and L. K. J. Vandamme, "Parameter extraction and 1/f noise in a surface and a bulk-type, p-channel LDD MOSFET," *Solid-State Electron.*, vol. 37, pp. 1853-1862, 1994.

[136] L. K. J. Vandamme, "Bulk and surface 1/*f* noise," *IEEE Trans. Electron Devices*, vol. 36, pp. 987-992, 1989.

[137] A. van der Ziel, "Flicker noise in semiconductors: not a true bulk effect," *Appl. Phys. Lett.*, vol. 33, pp. 883-884, 1978.

[138] A. van der Ziel, "Unified presentation of 1/*f* noise in electronic devices: fundamental 1/*f* noise sources," *Proc. IEEE*, vol. 76, pp. 233-258, 1988.

[139] G. Ghibaudo, O. Roux, Ch. Nguyen-Duc, F. Balestra, and J. Brini, "Improved analysis of low-frequency noise in field-effect MOS transistors," *Phys. Stat. Sol. A*, vol. 124, pp. 571-581, 1991.

[140] S. Christensson, I. Lundström, and C. Svensson, "Low-frequency noise in MOS transistors-I theory," *Solid-State Electron.*, vol. 11, pp. 797-812, 1968.

[141] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors," *IEEE Trans. Electron Devices*, vol. 37, pp. 654-665, 1990.

[142] N. Lukyanchikova, M. Petrichuk, N. Garbar, E. Simoen, A. Mercha, C. Claeys, H. van Meer, and K. De Meyer, "The $1/f^{1.7}$ noise in submicron SOI MOSFETs with 2.5 nm nitrided gate oxide," *IEEE Trans. Electron Devices*, vol. 49, pp. 2367-2370, 2002.

[143] G. Reimbold, "Modified 1/*f* trapping noise theory and experiments in MOS transistors biased from weak to strong inversion-influence of interface states," *IEEE Trans. Electron Devices*, vol. ED-31, pp. 1190-1198, 1984.

[144] H.-S. Fu and C.-T. Sah, "Theory and experiments on surface 1/*f* noise," *IEEE Trans. Electron Devices*, vol. ED-19, pp. 273-285, 1972.

[145] C. Surya and T. Y. Hsiang, "A thermal activation model for 1/f^{γ} noise in Si-MOSFETs," *Solid-State Electron.*, vol. 31, pp. 959-964, 1988.

[146] F. N. Hooge and L. K. J. Vandamme, "Lattice scattering causes 1/*f* noise," *Phys. Lett. A*, vol. 66, pp. 315-316, 1978.

[147] J. Rhayem, D. Rigaud, A. Eya'a, and M. Valenza, "1/*f* noise in metal-oxide-semiconductor transistors biased in weak inversion," *J. Appl. Phys.*, vol. 89, pp. 4192-4194, 2001.

[148] L. K. J. Vandamme and G. Trefán, "1/*f* noise in homogeneous and inhomogeneous media," *IEE Proc.-Circuits Devices Syst.*, vol. 149, pp. 3-12, 2002.

[149] M. J. Deen and O. Marinov, "Effect of forward and reverse substrate biasing on low-frequency noise in silicon PMOSFETs," *IEEE Trans. Electron Devices*, vol. 49, pp. 409-413, 2002.

[150] M. Marin, M. J. Deen, M. de Murcia, P. Llinares, and J. C. Vildeuil, "Effects of body biasing on the low frequency noise of MOSFETs from 130 nm CMOS technology," *IEE Proc.-Circuits Devices Syst.*, vol. 151, pp. 95-101, 2004.

[151] N. Park and K. K. O, "Body bias dependence of 1/*f* noise in NMOS transistors from deep-subthreshold to strong inversion," *IEEE Trans. Electron Devices*, vol. 48, pp. 999-1001, 2001.

[152] A. Asai, J. Sato-Iwanaga, A. Inoue, Y. Hara, Y. Kanzawa, H. Sorada, T. Kawashima, T. Ohnishi, T. Takagi, and M. Kubo, "Low-frequency noise characteristics in SiGe channel heterostructure dynamic threshold pMOSFETs (HDTMOS)," in *IEDM Tech. Dig.*, 2002, pp. 35-38.

[153] T.-L. Hsu, D. D.-L. Tang, and J. Gong, "Low-frequency noise properties of dynamic threshold (DT) MOSFET's," *IEEE Electron Device Lett.*, vol. 20, pp. 532-534, 1999.

[154] S. Haendler, J. Jomaah, G. Ghibaudo, and F. Balestra, "Improved analysis of low frequency noise in dynamic threshold MOS/SOI transistors," *Microelectron. Reliab.*, vol. 41, pp. 855-860, 2001.

[155] A. K. M. Ahsan and D. K. Schroder, "Impact of channel carrier displacement and barrier height lowering on the low-frequency noise characteristics of surface-channel n-MOSFETs," *Solid-State Electron.*, vol. 49, pp. 654-662, 2005.

[156] P. Gaubert, A. Teramoto, T. Hamada, M. Yamamoto, K. Nii, H. Akahori, K. Kotani, and T. Ohmi, "Impact of interface micro-roughness on low-frequency noise in (110) and (100) pMOSFETs," in *Proc. Int. Conf. Noise and Fluctuations (ICNF)*, 2005, pp. 199-202.

[157] M. N. Darwish, J. L. Lentz, M. R. Pinto, P. M. Zeitzoff, T. J. Krutsick, and H. H. Vuong, "An improved Electron and Hole Mobility Model for General Purpose Device Simulation," *IEEE Trans. Electron Devices*, vol. 44, pp. 1529-1538, 1997.

[158] A. Mercha, E. Simoen, and C. Claeys, "Impact of high vertical electric field on low-frequency noise in thin-gate oxide MOSFETs," *IEEE Trans. Electron Devices*, vol. 50, pp. 2520-2527, 2003.

[159] M. Valenza, A. Hoffmann, D. Sodini, A. Laigle, F. Martinez, and D. Rigaud, "Overview of the impact of downscaling technology on 1/*f* noise in p-MOSFETs to 90nm," *IEE Proc.-Circuits Devices Syst.*, vol. 151, pp. 102-110, 2004.

[160] J. H. Scofield, N. Borland, and D. M. Fleetwood, "Reconciliation of different gate-voltage dependencies of 1/*f* noise in n-MOS and p-MOS transistors," *IEEE Trans. Electron Devices*, vol. 41, pp. 1946-1952, 1994.

[161] T. Sakurai and T. Sugano, "Theory of continuously distributed trap states at Si-SiO_2 interfaces," *J. Appl. Phys.*, vol. 52, pp. 2889-2896, 1981.

[162] M. S. Kim, I. C. Nam, H. T. Kim, H. T. Shin, T. E. Kim, H. S. Park, K. S. Kim, K. H. Kim, J. B. Choi, K. S. Min, D. J. Kim, D. W. Wang, and D. M. Min, "Optical

subthreshold current method for extracting the interface states in MOS systems," *IEEE Electron Device Lett.*, vol. 25, pp. 101-103, 2004.

[163] M. J. Knitel, P. H. Woerlee, A. J. Scholten, and A. T. A. Zegers-Van Duijnhoven, "Impact of process scaling on 1/*f* noise in advanced CMOS technologies," in *IEDM Tech. Dig.*, 2000, pp. 463-466.

[164] R. Brederlow, W. Weber, D. Schmitt-Landsiedel, and R. Thewes, "Fluctuations of the low frequency noise of MOS transistors and their modeling in analog and RF-circuits," in *IEDM Tech. Dig.*, 1999, pp. 159-162.

[165] A. J. Scholten, L. F. Tiemeijer, R. van Langevelde, R. J. Havens, A. T. A. Zegers-van Duijnhoven, and V. C. Venezia, "Noise modeling for RF CMOS circuit simulation," *IEEE Trans. Electron Devices*, vol. 50, pp. 618-632, 2003.

[166] A. P. van der Wel, E. A. M. Klumperink, S. L. J. Gierkink, R. F. Waassenaar, and H. Wallinga, "MOSFET 1/*f* noise measurements under switched bias conditions," *IEEE Electron Device Lett.*, vol. 21, pp. 43-46, 2000.

[167] R. Brederlow, J. Koh, G. I. Wirth, R. da Silva, M. Tiebout, and R. Thewes, "Low frequency noise considerations for CMOS analog circuit design," in *Proc. Int. Conf. Noise and Fluctuations (ICNF)*, 2005, pp. 703-708.

[168] P. Srinivasan, E. Simoen, L. Pantisano, C. Claeys, and D. Misra, "Impact of gate material on low-frequency noise of nMOSFETs with 1.5 nm SiON gate dielectric: testing the limits of the number fluctuation theory," in *Proc. Int. Conf. Noise and Fluctuations (ICNF)*, 2005, pp. 231-234.

[169] S. T. Martin, G. P. Li, E. Worley, and J. White, "The gate bias and geometry dependence of random telegraph signal amplitudes," *IEEE Electron Device Lett.*, vol. 18, pp. 444-446, 1997.

[170] J. Koga, S. Takagi, and A. Toriumi, "A comprehensive study of MOSFET electron mobility in both weak and strong inversion regimes," in *IEDM Tech. Dig.*, 1994. p. 475-478.

[171] A. K. M. Ahsan and D. K. M. Schroder, "Impact of post-oxidation annealing on low-frequency noise, threshold voltage, and subthreshold swing of p-channel MOSFETs," *IEEE Electron Device Lett.*, vol. 25, pp. 211-213, 2004.

[172] J.-S. Lee, D. Ha, Y.-K. Choi, T.-J. King, and J. Bokor, "Low-frequency noise characteristics of ultrathin body p-MOSFETs with molybdenum gate," *IEEE Electron Device Lett.*, vol. 24, pp. 31-33, 2003.

[173] M. Fadlallah, G. Ghibaudo, J. Jomaah, and G. Guégan, "Static and low frequency noise characterization in surface- and buried-mode 0.1 μm PMOSFETS," *Solid-State Electron.*, vol. 47, 1155-1160, 2003.

[174] E. Emrani, F. Balestra, and G. Ghibaudo, "On the understanding of electron and hole mobility models from room to liquid helium temperatures," *Solid-State Electron.*, vol. 37, pp. 1723-1730, 1994.

[175] S. C. Sun and J. D. Plummer, "Electron mobility in inversion and accumulation layers on thermally oxidized silicon surfaces," *IEEE Trans Electron Devices*, vol. ED-27, pp. 1497-1508, 1980.

[176] A. Pacelli, S. Villa, A. L. Lacaita, and L. M. Perron, "Quantum effects on the extraction of MOS oxide traps by 1/*f* noise measurements," *IEEE Trans. Electron Devices*, vol. 46, pp. 1029-1035, 1999.

[177] E. P. Vandamme and L. K. J. Vandamme, "Unsolved problems on 1/*f* noise in MOSFETs and possible solutions," in *Proc. Unsolved Problems of Noise and fluctuations (UPoN)*, 1999, pp. 395-400.

[178] N. W. Ashcroft and N. D. Mermin, *Solid State Physics*, Brooks/Cole Thomson Learning, 1976.

[179] N. Takabatake, T. Kobayashi, Y. Show, and T. Izumi, "Photoacoustic evalutation of defects and thermal conductivity in the surface layer of ion implanted semiconductors," *Mat. Sci. Eng.*, vol. B91-92, pp. 186-188, 2002.

[180] L. K. J. Vandamme and S. Oosterhoff, "Annealing of ion-implanted resistors reduces the 1/*f* noise," *J. Appl. Phys.*, vol. 59, pp. 3169-3174, 1986.

[181] T. G. M. Kleinpenning, "On 1/*f* noise and random telegraph noise in very small electronic devices," *Physica B*, vol. 164, pp. 331-334, 1990.

[182] O. Roux Dit Buisson, G. Ghibaudo, and J. Brini, "Model for drain current RTS amplitude in small-area MOS transistors," *Solid-State Electron.*, vol. 35, pp. 1273-1276, 1992.

[183] N. V. Amarasinghe, Z. Çelik-Butler, and A. Keshavarz, "Extraction of oxide trap properties using temperature dependence of random telegraph signals in submicron metal-oxide-semiconductor field-effect transistors," *J. Appl. Phys.*, vol. 89, pp. 5526-5532, 2001.

[184] W. Shockley and W. T. Read, Jr., "Statistics of the recombinations of holes and electrons," *Phys. Rev.*, vol. 87, pp. 835-842, 1952.

[185] C. Leroux, J. Mitard, G. Ghibaudo, X. Garros, G. Reimbold, B. Guillaumot, and F. Martin, "Characterization and modelling of hysteresis phenomena in high k dielectrics," in *IEDM Tech. Dig.*, 2004, pp. 737-740.

[186] S. Jakschik, A. Avellan, U. Schroeder, and J. W. Bartha, "Influence of Al_2O_3 dielectrics on the trap-depth profiles in MOS devices investigated by the charge-pumping method," *IEEE Trans. Electron Devices*, vol. 51, pp. 2252-2255, 2004.

[187] Y. Nemirovsky, I. Brouk, and C. G. Jakobson, "1/*f* noise in CMOS transistors for analog applications," *IEEE Trans. Electron Devices*, vol. 48, pp. 921-927, 2001.

[188] E. Simoen, A. Mercha, C. Claeys, and E. Young, "Correlation between the 1/*f* noise parameters and the effective low-field mobility in HfO_2 gate dielectric n-channel metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 85, pp. 1057-1059, 2004.

[189] F. Dieudonné, S. Haendler, J. Jomaah, and F. Balestra, "Low frequency noise in 0.12 μm partially and fully depleted SOI technology," *Microelectron. Reliab.*, vol. 43, pp. 243-248, 2003.

[190] B. Min, S. P. Devireddy, and Z. Çelik-Butler, "Low-frequency noise characteristics of HfSiON gate-dielectric metal-oxide-semiconductor-field-effect transistors," *Appl. Phys. Lett.*, vol. 86, 082102, 2005.

[191] F. Dieudonné, S. Haendler, J. Jomaah, and F. Balestra, "Low frequency noise and hot-carrier reliability in advanced SOI MOSFETs," *Solid-State Electron.*, vol. 48, pp. 985-997, 2004.

[192] E. Simoen, A. Mercha, C. Claeys, N. Lukyanchikova, and N. Garbar, "Critical discussion of the front-back gate coupling effect on the low-frequency noise in fully depleted SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 51, pp. 1008-1016, 2004.

[193] J.-S. Lee, Y.-K. Choi, D. Ha, S. Balasubramanian, T.-J. King, and J. Bokor, "Hydrogen annealing effect on DC and low-frequency noise characteristics in CMOS FinFETs," *IEEE Electron Device Lett.*, vol. 24, pp. 186-188, 2003.

[194] Y. Akue Allogo, M. Marin, M. de Murcia, P. Llinares, and D. Cottin, "1/*f* noise in 0.18 μm technology n-MOSFETs from subthreshold to saturation," *Solid-State Electron.*, vol. 46, pp. 977-983, 2002.

[195] P. Srinivasan, E. Simoen, L. Pantisano, C. Claeys, and D. Misra, "Impact of high-k gate stack material with metal gates on LF noise in n- and p-MOSFETs," *Microelectron. Eng.*, vol. 80, pp. 226-229, 2005.

[196] N. Lukyanchikova, N. Garbar, M. Petrichuk, E. Simoen, and C. Claeys, "Flicker noise in deep submicron nMOS transistors," *Solid-State Electron.*, vol. 44, pp. 1239-1245, 2000.

[197] E. Simoen, G. Eneman, P. Verheyen, R. Delhougne, R. Loo, K. De Meyer, and C. Claeys, "On the beneficial impact of tensile-strained silicon substrates on the low-frequency noise of n-channel metal-oxide-semiconductor transistors," *Appl. Phys. Lett.*, vol. 86, 223509, 2005.

[198] V. Subramanian, A. Mercha, A. Dixit, K. G. Anil, M. Jurczak, K. De Meyer, S. Decoutere, H. Maes, G. Groeseneken, and W. Sansen, "Geometry dependence of 1/*f* noise in N- and P- Channel MuGFETs," in *Proc. Int. Conf. Noise and Fluctuations (ICNF)*, 2005, pp. 279-282.

[199] K. W. Chew, K. S. Yeo, and S.-F. Chu, "Effect of technology scaling on the 1/*f* noise of deep submicron PMOS transistors," *Solid-State Electron.*, vol. 48, pp. 1101-1109, 2004.

[200] M. A. Schmidt, F. L. Terry, Jr., B. P. Mathur, and S. D. Senturia, "Inversion layer mobility of MOSFET's with nitrided oxide gate dielectrics," *IEEE Trans. Electron Devices*, vol. 35, pp. 1627-1632, 1988.

[201] T. Ishihara, K. Matsuzawa, M. Takayanagi, and S. Takagi, "Comprehensive understanding of electron and hole mobility limited by surface roughness scattering in pure oxides and oxynitrides based on correlation function of surface roughness," *Jpn. J. Appl. Phys.*, vol. 41, pp. 2353-2358, 2002.

[202] P. Morfouli, G. Ghibaudo, T. Ouisse, E. Vogel, W. Hill, V. Misra, P. McLarty, and J. J. Wortman, "Low-frequency noise characterization of n- and p-MOSFET's with ultrathin oxynitride gate films," *IEEE Electron Device Lett.*, vol. 17, pp. 395-397, 1996.

[203] M. Da Rold, E. Simoen, S. Mertens, M. Schaekers, G. Badenes, and S. Decoutere, "Impact of gate oxide nitridation process on 1/f noise in 0.18 μm CMOS," *Microelectron. Reliab.*, vol. 41, pp. 1933-1938, 2001.

[204] M. Marin, J. C. Vildeuil, B. Tavel, B. Duriez, F. Arnaud, P. Stolk, and M. Woo, "Can 1/*f* noise in MOSFETs be reduced by gate oxide and channel optimization?," in *Proc. Int. Conf. Noise and Fluctuations (ICNF)*, 2005, pp. 195-198.

[205] J. Lee and G. Bosman, "Comprehensive noise performance of ultrathin oxide MOSFETs at low frequencies," *Solid-State Electron.*, vol. 48, pp. 61-71, 2004.

[206] J. Lee and G. Bosman, "Defect spectroscopy using $1/f^{\gamma}$ noise of gate leakage current in ultrathin oxide MOSFETs," *Solid-State Electron.*, vol. 47, pp. 1973-1981, 2003.

[207] J. Lee, G. Bosman, K. R. Green, and D. Ladwig, "Model and analysis of gate leakage current in ultrathin nitrided oxide MOSFETs," *IEEE Trans. Electron Devices*, vol. 49, pp. 1232-1241, 2002.

[208] J. Lee, G. Bosman, K. R. Green, and D. Ladwig, "Noise model of gate-leakage current in ultrathin oxide MOSFETs," *IEEE Trans. Electron Devices*, vol. 50, pp. 2499-2506, 2003.

[209] M. Sandén, O. Marinov, M. J. Deen, and M. Östling, "A new model for the low-frequency noise and the noise level variation in polysilicon emitter BJTs," *IEEE Trans. Electron Devices*, vol. 49, pp. 514-520, 2002.

[210] C. Claeys, A. Mercha, and E. Simoen, "Low-frequency noise assessment for deep submicrometer CMOS technology nodes," *J. Electrochem. Soc.*, vol. 151, pp. G307-G318, 2004.

[211] T. Tsuchiya, T. Matsuura, and J. Murota, "Low-Frequency Noise in $Si_{1-x}Ge_x$ p-Channel Metal Oxide Semiconductor Field-Effect Transistors," *Jpn. J. Appl. Phys. Part I*, vol. 40, pp. 5290-5293, 2001.

[212] P. W. Li, W. M. Liao, C. C. Shih, T. S. Kuo, L. S. Lai, Y. T. Tseng, and M. J. Tsai, "High performance Si/SiGe heterostructure MOSFETs for low power analog circuit applications," *Solid-State Electron.*, vol. 47, pp. 1095-1098, 2003.

[213] G. Ghibaudo and J. Chroboczek, "On the origin of the LF noise in Si/Ge MOSFETs," *Solid-State Electron.*, vol. 46, pp. 393-398, 2002.

[214] M. J. Prest, A. R. Bacon, D. J. F. Fulgoni, T. J. Grasby, E. H. C. Parker, T. E. Whall, and A. M. Waite, "Low-frequency noise mechanisms in Si and pseudomorphic SiGe p-channel field-effect transistors," *Appl. Phys. Lett.*, vol. 85, pp. 6019-6021, 2004.

[215] M. Myronov, O. A. Mironov, S. Durov, T. E. Whall, E. H. C. Parker, T. Hackbarth, G. Höck, H.-J. Herzog, and U. König, "Reduced 1/*f* noise in p-$Si_{0.3}Ge_{0.7}$ metamorphic metal-oxide-semiconductor field-effect transistor," *Appl. Phys. Lett.*, vol. 84, pp. 610-612, 2004.

[216] M. H. Lee, P. S. Chen, W.-C. Hua, C.-Y. Yu, Y. T. Tseng, S. Maikap, Y. M. Hsu, C. W. Liu, S. C. Lu, W.-Y. Hsieh, and M.-J. Tsai, "Comprehensive low-frequency and RF noise characteristics in strained-Si NMOSFETs," in *IEDM Tech. Dig.*, 2003, pp. 69-72.

[217] W.-C. Hua, M. H. Lee, L. P. S. Chen, S. Maikap, C. W. Liu, and K. M. Chen, "Ge outdiffusion effect on flicker noise in strained-Si nMOSFETs," *IEEE Electron Device Lett.*, vol. 25, pp. 693-695, 2004.

[218] M. Matloubian, F. Scholz, and L. Lum, "Low frequency noise in fully depleted SOI PMOSFET's," *IEEE Trans. Electron Devices*, vol. 41, pp. 1977-1980, 1994.

[219] N. Lukyanchikova, M. Petrichuk, N. Garbar, E. Simoen, and C. Claeys, "Back and front interface related generation-recombination noise in buried-channel SOI pMOSFETs," *IEEE Trans. Electron Devices*, vol. 43, pp. 417-423, 1996.

[220] Y.-C. Tseng, W. M. Huang, M. Mendicino, D. J. Monk, P. J. Welch, and J. C. S. Woo, "Comprehensive study on low-frequency noise characteristics in surface channel SOI CMOSFETs and device design optimization for RF ICs," *IEEE Trans. Electron Devices*, vol. 48, pp. 1428-1437, 2001.

[221] A. Mercha, E. Simoen, H. van Meer, and C. Claeys, "Low-frequency noise overshoot in ultrathin gate oxide silicon-on-insulator metal-oxide-semiconductor field-effect-transistors," *Appl. Phys. Lett.*, vol. 82, pp. 1790-1792, 2003.

[222] J.-P. Colinge, "Conduction mechanisms in thin-film accumulation-mode SOI p-channel MOSFET's," *IEEE Trans. Electron Devices*, vol. 37, pp. 718-723, 1990.

[223] Web-based simulation tool, http://www.nanohub.org

[224] J. Seger, P.-E. Hellström, J. Lu, B. G. Malm, M. von Haartman, M. Östling, and S.-L. Zhang, "Lateral encroachment of Ni-silicides in the source/drain regions on ultrathin silicon-on-insulator," *Appl. Phys. Lett.*, vol. 86, 253507, 2005.

[225] E. Simoen, A. Mercha, L. Pantisano, C. Claeys, and E. Young, "Tunneling 1/*f*$^{\gamma}$ noise in 5 nm HfO_2/2.1 nm SiO_2 gate stack n-MOSFETs," *Solid-State Electron.*, vol. 49, pp. 702-707, 2005.

[226] C. Claeys, E. Simoen, A. Mercha, L. Pantisano, and E. Young, "Low-frequency noise performance of HfO_2-based gate stacks," *J. Electrochem. Soc.*, vol. 152, pp. F115-F123, 2005.

[227] H .Yu, Y.-T. Hou, M.-F. Li, and D.-L. Kwong, "Investigation of hole-tunneling current through ultrathin oxynitride/oxide stack gate dielectrics in p-MOSFETs," *IEEE Trans. Electron Devices*, vol. 49, pp. 1158-1164, 2002.

[228] H.-H. Tseng, C. C. Capasso, J. K. Schaeffer, E. A. Hebert, P. J. Tobin, D. C. Gilmer, D. Triyoso, M. E. Ramón, S. Kalpat, E. Luckowski, W. J. Taylor, Y. Jeon, O. Adetutu, R. I. Hedge, R. Noble, M. Jahanbani, C. El-Chemali, and B.White, "Improved short channel device characteristics with stress relieved pre-oxide (SRPO)

and a novel tantalum carbon alloy metal gate/HfO_2 stack," in *IEDM Tech. Dig.*, 2004, pp. 821-824.

[229] D. Wu, J. Lu, H. H. Radamson, P.-E. Hellström, S.-L. Zhang, M. Östling, E. Vainonen-Ahlgren, E. Tois, and M. Tuominen, "Influence of surface treatment prior to ALD high-κ dielectrics on the performance of SiGe surface-channel pMOSFETs," *IEEE Electron Device Lett.*, vol. 25, pp. 289-291, 2004.

[230] D. Wu, M. von Haartman, J. Seger, E. Tois, M. Tuominen, P.-E. Hellström, M. Östling, and S.-L. Zhang, "Ni-salicided CMOS with a poly-SiGe/Al_2O_3/HfO_2/Al_2O_3 gate stack," *Microelectron. Eng.*, vol. 77, pp. 36-41, 2005.

[231] M. Sandén, B. Gunnar Malm, J. V. Grahn, and M. Östling, "Decreased low-frequency noise by hydrogen passivation of polysilicon emitter bipolar transistors," *Microelectron. Reliab.*, vol. 40, pp. 1863-1867, 2000.

[232] E. P. Gusev, C. Cabral Jr., B. P. Linder, Y. H. Kim, K. Maitra, E. Cartier, H. Nayfeh, R. Amos, G. Biery, N. Bojarczuk, A. Callegari, R. Carruthers, S. A. Cohen, M. Copel, S. Fang, M. Frank, S. Guha, M. Gribelyuk, P. Jamison, R. Jammy, M. Ieong, J. Kedzierski, P. Kozlowski, V. Ku, D. Lacey, D. LaTulipe, V. Narayanan, H. Ng, P. Nguyen, J. Newbury, V. Paruchuri, R. Rengarajan, G. Shahidi, A. Steegen, M. Steen, S. Zafar, and Y. Zhang, "Advanced gate stacks with fully silicided (FUSI) gates and high-κ dielectrics: Enhanced performance at reduced gate leakage," in *IEDM Tech. Dig.*, 2004, pp. 79-82.

[233] X. Yu, C. Zhu, M. F. Li, A. Chin, M. B. Yu, A. Y. Du, and D.-L. Kwong, "Mobility enhancement in TaN metal-gate MOSFETs using tantalum incorporated HfO_2 gate dielectric," *IEEE Electron Device Lett.*, vol. 25, pp. 501-503, 2004.

[234] D. Esseni, M. Mastrapasqua, C. Fiegna, G. K. Keller, L. Selmi, and E. Sangiorgi, "An experimental study of low-field electron mobility in double-gate ultra-thin SOI MOSFETs," in *IEDM Tech. Dig.*, 2001, pp. 445-448.

[235] E. Simoen, U. Magnusson, and C. Claeys, "A low-frequency noise study of gate-all-around SOI transistors," *IEEE Trans. Electron Devices*, vol. 40, pp. 2054-2059, 1993.

[236] B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C.-Y. Yang, C. Tabery, C. Ho, Q. Xiang, T.-J. King, J. Bokor, C. Hu, M.-R. Lin, and D. Kyser, "FinFET scaling to 10nm gate length," in *IEDM Tech. Dig.*, 2002, pp. 251-254.

[237] H. S. Momose, T. Ohguro, K. Kojima, S.-I. Nakamura, and Y. Toyoshima, "1.5-nm gate oxide CMOS on (110) surface-oriented Si substrate," *IEEE Trans. Electron Devices*, vol. 50, pp. 1001-1008, 2003.

[238] J.-S. Lee, Y.-K. Choi, D. Ha, T.-J. King, and J. Bokor, "Low-frequency noise characteristics in p-channel FinFETs," *IEEE Electron Device Lett.*, vol. 23, pp. 722-724, 2002.

[239] T. Tezuka, S. Nakaharai, Y. Moriyama, N. Sugiyama, and S. Takagi, "High-mobility strained SiGe-on-insulator pMOSFETs with Ge-rich surface channels fabricated by local condensation technique," *IEEE Electron Device Lett.*, vol. 26, pp. 243-245, 2005.

[240] A. D. Sadovnikov, A. Nathan, and T. Manku, "Numerical simulation of transconductance in Si/SiGe p-MOSFETs," *Solid-State Electron.*, vol. 39, pp. 1199-1203, 1996.

[241] M. von Haartman, et al., *to be published*