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Low-Loss Low-Cost Substrate-Integrated Waveguide and Filter in GaAs IPD Technology for Terahertz Applications

Te-Yen Chiu[1], Student Member, IEEE, and Chun-Hsing Li[2], Senior Member, IEEE

[1]Department of Engineering and System Science, National Tsing Hua University, Hsinchu 300044, Taiwan
[2]Department of Electrical Engineering and Graduate Institute of Communication Engineering, National Taiwan University, Taipei 10617, Taiwan

Corresponding author: Chun-Hsing Li (e-mail: chunhsingli@ntu.edu.tw).

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ABSTRACT A low-loss and low-cost terahertz (THz) substrate-integrated waveguide (SIW) and a SIW filter implemented in a commercially-available GaAs integrated-passive-devices (IPD) technology are proposed for THz applications. Ellipse vias penetrating through a 100-μm thick GaAs substrate are employed to realize a low-loss SIW. The via's orientation is designed as being transverse, instead of being longitudinal, to the propagation direction of the input wave, which can improve the insertion loss by 2.7 dB at 415 GHz due to lower signal leakage from the waveguide. The proposed SIW is able to provide simulated insertion loss of only 0.39 dB/mm, i.e., 0.14 dB/λ_g, at 340 GHz. A new SIW filter structure using the ellipse vias is proposed which not only successfully realizes a low-loss fourth-order Chebyshev filter under hard design-rule-check (DRC) rules imposed by the IPD technology, but also can enhance out-of-band rejection by 10.5 dB at 390 GHz as compared with conventional waveguide filters. A slot-coupled coplanar waveguide (CPW) to SIW transition structure without any impedance tuning stub required is also proposed to measure the proposed SIW and SIW filter. The proposed transition structure can give simulated insertion loss of 0.7 dB at 340 GHz while keeping return loss better than 10 dB from 307 to 374 GHz. Eight samples are measured to demonstrate the robustness of the proposed designs against process variations. Experimental results show that the proposed transition structure with a 220-μm long SIW and the SIW filter can provide measured insertion loss of 0.7 and 3.6 dB at 327.5 GHz, respectively. The reasons for the discrepancy between the simulation and measurement results are identified and discussed in detail. As compared with prior works, the proposed SIW and SIW filter exhibit lower loss, lower cost, higher repeatability, higher reliability, and mass-producible capability. To the best of the authors' knowledge, this is the first demonstration of the THz SIW and THz SIW filter designs using a commercially-available and mass-producible IPD technology reported thus far.

INDEX TERMS Chebyshev filters, ellipse vias, filters, GaAs, integrated-passive-devices, IPD, iris, substrate-integrated waveguides, SIW, terahertz, THz.

I. INTRODUCTION

Terahertz (THz) science and technology have drawn great attention recently since they can be employed for many interesting applications, including non-invasive biomedical and medical imaging, detection of concealed weapons and explosives, and high-speed wireless data communications [1]-[5]. They are also considered as candidate technologies for the next sixth-generation (6G) wireless communications systems to supply higher than 100 Gb/s communication capability enabled by the availability of wide bandwidth at THz frequencies [6]-[9]. Using an electronic approach to realize THz systems for the aforementioned applications is especially appealing since it can provide a low-cost, low-weight, compact, high-integration, and mass-producible solution. Of building blocks in these electronic THz systems, transmission lines are critical since their characteristics directly determine the quality of the passive components, dramatically impacting the system performance. However, transmission line design at THz frequencies is challenging due to unfriendly back end of the lines (BEOL) and lossy substrates, inevitably resulting in the planar transmission lines, e.g., microstrip lines and coplanar waveguides (CPW),

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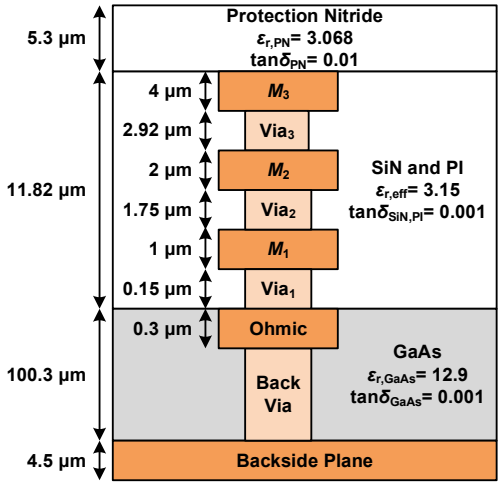

FIGURE 1. **Cross-sectional view of the BEOL of the GaAs IPD technology.**

to have high loss, low quality factors (Q), low power handling capability, and undesired coupling between nearby devices [10]. The issue becomes much more serious as the operation frequencies reach the THz band. Consequently, a low-loss THz transmission line must be developed in order to carry out high-performance electronic THz systems.

A substrate-integrated waveguide (SIW) is a good candidate to realize low-loss THz transmission lines. As compared with traditional planar transmission lines, the SIW has advantages of lower loss, higher Q, higher power handling capability, and excellent isolation between adjacent SIWs [10]. In contrast to its counterpart of metallic rectangular waveguides, the SIW is not only planer, but it can also be easily integrated with active devices, while retaining the advantages of the metallic waveguides. However, most reported SIW designs still operate below THz frequencies, i.e., below 300 GHz [11]-[28]. Few THz SIW designs were presented [29]-[33]. A thru-silicon via (TSV) technology was employed to realize a SIW operating from 150 to 300 GHz [29]. Yet the SIW shows high insertion loss of 8.3 dB/mm due to a lossy silicon substrate. Another SIW design using the TSV technology was reported to exhibit lower insertion loss of 1.5 dB at 331 GHz, but the measured results are acquired by an open-short de-embedding method, which might not be appropriate at THz frequencies [30]. Moreover, the adopted TSV technology is an in-house process, which is not only inaccessible to interested researchers, but is also lack of reliability, repeatability and mass-producible capability. On the other hand, micromachining technologies with a complicated fabrication process was proposed to realize a silicon SIW with insertion loss of 0.14 dB/λ_g at 325 GHz [31]. Nevertheless, as the same micromachining technology was exploited to realize a fifth-order filter, high insertion loss of 9.2 dB was measured at 270 GHz due to fabrication-induced underetching of the waveguide sidewalls. This might imply that the micromachining technology is still not reliable yet at

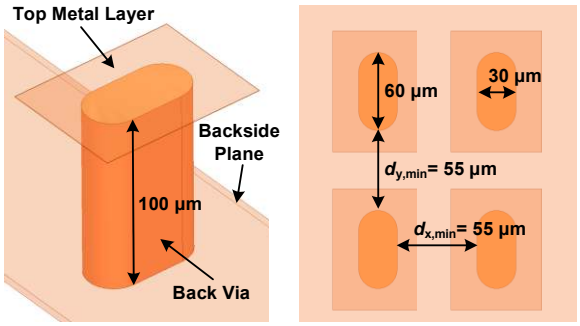

FIGURE 2. **Physical structure and size of the back vias.**

THz frequencies, resulting in large process variation. As such a high-loss filter is integrated with a THz transmitter or a receiver, it will unavoidably degrade the transmitter's output power and increase the receiver's noise figure. Alternatively, an IC organic packaging process developed at Intel Corporation was utilized to design a ridged SIW and a manifold triplexer operating from 220 to 320 GHz [32]. However, unexpected out-of-band resonances and a discrepancy of 7-dB insertion loss between simulation and measurement are observed in measured results due to the variation of dielectric properties and perturbations of device dimensions. Such a high-loss and high-variation SIW might implicitly explain that the organic process is still not ready for THz applications. A low-cost 130-nm CMOS technology was also attempted to implement a T-folded SIW (TFSIW) [33]. The TFSIW achieved simulated insertion loss of 1 dB/mm at 340 GHz, higher than that of 0.7 dB/mm of a conventional grounded CPW realized in the same CMOS technology. Thus, the CMOS technology may not be a good alternative to implement low-loss THz SIWs.

In this paper, a low-cost and low-loss THz SIW and a SIW filter which can solve aforementioned issues are proposed using a commercially-available GaAs integrated-passive-devices (IPD) technology from WIN Semiconductors Corporation. Ellipse vias penetrating through a 100-μm thick GaAs substrate are employed to realize a low-loss SIW. The via's orientation deployed as being transverse, instead of being longitudinal, to the propagation direction of the incident wave, can improve the insertion loss by 2.7 dB at 415 GHz. The proposed SIW is able to provide simulated insertion loss of 0.39 dB/mm, i.e., 0.14 dB/λ_g, at 340 GHz. A new SIW filter structure using the ellipse vias is proposed, which not only realizes a low-loss Chebyshev SIW filter under hard design-rule-check (DRC) rules imposed by the IPD technology, but it can also enhance out-of-band rejection by 10.5 dB at 390 GHz as compared with conventional waveguide filters. A slot-coupled CPW-to-SIW transition structure without any impedance tuning stub required is also proposed in order to measure the proposed SIW and SIW filter using an on-wafer measurement setup. The proposed transition structure can show simulated insertion loss of 0.7 dB at 340 GHz while keeping $|S_{11}|$ below -10 dB from 307 to 374 GHz. Measurement results indicate

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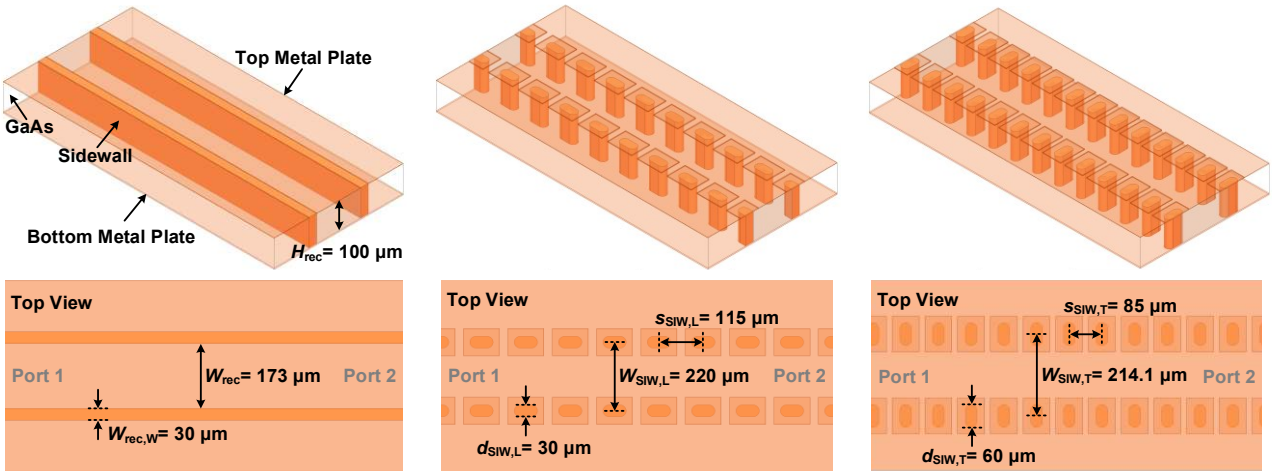

FIGURE 3. **(a) Rectangular waveguide in the GaAs IPD technology. (b) Proposed SIW with longitudinal vias. (c) Proposed SIW with transverse vias.**

that the proposed transition structure with a 220-μm long SIW and the SIW filter including a 240-μm long SIW can give a measured insertion loss of 0.7 and 3.6 dB, respectively, at 327.5 GHz. Moreover, the reasons for the discrepancy between simulation and measurement are identified and discussed in detail. As compared with previous works, the proposed SIW and SIW filter exhibit lower cost, lower loss, higher reliability, higher repeatability, and mass-producible capability. To the best of the authors' knowledge, this is the first demonstration of the THz SIW and SIW filter designs using a commercially-available and mass-producible IPD technology reported thus far. This paper is organized as follows. Section II explains the GaAs IPD technology and SIW design. The fourth-order Chebyshev SIW filter design is presented in Section III. A characterization method for measuring the proposed SIW and SIW filter is described in Section IV. Section V illustrates experimental results. Finally, Section VI concludes this work.

II. GaAs IPD TECHNOLOGY AND SIW DESIGN

A. GaAs IPD TECHNOLOGY

The GaAs IPD technology provided by the WIN Semiconductors Corporation has the advantages of low cost, low loss, high reliability, high repeatability, and mass-producible capability. Moreover, it can work quit well even at THz frequencies. Fig. 1 shows the cross-sectional view of the BEOL of the GaAs IPD technology which will be employed to realize the proposed SIW and SIW filter. Four metal layers, i.e., M_1, M_2, M_3, and Ohmic, with dielectric materials of SiN and polyimide (PI) in between are available and back vias can be utilized to connect these metal layers to a backside plane. All the metal layers have conductivity (σ) of 4.1×10^7 S/m except for the ohmic layer with higher σ of 6.61×10^7 S/m. The substrate is formed by a 100-μm thick GaAs material with dielectric loss tangent ($\tan\delta$) of only 0.001. Such a low-loss substrate can greatly reduce the substrate loss, making low-loss transmission lines feasible at THz frequencies. Moreover, the SIW size can be reduced due to a higher dielectric constant $\varepsilon_{r,GaAs}$ of 12.9 as compared to that with an air core. Note that $\tan\delta_{GaAs}$ of 0.001 and $\varepsilon_{r,GaAs}$ of 12.9 are given by the foundry. It will be shown later that $\tan\delta_{GaAs}$ and $\varepsilon_{r,GaAs}$ should be modified to 0.0077 and 12.3, respectively, in order to make the simulated results fit the measured ones. The back vias with a physical structure as shown in Fig. 2 are crucial for the SIW design. The top and bottom metal layers of the vias are formed by $M_{1\text{-}3}$ and Ohmic and the backside plane, respectively. The via shape is ellipse. Two ends of the via as looked from the top view have a shape of a semi-circle with a radius of 15 μm. The via size is 30 μm × 60 μm with a height of 100 μm. Despite many advantages offered by the IPD technology, the hard DRC rules imposed by it must be complied. As depicted in Fig. 2, the minimum distance, $d_{x,min}$ and $d_{y,min}$, between two vias must be longer than 55 and 55 μm along the x and y directions, respectively. Furthermore, other dimension and shape of the vias are not allowed due to violation of the DRC rules, that is, if many vias are required in a design, for instance, four vias as shown in Fig. 2, they must be laid out in a discrete way. Therefore, great attention shall be paid as the back vias are used to design SIWs and SIW filters under DRC constraints. Note that the IPD technology can be employed to realize a low-loss SIW at THz frequencies while a conventional printed-circuit board (PCB) technology cannot make it. For the conventional PCB technology whose vias are formed by mechanically cutting and plating the inner cylindrical wall with copper, the minimum diameter of the via hole is around 0.2 mm with tolerance of ±0.075 mm and the minimum center-to-center distance between two via holes is around 0.5 mm. Such a large via size and via-to-via distance are not able to realize a low-loss SIW at THz frequencies since the vias cannot satisfy the conditions of $p/\lambda_c < 0.25$ and $p \leq 2d$, where p, λ_c, and d are the pitch between adjacent via holes, the wavelength in the substrate, and the diameter of the via holes, respectively [34]. Moreover, the via hole tolerance of ± 0.075 mm corresponding to $\pm(0.075/0.2)\times100\% = \pm37.5\%$ variation also causes the devices using the vias to exhibit large performance variation.

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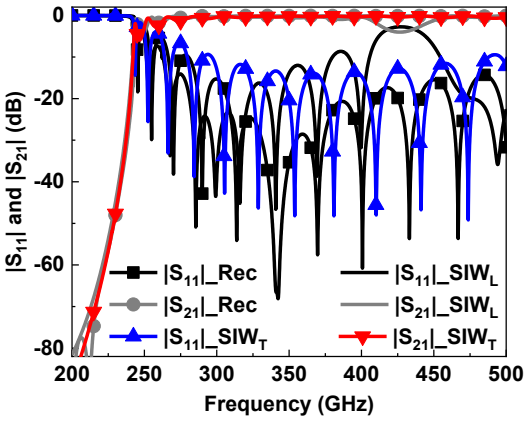
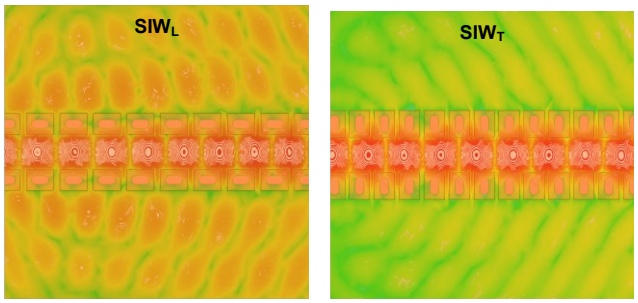
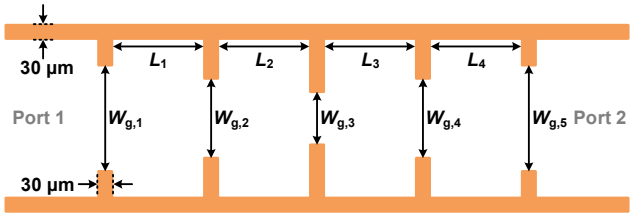


(a)



(b)

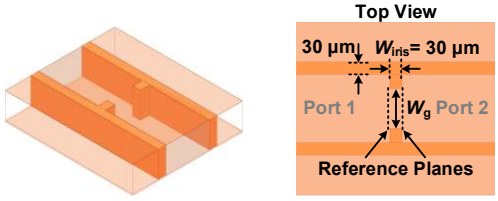
FIGURE 4. **(a) Simulated $|S_{11}|$ and $|S_{21}|$ of the rectangular waveguide, SIW_L, and SIW_T. (b) Simulated electric field distribution of SIW_L and SIW_T at 415 GHz.**



Parameter	L_1	L_2	L_3	L_4
Value (μm)	107.4	126.7	126.7	107.4

Parameter	$W_{g,1}$	$W_{g,2}$	$W_{g,3}$	$W_{g,4}$	$W_{g,5}$
Value (μm)	123.7	102.7	96.5	102.7	123.7

(a)



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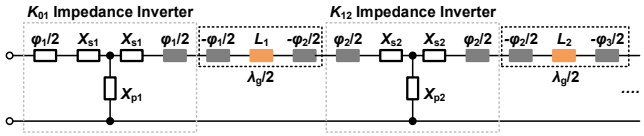

(c)

FIGURE 5. **(a) Physical structure of the ideal fourth-order Chebyshev waveguide filter. (b) EM simulation setup for the inductive iris to extract X_p and X_s values. (c) Equivalent circuit model of the ideal filter.**

B. IPD SIW DESIGN

A low-loss and compact SIW is designed using the GaAs IPD technology. A rectangular waveguide will be designed first and then converted to the SIW later. Fig. 3(a) shows a rectangular waveguide design using the IPD technology where M_1 and backside plane metal layers are utilized to form the top and bottom plates, respectively. Moreover, it is assumed that a solid and continuous sidewall with thickness $W_{rec,W}$ of 30 μm is available. The waveguide needs to provide single-mode operation covering the interested frequency range from 320 to 360 GHz. The analytic equation for finding the cutoff frequencies of the rectangular waveguide can be derived as

$$f_{c,mn} = \frac{1}{2\pi\sqrt{\mu\varepsilon}}\sqrt{\left(\frac{m\pi}{W_{rec}}\right)^2 + \sqrt{\left(\frac{n\pi}{H_{rec}}\right)^2}}, \qquad (1)$$

where m and n are integers and W_{rec} and H_{rec} are the width and height of the rectangular waveguide, respectively. The first and second modes are TE_{10} and TE_{01}, respectively, since W_{rec} is larger than H_{rec}. As H_{rec} is fixed equal to the substrate thickness of 100 μm, only W_{rec} can be freely adjusted to design the waveguide. In this work, W_{rec} is designed as 173 μm to have TE_{10} and TE_{01} modes started at 242 and 415 GHz, respectively, which covers the interested band from 320 to 360 GHz. Once the design of the rectangular waveguide is completed, its physical dimensions are converted to those of the SIW by using the following empirical conversion equation

$$W_{rec} = W_{SIW} - 1.08\frac{d_{SIW}^2}{s_{SIW}} + 0.1\frac{d_{SIW}^2}{W_{SIW}}, \qquad (2)$$

where W_{rec}, d_{SIW}, W_{SIW}, and s_{SIW} are the width of the rectangular waveguide, diameter of the metal vias, transverse center-to-center distance of the vias, and the longitudinal center-to-center spacing of the vias, respectively [35]. Note that (2) is valid if the via shape is circle. However, the vias in the GaAs IPD technology are ellipse, implying that d_{SIW} used in (2) can have a possible value between 30 to 60 μm. Hence the design values obtained from (2) are only initial ones and have to be modified later according to 3D electromagnetic (EM) simulation results. The non-circle shape of the vias also makes the SIW design to have two different layout orientations. As shown in Fig. 3(b), the first one is that the vias are orientated as being longitudinal to the propagation direction of the input wave, designated as SIW_L. Instead, as depicted in Fig. 3(c), the other is deployed as being transverse, designated as SIW_T. The center-to-center spacing between vias of $s_{SIW,L}$ and $s_{SIW,T}$ is designed as 115

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and 85 μm, respectively, which is the minimum value allowed by the DRC rules. $d_{SIW,L}$ and $d_{SIW,T}$ are assigned as 30 and 60 μm, respectively, equal to the width of the ellipse via along the transverse direction. Once $s_{SIW,L,T}$ and $d_{SIW,L,T}$ are known, $W_{SIW,L}$ and $W_{SIW,T}$ can be found to be 181 and 217.1 μm by (2), respectively. Next EM simulations using ANSYS HFSS are conducted to adjust $W_{SIW,L}$ and $W_{SIW,T}$ from 181 and 217.1 μm to 220 and 214.1 μm, respectively, ensuring SIW_L and SIW_T to have the same cutoff frequencies as those of the rectangular waveguide, i.e., 242 and 415 GHz. It is interesting to see that (2) is not able to predict the required $W_{SIW,L}$ accurately since the via shape is ellipse instead of being circle.

Fig. 4(a) shows the simulated $|S_{11}|$ and $|S_{21}|$ of the rectangular waveguide, SIW_L, and SIW_T as the length is around 1 mm. $|S_{22}|$ and $|S_{12}|$ are not illustrated since they are identical to $|S_{11}|$ and $|S_{21}|$, respectively. Three waveguide designs show similar frequency responses, which verifies the aforementioned design flows. The insertion loss of SIW_L and SIW_T is 0.3 and 0.4 dB, respectively, at 340 GHz. However, it is noticed that SIW_L exhibits higher insertion loss than that of SIW_T as the operation frequency is higher than 345 GHz. The insertion loss reaches a maximal difference of 2.7 dB between SIW_L and SIW_T at 415 GHz, i.e., the end frequency of the mono-mode operation band from 242 to 415 GHz. To investigate the reason for the loss difference, the electric-field distribution of SIW_L and SIW_T is simulated at 415 GHz and log-plotted in Fig. 4(b) where 200 divisions are taken between 2×10^5 to 1×10^{-1} V/m. Obviously SIW_L has much more signal leakage from the waveguide due to shorter via length along the waveguide's transverse direction in comparison to SIW_T. Consequently, the layout structure of SIW_T shall be chosen in order to realize a low-loss THz SIW in the GaAs IPD technology.

III. CHEBYSHEV SIW FILTER DESIGN

The GaAs IPD technology with the ellipse vias is employed to realize a fourth-order Chebyshev SIW filter. The design flow of the SIW filter is the same as that of the SIW. An ideal waveguide filter is firstly designed assuming that a solid and continuous sidewall with thickness equal to the width of the ellipse via of 30 μm is available. The design is then converted to the SIW filter with the ellipse vias later. Fig. 5(a) shows the ideal SIW filter which consists of four SIWs with length of L_m and five inductive irises with gap width of $W_{g,n}$ where m and n are integers ranging from 1 to 4 and 1 to 5, respectively. The inductive iris can be modeled as a T-network which composes of two series inductances represented as X_s and a shunt inductance represented as X_p. The relationship between X_s and X_p and the iris gap width can be obtained by using EM simulations with a setup illustrated in Fig. 5(b). The input and output wave ports are de-embedded exactly before the iris structure to obtain a two-port S-parameter matrix of the iris only. The iris width W_{iris} is assumed equal to the width of the ellipse via of 30 μm. With the iris' S-parameter matrix, X_s and X_p can be extracted by [36]

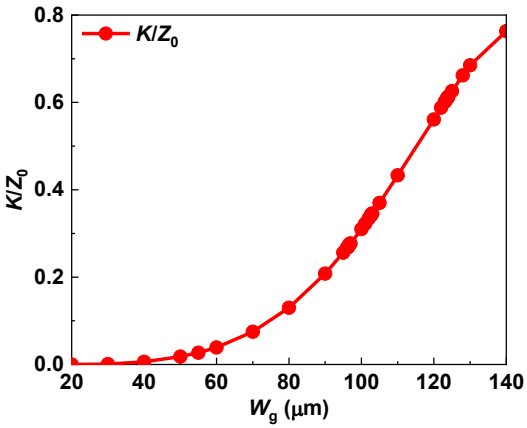

FIGURE 6. Simulated dependence of K/Z_0 on the iris gap width W_g.

$$j\frac{X_s}{Z_0}=\frac{1-S_{12}+S_{11}}{1-S_{11}+S_{12}}, \tag{3}$$

$$j\frac{X_p}{Z_0}=\frac{2S_{12}}{(1-S_{11})^2-S_{12}^2}. \tag{4}$$

As each inductive iris is replaced by the equivalent T-network, an equivalent circuit model for the ideal SIW filter can be established as shown in Fig. 5(c) where additional transmission line sections of $\varphi_n/2$ are intentionally added on each side of the iris' T-network. With this special arrangement, the T-network with $\varphi/2$ on each side forms a K-impedance inverter where the constant K is related to φ, X_s, and X_p by

$$\frac{K}{Z_0}=\left|\tan\left(\frac{\varphi}{2}+\arctan\frac{X_s}{Z_0}\right)\right|, \tag{5}$$

$$\varphi=-\arctan\left(2\frac{X_p}{Z_0}+\frac{X_s}{Z_0}\right)-\arctan\left(\frac{X_s}{Z_0}\right), \tag{6}$$

and Z_0 is the characteristic impedance of the SIW while the three transmission lines, L_m, $-\varphi_m/2$, and $-\varphi_{m+1}/2$, together effectively work as a half-wavelength resonator, that is

$$L_m=\frac{\lambda_g}{2\pi}\left[\pi+\frac{1}{2}(\varphi_m+\varphi_{m+1})\right], \tag{7}$$

where λ_g is the wavelength at the center frequency f_o of the filter [36]. Therefore, the equivalent circuit shown in Fig. 5(c) can be considered as four half-wavelength transmission line resonators coupled by five K-impedance inverters, which is exactly identical to an impedance inverter model for a Chebyshev filter design. Therefore, the impedance inverter constants $K_{n,n+1}$ of each section can be found by (8)-(10) using the lumped low-pass elements where Δ is defined in (11) [36].

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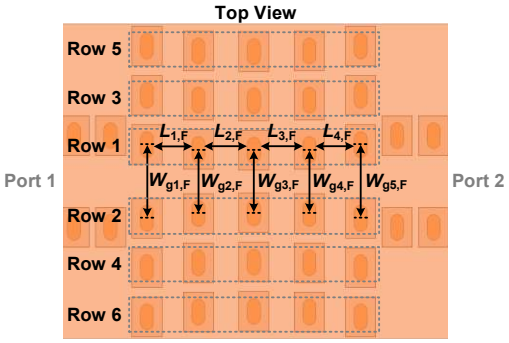
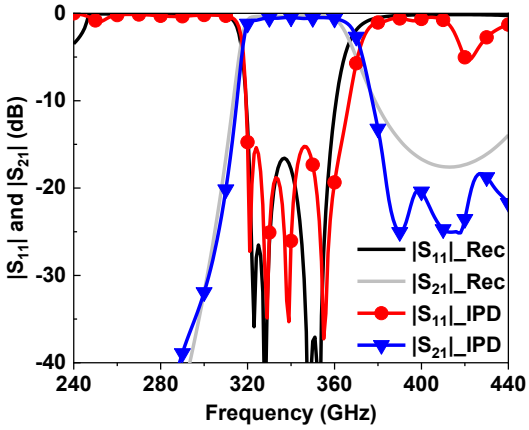


Parameter	$L_{1,f}$	$L_{2,f}$	$L_{3,f}$	$L_{4,f}$
Initial Value (μm)	107.4	126.7	126.7	107.4
Design Value (μm)	89.5	99.5	99.5	89.5

Parameter	$W_{g1,f}$	$W_{g2,f}$	$W_{g3,f}$	$W_{g4,f}$	$W_{g5,f}$
Initial Value (μm)	167.3	146	139.7	146	167.3
Design Value (μm)	172	149.5	146	149.5	172

(a)



(b)

FIGURE 7. **(a) Proposed SIW filter. (b) Simulated $|S_{11}|$ and $|S_{21}|$ of the ideal waveguide filter and the proposed SIW filter.**

$$\frac{K_{01}}{Z_0}=\sqrt{\frac{\pi\Delta}{2g_0g_1}}, \tag{8}$$

$$\frac{K_{j,j+1}}{Z_0}=\frac{\pi\Delta}{2\sqrt{g_jg_{j+1}}}, \tag{9}$$

$$\frac{K_{N,N+1}}{Z_0}=\sqrt{\frac{\pi\Delta}{2g_Ng_{N+1}}}, \tag{10}$$

$$\Delta=\frac{\lambda_{g1}-\lambda_{g2}}{\lambda_{g0}}. \tag{11}$$

In this work, the proposed filter aims to provide 16-dB return loss corresponding to in-band ripple of 0.1 dB while possessing 40-GHz bandwidth at f_o of 340 GHz. Given the filter specs, the low-pass element values of g_0, g_1, g_2, g_3, g_4, and g_5 can be known as 1, 1.1088, 1.3061, 1.7703, 0.818, and

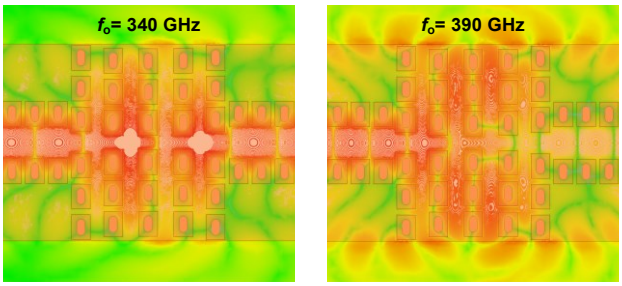


FIGURE 8. **Simulated electrical field distribution of the proposed SIW filter at 340 and 390 GHz, respectively.**

1.3554, respectively. With f_o of 340 GHz and bandwidth of 40 GHz, Δ is found to be 0.25306 by (11). Accordingly, the required values of K_{01}/Z_0, K_{12}/Z_0, K_{23}/Z_0, K_{34}/Z_0, and K_{45}/Z_0 can be obtained as 0.599, 0.33, 0.261, 0.33, and 0.599 by (8)-(10), respectively. Next, the gap width W_g of each iris is designed to meet the required K/Z_0 values. As mentioned before, X_p and X_s under different W_g values can be extracted by using the EM simulation setup as shown in Fig. 5(b). The dependence of K/Z_0 on W_g can be grabbed by (3)-(6) as interpreted in Fig. 6. Therefore, W_{g1}, W_{g2}, W_{g3}, W_{g4}, and W_{g5} for K_{01}/Z_0, K_{12}/Z_0, K_{23}/Z_0, K_{34}/Z_0, and K_{45}/Z_0 of 0.599, 0.33, 0.261, 0.33, and 0.599 can be designed as 123.7, 102.7, 96.5, 102.7, and 123.7 μm, respectively. Moreover, φ_m of each iris is also acquired from (6) during the process of finding the dependence of K/Z_0 on W_g. Accordingly, L_1, L_2, L_3, and L_4, can be found as 107.4, 126.7, 126.7, and 107.4 μm, respectively, by (7). The design values of $W_{g,n}$ and L_m are also summarized in Fig. 5(a). Once the design of the ideal waveguide filter is completed, it is ready to be converted to a SIW filter in the GaAs IPD technology which uses ellipse vias to realize the inductive iris.

Due to the limitation of the ellipse via shape and DRC rules imposed by the GaAs IPD technology, the layout of the SIW filter must be carefully deployed. A new SIW filter structure is proposed as shown in Fig. 7(a). The via rows of Row 1 and 2 are employed to realize each inductive iris. The transverse center-to-center distances between the vias in Row 1 and 2, designated as $W_{g1\text{-}g5,F}$, are initially set to be revised values of $W_{g1\text{-}g5}$ after being corrected by (2), that is, $W_{g1,F}$, $W_{g2,F}$, $W_{g3,F}$, $W_{g4,F}$, and $W_{g5,F}$ are equal to the revised value of 172, 149.5, 146, 149.5, and 172 μm, respectively. In contrast, the longitudinal distances between the vias, designated as $L_{1\text{-}4,F}$, are originally set equal to $L_{1\text{-}5}$ without modifications, that is, $L_{1,F}$, $L_{2,F}$, $L_{3,F}$, and $L_{4,F}$ are initially equal to 107.4, 126.7, 126.7, and 107.4 μm, respectively. The vias rows of Row 3 and 4 arranged as parallel to Row 1 and 2 are exploited to form the sidewalls to realize the filter resonator sections. Additional Row 5 and 6 are further added to decrease signal leakage from the waveguide, which can improve the insertion loss by 0.5 dB. Moreover, the proposed SIW filter is able to provide better out-of-band rejection capability without adding any additional filtering elements in comparison to conventional waveguide filters. As the operation frequency is within the filter bandwidth, the vias in Row 3, 4, 5, and 6 work appropriately as sidewalls to

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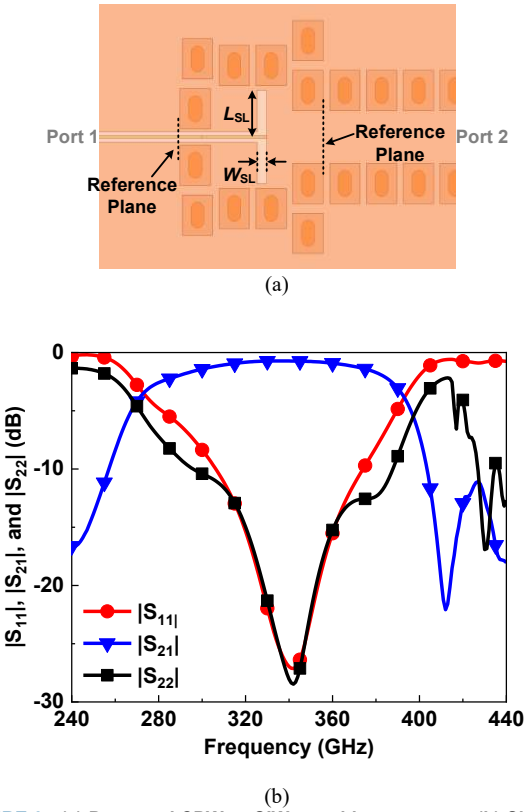

FIGURE 9. (a) Proposed CPW-to-SIW transition structure. (b) Simulated $|S_{11}|$ and $|S_{21}|$ of the proposed CPW-to-SIW transition structure.

realize the SIW resonators while simultaneously preventing in-band signals from leaking from the waveguide. In contrast, as the operation frequency is higher than the filter bandwidth, these undesired out-of-band signals are allowed to escape from the waveguide through the gaps between the vias in Row 3, 4, 5, and 6, leading to improvement of the out-of-band rejection. Finally, the EM simulator of the ANSYS HFSS is employed to adjust the initial design values of $L_{1\text{-}5,F}$ and $W_{g1\text{-}g5,F}$ to meet the filter specs. The final design values of $L_{1\text{-}5,F}$ and $W_{g1\text{-}g5,F}$ are summarized in Fig. 7(a), which are close to the initial design values. The simulated $|S_{11}|$ and $|S_{21}|$ of the proposed SIW filter are shown in Fig. 7(b). Obviously, the frequency response of the proposed SIW filter follows well with that of the ideal waveguide filter, verifying the design flows as explained above. The proposed filter can give insertion loss lower than 1.3 dB with a minimum value of 0.5 dB at 340 GHz while keeping return loss better than 10 dB from 320 to 366 GHz with a value of 26.1 dB at 340 GHz. The filter performance fulfills the required filter specs. Additionally, as mentioned before, the proposed SIW filter can provide higher out-of-band rejection by intentionally allowing the out-of-band signal to leak from the waveguide as compared with traditional waveguide filters. Fig. 7(b) shows that the proposed filter can provides maximal 10.6-dB rejection improvement at 390 GHz without needing to add any additional filtering elements. To verify the proposed out-of-band rejection mechanism, the electric filed distribution

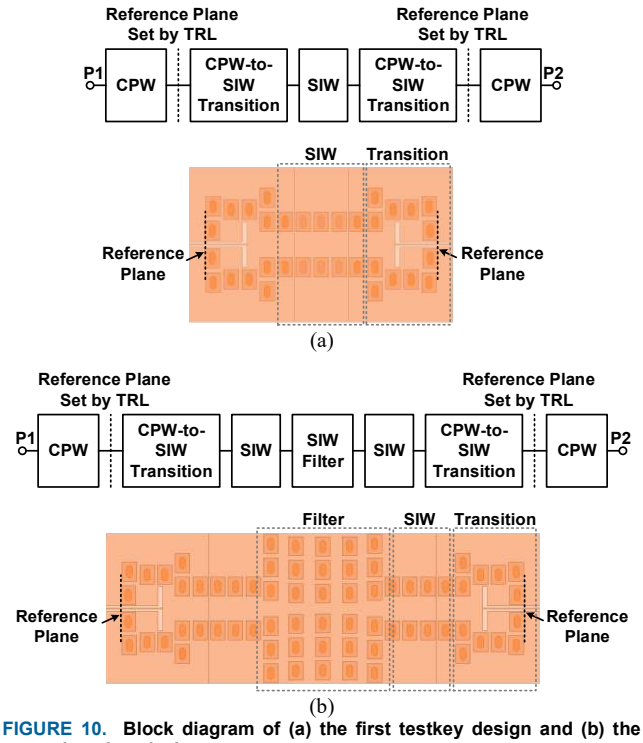

FIGURE 10. Block diagram of (a) the first testkey design and (b) the second testkey design.

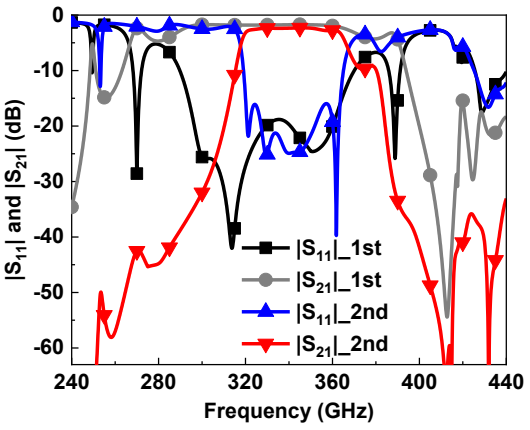

FIGURE 11. Simulated $|S_{11}|$ and $|S_{21}|$ of the first and second testkeys.

of the proposed filter is simulated at 340 and 390 GHz, respectively, as depicted in Fig. 8. The in-band signal at 340 GHz is well confined within the filter structure while a large portion of the out-of-band signal at 390 GHz is escaped from the filter. Hence less signal power at 390 GHz is transferred to the output port, resulting in the enhancement of the out-of-band rejection. Such a low-loss filter with high out-of-band rejection capability is very suitable to realize duplexers or triplexers for THz applications [28], [32].

IV. CHARACTERIZATION METHOD

To characterize the proposed SIW and SIW filter in the GaAs IPD technology using an on-wafer measurement setup, a CPW-to-SIW transition structure is a must. Fig. 9 (a) shows the proposed CPW-to-SIW transition structure by using slots

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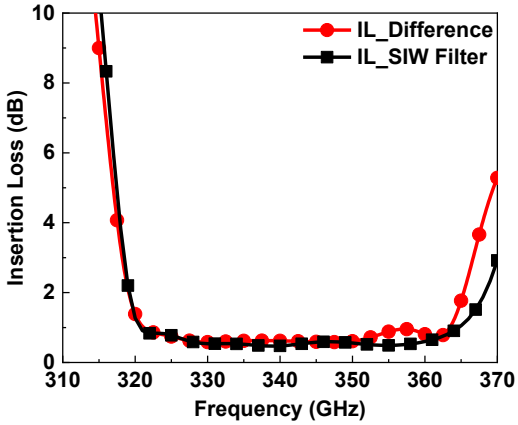
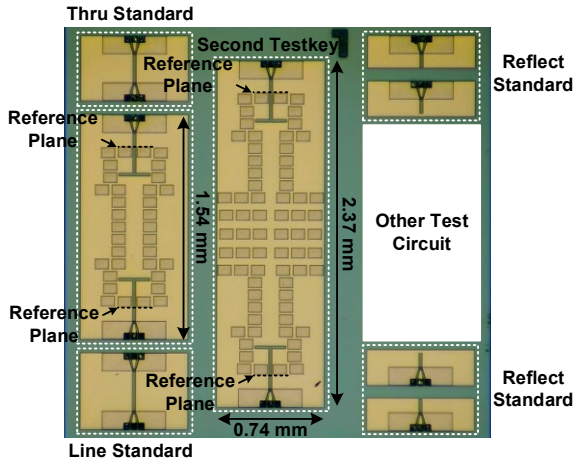
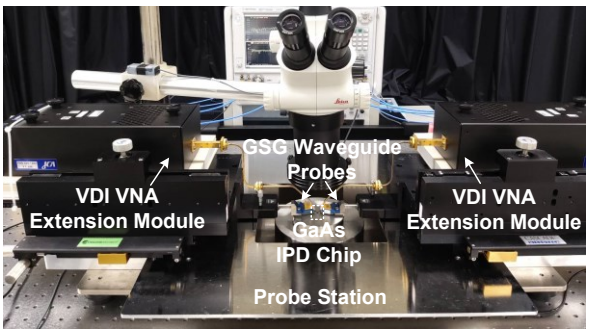


FIGURE 12. Simulated insertion loss (IL) difference of the first and second testkeys and the SIW filter IL.



(a)



(b)

FIGURE 13. (a) Chip photo of the first and second testkeys and TRL calibration standards. (b) Photo of the measurement setup.

to convert the quasi-TEM mode of the CPW to the TE_{10} mode of the SIW [37]. The length of the slot L_{SL} is designed as 107.5 μm, approximately $\lambda_g/4$ at 340 GHz. The width of the slot W_{SL} affects the real-part of the input impedance of the transition structure. W_{SL} is designed as 22 μm to match the transition input to 50 Ω at 340 GHz. As compared with the previous K_a-band design in [37], the proposed transition structure can achieve impedance matching without any additional impedance tuning stub required, thanks to fine fabrication

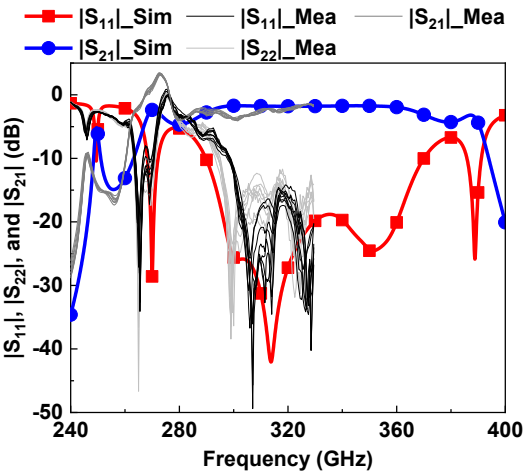


FIGURE 14. Measured S-parameters of the first testkey.

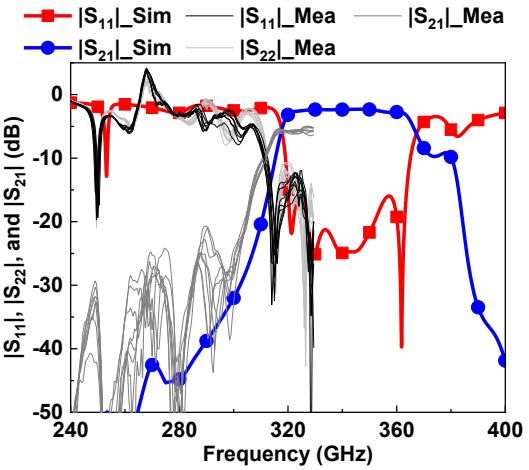


FIGURE 15. Measured S-parameters of the second testkey.

capability the IPD technology provides. A minimum slot width of 5 μm is allowed by the DRC rules in the IPD technology, which provides greater flexibility for the impedance matching design in contrast to a design using PCB technologies. Without the impedance tuning stub, the insertion loss and occupied chip area of the transition structure can all be greatly reduced. Fig. 9(b) illustrates the simulated $|S_{11}|$ and $|S_{21}|$ of the proposed CPW-to-SIW transition structure. The proposed transition structure can give insertion loss lower than 1.4 dB with a minimum value of 0.7 dB at 340 GHz while maintaining return loss better than 10 dB from 307 to 374 GHz.

With the proposed low-loss CPW-to-SIW transition structure, two testkeys as shown in Fig. 10 are designed to characterize the proposed SIW and SIW filter. The first testkey illustrated in Fig. 10(a) is composed of two CPWs, two CPW-to-SIW transition structures, and a 0.4-mm long SIW while the second one depicted in Fig. 10(b) is of two CPWs, two CPW-to-SIW transition structures, two 0.34-mm long SIWs, and a SIW filter. A thru-reflect-line (TRL) calibration technique with on-chip customized standards is utilized to move the reference plane of the S-parameters to the location exactly before the transition structures as indicated in Fig. 10, which

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simultaneously removes the undesired effects contributed by probing pads and input feeding CPWs. After TRL calibration, the insertion loss of the proposed SIW filter can be estimated by subtracting the measured insertion losses of the two testkeys at the frequencies with return loss better than 10 dB. Note that the total length of the two SIWs in the second testkey is 0.68 mm, longer than 0.44 mm of the SIW in the first testkey. The measured insertion loss of the proposed SIW filter actually includes the loss caused by the 0.24-mm long SIW.

To verify the characterization method, ANSYS HFSS is used to simulate the two testkeys. Fig. 11 shows the simulated $|S_{11}|$ and $|S_{21}|$ of the first and second testkeys. The simulated frequency response of the second testkey are equivalent to that of a SIW filter alone, verifying that the proposed CPW-to-SIW transition structure works well within the interested band. The first and second testkeys can give insertion loss lower than 3.1 and 4.1 dB with a minimum value of 1.7 and 2.4 dB at 340 GHz while maintaining return loss better than 10 dB from 290 to 370 GHz and 319 to 365 GHz, respectively. As expected, the simulated loss difference of the first and second testkeys as exhibited in Fig. 12 follows well with the simulated insertion loss of the SIW alone as shown in Fig. 7(b) from 319 to 365 GHz, confirming that the insertion loss of the SIW filter can be accurately estimated by the two designed testkeys at the frequencies with return loss better than 10 dB.

V. EXPERIMENTAL RESULTS

The proposed SIW and SIW filter are realized in the GaAs IPD technology provided by WIN Semiconductor Corporation. The chip photo of the first and second testkeys is shown in Fig. 13(a). The physical size of each testkey is also marked. As illustrated in Fig. 13(b), the measurement is conducted by an on-wafer setup where the input and output signals are applied through high-frequency ground-signal-ground (GSG) waveguide probes. A line-reflect-reflect-match (LRRM) calibration technique is employed to movie the reference plane of the measured S-parameters to the tips of the GSG probes. Subsequently, a TRL calibration technique with on-chip TRL standards is employed to move the reference plane of the S-parameters to the desired position as indicated in Fig. 13(a) while simultaneously removing undesired components of the GSG probing pads and input feeding CPWs. The measurement was conducted in a national research laboratory and was originally confirmed to have the capability of the S-parameter measurement up to 500 GHz. However, it is still having difficulties of offering an on-wafer 500-GHz S-parameter measurement. Hence, the S-parameters of the proposed SIW and SIW filter can only be characterized from 220 to 330 GHz due to the equipment limitation. However, the measured results from 220 to 330 GHz including a portion of the passband from 320 to 330 GHz can still demonstrate the proposed advantages of high reliability, high repeatability, and mass-producible capability as compared with prior works. Though the remaining portion of the passband from 330 to 360 GHz cannot be measured, it is expected to be predicted well by using the ANSYS HFSS since the proposed SIW and SIW filter are pure passive components in nature.

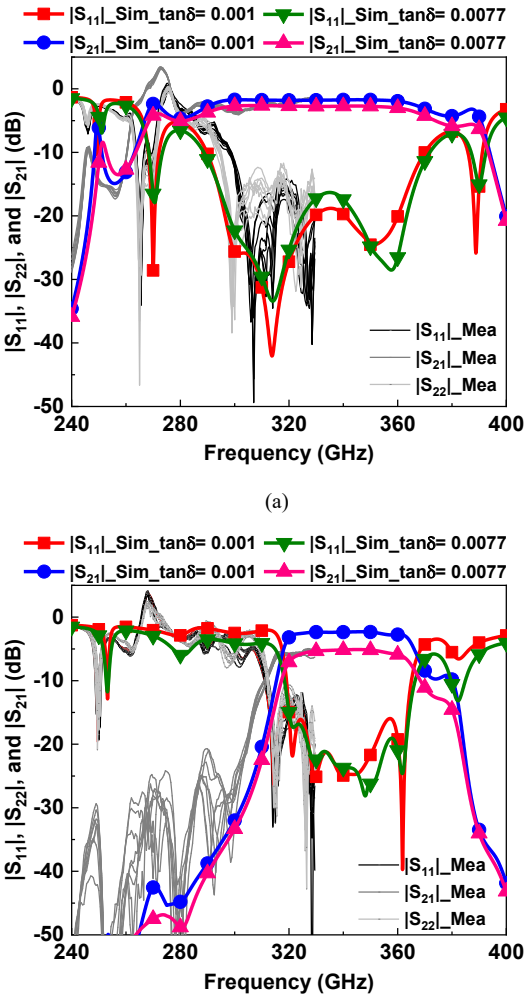

FIGURE 16. Simulated $|S_{11}|$ and $|S_{21}|$ of (a) the first testkey and (b) the second testkey as the loss tangent of the GaAs is varied from 0.001 to 0.0077.

Fig. 14 illustrates the measured S-parameters of the first testkey which composes of two CPW-to-SIW transition structures and a 0.44-mm long SIW. Eight samples are measured to demonstrate the robustness of the proposed SIW and SIW filter to the process variation using the GaAs IPD technology. The measured results track well with the simulated ones. The proposed first testkey can provide measured insertion loss lower than 3.7 dB with a minimum value of 1.5 dB at 327.5 GHz while keeping return loss better than 10 dB from 298.5 to 330 GHz. The measured loss is higher than the simulated one at some frequencies. The total insertion loss of a CPW-to-SIW transition structure and a 0.22-mm long SIW can be estimated as 1.5/2 dB, i.e., around 0.8 dB at 328.5 GHz. Fig. 15 shows the measured S-parameters of the second testkey which consists of two CPW-to-SIW transition structures, two 0.34-mm long SIWs,

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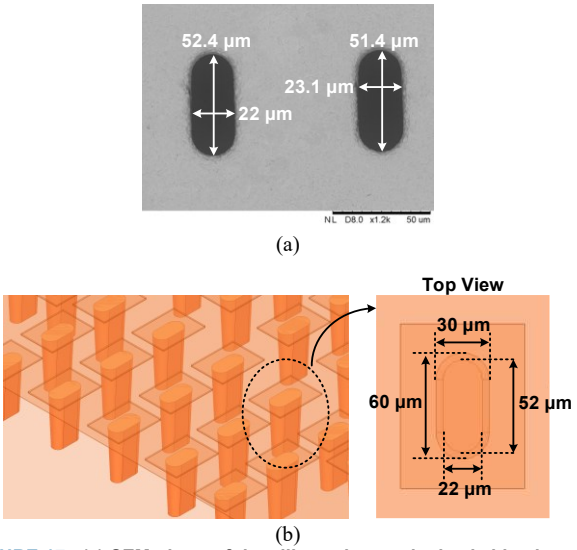

FIGURE 17. (a) SEM photo of the ellipse vias on the backside plane. (b) Modification of the via's physical structure for EM simulations.

and a SIW filter. The measured results follow well with the simulated ones. The proposed second testkey can give measured insertion loss better than 8.8 dB with a minimum value of 5.2 dB at 328.5 GHz while having $|S_{11}|$ and $|S_{22}|$ lower than -10 dB from 312.5 to 330 GHz. The measured loss is around 2.8 dB higher than the simulated one. As mentioned before, the insertion loss of the SIW filter can be estimated by subtracting the insertion loss of the first and second testkeys. Hence, the total insertion loss of the proposed filter and a 0.24-mm SIW is estimated as 3.6 dB at 328.5 GHz accordingly, which is 3.1 dB higher than the simulated one of 0.5 dB. It is interesting to see that eight samples show consistent measured results even the operation frequency reaches the THz band, implying that the GaAs IPD technology has high repeatability, reliability, and robustness to the fabrication variation. Note that unphysical behaviors with $|S_{11}|$ and $|S_{21}|$ larger than 0 dB are perceived at the corner around 270 GHz as depicted in Fig. 14 and 15. The reason for this is the inaccuracy occurred during the TRL calibration procedure, frequently observed especially at such high operation frequencies [38]. However, this will not affect the accuracy of the measured trends at other frequencies.

Though the measured result of the first and second testkeys tracks well with the simulated ones, the discrepancy between simulation and measurement regarding to the insertion loss and frequency shifting toward a lower band indeed exists. It will be explained later that the discrepancy may be caused by the underestimation of the loss tangent of the GaAs material, and the variation of the GaAs dielectric constant and the shape of the ellipse vias. Fig. 16(a) and (b) show the simulated S-parameters of the first and second testkeys, respectively, as the loss tangent, tanδ, of the GaAs material is changed from an originally set value of 0.001 given by the foundry to 0.0077. The simulated insertion loss is increased from 1.7 to 2.7 dB and 2.4 to 5.2 dB for the first

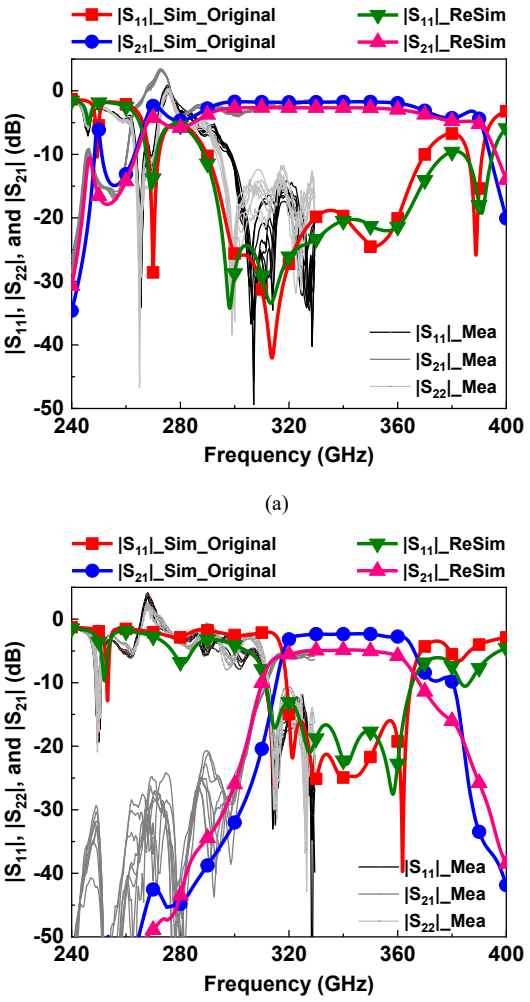

FIGURE 18. Simulated $|S_{11}|$ and $|S_{21}|$ of (a) the first testkey and (b) the second testkey as the via shape and the loss tangent and dielectric constant of the GaAs material are changed.

and second testkeys, respectively, as tanδ is increased from 0.001 to 0.0077. The simulated insertion loss can match the simulated one quite well as the loss tangent is modified. Note that tanδ of 0.001 provided by the foundry is acquired by measurements below 30 GHz and is expected to become much higher at THz frequencies. Yet the frequency shifting to a lower band cannot be explained by simply considering the variation of the loss tangent. The drift of the operation frequency is expectedly caused by the variation of the physical shape of the ellipse vias and the dielectric constant of the GaAs material after fabrication. Fig. 17(a) illustrates a photo of the ellipse vias on the backside plane taken by a scanning electron microscope (SEM). As compared with an ideal vias with a perfectly vertical sidewall as shown in Fig. 2, the length and width of the vias measured on the backside plane shrink from 60 to 52.4 and 51.4 μm and 30 to 22 and 23.1 μm, respectively. Thus, the shape of the vias must be modified as shown in Fig. 17(b) to account for the fabrication variation. Besides, the dielectric constant of the GaAs material is also adjusted from 12.9 to 12.3 to better fit the

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TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR WORKS

Reference	TCPMT'11 [29]	TTST'20 [30]	TMTT'20 [31]		TMTT'20 [32]	TMTT'17[a] [33]	**This Work**	
Devices	SIW	Filter	SIW	Filter	Filter	SIW	**SIW[c]**	**Filter**
f_o (GHz)	300	331	325	270	315	340	**340**	**328.5**
Filter Order	--	5	--	5	9	--	**--**	**4**
Bandwidth (GHz)	--	51	--	5	30	NA	**242-415**	**46[a]**
Insertion Loss	8.3 dB/mm	1.5 dB	0.43 dB/mm 0.14 dB/λ_g	9.2 dB	3.75 dB/mm	1 dB/mm	**0.59 dB/mm 0.22 dB/λ_g**	**3.6[d]**
Return Loss (dB)	NA	15	NA	18.5	8	NA	**23.2**	**16.1[e]**
SIW Size[b] (mm^2)	0.6 × 0.055	--	0.2 × 0.15	--	--	0.53 × 0.29	**0.31 × 0.1**	**--**
Filter Size (mm^2)	--	0.68 × 0.21	--	1.36 × 0.2	2 × 0.3	--	**--**	**0.73 × 0.57**
Substrate Material	High-Z Si	High-Z Si	High-Z Si		Organic Material	NA	**GaAs**	
Calibration Technique	NA	Open-Short	TRL		NA	NA	**LRRM + TRL**	
Technology	In-House TSV Technology	In-House TSV Technology	In-House Micromachining Technology		IC Organic Packaging Process	130-nm CMOS	**IPD**	

(a) Simulation result. (b) Cross-sectional size. (c) Re-simulated results using modified material properties and via shape. (d) Include the loss of a 0.24-mm long SIW. (e) Measured return loss of the second testkey.

measured results. Fig. 18 shows the simulated S-parameter of the first and second testkeys as the variation of the via shape and the loss tangent and dielectric constant of the GaAs material are considered. Now the simulated results fit the measured ones very well. Therefore, the dielectric constant and loss tangent of the GaAs material are recommended to be changed to 12.3 and 0.0077, respectively, and the via shape can be modified as shown in Fig. 17(b) to provide better prediction for future THz designs using the same GaAs IPD technology. Table I shows the performance summary of the proposed SIW and SIW filter and their comparisons with prior works. Obviously, the proposed SIW and SIW filter exhibit lower insertion loss while possessing the advantages of low cost, high reliability, high repeatability, and mass-producible capability. Furthermore, it is the first demonstration of the THz SIW and THz SIW filter using a commercially-available IPD technology reported thus far. These low-loss SIW and SIW filter realized in the GaAs IPD technology are very suitable for being a heterogeneous substrate integration platform for THz applications.

VI. CONCLUSION

Low-loss and low-cost THz SIW and THz SIW filter realized in a commercially-available and mass-productive GaAs IPD technology are proposed and successfully verified by the experimental results. The orientation of the IPD vias are carefully selected to minimize the insertion loss. A new SIW filter structure is proposed, which not only can conquer the hard DRC rules imposed by the IPD technology, but it can also enhance the out-of-band signal rejection by 10.5 dB at 390 GHz as compared with conventional waveguide filters. The measured insertion loss of the proposed CPW-to-SIW transition with a 0.22-mm long SIW and the proposed SIW filter with a 0.24-mm long SIW is only 0.7 and 3.6 dB at 327.5 and 328.5 GHz, respectively. The recommended modifications of the dielectric constant, loss tangent, and via shape are also given to increase the prediction accuracy for future THz designs using the GaAs IPD technology. These low-loss SIW and SIW filter are very suitable to be used as a heterogeneous substrate integration platform for THz applications

ACKNOWLEDGMENT

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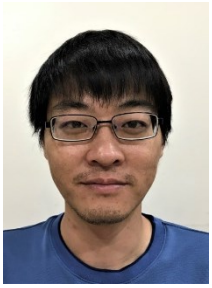
Te-Yen Chiu (Student Member, IEEE) received the B.S. degree in communication engineering from Chung Hua University, Hsinchu, Taiwan, in 2015, and the M.S. degree in electrical engineering from National Central University, Jhongli, Taiwan, in 2017. He is currently pursuing the Ph.D. degree at the Department of Engineering and System Science, National Tsing Hua University, Hsinchu, Taiwan.



Chun-Hsing Li (Senior Member, IEEE) received the B.S. degree in electrophysics, and M.S. and Ph.D. degrees in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2005, 2007, and 2013, respectively.

In 2014, he joined MediaTek, Hsinchu, Taiwan, as a Senior Engineer. In 2014 and 2018, he joined the Department of Electrical Engineering, National Central University, Jhongli, Taiwan, and the Department of Engineering and System Science, National Tsing Hua University, Hsinchu, Taiwan, respectively, as an Assistant Professor. In August 2020, he joined the Department of Electrical Engineering and Graduate Institute of Communication Engineering, National Taiwan University, Taipei, Taiwan, where he is currently an

Associate Professor. His current research interests include RF, millimeter-wave, and terahertz integrated circuit and system design.

Dr. Li was a recipient of Outstanding Young Scholar Award from Taiwan IC Design Society 2020, the FineTek Technology Gold Award 2013 and the Best Paper Award from the Chinese Institute of Engineers 2013. He was a co-recipient of the Best Paper Award of the 13th IEEE International Conference on Electronics, Circuits, and Systems, Nice, France, 2006.