Low-Loss, Low-Crosstalk, and Large-Scale Optical Switch Based on Silicon Photonics

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***Abstract*—We review the research progress of strictly nonblocking optical switches based on silicon photonics. We have developed a switch chip fabrication process based on a complementary metal-oxide-semiconductor pilot line and optical and electrical packaging technologies. We demonstrated all-paths transmission and switching of up to 32 input ports × 32 output ports with an average fiber-to-fiber insertion loss of 10.8 dB. Furthermore, we demonstrated an operating bandwidth wider than 100 nm for −30 dB crosstalk with double-Mach–Zehnder element switches in an 8 × 8 switch. For polarization-insensitive operation, we adopted a polarization diversity scheme and fabricated an 8 × 8 switch with fiber-based polarization-beam-splitters and two switch chips. The 8 × 8 switch exhibited a polarization-dependent loss of less than 0.5 dB. Moreover, an on-chip polarization diversity 8 × 8 switch integrated with polarization splitter rotators and two switch matrices on a single chip demonstrated a differential group delay less than 1 ps. Based on current technologies, we discuss the prospects for further port count expansion and remaining challenges for commercial deployment.**

***Index Terms*—Optical fiber coupling, optical switches, photonic integrated circuits, silicon photonics, strictly nonblocking switches.**

I. Introduction

DATACENTER-RELATED traffic is growing, especially within data centers, with traffic forecast to grow at a rate of 25% per year until 2021 [3]. The switching capacity requirements for the switch ASICs to handle the massive data flow is outpacing Moore's law. This switching capacity expansion is accompanied by increased power consumption that is approaching the thermal limit (∼300 W) of practical integrated electronic circuit cooling technology [5]. To overcome this energy bottleneck and build sustainable data centers with reasonable power consumption, optical switches are expected to be one of the key enablers.

TABLE I
Optical Switch Technologies

Switching Time	Platform	Mechanism	Port Count	SNB	On-chip Loss [dB]	Ref.
~10 ms	Space Optics	MEMS Mirror	320	Yes	≤3 dB*	[1]
~10 ms	Space Optics	Piezo Actuator	384	Yes	≤3 dB*	[2]
~ms	Silica PLC	TO	32	Yes	6.6*	[4]
~10 μs	CMOS compatible Si Ph.	TO	32	Yes	6.1	[6]
~μs	MEMS Si Ph	MEMS	240	Yes	9.8	[7]
~10 ns	CMOS compatible Si Ph.	Carrier Plasma	32	No	12.9 – 16.5	[9]
~ns	InP	Carrier Plasma	8	Yes	24.0 – 28.5	[13]
~ns	InP	SOA	8	No	7.7 **	[15]

SNB: strictly non-blocking, PLC: planar lightwave circuit, Si Ph.: silicon photonics, TO: thermo-optic, SOA: semiconductor optical amplifier, *Fiber-to-fiber insertion loss, **On-chip gain.

Table I summarizes various optical switch technologies. Free-space optical switches can provide several hundred switching ports with a fiber-to-fiber insertion loss of only a few dB, and are commercially available. Silica planar lightwave circuit (PLC) based switches are also commercially available and can provide up to 32 ports switching with an insertion loss of 6.6 dB. However, the switching time of the three switches is of the order of milliseconds, and this limits their application to job-level system reconfiguration. On the contrary, optical switches based on integrated optical waveguides can provide fast switching ranging from ns to 10 μs. For further reduction of the electric power consumption in a data center, a fast ($<<$1 ms) circuit switch or a flow switch is required [8]. Although optical characteristics and port-count scalability of integrated optical waveguides (such as loss, crosstalk, and polarization-dependent loss (PDL)) are not as good as those of the free-space optical switches, they can meet the fast switching requirement, and have thus been attracting attention.

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Among the integrated waveguide-based optical switches, we focus on the complementary metal-oxide-semiconductor (CMOS)-compatible silicon photonics switch, because the CMOS-compatible silicon photonics platform provides high density and uniform integration, and potentially low cost owing to its mass producibility. As for the switching mechanism, we chose the thermo-optic (TO) switch because it can provide ∼10-μs or faster switching without any additional losses. Although the carrier plasma switch can provide ∼ns order switching time, it accompanies absorption loss. As for micro electro mechanical system (MEMS) based silicon switches, they possess a switching speed of ∼μs and the maximum port count of 240. However, their electrical packaging is challenging, and transmissions of all paths have not been demonstrated yet. Moreover, tens of voltages are required to actuate the MEMS switch, which is difficult to handle with the CMOS technology. Hereafter, therefore, we focus on CMOS-based silicon photonics switches.

The strictly-non-blocking type of optical switch has the property that any optical path changes do not interfere any other established paths. This is an important characteristic for flexible network operation, and several groups reported such optical switches based on CMOS silicon photonics [10]–[12]. There are three typical topologies for the strictly-non-blocking switches, including the cross-point, the switch-and-select [14], and the path-independent insertion-loss (PILOSS) [16], which are illustrated in Fig. 1(a)–(c). Fig. 1(d) compares the insertion losses of the worst paths of the three topologies, in which the insertion losses of the element switch and the intersection are assumed to be 0.1 dB and 0.02 dB, respectively. We note that the insertion loss of the switch-and-select rapidly increases with the port count and moreover that the loss of the PILOSS remains the lowest. Therefore, we consider that the PILOSS topology has potential advantages for larger port count switches. In future, however, if multilayer platform technologies [17], [18] that can eliminate the insertion loss of the intersection get matured, the switch-and-select topology may be an option. The double-layer network [19] that is a different version of switch-and-select topology will be also another option in terms of loss, although the power consumption of the switch-and-select topology will be an issue for a large-port-count switch since the number of bar-state switches (ON switches) is much larger than that of the other topologies.

In this paper, we review the current performance of CMOS-based silicon photonics PILOSS switches and discuss the remaining challenges for their practical application [20]. In Section II, we describe a 32 × 32 switch that is the largest port count silicon PILOSS switch. In Sections III and IV, we discuss wavelength and polarization insensitivities, respectively. In Section V, we discuss some obstacles and possible solutions toward further improvement of transmission characteristics and port count expansion. Finally, in Section VI, the conclusions of this paper are presented.

II. 32 × 32 PILOSS Switch

The 32 × 32 PILOSS switch chip was fabricated using our CMOS pilot line that can process 300-mm silicon-on-insulator wafers with an immersion ArF lithography. The switch chip has 2,112 electrodes for the thermo-optic phase-shifter control, which were fanned out to a 0.5-mm-pitch land-grid-array (LGA) by a flip-chip bonded ceramic interposer. Optical connectors based on an extremely high-Δ silica PLC [21] were attached and secured with refractive-index-matched UV-cured glue. Finally, the assembled switch chip was inserted into an LGA socket on a printed circuit board (PCB) with control electronics [Fig. 2(a)]. We note that the switch chip with the optical connector is not placed under high temperature owing to the socket packaging. We controlled the thermo-optic phase shifters on the chip by adjusting the pulse width of the square pulse train generated by five field-programmable-gate-arrays (FPGAs) on the PCB [22]. The initial phase errors of the element switches, which are directional-coupler-based Mach–Zehnder (MZ) switches, were automatically calibrated [23]. The heating efficiency is 18.1 mW/π-shift [6]. The electric power consumption on the chip in the full-load condition was 1.9 W.

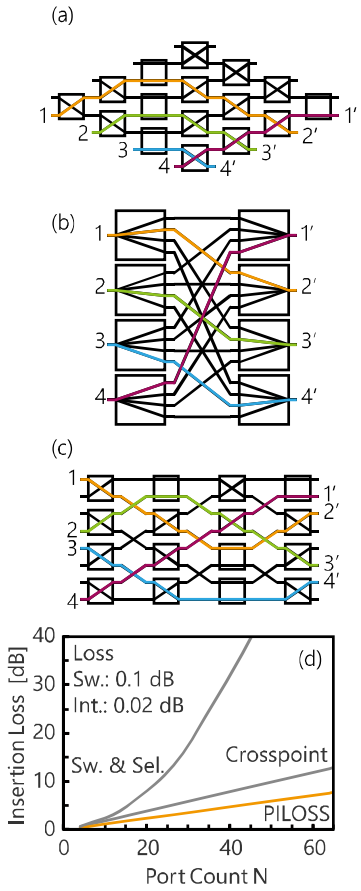


Fig. 1. Schematics of 4 × 4 switch based on (a) cross-point, (b) switch-and-select, and (c) path-independent insertion-loss (PILOSS) topologies. (d) Comparison of worst insertion loss. The losses of the element switch and the intersection were assumed to be 0.1 and 0.02 dB, respectively.

First, we evaluated fiber-to-fiber insertion loss of all (1,024) paths, and its distribution is shown in Fig. 2(b). The switch exhibited 10.8 dB average loss with 0.54 dB standard deviation. The maximum and minimum losses were 12.8 dB and 8.9 dB, respectively. We consider that the insertion loss variation was caused by the coupling loss variation, especially the input side, and the propagation loss difference among the routing waveguides that connect the edge couplers and the switch matrix.

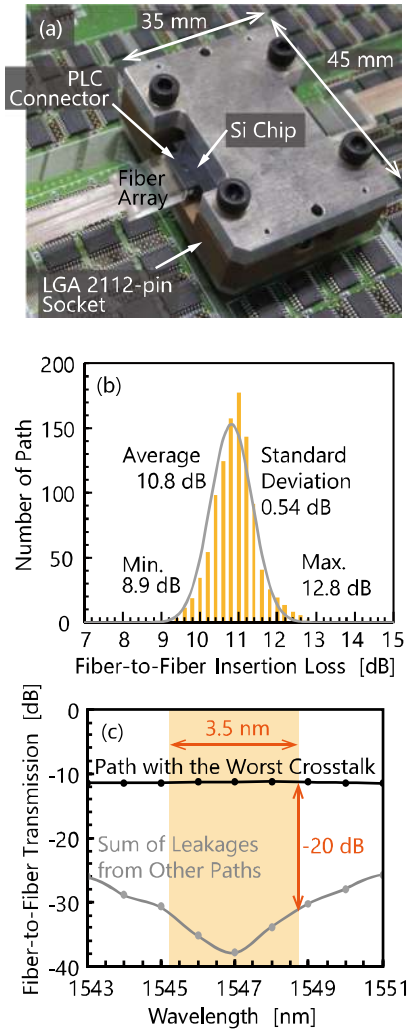


Fig. 2. (a) Fabricated 32 × 32 switch mounted on printed circuit board with control electronics. (b) Distribution of fiber-to-fiber insertion loss. The gray line is the fitted Gaussian whose standard deviation is 0.54 dB. (c) Wavelength spectrum of one of the worst crosstalk paths and sum of leakages from other paths.

Second, we characterized the crosstalk in one of the severest paths. Here, we defined the crosstalk as the ratio between the transmitted power from a path (path A) and the sum of the leaked powers from other paths to the path A. Fig. 2(c) presents the transmission spectra of one of the worst crosstalk paths and the sum of the leakages from other paths. We note that the crosstalk was less than −20 dB in a bandwidth of 3.5 nm due to the wavelength dependence of the directional coupler in the MZ switch. The wavelength dependence can be relaxed by exchanging the output port of the element MZ switch, resulting in the bandwidth expansion to 14.2 nm [6].

III. Wavelength Insensitivity

A straightforward method to expand the low crosstalk bandwidth is replacing the directional couplers with broadband couplers such as a multi-mode interference (MMI) coupler, or an adiabatic directional coupler. However, they are not suited for large port-count optical switches, because the MMI and

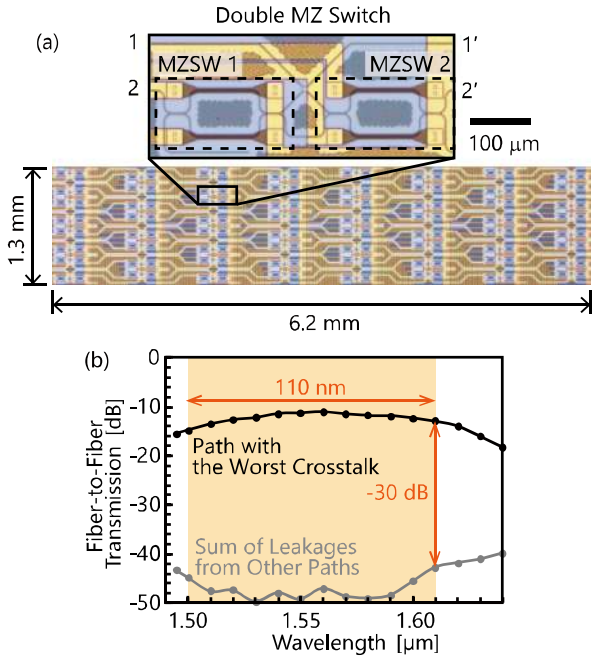


Fig. 3. (a) Microscope image of fabricated double Mach–Zehnder 8 × 8 switch. (b) Fiber-to-fiber transmission spectra of one of the severest crosstalk paths and sum of leakages from other paths.

the adiabatic coupler possess high insertion loss. Therefore, we adopted a double-MZ switch that was originally proposed by Goh et al. for the silica PLC platform [24]. The double-MZ switch consists of two MZ switches and one intersection, as shown in Fig. 3(a). The rear MZ switch suppresses the leakage from the front MZ switch at the cross state or leads it to an idle port at the bar state, resulting in lower crosstalk and wider bandwidth of the switch matrix than those of a single MZ switch case. The numbers of the MZ switches and the intersections on a path in the double-MZ $N \times N$ switch increase by one, and $N-1$, respectively, compared with those in the single-MZ $N \times N$ switch. If we composed the double-MZ 32 × 32 switch, the additional loss would be less than 1 dB (≈0.13 dB (MZ switch) + 0.024 dB (intersection) × (32 −1)), which is acceptable.

We fabricated an 8 × 8 switch based on the double-MZ switch, as shown in Fig. 3(a). The switch chip was fabricated in the same manner described in Section II. Then, the switch chip was die-bonded and wire-bonded to a ceramic chip carrier with a 304-pin pin-grid-array (PGA). An optical fiber array was butt-coupled to the switch chip, then the chip carrier was inserted into a PGA socket on a PCB, which has one FPGA for thermo-optic phase-shifter control.

Fig. 3(b) presents the transmission spectra of one of the severest crosstalk paths and the sum of leakages from the other paths [25]. We note that the 8 × 8 switch exhibited less than −30 dB crosstalk in a bandwidth of 110 nm.

IV. Polarization Insensitivity

The silicon waveguide exhibits significant polarization dependency due to strong optical confinement, and this prevents the deployment of silicon devices in practical applications. To

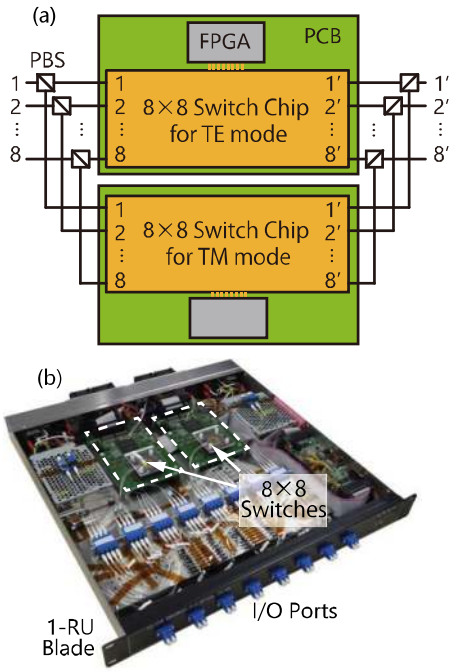


Fig. 4. (a) Configuration of polarization diversity 8 × 8 switch by using polarization beam splitters with fiber pigtails. (b) Polarization-diversity double Mach–Zehnder 8 × 8 switch assembled into 1-RU blade.

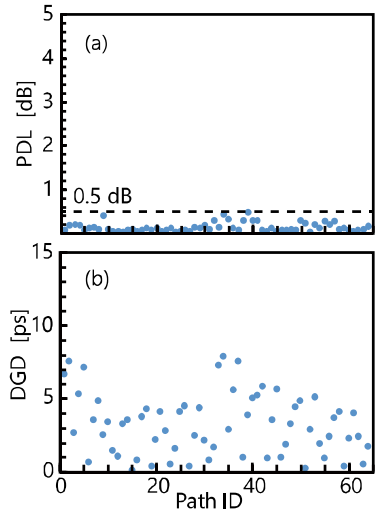


Fig. 5. (a) Measured polarization dependent loss and (b) differential group delay of polarization diversity 8 × 8 switch shown in Fig. 4 at a wavelength of 1535 nm. Path ID means input-output connections. 1: 1 (input) −1' (output), 2: 1–2, …, 64: 8-8'.

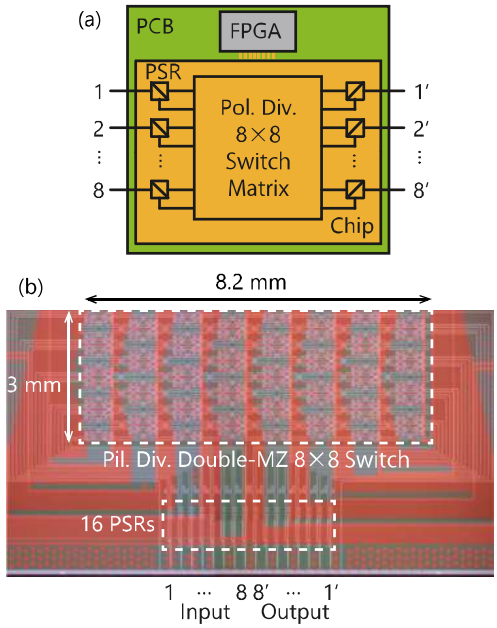


Fig. 6. (a) Configuration of polarization diversity 8 × 8 switch by using on-chip polarization splitter rotators. (b) Microscopic image of fabricated polarization-diversity 8 × 8 switch chip.

realize polarization-insensitive operation, there are two options; the polarization diversity scheme and the polarization-insensitive structure. We consider that the polarization diversity scheme is a realistic option at this time because the polarization-insensitive structure requires very high fabrication accuracy [26]. In the polarization diversity scheme, two switch matrices deal with the two orthogonal polarizations. This may become a disadvantage for high-radix switches because it requires handling double the footprint and optical and electrical input/output connections. However, a non-duplicate polarization diversity PILOSS topology will overcome the disadvantage [27].

Fig. 4(a) illustrates the configuration of a polarization diversity 8 × 8 switch by using two double-MZ 8 × 8 switches on the PCBs and 16 fiber-based polarization-beam-splitters (PBSs) [28]. We term this configuration as "off-chip" polarization-diversity. The input light was separated into two orthogonal polarizations with the PBS, then launched into each switch. The output lights from each switch were mixed with another PBS. The polarization diversity switch was assembled into a 1-RU chassis, as shown in Fig. 4(b).

We measured the PDL and the differential group delay (DGD) of all paths with an optical component analyzer based on the Muller matrix, and the results are presented in Fig. 5(a) and (b). The PDL at a wavelength of 1535 nm was less than 0.5 dB. The residual PDL was attributed from the polarization variation of the experimental setup. The DGD was less than 8 ps, which reflects fiber length variations (∼±1 mm) of the PBS and the optical fiber array. These polarization characteristics are low enough for optical signal transmission with digital signal recovery. In fact, the 8-stage cascaded operation of the 8 × 8 switch was demonstrated, in which 11-channel 44-Gbaud DP-16QAM signals transmitted through all the paths of this 8 × 8 switch [32]. Furthermore, we conducted a long-term (∼2 years) reliability test in a test bed that simulates real-world deployment. Specifically, we have observed no degradations in fiber-to-fiber insertion loss and no drifts of calibration settings for the initial phase-error compensation since the installation of our switch [33].

As a next step, we integrated the two double-MZ 8 × 8 switch matrices and 16 on-chip polarization splitter rotators (PSRs) on a single die, as shown in Fig. 6(a). We term this configuration as "on-chip" polarization diversity. The PSR exploits adiabatic

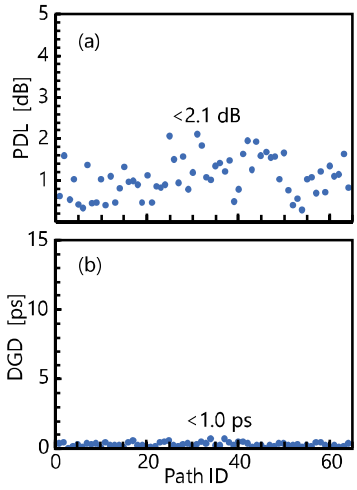
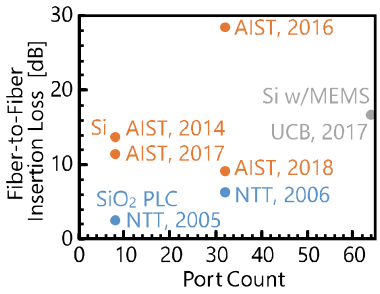


Fig. 7. (a) Measured polarization dependent loss and (b) differential group delay of polarization diversity 8 × 8 switch shown in Fig. 6 at a wavelength of 1550 nm. Path ID means input-output connections. 1: 1 (input) −1' (output), 2: 1–2, …, 64: 8-8'.



Si	Ref.
AIST, 2014	[29]
AIST, 2016	[22]
AIST, 2017	[25]
AIST, 2018	[6]
SiO_2 PLC	
NTT, 2005	[30]
NTT, 2006	[4]
Si w/ MEMS	
UCB, 2017	[31]

Fig. 8. Comparison of fiber-to-fiber insertion losses.

modal conversion and directional coupling in a vertically asymmetric structure [34]. The PSRs at the input port and those at the output ports were placed so as to rotate original polarization by 90° (i.e., the originally TE (TM) mode is converted to TM (TE) mode). This configuration compensates the polarization dependence of input and output fiber coupling efficiency. Fig. 6(b) depicts the fabricated on-chip polarization-diversity double-MZ 8 × 8 switch chip. The switch chip was packaged in the same manner as described in Section III.

Fig. 7(a) and (b) present the PDL and the DGD of all paths, respectively. The measurement setup is the same as that of the "off-chip" polarization-diversity case. The measured PDL was less than 2.1 dB. We suspect that the residual PDL was caused by variations of the insertion loss and the conversion efficiency of the PSR. The design optimization of the PSR, especially robust design against structural fluctuation, improves the PDL. On the other hand, the DGD is less than 1.0 ps owing to fully integrated optical paths from the PSR and the switch matrix.

V. Discussion

In this section, we discuss the remaining challenges for switch performance improvements and port count expansion. Regarding the fiber-to-fiber insertion loss of the 32 × 32 switch, we believe that about 6 dB is possible. If we adopt the latest fabrication process, propagation loss of less than 0.5 dB/cm is achievable, resulting in 2 dB loss reduction. Moreover, there is potential for coupling loss reduction because the numerical simulation shows 0.6 dB/facet coupling [21]. Fig. 8 compares the fiber-to-fiber insertion losses of the multi-port switches fabricated on the integrated waveguide platforms. We note that 6 dB insertion loss is comparable with that of the silica PLC platform. For further loss reduction, integration with semiconductor optical amplifiers is an available option [35].

To realize larger port counts, one of the limiting factors is fan-out of the electrodes. For example, if we simply expanded the 32 × 32 switch to a 64 × 64 switch, we would have to handle 8320 electrodes, which is much larger than that of the latest CPU packaging (LGA 3647). Therefore, some technology that reduces the number of electrodes, such as dynamic control using diodes [36] or integration with an address decoder, is necessary.

VI. Conclusion

We have reviewed the switching performance of strictly nonblocking silicon photonics switches. The largest port count 32 × 32 PILOSS switch, fully packaged and controlled, exhibited an average fiber-to-fiber insertion loss of 10.8 dB with a standard deviation of 0.54 dB. In the double-MZ 8 × 8 switch, −30 dB crosstalk bandwidth was wider than 100 nm. Regarding polarization insensitivity, we demonstrated 0.5 dB PDL in the polarization diversity 8 × 8 switch with fiber-based PBSs, and less than 1.0 ps DGD in the fully integrated polarization diversity 8 × 8 switch. We pointed out that further port count expansion requires the reduction of the number of electrode pads on the chip. As mentioned above, some technological challenges remain to be addressed for practical applications. However, we expect that silicon photonics switches offer new solutions for future energy efficient networks.

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