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Chang-Tsung Fu, Chien-Nan Kuo, Stewart S. Taylor

Institutions: National Chiao Tung University, Intel

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Low-Noise Amplifier Design With Dual Reactive Feedback for Broadband Simultaneous Noise and Impedance Matching

Chang-Tsung Fu, *Member, IEEE*, Chien-Nan Kuo, *Member, IEEE*, and Stewart S. Taylor, *Fellow, IEEE*

***Abstract*—The simultaneous noise and impedance matching (SNIM) condition for a common-source amplifier is analyzed. Transistor noise parameters are derived based on the more complete hybrid-π model, and the dominant factors jeopardizing SNIM are identified. Strategies for narrowband and broadband SNIM (BSNIM) are derived accordingly. A dual reactive feedback circuit along with an *LC*-ladder matching network is proposed to achieve the BSNIM. It includes a capacitive and an inductive feedback, where the former utilizes the transistor parasitic gate-to-drain capacitance and the latter is formed by transformer coupling. This circuit topology has been validated in 0.18- and 0.13-μm CMOS technologies for a 3–11-GHz ultra-wideband (UWB) and a 2.4–5.4-GHz multistandard application, respectively. The 3–11-GHz UWB low-noise amplifier is detailed as a design example.**

***Index Terms*—Broadband input matching, capacitive feedback, low-noise amplifier (LNA), low power, noise optimized design, simultaneous noise and impedance matching (SNIM), transformer feedback, ultra-wideband (UWB).**

I. Introduction

A LOW-NOISE amplifier (LNA) in a wireless receiver is expected to have high gain and low noise figure (NF) for a sufficient signal-to-noise ratio to demodulate signals. Among various MOSFET LNA circuit topologies, the common-source (CS) based amplifier is generally preferred, as it has better noise performance within limited power consumption. It is especially popular for extreme applications in which ultra-low power or very high frequency is demanded. It is well known that gain and noise performance of a linear two-port amplifier can be optimized by fulfilling the condition of simultaneous noise and impedance matching (SNIM) at the input [1], [2]. SNIM is a condition that the input impedance $(Z_{\rm in})$ and the conjugate of the noise optimized source impedance $(Z^*_{\rm opt})$ of the entire amplifier are simultaneously matched to the source impedance Z_0, i.e., $Z_{\rm in} = Z^*_{\rm opt} = Z_0$, as shown in Fig. 1. As such, the NF of the amplifier approaches the minimum NF $(\rm NF_{min})$.

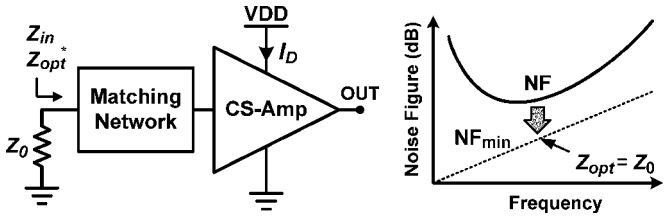

Fig. 1. SNIM approaching for a CS LNA.

The concept of SNIM was first brought up in [2] with a complete two-port analysis on feedback amplification, yielding a series of matrices suitable for computer-aided design in which the design is accomplished by an iterative graphical maneuver on a Smith chart. However, since limited circuit insight can be directly obtained from such an approach [2]–[6], optimization methods by analyzing simplified transistor noise models were proposed [7]–[14], in which most of them are specifically for the inductive source degenerated CS amplifier. While van der Ziel's analysis is widely adopted to explain the $Z_{\rm in}$-to-$Z^*_{\rm opt}$ mismatch of a MOS transistor, it was found, however, that induced gate noise is not the dominant cause of this mismatch. The noise from gate resistance was mentioned, but not included in SNIM analysis. Hence, there is a gap between the analysis and practical design that relies on iterative steps to resolve. At this point the approaches by [7] and [8] provide more consistent results with simulation.

For a broadband SNIM (BSNIM) LNA design, frequency dependency of the noise parameters should be considered. Whereas the $Z^*_{\rm opt}$ and $Z_{\rm in}$ derived in the literatures have different frequency dependency, BSNIM seems difficult to achieve. This is observed in the broadband amplifier realized by employing a multiorder *LC* matching network [15], of which the noise performance is still band-limited. In 2006, two ultra-wideband (UWB) LNAs utilizing distinct transformer feedback structures were reported [16], [17], both showing a broadband noise performance. In [16], we demonstrated the first BSNIM LNA by employing a dual reactive feedback topology. We infer the work in [17] might also achieve BSNIM as two reactive feedback paths are employed in the first stage, although this was not discussed. To the best of the authors'

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C.-T. Fu was with the Department of Electronic Engineering, National Chiao-Tung University, Hsinchu, 300 Taiwan. He is now with the Intel Laboratory, Intel Corporation, Hillsboro, OR 97124 USA (e-mail: ctfu@ieee.org; changtsung.fu@intel.com).

C.-N. Kuo is with the Department of Electronic Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan (e-mail: cnkuo@mail.nctu.edu.tw).

S. S. Taylor is with the Intel Laboratory, Intel Corporation, Hillsboro, OR 97124 USA (e-mail: stewart.s.taylor@intel.com).

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knowledge, an effective BSNIM LNA design approach has not been revealed yet.

In this paper, we provide a design approach for a BSNIM LNA in CMOS based upon transistor noise parameter analysis and provide an example. It is the theoretical extension of our earlier papers [16], [18]. Starting in Section II, we first analyze the practical mechanisms jeopardizing the ideal SNIM condition inside a CMOS transistor, including the effects of the gate resistance, gate-to-drain capacitance, and induced gate noise. Based on the derived four noise parameters, the strategies to achieve SNIM are proposed for both narrowband and broadband applications as design guidelines. In Section III, a dual reactive feedback amplifier with an *LC* ladder matching network achieving BSNIM is introduced as a solution. Section IV demonstrates the design example of an UWB LNA implemented in a TSMC 0.18-μm CMOS process [16], along with the experiment results. Section V summarizes and concludes this paper. In the Appendix, the noise analysis to obtain the input-referred noise sources for noise parameters is presented. The effect of noise contributed by the succeeding stages following an LNA is also briefly discussed in the Appendix.

II. Simultaneous Noise and Input Matching: Analysis and Solution

In traditional microwave theory, a CS amplifier can be designed to be either gain optimized by impedance matching or noise optimized by noise matching [1]. Whereas the latter is more critical in an LNA design, input impedance matching is necessary to minimize the variation in the voltage standing-wave ratio (VSWR) with transmission line length, and the accompanying variation in gain and linearity. However, as shown later, SNIM is not "gain optimized" since it can only be achieved by employing feedback techniques with the gain somewhat reduced. This may not be a practical problem as modern scaled technology usually has adequate or excess gain. The approach for SNIM optimizes the noise performance first, and then designs with feedback for a small input reflection. The gain response is typically dominated by the output network of a CS amplifier and has limited correlation with SNIM.

The development of BSNIM design requires an accurate derivation of input-referred noise sources for the noise parameters. In this paper, it is obtained with the developed analysis technique, as in the Appendix. After the noise parameter equations are obtained, a simplification is made and validated numerically. By comparing $Z_{\rm in}$ and $Z^*_{\rm opt}$, the strategies for BSNIM is derived.

A. Mismatch Between $Z_{\rm in}$ and $Z^*_{\rm opt}$ of a CS MOS Amplifier

The noise model employed for the transistor noise analysis is shown in Fig. 2, in which $\overline{i^2_{nd}}$ is the channel thermal noise and $\overline{i^2_{ng}}$ is the induced gate noise. Their values are formulated as

$$\overline{i^2_{nd}} = 4kT\gamma g_{do}\cdot\Delta f \tag{1}$$

$$\overline{i^2_{ng}} = 4kT\delta g_g\cdot\Delta f = 4kT\delta\frac{\omega^2 C^2_{\rm gsi}}{5g_{do}}\cdot\Delta f. \tag{2}$$

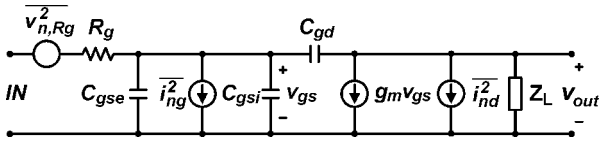

Fig. 2. Noise model employed for transistor noise analysis.

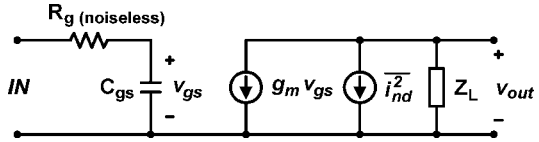

Fig. 3. Ideal case of a CS amplifier satisfying SNIM condition at all frequency.

Here, g_{do} is the drain-to-source channel conductance with zero $V_{\rm DS}$. $C_{\rm gsi}$ is the intrinsic gate-to-source capacitance via the channel, and $C_{\rm gse}$ is the extrinsic parasitic gate-to-source capacitance from metal overlap, roughly equal to $C_{\rm gd}$. $C_{\rm gsi}$ and $C_{\rm gse}$ constitute $C_{\rm gs}$. The noise contribution of Z_L is conditionally ignored here and will be discussed in the Appendix. γ and δ in (1) and (2) are derived as 2/3 and 4/3, respectively, for long channel MOS transistors [9]. Since $\overline{i^2_{nd}}$ and $\overline{i^2_{ng}}$ are introduced by the same channel resistance, they are partially correlated to each other with the correlation factor defined as

$$\text{corr.} = \frac{\overline{i_{ng}i^*_{nd}}}{\sqrt{\overline{i^2_{ng}}\cdot\overline{i^2_{nd}}}} = jc_i \tag{3}$$

where c_i is derived as $\sqrt{5/32}$ for long channel devices and the imaginary unit j comes from the capacitive coupling by $C_{\rm gsi}$. The directions of $\overline{i^2_{nd}}$ and $\overline{i^2_{ng}}$ in Fig. 2 decide the sign of the correlation factor. $\overline{v^2_{n,Rg}}$ is the associated noise source of gate resistance R_g, whose value is

$$\overline{v^2_{n,Rg}} = 4kTR_g\cdot\Delta f. \tag{4}$$

The metal overlap parasitic capacitances such as $C_{\rm gd}$ and $C_{\rm gse}$ are included in this model for analysis.

The mismatch between $Z_{\rm in}$ and $Z^*_{\rm opt}$ of a CS amplifier is well known. To identify the factors causing this mismatch, we start with the ideal case that always meets the SNIM condition, i.e., $Z_{\rm in} = Z^*_{\rm opt}$. Consider the ideal hybrid-π model of a MOS transistor, shown in Fig. 3, which includes $\overline{i^2_{nd}}$ and a *noiseless* gate resistor R_g. By applying the noise analysis technique in the Appendix, $Z^*_{\rm opt}$ of this ideal transistor can be shown to be

$$Z^*_{\rm opt} = R_g + 1/j\omega C_{\rm gs} \tag{5}$$

and $Z_{\rm in}$ is

$$Z_{\rm in} = R_g + 1/j\omega C_{\rm gs}. \tag{6}$$

Obviously $Z^*_{\rm opt}$ is equal to $Z_{\rm in}$ at all frequency. Therefore, $Z^*_{\rm opt}$ and $Z_{\rm in}$ can both be tuned and matched to Z_0 in Fig. 1 simultaneously with a lossless matching network to meet the SNIM condition.

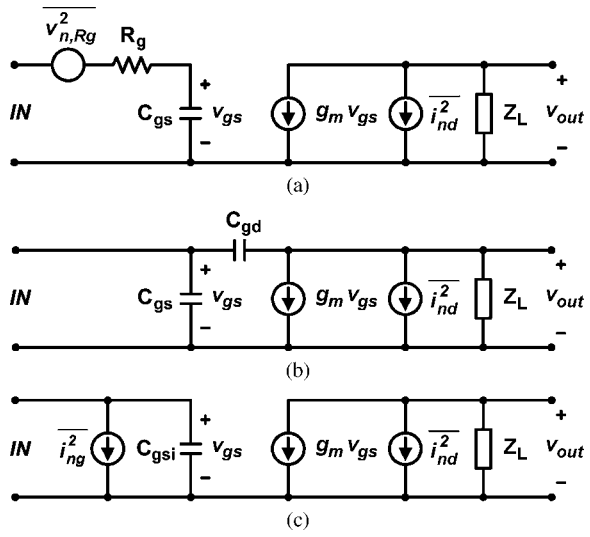

Fig. 4. Simplified MOS transistor noise models testing effects of: (a) associated noise of gate resistance, (b) $C_{\rm gd}$, and (c) the induced gate noise.

In practice, as shown in Fig. 2, $Z_{\rm opt}^*$ and $Z_{\rm in}$ are found to differ from each other by three major factors, referred to as $Z_{\rm in}$-to-$Z_{\rm opt}^*$ *discrepancy factors*, which are: 1) independent noise sources at the gate; 2) gate-to-drain capacitance; and 3) induced gate noise. Effects of these three factors can be observed individually by the three test cases, as shown in Fig. 4.

The first factor is the independent noise source at the gate port. Typically, this is the gate resistance noise $\overline{v_{n,Rg}^2}$. Using the noise model shown in Fig. 4(a), the analysis of $Z_{\rm opt}^*$ is significantly changed to be

$$Z_{\rm opt}^* = \sqrt{R_g^2 + \frac{\alpha}{\gamma g_m}\frac{g_m^2 R_g}{\omega^2 C_{\rm gs}^2}} + \frac{1}{j\omega C_{\rm gs}} \tag{7}$$

where $\alpha = g_m/g_{do}$. In comparison to (5), the noise source $\overline{v_{n,Rg}^2}$ increases the real part of $Z_{\rm opt}^*$ with a frequency-dependent term, and thus makes $Z_{\rm opt}^*$ larger than $Z_{\rm in}$. This factor is found to be the primary factor in $Z_{\rm in}$-to-$Z_{\rm opt}^*$ discrepancy in most CMOS LNA design. The noise from a nonideal input matching network also has the same effect.

The second factor results from parasitic feedback via gate-to-drain capacitance $C_{\rm gd}$. Consider the simplified transistor noise model with $R_g = 0$, as shown in Fig. 4(b). In comparison with the ideal case in Fig. 3 with $Y_{\rm in} = Y_{\rm opt}^* = j\omega C_{\rm gs}$ ($R_g = 0$), the inclusion of $C_{\rm gd}$ changes $Y_{\rm in}$ due to the effect of feedback such that

$$Y_{\rm in} = j\omega C_{\rm gs} + j\omega C_{\rm gd}\frac{1 + g_m Z_L}{1 + j\omega C_{\rm gd} Z_L}. \tag{8}$$

Via $C_{\rm gd}$ feedback, the loading impedance Z_L affects $Y_{\rm in}$ significantly. In contrast, $C_{\rm gd}$ impacts $Y_{\rm opt}^*$ only by its loading effect ($C_{\rm gd}$ itself) such that

$$Y_{\rm opt}^* \approx j\omega(C_{\rm gs} + C_{\rm gd}). \tag{9}$$

The change of loading impedance Z_L has no effect on $Y_{\rm opt}^*$.

The third factor is the induced gate noise. Consider the noise model with $R_g = 0$, as shown in Fig. 4(c). $C_{{\rm gs}e}$, $C_{\rm gd}$, and $\overline{i_{n,L}^2}$ are ignored. The derived $Y_{\rm opt}^*$ is approximately as

$$Y_{\rm opt}^* \approx \omega C_{{\rm gs}i}\cdot\alpha\sqrt{\frac{\delta}{5\gamma}(1-c_i^2)} + j\omega C_{{\rm gs}i}\left(1 - c_i\cdot\alpha\sqrt{\frac{\delta}{5\gamma}}\right). \tag{10}$$

It is beneficial to define the output noise contribution ratio of $\overline{i_{ng}^2}$ to $\overline{i_{nd}^2}$ as

$$\kappa = \sqrt{\frac{\overline{i_{ng}^2}\cdot(g_m/\omega C_{{\rm gs}i})^2}{\overline{i_{nd}^2}}} = \alpha\sqrt{\frac{\delta}{5\gamma}}. \tag{11}$$

$Y_{\rm opt}^*$ in (10) can then be simplified as

$$Y_{\rm opt}^* \approx \omega C_{{\rm gs}i}\kappa\sqrt{1-c_i^2} + j\omega C_{{\rm gs}i}(1 - c_i\kappa). \tag{12}$$

By comparing this $Y_{\rm opt}^*$ with the corresponding $Y_{\rm in}$, equal to $j\omega C_{{\rm gs}i}$, the induced gate noise is found to reduce the effective capacitance of $Y_{\rm opt}^*$ and introduces a frequency-dependent real part on $Y_{\rm opt}^*$.

With all of the three factors considered, it can be shown that

$$Z_{\rm opt}^* = \sqrt{R_g^2 + \left(\frac{\alpha}{\gamma g_m}g_m^2 R_g + 1 - |c|^2\right)\frac{1}{\omega^2 C_N^2}} + \frac{|c|}{j\omega C_N} \tag{13}$$

where

$$C_N = \sqrt{(C_{\rm gs} + C_{\rm gd})^2 - 2c_i\kappa C_{{\rm gs}i}(C_{\rm gs} + C_{\rm gd}) + \kappa^2 C_{{\rm gs}i}^2} \tag{14}$$

and

$$|c| = \sqrt{\frac{1 - (1 - c_i^2)\,\kappa^2 C_{{\rm gs}i}^2}{C_N^2}}. \tag{15}$$

With typical device parameters in 0.18-μm CMOS technology, C_N and $|c|$ are about $0.94\cdot(C_{\rm gs} + C_{\rm gd})$ and 0.98, respectively. More than 99.5% of ${\rm Re}\{Z_{\rm opt}^*\}$ comes from the second term in (13). Hence, $Z_{\rm opt}^*$ can be approximated as

$$Z_{\rm opt}^* \approx \frac{1}{\omega(C_{\rm gs} + C_{\rm gd})}\sqrt{\frac{\alpha}{\gamma g_m}g_m^2 R_g} + \frac{1}{j\omega(C_{\rm gs} + C_{\rm gd})} \tag{16}$$

where the effect of the induced gate noise, represented by κ in the above equations, can be ignored. From (16), $Z_{\rm opt}^*$ has a *frequency-independent quality factor* equal to $\sqrt{\gamma/(\alpha g_m R_g)}$. Hence, on the Smith chart, the $S_{\rm opt}^*$ curve roughly follows the constant-Q contour, different from the behavior of a physical *RC* network.

The other noise parameters are easily obtained. The Z-parameter representation of the noise factor is

$$F = F_{\rm min} + \frac{G_n}{R_S}\cdot|Z_S - Z_{\rm opt}|^2. \tag{17}$$

Here, G_n and $F_{\rm min}$ are

$$G_n \approx \frac{\gamma g_m}{\alpha}\cdot\left[\frac{\omega(C_{\rm gs} + C_{\rm gd})}{g_m}\right]^2 = \frac{\gamma g_m}{\alpha}\left(\frac{f}{f_T}\right)^2 \tag{18}$$

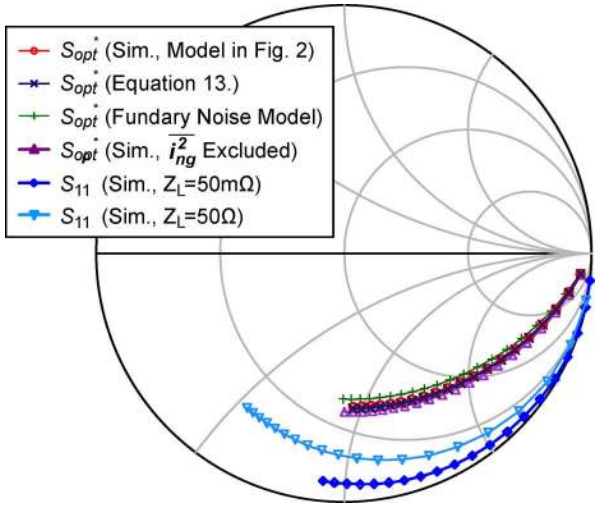

Fig. 5. Equation verification of $Z_{\rm opt}^*$ and the analysis of discrepancy factor effects on Smith chart. Frequency swept from 1 to 20 GHz with 1-GHz step.

and

$$\begin{aligned} F_{\rm min} &= 1 + 2G_n\left(\mathrm{Re}\{Z_{\rm opt}\} + R_g\right) \\ &\approx 1 + 2G_n \mathrm{Re}\{Z_{\rm opt}\} \\ &\approx 1 + 2\frac{\omega(C_{\rm gs}+C_{\rm gd})}{g_m}\sqrt{\frac{\gamma g_m}{\alpha}R_g} \\ &= 1 + 2\frac{f}{f_T}\sqrt{\frac{\gamma g_m}{\alpha}R_g}. \end{aligned} \tag{19}$$

Equation (19) corresponds to Fukui's empirical equation of $F_{\rm min}$ [19]. We can see R_g not only introduces $Z_{\rm in}$-to-$Z_{\rm opt}^*$ discrepancy, but also increases $F_{\rm min}$. R_g is identified as a dominant noise contributor to an LNA. On the other hand, $Z_{\rm in}$ is derived as

$$Z_{\rm in} = R_g + \frac{1}{j\omega C_{\rm gs} + j\omega C_{\rm gd}\frac{1+g_m Z_L}{1+j\omega C_{\rm gd} Z_L}}. \tag{20}$$

The accuracy of (13)–(15) was verified with several test cases by MATLAB and Agilent ADS. The calculated $S_{\rm opt}^*$ (S-parameter of $Z_{\rm opt}^*$) agrees closely with the simulated $S_{\rm opt}^*$. Representative results are plotted in Fig. 5. In this test case, the component parameters in the model of Fig. 2 were extracted from a 0.18-μm NMOS transistor operated in strong inversion in the saturation region. These were applied to (13) and the model in Fig. 2 for the calculation and simulation, respectively. Noise from Z_L is not included in the test case. The simulation result employing the foundry noise model is also included as a reference. Different test conditions are applied to analyze the effect of different factors. As can be seen, the calculation result fits the simulation results very well. The $S_{\rm opt}^*$ curve behaves as a constant-Q curve, showing a strongly frequency-dependent $\mathrm{Re}\{Z_{\rm opt}^*\}$, not matched to the S_{11} curve. R_g dominates the real part discrepancy, whereas induced gate noise $\overline{i_{ng}^2}$ has a marginal effect on $S_{\rm opt}^*$.

Different values of Z_L are applied in Fig. 5 to show the effect of $C_{\rm gd}$ feedback on $Z_{\rm in}$. It can be observed that $\mathrm{Im}\{Z_{\rm in}\}$ is significantly affected by a resistive Z_L because of $C_{\rm gd}$ feedback, while $\mathrm{Re}\{Z_{\rm in}\}$ is also slightly affected, as predicted by (20). In addition, if a reactive Z_L is applied, a capacitive Z_L provides an additional noiseless resistance, whereas an inductive Z_L results in positive feedback, causing an unstable resonance. The former can be utilized for BSNIM as described in Section II-B. With approximate equations (16), (18), and (19), one can quickly evaluate transistor noise parameters of sufficient accuracy by ac simulation or vector network analyzer (VNA) measurement results.

By comparing $Z_{\rm opt}^*$ and $Z_{\rm in}$ in (16) and (20), respectively, their differences are summarized as follows.

- For the real part, the noise contributed by R_g makes $\mathrm{Re}\{Z_{\rm opt}^*\}$ much larger than $\mathrm{Re}\{Z_{\rm in}\}$ by a frequency-dependent amount.
- For the imaginary part, with a resistive Z_L, the $C_{\rm gd}$ feedback makes $\mathrm{Im}\{Z_{\rm in}\}$ smaller than $\mathrm{Im}\{Z_{\rm opt}^*\}$. When represented by a series capacitance, the equivalent series capacitance in $Z_{\rm in}$ is larger than that in $Z_{\rm opt}^*$.

An important insight, if noise from the succeeding stages is ignored, is that $C_{\rm gd}$ feedback changes $Z_{\rm opt}^*$ only by its loading effect, whereas it changes $Z_{\rm in}$ due to feedback, as shown in (8) and (9). The same phenomenon applies to other lossless feedback topologies such as source inductive degeneration [14]. Hence, one can manipulate the difference between $Z_{\rm opt}^*$ and $Z_{\rm in}$ with lossless feedback to achieve SNIM.

Another important consideration is the gain of the CS amplifier. If it is not sufficiently high, the noise parameters will be significantly affected by the noise of succeeding stages. As shown in the Appendix, this increases G_n as well as $F_{\rm min}$, and reduces the discrepancy between $Z_{\rm opt}^*$ and $Z_{\rm in}$. Care should be taken, noting that lower gain may degrade noise performance while satisfying the condition for SNIM.

B. Strategies to Achieve BSNIM

With the mechanism of $Z_{\rm in}$-to-$Z_{\rm opt}^*$ discrepancy identified, strategies to achieve BSNIM for minimized NF can be pursued. Since $\mathrm{Re}\{Z_{\rm in}\}$ is smaller than $\mathrm{Re}\{Z_{\rm opt}^*\}$, the difference can be compensated by introducing a noiseless resistance with a reactive feedback technique. It is critically important to minimize the series capacitance expansion of $Z_{\rm in}$ induced by $C_{\rm gd}$ and the real part of Z_L. From (20), it is necessary to meet the following condition:

$$\mathrm{Re}\{Z_L\} \ll \frac{1}{g_m} \text{ and } \mathrm{Re}\{Z_L\} \ll \frac{1}{\omega C_{\rm gd}}. \tag{21}$$

The proposed SNIM strategy first matches $Z_{\rm opt}^*$ to the source impedance Z_0 with the loading effect of the feedback components included, but without feedback loop gain, then to adjust the loop gain to match $Z_{\rm in}$ to Z_0 without affecting $Z_{\rm opt}^*$ and $F_{\rm min}$. Consider the source inductive degenerated LNA as an example. When matching $Z_{\rm opt}^*$ to Z_0, make $Z_L = 0$ and combine the inductance of the source inductor (L_s) to the gate matching inductor (L_g) such that the loading effects of $C_{\rm gd}$ and L_s are included, but the loop gain of $C_{\rm gd}$ and L_s feedback are equal to zero. Then adjust Z_L and increase L_s, with L_g reduced correspondingly, to adjust the feedback loop gain to match $Z_{\rm in}$ to Z_0. The loop gain adjustment does not affect $Z_{\rm opt}^*$ and $F_{\rm min}$.

For a narrowband LNA at frequency f_0, the design criteria for SNIM are summarized as follows.

1) Apply the smallest channel length for the best transistor performance. From (19), $F_{\rm min}$ increases roughly with

$(C_{\rm gs}+C_{\rm gd})\sqrt{R_g/g_m}$, which can usually be minimized with the shortest channel length.

2) The real part of Z_L should be as small as possible to avoid increasing the difference between $\mathrm{Im}\{Z_{\rm in}\}$ and $\mathrm{Im}\{Z^*_{\rm opt}\}$. This difference introduces a frequency offset between the impedance and noise matching.
3) Given a specified drain current, co-design the transistor size and matching network to make $Z^*_{\rm opt}$ match to the source impedance Z_0 at f_0 with the loading effect of feedback components included.
4) Increase $\mathrm{Re}\{Z_{\rm in}\}$ to match Z_0 without adding noise and changing $\mathrm{Re}\{Z^*_{\rm opt}\}$ with appropriate lossless feedback. A well-known feedback technique is *inductive source degeneration*.

For a prescribed dc drain current (power constraint), $Z^*_{\rm opt}$ is adjusted by varying the transistor size. If the transistor size is increased, g_m increases, R_g decreases, and f_T decreases. From (16) and (19), $\mathrm{Re}\{Z^*_{\rm opt}\}$ decreases, but $F_{\rm min}$ increases. Nonetheless, the $F_{\rm min}$ increase is generally insignificant compared to the noise factor improvement from noise matching.[1] For applications of $f_0 \ll f_T$, this adjustment leads to an extremely low transistor current density (biasing at weak inversion), which may increase sensitivity from process variation and degrade linearity. In this case, an external capacitor in parallel with the transistor $C_{\rm gs}$ to lower f_T is an alternative choice. This increases $F_{\rm min}$ slightly, but helps maintain noise matching with a transistor in moderate inversion.

For broadband applications, both $Z^*_{\rm opt}$ and $Z_{\rm in}$ need to be close to Z_0 over the entire bandwidth. A broadband response requires a high-order input matching network. Equation (16) and (20) show that the frequency dependencies of $\mathrm{Re}\{Z^*_{\rm opt}\}$ and $\mathrm{Re}\{Z_{\rm in}\}$ are different. Hence, the reactive feedback, as described in 4) above, needs to increase $\mathrm{Re}\{Z_{\rm in}\}$ by a *frequency-dependent* amount. This can be realized by employing *multiple reactive feedback* to make $\mathrm{Re}\{Z_{\rm in}\}$ close to $\mathrm{Re}\{Z^*_{\rm opt}\}$ in different frequency regions. Consequently, the design criteria for BSNIM are proposed as follows.

1) Same as above 1) in narrowband cases.
2) Minimize Z_L or employ a capacitive Z_L.
3) With the drain current specified, the transistor size is chosen to make $\mathrm{Re}\{Z^*_{\rm opt}\}$ of the transistor close to the source impedance Z_0 at the center frequency f_c of the passband. Apply a high-order input matching network (typically a ladder *LC* network structure) to make $Z^*_{\rm opt}$ close to Z_0 over the entire band.
4) Increase $\mathrm{Re}\{Z_{\rm in}\}$ to match Z_0 by employing *multiple reactive feedback*.

While multiple reactive feedback is necessary for BSNIM, the loop gain actually results in a higher order impedance function of $Z_{\rm in}$ than that of $Z^*_{\rm opt}$ such that $Z_{\rm in}$ and $Z^*_{\rm opt}$ behave differently with frequency. Nevertheless, this difference can be accommodated with a high-order input matching network if both $\mathrm{Re}\{Z_{\rm in}\}$ and $\mathrm{Re}\{Z^*_{\rm opt}\}$ are designed close to Z_0 in the passband.

The procedure described above enables a BSNIM LNA design, which provides power-efficient noise performance. In Section III, an exemplary *dual reactive feedback technique* is proposed as a BSNIM solution, which has been demonstrated to be effective for broadband LNA design from 3 to 11 GHz (fractional bandwidth larger than 130%). In comparison to the area-saving, but power-hungry, resistive/source-follower feedback amplifier [20]–[23], an SNIM/BSNIM LNA saves a considerable amount of power.

[1]If a large amount of dc power is applied such that the G_n in (20) is very small, the noise matching is less critical for noise performance [6]. However, this is not the power efficient case that the SNIM approach strives for.

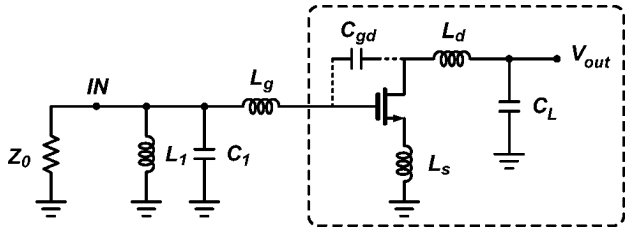

Fig. 6. Proposed BSNIM amplifier.

III. Proposed BSNIM Amplifier

As discussed above, a BSNIM LNA necessitates a high-order matching network and multiple reactive feedback networks. The proposed BSNIM solution is an *LC*-ladder matching network [24] along with a dual reactive feedback topology, composed of capacitive shunt feedback and inductive series feedback, as shown in Fig. 6. The *LC*-ladder matching network and the dual reactive feedback are co-designed following the BSNIM design criteria in Section II-B. Each feedback network attains SNIM in different frequency regions for BSNIM. They are seamlessly combined by employing an inductor L_d at the transistor drain port to obtain different loading conditions for each feedback structure. To quantitatively illustrate the design concept, a 3.1–10.6-GHz UWB LNA designed in 0.18-μm CMOS is employed as an example.

A. Proposed Dual Reactive Feedback Topology

The proposed dual reactive feedback structure and the *LC* ladder input matching network results in $Z^*_{\rm opt}$, represented by the equivalent circuit, as shown in Fig. 7. The $Z^*_{\rm opt}$-to-Z_0 matching bandwidth is extended by the second-order bandpass *LC*-ladder structure. The choice of component values follows the guideline as

$$L_1 \cdot C_1 = (L_g + L_s)\cdot(C_{\rm gs}+C_{\rm gd}) = 1/(2\pi f_c)^2 \qquad (22)$$

where f_c is located at 5.76 GHz, the geometric mean of 3.1 and 10.6 GHz in this design. Bandwidth expansion is determined by the *L/C* ratios, where the preliminary values can be obtained by traditional filter design such as a Chebyshev filter. Slight trimming of *LC* values can compensate for the frequency dependency of $R_{\rm opt}$. For the optimal broadband matching result, $R_{\rm opt}$ is, in general, designed slightly less than Z_0 to make the $S^*_{\rm opt}$ curve circling the Smith chart center over the entire passband. The design of L_1 and C_1 also takes into account the gain response, as will be described later.

While broadband noise matching is achieved, the input impedance is also matched to Z_0 by the proposed dual reactive feedback circuit, as shown via the dashed-line box of Fig. 6. A similar circuit structure was demonstrated with broadband

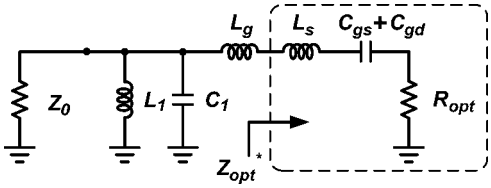

Fig. 7. Equivalent-circuit presentation of $Z_{\rm opt}^*$ to the circuit in Fig. 6.

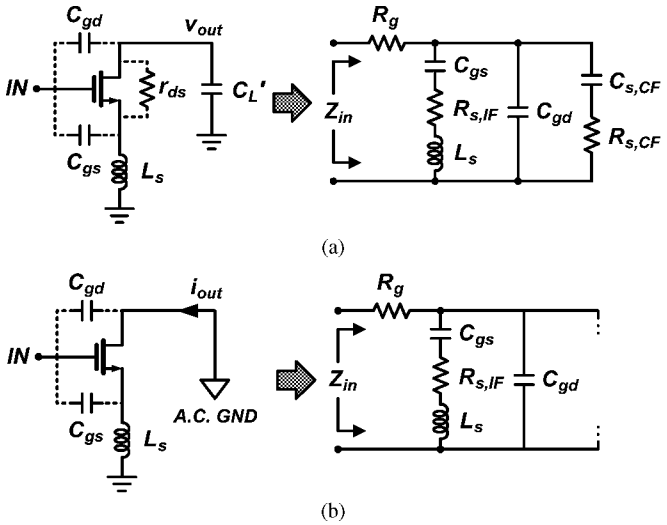

Fig. 8. Input impedance changed among the two feedbacks with frequency. (a) Capacitive shunt feedback in lower frequency region. (b) Inductive series feedback in higher frequency region.

input impedance matching [25]. In contrast to [25], the proposed approach here utilizes each reactive feedback in different frequency regions. This configuration can minimize the difference between $\mathrm{Re}\{Z_{\rm in}\}$ and $\mathrm{Re}\{Z_{\rm opt}^*\}$ over a wide frequency range, and therefore enable BSNIM. In the frequency region much lower than the $L_d - C_L$ series resonance frequency, the $L_d - C_L$ tank behaves like a capacitor C_L' to the transistor. Hence, $Z_{\rm in}$ can be represented by the equivalent circuit shown in Fig. 8(a), where

$$R_{s,\rm IF} = \frac{g_m \cdot L_s}{C_{\rm gs}} \tag{23}$$

$$R_{s,\rm CF} = \frac{C_L' + C_{\rm gd}}{g_m C_{\rm gd}} \approx \frac{C_L + C_{\rm gd}}{g_m C_{\rm gd}} \tag{24}$$

and

$$C_{s,\rm CF} = g_m r_{\rm ds} \cdot C_{\rm gd}. \tag{25}$$

Two noiseless resistances can be found: $R_{s,\rm IF}$ from the series inductive feedback of L_s, and $R_{s,\rm CF}$ from the shunt capacitive feedback of $C_{\rm gd}$ with C_L'. Since $C_{s,\rm CF}$ in (25) is usually much larger than $C_{\rm gs}$, the branch of $C_{s,\rm CF}$ dominates the input impedance in this frequency region such that $R_{s,\rm CF}$ is the noiseless resistance contributing to $\mathrm{Re}\{Z_{\rm in}\}$ to match with $R_{\rm opt}$.

In the higher frequency region close to the $L_d - C_L$ resonance, the output appears as a short circuit at the drain. $Z_{\rm in}$ can be represented by the equivalent circuit, as shown in Fig. 8(b). The $C_{s,\rm CF}$ branch becomes open because the $C_{\rm gd}$ feedback loop

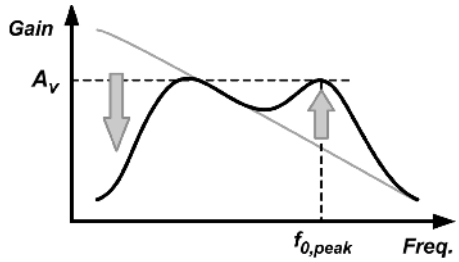

Fig. 9. Gain response of the circuit with dual reactive feedback in Fig. 6. The low-frequency gain is suppressed by L_1 and the high-frequency gain is enhanced by L_d.

gain is approximately zero. The series inductive feedback is significant under this condition and $R_{s,\rm IF}$ is the dominant noiseless resistance in this frequency region.

As shown in (16), $R_{\rm opt}$ of the transistor is inversely proportional to frequency. Its variation is larger than $\pm 70\%$ over the entire frequency range of interest. To make $\mathrm{Re}\{Z_{\rm in}\}$ match with $R_{\rm opt}$, $R_{s,\rm IF}$ is designed to be about half of $R_{s,\rm CF}$, accommodating the required $\mathrm{Re}\{Z_{\rm in}\}$ variation. In practice, the $C_{s,\rm CF}$ branch in Fig. 8(a) has a low-Q property such that the capacitive feedback is active over a larger portion of the frequency range.

The choice of L_1, C_1, and L_g is made in consideration of $\mathrm{Im}\{Z_{\rm in}\}$, making $Z_{\rm in}$ close to Z_0 over the entire frequency range. In practice, L_g results in two resonance frequencies with the transistor circuit. At low frequencies, L_g and $C_{s,\rm CF}$ constitute a resonance tank with the resonance frequency of

$$f_{0,\rm CF} = 1/2\pi\sqrt{L_g C_{s,\rm CF}} = 1/2\pi\sqrt{L_g \cdot g_m r_{\rm ds} \cdot C_{\rm gd}}. \tag{26}$$

For the inductive feedback, the resonance frequency is located at a higher frequency

$$f_{0,\rm IF} = 1/2\pi\sqrt{(L_g + L_s) \cdot (C_{\rm gs} \| C_1)}. \tag{27}$$

Therefore, the frequency dependence of $Z_{\rm in}$ turns out to be an order higher than that of $Z_{\rm opt}$. In this design $f_{0,\rm CF}$ and $f_{0,\rm IF}$ are located at 5 and 9 GHz, respectively. As to the choice of L_d, it is expected to tune out C_L to accommodate the inductive feedback

$$L_d \cdot C_L \approx 1/(2\pi f_{0,\rm IF})^2. \tag{28}$$

As the input matching is sensitive to the output impedance Z_L with $C_{\rm gd}$ feedback, the proposed BSNIM amplifier is not unconditionally stable. An unwanted resonance could occur whereas Z_L behaves inductive at frequency higher than $f_{0,\rm IF}$. This can be controlled by making a quality factor of $R_d' - L_d - C_L$ network lower than a certain value. Here, R_d' is the effective output resistance of the transistor to be discussed in Section III-B. Meanwhile, a good output-to-input isolation should be provided in the succeeding stage for good overall stability. To meet this requirement, we employ a cascode amplifier as the second stage, as will be shown in Section IV.

B. Gain Response

As mentioned in Section II-A, a sufficiently high gain over the entire band is necessary to reduce the noise contribution of succeeding stages. The proposed BSNIM amplifier is expected

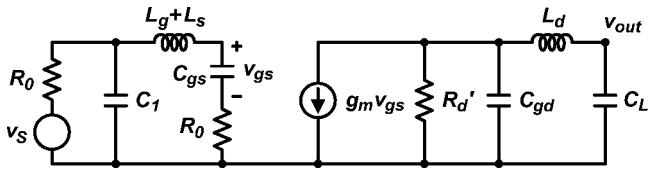

Fig. 10. Equivalent circuit for gain derivation at $f_{0,\mathrm{Peak}}$.

to fulfill this gain requirement. This design concept is shown in Fig. 9. The gain response is mainly shaped by the drain network in Fig. 6 as the input network is a broadband structure. Based on the low-pass response by C_L (the gray curve in Fig. 9), L_d creates series gain peaking at the frequency

$$f_{0,\mathrm{Peak}} = 1/2\pi\sqrt{L_d \cdot (C_{\mathrm{gd}} \| C_L)} \tag{29}$$

which is higher than $f_{0,\mathrm{IF}}$ in (27). The voltage gain at this frequency can be derived with the circuit approximation, as shown in Fig. 10, where R_d' is the effective output resistance of the transistor at frequency higher than $f_{0,\mathrm{IF}}$ as

$$R_d' \approx \frac{C_{\mathrm{gs}} + C_{\mathrm{gd}}}{g_m C_{\mathrm{gd}}}. \tag{30}$$

The gain in the lower out-of-band frequency is suppressed by the input shunt inductor L_1. As a result, a gain peak is formed at the lower band edge. The magnitude of this peak is designed close to the peak gain at the higher band edge such that the expected gain response is the solid curve in Fig. 9. With this design approach, the voltage gain is determined at $f_{0,\mathrm{Peak}}$, which is designed at 11 GHz.

The gain response of this amplifier is composed of the two gain peaks at both band edges. If a flat gain over a very wide bandwidth is desired, an additional mid-band gain peak by the next stage is necessary to compensate the mid-band sag. This case applies to our 3–11-GHz UWB LNA. On the other hand, if the required bandwidth is moderate, such as the 2–6-GHz application in [18], a flat gain response is obtainable by this stage itself as the two gain peaks can be designed fairly close to each other.

C. Transformer for Inductive Series Feedback

The proposed dual reactive feedback amplifier, as shown in Fig. 6, requires four inductors that may occupy a large die area. To reduce the inductor number and die area, transformer feedback is proposed to replace the three inductors L_g, L_d, and L_s, as shown in Fig. 11(a). With transformer feedback, L_g' and L_d overlap, sharing the same die area with mutual inductance M to constitute a transformer. The mutual inductance M senses the drain current and contributes series voltage feedback at the input similar to the series-series feedback function of L_s in an inductive source degenerated amplifier. By neglecting the C_{gd} feedback effect and the transformer feed-forward coupling at the frequency of interest, the input impedance can be approximately represented by the equivalent circuit, as shown in Fig. 11(b), in which $L_g' = L_g + L_s$ and

$$R_{s,TF} = \frac{g_m \cdot M}{C_{\mathrm{gs}}} \tag{31}$$

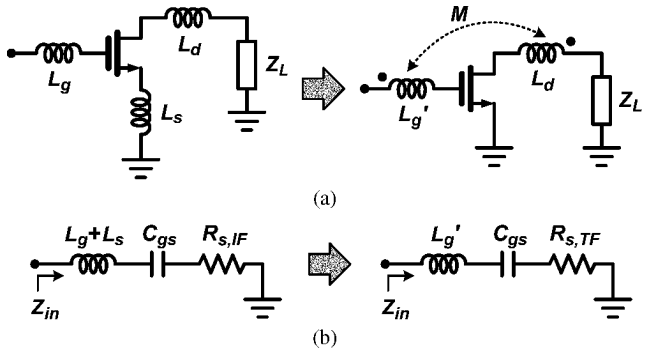

Fig. 11. (a) Inductive source degeneration feedback can be substituted by the transformer feedback. (b) Their equivalent circuit for input impedance.

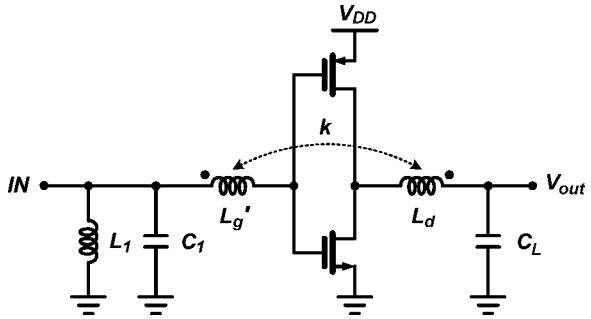

Fig. 12. Proposed dual reactive feedback amplifier with transformer feedback.

which provides the wanted noiseless resistance similar to $R_{s,\mathrm{IF}}$ in (23). The above assumption is valid for the general source inductive degenerated amplifier design.

This transformer feedback topology is also beneficial in that the transistor source is connected to ground directly. This allows the amplifier to be implemented with a CMOS inverter structure, which employs both NMOS and PMOS to reuse drain current for high transconductance. The final schematic diagram of the proposed BSNIM amplifier is shown in Fig. 12. Here, the mutual inductance is represented by the coupling factor k with the relation $M = k\sqrt{L_g' \cdot L_d}$.

Since M is generally much smaller than L_g' and L_d, the coupling factor k is much smaller than 1. Design simulations show that the optimal k value is slightly less than 0.2. Possible layout schemes that facilitate a weakly coupled transformer include common-centric coils and overlapped coils, as shown in Fig. 13. Generally, the common-centric coils have a better quality factor, but occupy more die area. In the design example in Section IV, the common-centric coil was adopted for better performance.

IV. Design Example: 3–11-GHz UWB LNA

A design example of a 3–11-GHz UWB LNA employing the proposed BSNIM amplifier is shown in Fig. 14 [16]. In this prototype design, the inverter amplifier $(M_{1P}-M_{1N})$ is self-biased with a 10-kΩ feedback resistor. C_{gs} of M_2 plays the role of C_L in Fig. 12. L_2 between M_2 and M_3 further increases the gain peak at the higher band edge. The body of M_3 is biased to its source with a 10-kΩ resistor. L_3 and R_3 provide voltage gain with a low-Q peak at the center frequency to compensate the mid-band gain dip by the first stage. M_o and M_{ob} constitute the

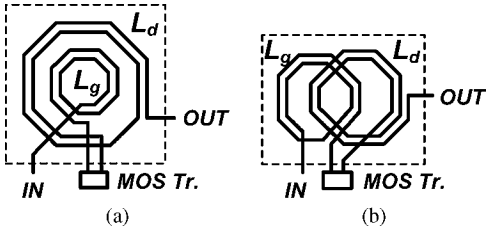

Fig. 13. Possible layout schemes of a weak coupling transformer. (a) Common-centric coil. (b) Overlapping coil.

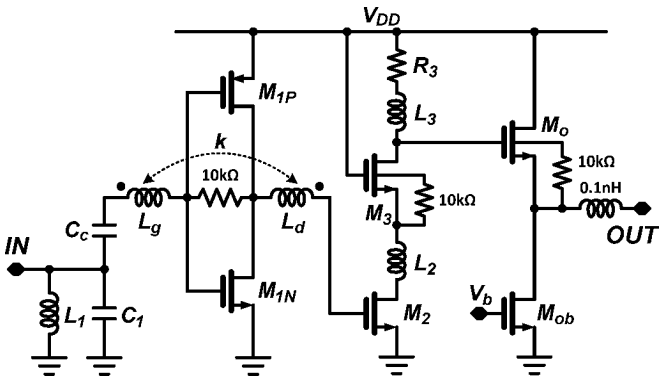

Fig. 14. 3–11-GHz UWB LNA as a design example of the proposed BSNIM amplifier.

TABLE I
DEVICE VALUES OF THE 3–11-GHz UWB LNA

Transistor	M_{1N}	M_{1P}	M_2	M_3	M_o	M_{ob}
Width (μm) (Length:0.18μm)	80	160	35.2	35.2	70	35

Device	L_1	C_1	C_c	L_g	L_d	k	L_2	L_3	R_3
Value	2.4nH	262fF	4pF	1.4nH	2.6nH	0.18	1.3nH	4.7nH	128Ω

Note: The values here are of the practical devices, which in some degree deviate from the theoretical values with the device parasitic effects.

output buffer and the 0.1-nH output inductor improves the 50-Ω output match. The detailed design parameters of the devices are listed in Table I.

Simulation were performed with Agilent Technologies' Advanced Design System (ADS). S_{11} and $S^*_{\rm opt}$ of the LNA is shown on the Smith chart on the left side of Fig. 15. On the right side of Fig. 15 is the result without L_1 and C_1 to show how the dual reactive feedback enables BSNIM. $\mathrm{Re}\{Z^*_{\rm opt}\}$ can be observed to decrease as the frequency increases. At low frequencies, the plot shows that $\mathrm{Re}\{Z_{11}\}$ appears close to $\mathrm{Re}\{Z^*_{\rm opt}\}$ over a large frequency range, but begins to deviate around 7.5 GHz. The resonance due to the transformer feedback helps reduce this deviation. As shown in the plot, however, the improvement is limited to a small frequency region up to 11 GHz.

$\mathrm{Re}\{Z^*_{\rm opt}\}$ and $\mathrm{Re}\{Z_{11}\}$ in the higher frequency region are slightly larger than the expected because of the parasitic capacitance of L_g. With the addition of L_1 and C_1, the order of matching network is increased such that S_{11} and $S^*_{\rm opt}$ both move toward the center of Smith chart, achieving broadband matching. With this high-order matching network, the noise

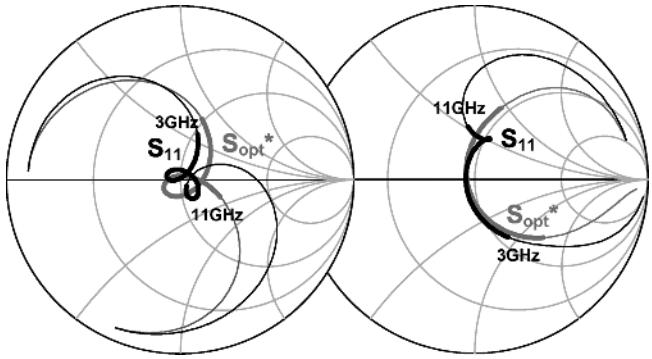

Fig. 15. On the left is the simulated S_{11} and $S^*_{\rm opt}$ of the designed UWB LNA. The bold face section of each curve represents the results in frequency range from 3 to 11 GHz. On the right is the result without L_1 and C_1.

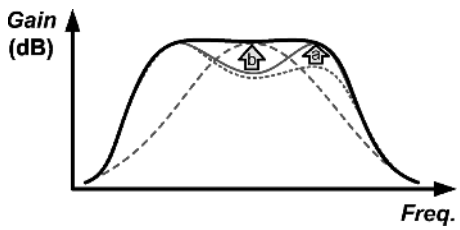

Fig. 16. Gain response trimming in the second stage. a: High-band expansion by L_2. b: Mid-band compensation by L_3 and R_3. The bold black curve is the expected result.

matching and input matching performance are also robust with process variations.

The second stage of the LNA is a CS–common gate (CG) cascode amplifier providing output-to-input isolation for the good circuit stability. It also compensates the LNA gain for a flat in-band response: L_2 further peaks the gain response at the higher band edge with series peaking, and L_3 and R_3 provide low-Q shunt peaking at mid-band, as shown in Fig. 16. The third stage is an output buffer.

This LNA was designed in a TSMC 0.18-μm CMOS process with aluminum metal. It was designed to achieve >15-dB return loss, <4-dB maximum in-band NF, >10-dB power gain with less than 0.5-dB in-band variation, and <0.1-ns maximum group-delay variation while consuming <10 mW of power from a 1.5-V supply. The broadband noise performance is mainly limited by the input matching network where the resistive losses substantially increase $F_{\rm min}$.

Figs. 17–20 show the simulation and measurement results. Also included are the post-layout simulation results with the transistor model in the slow–slow (SS) corner, which are found closer to the measured results. Fig. 17 shows the measured S_{11} and $S_{\rm opt}$ from an ATN NP-5 noise parameter analysis system. Both have good in-band matching to 50 Ω. Fig. 18 shows the power gain S_{21}. The measured S_{21} closely matches simulations with a transistor model from the SS corner, but is about 5-dB lower than that in the typical–typical (TT) corner. The NF and circuit minimum NF $(\mathrm{NF}_{\rm min})$ are shown in Fig. 19, where the NF is very close to $\mathrm{NF}_{\rm min}$ in the passband. The measured in-band NF is less than 5 dB. Fig. 20 shows the noise parameter R_n. As can be observed in Figs. 19 and 20, the broadband noise matching maintains the NF even as R_n varies. The mea-

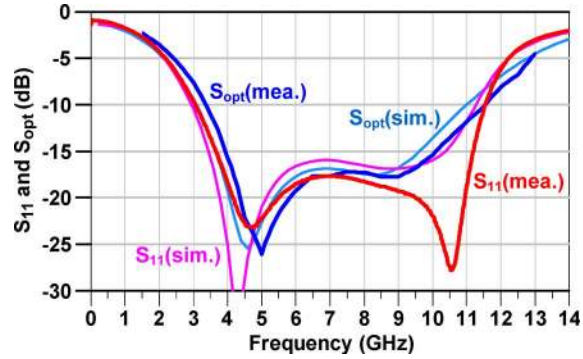

Fig. 17. Measured and simulated S_{11} and $S_{\rm opt}$.

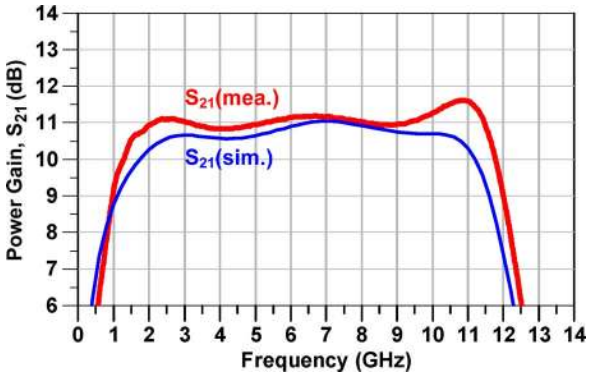

Fig. 18. Measured and simulated S_{21}. The simulation is with the transistor model of the SS corner.

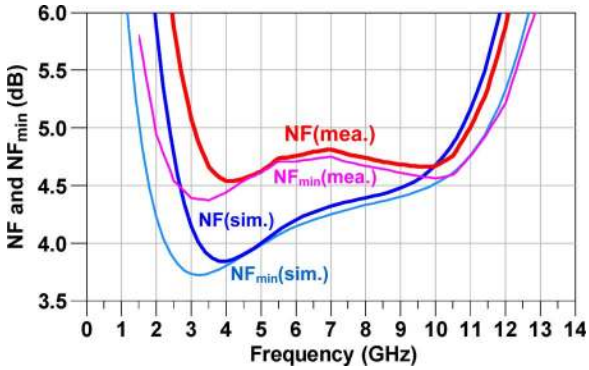

Fig. 19. Measured and simulated NF and $\rm NF_{min}$. The simulations are with the transistor model of the SS corner.

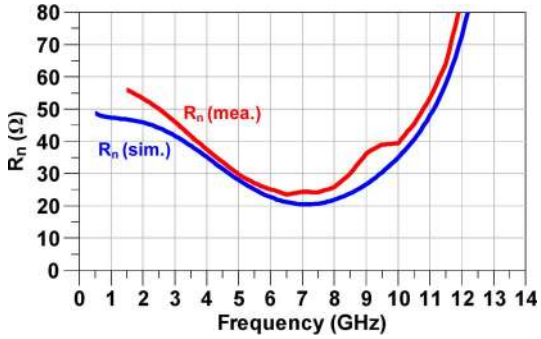

Fig. 20. Measured and simulated R_n.

sured third-order intermodulation intercept point (IIP3) is about -12 dBm. Linearity is degraded by the voltage gain of the first stage driving the gate of M_2 (Fig. 14). The power consumption without the output buffer is 9 mW from a 1.5-V supply. The performance is summarized and compared with other UWB LNAs in Table II. The simulation and measurement results validate the proposed BSNIM solution.

V. Conclusion

The SNIM technique is important for power-efficient noise performance of an LNA. A successful approach for broadband simultaneous noise and impedance matching (BSNIM) on a CS amplifier has been demonstrated. The root causes of $Z_{\rm in}$-to-$Z^*_{\rm opt}$ discrepancy of a MOS transistor were analyzed and the SNIM/BSNIM design criteria were proposed. Reactive feedback to equalize the real part of $Z_{\rm in}$ and $Z^*_{\rm opt}$ are essential for SNIM. The proposed BSNIM technique employs dual reactive feedbacks and an *LC* ladder matching network to accommodate a wide bandwidth. Band handover between the two reactive feedback paths is facilitated by a drain inductor L_d. Transformer feedback is employed to provide the same series-series feedback with a reduced die area.

The design example of a 3–11-GHz UWB LNA shows a robust BSNIM condition is achieved for an application having over 130% fractional bandwidth. The noise contribution of the nonideal input matching network is found to be as significant as that of the transistor. The low NF up to 11 GHz is maintained on a 0.18-μm CMOS process. Another design example in 0.13-μm CMOS [18] also shows the benefit of low power and low noise employing the proposed BSNIM technique.

Appendix

The input-referred noise sources are obtained by calculating the corresponding output noise voltages for a short-circuited input and the open-circuited input cases, and then divide them by the signal gain to obtain the input-referred voltage and current noise sources, respectively [26]. This method, however, makes the equations very complicated, making the effects of device components on $Z^*_{\rm opt}$, as well as the correlation of equivalent noise sources, confusing.

The noise analysis developed in this study includes noise model simplification and the equivalent noise source conversion. The model simplification is for a CS amplifier with noiseless feedback networks, as illustrated in Fig. 21(a), in which Z_{FS} and Y_{FP} contribute no noise. $\overline{v^2_{n,g}}$ is the equivalent voltage noise source at the gate representing the noise contribution from $\overline{i^2_{nd}}$ and $\overline{i^2_{n,L}}$, where the latter is a drain-referred noise current source of the succeeding stages,[2] including the noise by Z_L. $\overline{v^2_{n,g}}$ is equal to

$$\overline{v^2_{n,g}} = \left(\overline{i^2_{nd}} + \overline{i^2_{n,L}}'\right) \Big/ g^2_m. \tag{A1}$$

Here, $\overline{i^2_{n,L}}'$ is equal to $\overline{i^2_{n,L}} \cdot |1 + g_m Z_\beta|^2$, where Z_β is the equivalent feedback transimpedance of the total feedbacks from drain current i_d to gate voltage $v_{\rm gs}$ via Z_{FS} and Y_{FP}. With $\overline{v^2_{n,g}}$, the noise model in Fig. 21(a) can be simplified to the model in Fig. 21(b) by simply observing that Z_{FS} and Y_{FP} load the transistor gate, where Z_{FS} is in series and Y_{FP} is in

[2]By the two-port noise theory, noise contribution of the succeeding stages can be represented as a pair of correlated voltage and current noise sources at output of the CS-Amp. With the given output impedance (Z_L and $C_{\rm gd}$), the two noise sources can be further merged as one current noise source $i^2_{n,L}$.

TABLE II
COMPARISON OF BROADBAND LOW-NOISE CS AMPLIFIER

Ref.–Year	CMOS Technology	Feedback Topology	Frequency Coverage (GHz)	Max. Noise Figure (dB)	Min. Power Gain (dB)	Max. S_{11} (dB)	Min. IIP_3 (dBm)	Supply Voltage (V)	DC Power (mW)	Active Area (mm^2)
[13] –2004	0.18µm	Source Inductive Deg.	2.3 – 9.2	8	9.3	-9.4	-16	1.8	9	0.66
[18] –2007	90nm	Source-Follower	DC – 6.0	3.2	17.4	-10	N/C	1.2	9.7[a]	0.019
[19] –2007	0.13µm	Resistive/Source-Follower	1.0 – 7.0	3.0	17	-10	-4.1	1.2	25	0.0017
[20] –2007	90nm	Resistive/Source-Follower	0.5 – 7.0	2.9	21	-7.2	-10.5	1.2	12	0.012
[21] –2008	90nm	Resistive	0.2 – 9.0	7.8	7	-11	-9.5	1.2	20[a]	0.066
[15] –2007	0.13µm	Source Ind. Deg. & Shunt-Series Transformer feedback	3.1 – 10.6	3.0	-13.7	-9.9	-8.5	1.2	9	0.4
This work [14]	**0.18µm**	**Shunt Capacitive & Series Transformer feedbacks**	**3.1 – 10.6**	**5.1 / 4.5**	**11 / 14**	**-11**	**-12**	**1.5 / 1.8**	**9 / 21**	**0.46**
Alt. work [16]	**0.13µm**	**Shunt Capacitive & Series Transformer feedbacks**	**2.4 – 5.4**	**3.1**	**22**	**-12**	**-21**	**1.0**	**4.6**	**0.49**

[a] Differential LNA.

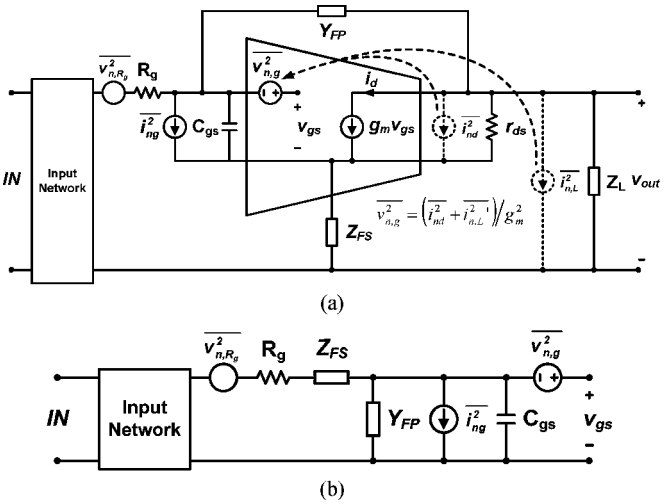

Fig. 21. Developed simplification technique for noise parameters derivation. (a) General case for the CS amplifier with lossless feedback networks. (b) Equivalent circuit for noise analysis.

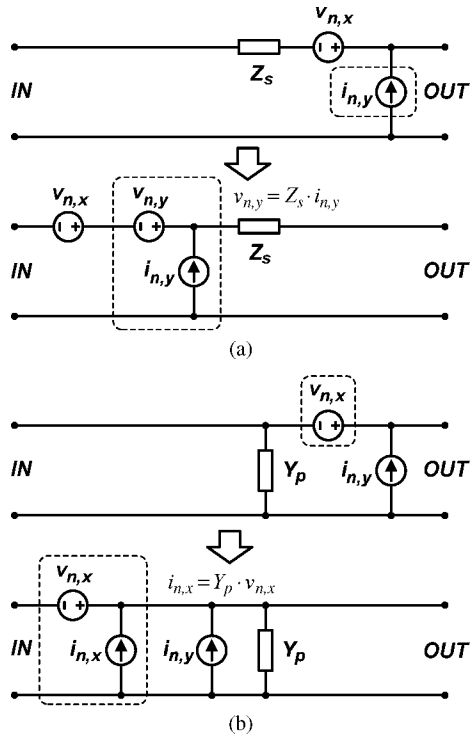

Fig. 22. Two elementary cases of equivalent noise sources conversion over passive devices: (a) in series and (b) in parallel to the input port.

parallel with $C_{\rm gs}$. This is based on the principle that the equivalent input referred noise sources of a feedback amplifier are equal to those of same amplifier with the feedback loop opened [26]. In our derivation of the input-referred voltage and current noise sources with the input shorted and opened, respectively, this simplification is valid with the condition that $g_m \gg |Y_{FP}|$ and $f/f_T \gg |Z_{FS}|/r_{\rm ds}$, which is usually satisfied.

With this simplified model, the derivation of input referred noise sources can simply start from the input of the voltage-controlled current source, i.e., $v_{\rm gs}$ in Fig. 21(b). When this model is applied to the transistor noise model in Fig. 2, $C_{\rm gd}$ plays the role of Y_{FP}, Z_{FS} is equal to 0, and $\overline{i_{n,L}^2}$ is not included. The effect of $\overline{i_{n,L}^2}$ will be discussed at the conclusion of this Appendix. Note that the equivalent circuit in Fig. 21(b) is only for noise analysis and should not be used for input impedance analysis.

When referring these noise sources in Fig. 21(b) to the input, the equivalent noise source conversion, a derivative concept from the equivalent noise four-poles [27], can be applied. As shown in Fig. 22(a), the shunt current noise source $i_{n,y}$ after a passive device Z_S in series with the input port has input-referred noise sources including the original $i_{n,y}$ and a series voltage noise source $v_{n,y}$ fully correlated to $i_{n,y}$, whereas the series voltage noise source $v_{n,x}$ remains unchanged at the input. The total input-referred voltage noise source $v_{n,i}$ can be obtained by combining $v_{n,x}$ and $v_{n,y}$. Note that the direction of the noise sources in Fig. 22 carries the correlation information between noise sources. In comparison with [27], the opposite direction of current sources is adopted such that the correlation factor is positive when Z_S is resistive.

$v_{n,x}$ and $v_{n,y}$ should be combined by employing the 3-D vector operation, as shown in Fig. 23. Assume any vector along the direction of unit vector $\hat{a}_z$ is uncorrelated to $i_{n,y}$, then $v_{n,x}$ can be seen as a combination of two orthogonal vectors: one along $\hat{a}_z$ and the other on the z-plane, a complex plane perpendicular to $\hat{a}_z$. Any complex vector on the z-plane is fully correlated to $i_{n,y}$. Here, $\hat{a}_y$ is defined as the direction *in phase* with

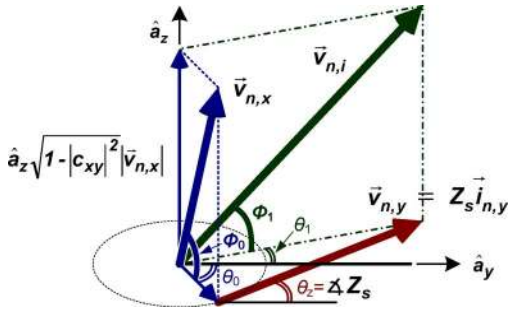

Fig. 23. 3-D vector operation to combine the two partially correlated voltage noise sources in Fig. 22(a).

$i_{n,y}$. The correlation factor cxy between $v_{n,x}$ and $i_{n,y}$ is equal to $\cos\Phi_0 \cdot e^{j\theta_0}$, in which $\cos\Phi_0$ is the absolute value of the correlation factor and θ_0 is the phase difference between $v_{n,x}$ and $i_{n,y}$, as shown in Fig. 23. In Fig. 23, all the θ's and $\vec{v}_{n,y}$ are on the z-plane. After the vector addition of $\vec{v}_{n,x}$ and $\vec{v}_{n,y}$, the total input-referred noise voltage $v_{n,i}$ can be obtained with the correlation to $i_{n,y}$ equal to $\cos\Phi_1 \cdot e^{j\theta_1}$, where θ_1 is the phase difference between $v_{n,i}$ and $i_{n,y}$.

The equivalent noise source conversion for a passive device in parallel with the input port can be derived in the same manner as shown in Fig. 22(b). The noise contribution from Z_s and Y_p in Fig. 22 can be included in $v_{n,x}$ and $i_{n,y}$, respectively. By alternately applying conversions as in Fig. 22(a) and (b), the input referred noise sources can be obtained. Noise parameters such as $Z^*_{\rm opt}$, G_n (or $Y^*_{\rm opt}$, R_n), and $F_{\rm min}$ can be derived with the two-port noise theory introduced in [1].

The effect of $\overline{i^2_{n,L}}$ on noise parameters depends on the feedback, as shown in (A1) with $\overline{i^2_{n,L}}' = \overline{i^2_{n,L}} \cdot |1+g_m Z_\beta|^2$. The more feedback, represented by the larger Z_β, results in the lower gain of LNA and the less attenuation of noise from the succeeding stages, yields to the larger $\overline{i^2_{n,L}}'$. One can replace $\gamma g_m/\alpha$ in (13)–(19) with $[\gamma g_m/\alpha + \overline{i^2_{n,L}} \cdot |1 + g_m Z_\beta|^2/4kT\Delta f]$ to include $\overline{i^2_{n,L}}$ into the noise parameters. It is found that both $\overline{i^2_{n,L}}$ and Z_β increase G_n and $F_{\rm min}$, and decrease $\mathrm{Re}\{Z^*_{\rm opt}\}$. The decrease of $\mathrm{Re}\{Z^*_{\rm opt}\}$ reduces the discrepancy between $Z^*_{\rm opt}$ and $Z_{\rm in}$. We observe that feedback loop gain affects noise parameters only when $\overline{i^2_{n,L}}$ is included in the analysis because $\overline{i^2_{n,L}}$ is outside the feedback loop. Nonetheless, if the CS amplifier has sufficiently high gain such that the effect of $\overline{i^2_{n,L}}$ is negligible compared to $\overline{i^2_{nd}}$, the loop gain has almost no effect on the noise parameters.

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Chang-Tsung Fu (S'00–M'09) received the B.S. degree in communication engineering, and the M.S. and Ph.D. degrees in electrical engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1996, 2001, and 2009, respectively. His doctoral research concerned broadband low-noise amplification theory and circuit techniques for RF front-ends.

In 2006, he was with the Intel Corporation, Hillsboro, OR, as an Intern, during which time his research was focused on CMOS WiFi T/R switch design. He is currently with the Intel Laboratory, Intel Corporation, as a Research Scientist dedicated to pathfinding wireless front-end design in advanced CMOS technology.

Chien-Nan Kuo (S'93–M'97) received the B.S. degree in electronic engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1988, the M. S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1990, and the Ph.D. degree in electrical engineering from the University of California at Los Angles (UCLA), in 1997.

In 1997, he joined ADC Telecommunications, San Diego, CA, as a Member of Technical Staff with the Mobile System Division, where he was involved in wireless base-station design. In 1999, he joined Broadband Innovations Inc. In 2001, he joined the Microelectronics Division, IBM. In 2002, he joined the faculty of National Chiao Tung University, Hsinchu, Taiwan, as an Assistant Professor. His research interests include reconfigurable RF circuit and system integration design, low-power design for the application of wireless sensor networks, and development of circuit-package co-design in the system-in-package (SiP) technique.

Dr. Kuo was the recipient of the Best Paper Award presented at the 13th IEEE International Conference on Electronics, Circuits, and Systems in 2006.

Stewart S. Taylor (S'74–M'77–SM'99–F'08) received the Ph.D. degree in electrical engineering from the University of California at Berkeley, in 1978.

He is a Senior Principal Engineer with the Intel Laboratory, Intel Corporation, Hillsboro, OR, where he has been since January 2003. His current research focus is on radio architecture and circuit design that leverages the strengths and compensates for the weaknesses of CMOS technology. Prior to joining the Intel Corporation, he was with Tektronix, TriQuint, and Maxim. He has taught part-time at Portland State University, Oregon State University, and the Oregon Graduate Institute for 30 years, and has served on the graduate committees of seven Ph.D. students. He has authored or coauthored over 50 publications. He holds 51 patents with 17 pending.

Dr. Taylor served on the Program Committee of the International Solid-State Circuits Conference for ten years, chairing the Analog Subcommittee for four years. He was the conference program chair in 1999. He was an associate editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He was the recipient of the IEEE Third Millennium Medal for Outstanding Achievements and Contributions from the IEEE Solid-State Circuits Society.