Low-noise current excitation sub-system for medical EIT

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Low-noise current excitation sub-system for medical EIT

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Abstract. Electrical Impedance Tomography (EIT) has many potential applications in medicine. The sensitivity and spatial resolution of EIT can be enhanced significantly by increasing measurement signal-to-noise ratio (SNR), to which a significant contribution is made by the SNR of the current excitation sub-system. In this paper we present a prototype EIT current excitation subsystem with 80 dB SNR, exploiting both digital and analogue techniques. It uses digital waveform synthesis, a 16-bit DAC and subsequent reconstruction filter, to drive an enhanced Howland current source. Detailed analysis and testing of the current sub-system is presented. Its output impedance is 10 MΩ for different load impedances, varying slowly over the frequency range from 10 kHz up to 4 MHz.

Keywords: Current source, digital, analogue, EIT, low-noise

1. Introduction

The required sensitivity for EIT instrumentation varies according to the nature of the clinical application (Boone and Holder, 1996). It has been suggested that an EIT system with measurement sensitivity of 80 dB is required for measurement of impedance changes in the brain occurring directly due to neural function (Polydorides et al., 2002; Towers et al., 2000), an application that requires measurement bandwidths ranging from several hundreds of Hz to several kHz, depending on the measurement strategy adopted. Typical signal levels for this application are of the order of 10 mV (Murrieta-Lee et al., 2004). The brain's processing of a short stimulus leads to changes in regional blood flow after about 4 − 6 s. When exposing volunteers to repetitive (8 Hz) visual stimuli, (Tidswell et al., 2001) reported that correspondingly delayed changes in brain impedance can be monitored with SNR about 60 dB for measurement bandwidth about 10 Hz, leading to a frame rate of 1 every 25 s, i.e. 0.04 fps. By direct measurement with electrodes inserted into the brains of cats subject to visual and auditory stimuli, (Galambos and Velluti, 1968; Klivington, 1975; Klivington and Galambos, 1967; Klivington and Galambos, 1968) measured changes of the resistance of brain tissue that occur on the same timescales after stimulus (tens to hundreds of milliseconds) as observed in evoked potentials, and simultaneous with evoked potentials. Those authors also observed that this so-called Evoked Resistance Shift (ERS) decreased monotonically from 1 kHz to 100 kHz, by about an order of magnitude.
In our work, it is intended to achieve a frame rate of 100 fps with measurement SNR 80 dB. Many factors contribute to measurement SNR in EIT, and one critical limit is the precision of current excitation. Many researchers reported the output impedance of the current source, as discussed below, but to our knowledge the SNR performance of the current excitation sub-system has not been addressed in the literature.
Further demands on the current excitation sub-system arise from the fact that the skin-electrode contact has significant impedance (around 1 kΩ) which, when coupled to the limitations of EIT instruments, results in significant effects on image quality (Boone and Holder, 1996). Ideally the applied current should be independent of the load. In reality, however, current sources are limited because their output impedance shunts source current away from the load (see figure 1). Therefore the relationship between the applied current i_L

and the source current i_S varies with the value of the load impedance Z_L. The output impedance of the current source is usually defined as a parallel combination of resistance R_O and capacitance C_O as shown in figure 1. Therefore, in a multi-frequency EIT system the output impedance, Z_O, of the current source reduces as the frequency increases. Constant output impedance for the enhanced Howland current source up to 100 kHz has been reported in the literature (Bertemes-Filho et al., 2000; Cheng et al., 2006). To compensate for output impedance changes at higher frequencies due to the capacitive component of the current source output impedance, various ways are proposed by (Bragos et al., 1994; Ross et al., 2003; Terzopoulos et al., 2005) which result in complexity in the design of the current source or in a requirement to retune whenever the frequency is changed. Such approaches cannot be applied in systems with wide frequency ranges.

The variation of output current amplitude with frequency is made worse by the presence of additional stray or parasitic capacitances C_S due to leads, printed circuit board tracks and switches (Ross et al., 2003; Saulnier, 2005). The difference between i_S and i_L, in addition to causing errors in image reconstruction, also leads to errors in system calibration (Cook et al., 1994).
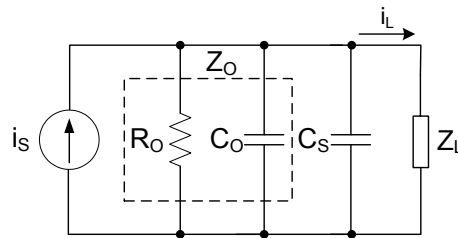

Figure 1- Norton equivalent circuit of a real current source
with the presence of stray capacitance.

In this work we have designed and tested a current excitation subsystem with 80 dB SNR at measurement bandwidths of several kHz, to operate over the current excitation frequency range of 10 kHz to 100 kHz. This has been achieved by a combination of optimised Direct Digital Synthesis (DDS) of a waveform using a Field-Programmable Gate Array (FPGA), careful conversion to the analogue domain via a 16-bit Digital-to-Analogue Convertor (DAC) followed by an 8th order reconstruction filter, and voltage-to-current conversion using an enhanced Howland circuit as a voltage-controlled current source (VCCS). A schematic of the current excitation sub-system is shown in figure 2. Each of these steps is described further below, along with data on the performance achieved at the various stages. The requirements of the current source are translated to frequency response, transient performance, voltage compliance, and output impedance, as well as precision expected in terms of SNR.
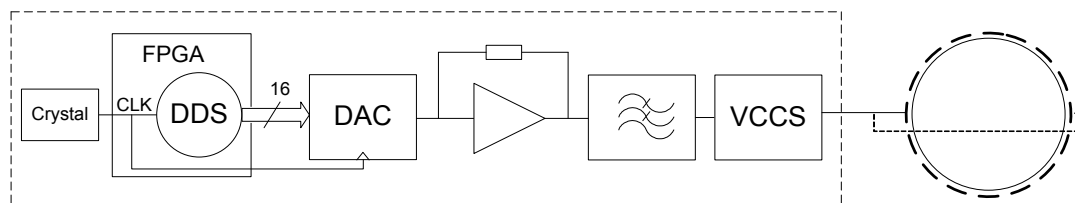

Figure 2- Current excitation subsystem of EIT system.

2. Circuit Design

2-1. Waveform Synthesizer

2

The Xilinx Spartan 3-1000 FPGA was used in this work. Digital samples of the sine-wave are generated with 16-bit resolution and with frequencies in the range of 10 kHz to 100 kHz. The DDS Scheme was implemented using the available DDS Intellectual Property (IP) core (Xilinx Inc., 2005). To achieve overall 80 dB SNR for the current excitation subsystem, the digital signal has to be generated with SNR significantly better than 80 dB. As can be seen in figure 3, the DDS consists of two main parts: a lookup table and a phase increment module. The lookup table stores the samples of a sinusoidal waveform. The phase increment module is used to generate a suitable phase argument that is presented to the address port of the lookup table and is mapped by the lookup table. The SNR of the digital signal generated by recalling samples from the lookup table is affected by both the phase and amplitude quantisation of the process. These limits are equivalent to time-base jitter and to amplitude quantisation of the signal, and these add, respectively, spectral modulation lines and white broad-band noise floor to the signal's spectrum (Xilinx Inc., 2005).

The time-base jitter due to phase quantization results in undesired phase modulation that is proportional to the quantization error. The spectral artefacts of time-base jitter are periodic error sequences with peak distortion level related to incidental phase modulation. The peak distortion level is consistent with 6 dB/bit of address space (Xilinx Inc., 2005). In other words, to achieve X dB of suppression of the peak distortion in the output waveform, the DDS lookup table must have at least $B_{\theta(n)} = \lceil X/6 \rceil$ address bits. In turn, this requires a $\lceil X/6 \rceil$-bit phase accumulator, which translates to a $2^{\lceil X/6 \rceil}$ bit-deep table. Choosing a higher precision output sample, however, does not have any effect on the time-base jitter (Xilinx Inc., 2005).

The output resolution of the DDS is specified by setting the spurious free dynamic range (SFDR) via the DDS user interface. The number of bits of the phase accumulator $B_{\theta(n)}$ (where $\theta(n)$ is the phase angle and n is the time-series sample index) is determined by (Xilinx Inc., 2005)

$$B_{\theta(n)} = \log_2 \left\lceil \frac{f_{clk}}{\Delta f} \right\rceil \tag{1}$$

where Δf is the frequency resolution and f_{clk} is the clock frequency.

Due to the limitation of memory resources inside the FPGA there is a limitation in the number of bits that can be used for the phase accumulator, viz. 32 (Xilinx Inc., 2005). Hence, for a given clock frequency, there is a restriction on defining the frequency resolution in the DDS user interface.

In this work, the SFDR is set to 96 dB in order to generate an output sine wave with 16 bit resolution. Based on the available clock frequency for the DDS in our system, the frequency resolution of the output waveform is chosen conservatively to set the phase accumulator to use the maximum 32-bit address words, ensuring the peak distortion due to the time-base jitter is significantly below the main signal level and hence below the noise floor.
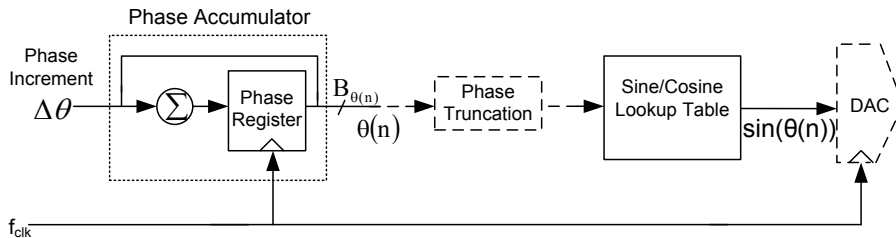

Figure 3. DDS block diagram.

2-2. Digital to Analogue Converter

Factors affecting the noise content of the DAC output are considered more fully in (Saulnier, 2005) but, in general, increasing the DAC resolution and/or sampling frequency reduces the noise density. A 16-bit DAC is used to convert the digital sine wave to an analogue voltage waveform. The SNR limit of a data converter, due to quantisation noise, is given in terms of the number of bits available by (Kester and Bryant, 2005)

$$SNR = 6.02 \times N + 1.76 \qquad dB \qquad (2)$$

where N is the DAC resolution. For a 14-bit DAC, equ. 2 yields 86.04 dB and for a 16-bit DAC, 98.08 dB. Practical DACs also have other sources of error which appear as lower-order harmonics of the fundamental. Both quantization noise and the non-ideal DAC properties produce a response that consists of harmonically related spurs of the fundamental. Practical converters therefore have SFDR values considerably less than the theoretical SNR of quantization noise given by equ. (2). To decrease the magnitudes of these spurs it is necessary to use a DAC with greater resolution (Brandon and Analog Devices Inc, 2004). Therefore, by using a 16-bit converter, we obtain SFDR performance in excess of 80 dB from DC to Nyquist, effectively ensuring that the DAC will not degrade the overall measurement performance.

The noise density due to the DAC itself can be expressed as:

$$v_{NQ} = \frac{A}{2^N \sqrt{12f_s}} \qquad V/\sqrt{Hz} \qquad (3)$$

where A is the peak-to-peak voltage range of the waveform (2.8 V in our case), and f_S is the sampling frequency. We use f_S = 6 MHz, providing 14 dB of noise floor reduction through oversampling, relative to our maximum Nyquist frequency of 200kHz.

A reconstruction filter is used to smooth the output of the DAC. The filter used in this work is a 4-bit digitally controlled 8th.-order low-pass filter, LTC1564, (Linear Technology corporation, 2001). The cut-off frequency (f_C) is adjustable from 10 kHz to 150 kHz in steps of 10 kHz. The filter gives approximately 100 dB attenuation at a frequency equal to 2.5 times f_C. The gain of the filter is programmable from 1 to 16 in unit steps. The variable gain capability at the input is an integral part of the filter and increases low level input signals with little increase in output-referred noise. This enhances the SNR at lower signal levels by enabling the use of gain in the pass-band. This is a very useful feature for our application as it enables the full resolution of the DAC output to be used and then straightforwardly scaled to achieve the desired current amplitude to the patient.

2-3. Voltage-Controlled Current Source (VCCS)

VCCS circuits that provide controllable means of current injection into variable load impedance are commonly used in EIT systems. In this work the maximum rms value of current ranges from 1 mA to 10 mA, depending on frequency based on the BS EN 60601-1 standard (BSI British Standards). A comparison was made of various current source circuits presented in the literature (Bragos et al., 1994; Cheng et al., 2006; Cook et al., 1994; Denyer et al., 1993; Ross et al., 2003; Saulnier, 2005). The Howland current source was felt to offer the best solution as it combines high performance and simplicity. We have built the classical Howland current source, shown in figure 4. When driven by the system described in sections 2-1 and 2-2, the output current of the classical circuit showed 80 dB SNR (see discussion of methods in section 3). The two capacitors, C_1 and C_2, are employed to avoid circuit oscillation at higher frequencies due to the presence of both positive and negative feedback. In the literature these two capacitors are recommended to be small, around 10 pF (Franco, 1998;

Ross et al., 2003). The output impedance of the classical circuit at DC was around 4.5 MΩ and degraded significantly over the frequency range up to 100 kHz.
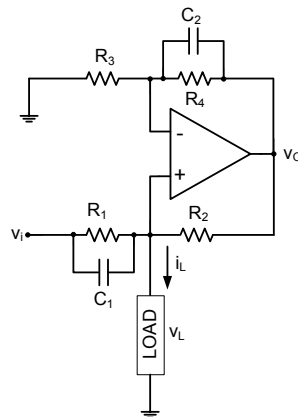

Figure 4-Classical Howland current source.

Consequently, we have designed and built an enhanced Howland current source (Franco, 1998), as shown schematically in figure 5. This circuit has some immediate advantages over the classic Howland current source. One is that by splitting R_2 to R_{2A} and R_{2B} the consumption of power by the R_1 resistor is reduced (Franco, 1998). The unwanted power consumption by R_1 heats it and can potentially change its value depending on its temperature coefficient. This unbalances the resistor bridge formed by R_1, R_2, R_3 and, R_4. The second advantage of the enhanced Howland current source is that larger resistor values can be selected to deliver the same current as the classical circuit with the same voltage compliance. This reduces the effect of the length of PCB tracks on the balancing of the resistors. In the classical Howland current source, generating 1 mA rms current in the output when the input voltage is equal to 1 V rms, requires R_1 equal to 1 kΩ. R_2 and R_4 need to have significantly less resistance in comparison to R_1 and R_3 to improve the voltage compliance, around 100 Ω (Franco, 1998).
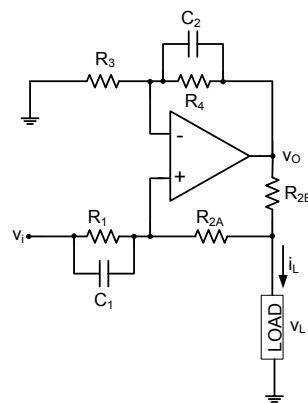

Figure 5- Schematic diagram of enhanced Howland current source.

The DC output impedance R_O of a circuit can be calculated by grounding the input signal and replacing the load with a voltage source v_{TEST}. The output impedance R_O is then given by:

$$R_O = v_{TEST} / i_{TEST} \tag{4}$$

where, in the case of the circuit given in fig. 5, i_{TEST} is given by

$$i_{TEST} = \frac{v_{TEST} - v_O}{R_{2B}} + \frac{v_{TEST}}{R_{2A} + R_1} \tag{5}$$

and v_O is given by

$$v_O = \frac{R_3 + R_4}{R_3} v \tag{6}$$

where v is the input voltage of the op-amp, $v = v_+ = v_-$ and v_{TEST} is given by

$$v_{TEST} = \frac{R_{2A} + R_1}{R_1} v \tag{7}$$

From equations (4) – (7) R_O is given by

$$R_O = \frac{R_3 R_{2B}(R_{2A} + R_1)}{R_3(R_{2A} + R_{2B}) - R_1 R_4} \tag{8}$$

To achieve infinite output impedance, the resistors R_1, $(R_{2A}+R_{2B})$, R_3 and, R_4 must form a balanced bridge, that is:

$$\frac{R_{2A} + R_{2B}}{R_1} = \frac{R_4}{R_3} \tag{9}$$

In this condition the load current is given by

$$i_L = \frac{R_2/R_1}{R_{2B}} v_I \tag{10}$$

where v_I is the input voltage.

The voltage compliance (i.e. the maximum load voltage v_L at which the output current continues to behave linearly) for the enhanced Howland current source is approximately (Franco, 1998)

$$|v_L| \leq |v_{SAT}| - \frac{R_2}{R_1}|v_I| \tag{11}$$

where v_{SAT} is the output saturation voltage of the op-amp given in the datasheet.
Therefore to achieve 1mA rms current output when the input voltage is 1V rms, we chose $R_1 = R_3 = R_4 = 2\,k\Omega$ and $R_{2A} = R_{2B} = 1\,k\Omega$, as shown in figure 6.
In practice, the resistor balancing will be imperfect because of tolerances as well as the effect of finite open-loop gain of the op-amp on the transfer characteristics of the circuit (Franco, 1998). In the work reported here, precision (0.01%) resistors with low temperature coefficient ($2\,ppm/°C$), and an operational amplifier with high open-loop gain, were chosen to ensure high output impedance. Highly symmetric PCB layout, with well balanced track resistances, is essential in maintaining the performance of this circuit.
The limiting effect of the finite open-loop gain of the op-amp on the output impedance of the Howland current source is discussed in more detail in (Franco, 1998). By selecting these values of resistance for the enhanced Howland current source circuit, this limiting effect can be reduced by more than a factor 4 when using the same op-amp. In the enhanced Howland current source, the effect of finite op-amp open-loop gain (a) on the output impedance is given by

$$R_O = ((R_1 + R_{2A})\|R_{2B}) \times \left(1 + \frac{a}{1 + R_2/R_1}\right) \tag{12}$$

6

The AD8021 is chosen as the op-amp for its wide bandwidth. It has a variable gain-bandwidth product using a single compensation capacitor, which allows the user to optimise this property for the application. In our case C_C is set at 7 pF. Using the AD8021, increasing the compensation capacitor is one way to compensate for the capacitive loads at higher frequencies. If necessary, to prevent circuit oscillation at high frequencies, in the presence of capacitive load, C_1 and C_2 values of 0.1 pF are adequate. Experiments showed that increasing the value of these capacitances degrades the transfer function of the circuit noticeably at higher frequencies. The AD8021 which is used in 16-bit resolution systems, has low total harmonic distortion and input voltage noise density (2.1 nV/$\sqrt{\text{Hz}}$) (Analog Devices Inc., 2006). Using the AD8021, the voltage compliance of the output is $|v_L| = 9V$.
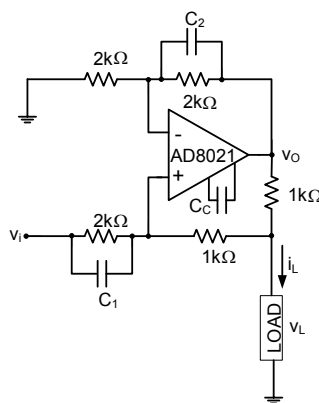

Figure 6- Schematic diagram of the enhanced Howland current source used in this work.

3. Test Methods and Results

Spectral analysis, using an HP 3585A (Hewlett-Packard) with 1 MΩ input impedance, has confirmed the quality of the analogue signal generated. Figure 7 shows the spectral composition of the reconstruction filter output for a 10 kHz signal. The spectral peak is at 10,000.0 Hz and for 1 V rms signal, the 80 dB SNR requirement has been confirmed. Similar results have been seen for the generation of other excitation frequencies up to 100 kHz.

Figure 7 shows the spectrum obtained with 100 Hz resolution bandwidth (RBW) and 300 Hz video bandwidth (VBW). Narrow RBW is used for detailed examination of distortion products and the actual noise level of the circuit, since it improves the frequency resolution and lowers the internal noise level of the spectrum analyzer (Hewlett-Packard Company, 1978). Reducing the resolution bandwidth below 100 Hz, however, makes the sweeping time excessively long.

The intended function of the VBW setting of this instrument is to reduce the display fluctuations, by averaging the values of sets of displayed points. However we wish to see the true signal noise. Therefore in the work described here, VBW is typically set to be three times the value of RBW.

The apparent width of the peak is an artefact due to the sweeping mode of the spectral analyser measurement system. When the RBW of the analyzer is set to 3 Hz (minimum) and VBW is set to 30 kHz (maximum), the excitation signal FWHM is about 16 Hz.
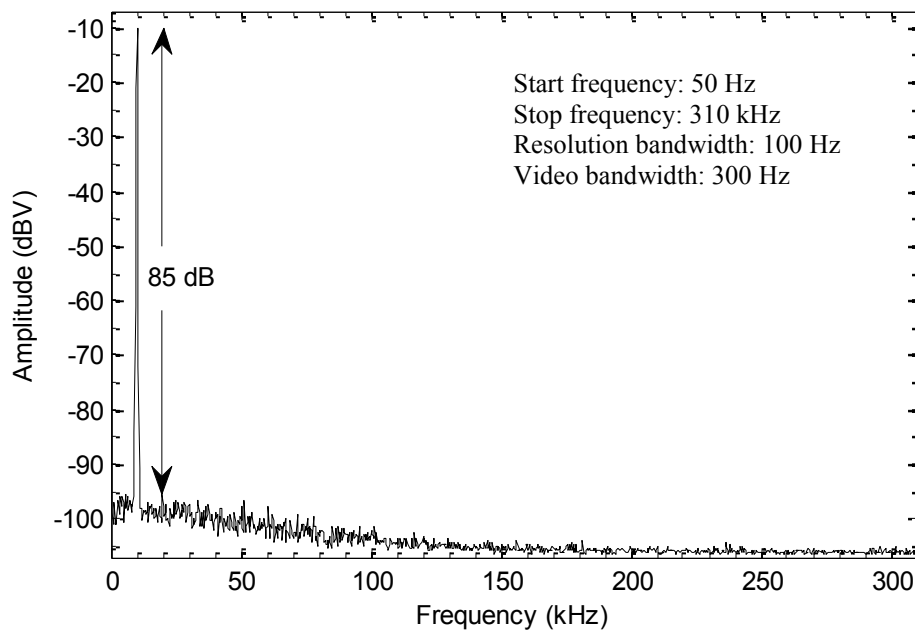
Figure 7- Analogue sine-wave spectrum with resolution bandwidth of 100 Hz for 10 kHz excitation frequency.

Similar settings on the HP 3585A are used to analyse the SNR performance of the VCCS for all the excitation frequencies, when driven by the system described in sections 2-1 and 2-2. Figure 8 shows a typical VCCS output spectrum, whilst driving a 1 kΩ load at 10 kHz. For 100 Hz RBW, the SNR of the current excitation waveform is found to be better than 80 dB over the frequency range 10 kHz – 100 kHz. With this analyser, therefore, it is not possible to detect any degradation of the waveform due to the VCCS, over 10 kHz – 100 kHz.
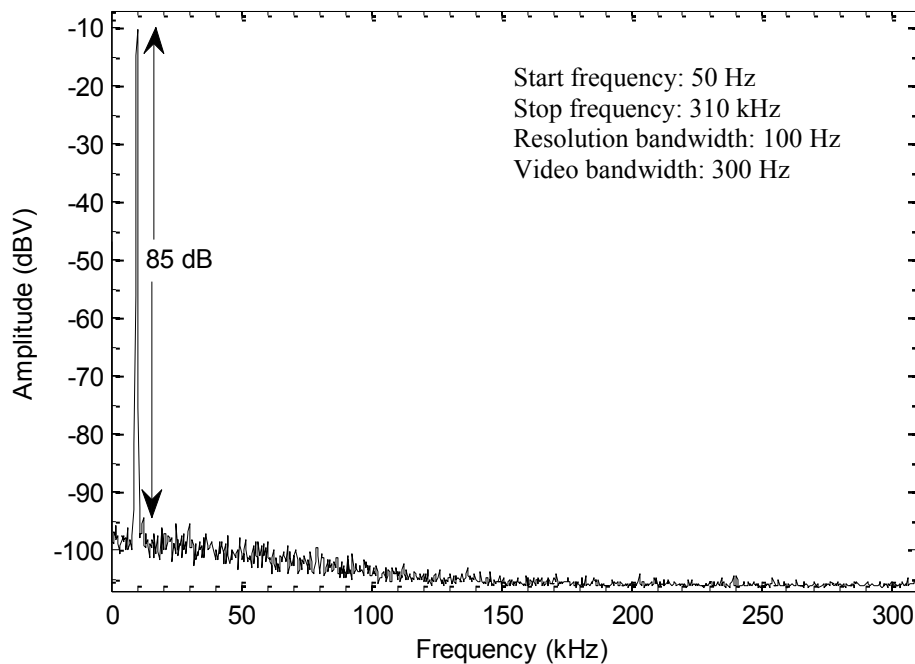

Figure 8- VCCS output spectrum with resolution bandwidth of 100 Hz for 10 kHz excitation frequency and a 1 kΩ load.

The output impedance of this circuit has been measured using a network analyser HP 4195A (Hewlett-Packard), for resistive loads from 1 $k\Omega$ to 10 $k\Omega$, and additional capacitive loads from 100 pF to 1.5 nF. (These values have been measured in a parallel project in our lab, using electrodes attached to human skin, as intended for the brain function monitoring application (Robinson et al., 2008).) Figure 9 shows the transfer function of the enhanced Howland current source with loads of 1.3 $k\Omega$, 1.3 $k\Omega\|1nF$ and 1.3 $k\Omega\|1.5nF$. The transfer function in the work presented here is defined as the ratio of the voltage across the input impedance of the network analyser to the input voltage of the enhanced Howland current source. Figure 10 shows the transfer function of the circuit with loads of 2.7 $k\Omega$, 2.7 $k\Omega\|1nF$ and 2.7$k\Omega\|1.5nF$. For the purely resistive load of 2.7 $k\Omega$, the -3 dB cut-off frequency of the transfer function is 8.7 MHz.

Figure 9- Transfer function of enhanced Howland current source with 1.3kΩ purely resistive load, and in parallel with 1nF and1.5nF.
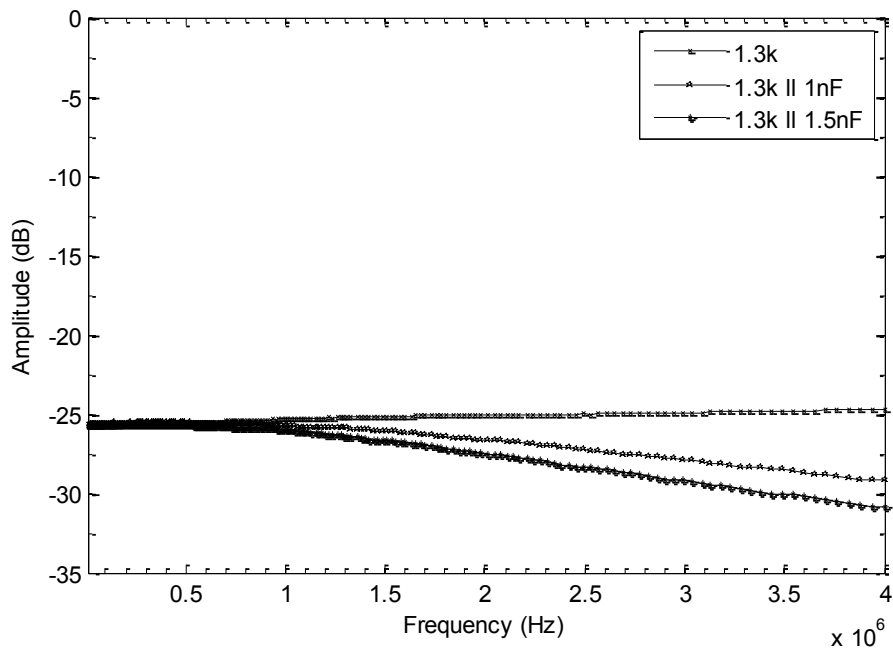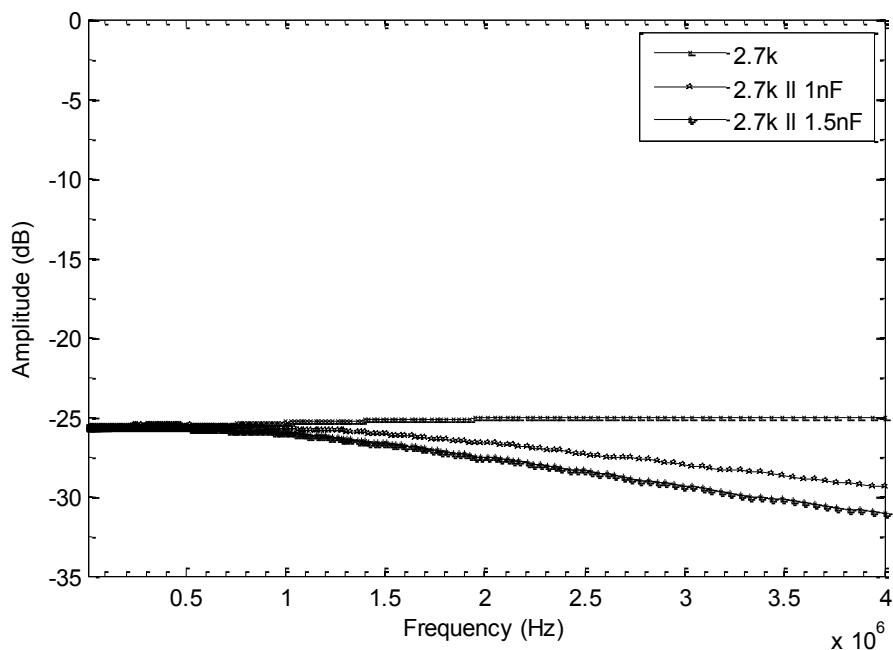
Figure 10- Transfer function of enhanced Howland current source with 2.7kΩ purely resistive load, and in parallel with 1 nF and 1.5 nF.

To calculate the output impedance using the transfer function of the circuit, a simplified model of the circuit is used, as can be seen in figure 11. The output resistance of the current source is estimated from the amplitude transfer function at low frequencies. The capacitive component of the output impedance can then be obtained from the -3dB point of the amplitude transfer function.
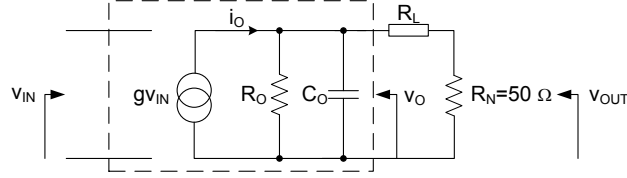

Figure 11- Simplified model of the Howland current source to measure output impedance.

The input impedance of the network analyser, R_N, is $50\,\Omega$ and R_L is the load. In this circuit V_{OUT} is

$$v_{OUT} = \frac{R_N}{R_L + R_N} v_O \tag{13}$$

where v_O is given by

$$v_O = i_O \left(R_O \| X_{C_O} \| (R_L + R_N) \right) \tag{14}$$

and i_O is given by

$$i_O = g \times v_{IN} \tag{15}$$

The transfer function based on the simplified model of the current source is

$$H(j\omega) = \frac{v_{OUT}}{v_{IN}} = g \times R_N \times \frac{\left(R_O \| \dfrac{1}{j\omega C_O} \| (R_L + R_N) \right)}{R_N + R_L} \tag{16}$$

R_O can be calculated from equation (15) at low-frequencies. Since the transconductance gain, g, is unknown, the value of R_O is obtained by measuring the transfer function for two different loads R_{L1} and R_{L2} at very low frequency. Hence R_O is given by:

$$R_O = \left(H_2 (R_{L2} + R_N) - H_1 (R_{L1} + R_N) \right) / (H_1 - H_2) \tag{17}$$

The output capacitance can be measured from the transfer function at the f_{-3dB} frequency as follows:

$$H(j2\pi f_{-3dB}) = 1/\sqrt{2} \tag{18}$$

$$C_O = (R_O + R_L + R_N) / (2\pi f_{-3dB} R_O (R_L + R_N)) \tag{19}$$

From equation (17) and (19) and the measurements obtained we calculate that the output resistance and capacitance of the enhanced Howland current source designed and built here are $R_O = 10\,M\Omega$ and $C_O = 6.65$ pF. It should be noted that the performance of the current source may be enhanced further by using matched resistor sets with 0.005% tolerance (VISHAY, 2006).

4. Discussion and Conclusion

In this paper the design and performance of a current excitation sub-system for a medical EIT system has been discussed. This system combines high-performance digital and analogue elements and will form the basis of a new EIT instrument, currently under construction. It is designed to operate at frequencies from 10 kHz to 100 kHz. The digital element of the design is a waveform synthesizer with 96 dB SNR. The associated analogue circuitry has been designed to 80 dB SNR throughout. Experimental tests have verified this performance.

Comparison has been made between the classical Howland current source and the enhanced Howland current source. The performance of the enhanced Howland-based current excitation circuit has been validated up to 4 MHz. This frequency is beyond the maximum operational frequency in our intended EIT system, but it is common to apply the EIT technique in the MHz range, and this design may have relevance to those applications.

The enhanced Howland current source designed here yields excellent output impedance performance for EIT application. The values measured here being 10 MΩ resistive in parallel with 6.65 pF capacitive. This performance owes much to optimal choice of circuit components and careful PCB design.

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