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Low Noise NMOS Imager Fabrication with a Study on the

Effect of Photodiode Shape on Dark Current

Steven Taylor

A Thesis Submitted to the Graduate Faculty of

GRAND VALLEY STATE UNIVERSITY

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Abstract

The purpose of this project was to fabricate a low noise N-type Metal-Oxide-Semiconductor (NMOS) imager in the Grand Valley State University (GVSU) Cleanroom with a focus on reducing pixel dark current. Previous research suggests Photodiode (PD) shape affects dark current and charge transfer characteristics of the pixel. Five PD shapes were designed to determine an optimized pixel shape with respect to dark performance. PN junction PDs with the Three Transistor (3T) pixel architecture were found to be the most suitable for imager fabrication in the GVSU cleanroom. The integrated circuit layout of several 8x8 pixel arrays was designed to test the influence of PD shape on dark current. The fabricated PDs exhibited dark current in the range of 9-18uA/cm^2. The results indicate PDs with "rounder" geometry exhibit improved dark response; however, small saturation to cutoff current ratios prevented imager functionality. Improved charge transfer as a result of triangular PD shape was suggested but may have been masked by higher dark currents in these shapes.

A low noise Voltage and Sample and Acquisition Controller (VSAC) was developed to capture the output from the imager die and transfer the data to a computer. The VSAC was designed for flexible timing and voltage control while exhibiting low noise. Analysis with a logic analyzer verified timing flexibility which allowed the integration, reset, and other control pulses to be optimized for the application. Reset voltage control circuitry allowed a wide range of analog voltages to be supplied to the imager reset transistors. This prevented image lag due to incomplete reset. The noise performance of the VSAC was characterized by sampling a known voltage and observing the output deviation. With an output voltage accuracy of 99 percent to the input signal and less than 3.6 mV_{RMS} output noise, the VSAC exhibited excellent low noise operation.

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Abbreviations

3T – Three Transistor
4T – Four Transistor
ADC – Analog to Digital Converter
APS – Active Pixel Sensor
BOE – Buffered Oxide Etch
CCD – Charge Coupled Device
CDS – Correlated Double Sampling
CMOS – Complementary Metal-Oxide-Semiconductor
DDS – Delta Difference Sampling
EHP – Electron-Hole Pair
ENIG – Electroless Nickel Immersion Gold
FD – Floating Diffusion
FF – Fill Factor
FOX – Field Oxide
IC – Integrated Circuit
MUX – Multiplexor
NMOS – N-type Metal Oxide Semiconductor
PD – Photodiode
PPD – Pinned Photodiode
PPS – Passive Pixel Sensor
RS – Row Select
RST – Reset
SEM – Scanning Electron Microscope
SF – Source-Follower
SOG – Spin on Glass
VSAC – Voltage and Sample Acquisition Controller

1 Introduction

Electronic cameras have traditionally been fabricated in one of two ways. The traditional Charge-Coupled Device (CCD) photodetector was first conceptualized in the 1970's at Bell Laboratories [1]. The second type of photodetector is the Complementary Metal-Oxide-Semiconductor (CMOS) imager. CMOS imagers are similar to CCDs in that they are based on MOS technology; however, the integration and charge transfer circuitry of the CMOS imager are implemented locally at each pixel allowing for individual pixel referencing. Although CMOS imagers were conceptualized around the same time period as CCDs, CMOS imagers did not see wide adoption until the late 1990s [2]. The pixel architecture of the CMOS imager requires smaller feature than CCD imagers for practical implementation. As trends in Integrated Circuit (IC) technology allowed for smaller features to be reliably fabricated, the realization of practical CMOS imagers became possible.

The different imagers exhibit different device characteristics. Table 1.1 shows the advantages of each type of imager as compared to the other [2]. The lower power consumption and lower cost of CMOS imagers has led to a significant effort in improving the quality of images obtained with CMOS technology and nearly ubiquitous adoption of the CMOS imager in consumer electronics.

Table 1.1 - Comparison between CMOS imagers and CCD photodetectors.

CMOS Imagers	**CCDs**
Power consumption	Sensitivity
Fabrication cost	Quantum efficiency
On chip functionality	Noise
Miniaturization	Dynamic Range
Random access of image data	Image Quality
Selective readout mechanism	
High speed imaging	
Avoidable blooming and smearing effects	

Unlike CCDs, CMOS imagers can be fabricated in a standard CMOS process so the fabrication cost, integration density, and on chip functionality are improved over CCDs. Currently, the best performing CMOS imagers are fabricated in a non-standard CMOS process to utilize the Pinned Photodiode (PPD) structure [3]. The PPD exhibits low dark current (current that flows through the diode under no illumination), but because it cannot be fabricated in a standard process, the realization of a high performance CMOS imager fabricated in a standard process has significant cost saving implications.

In CMOS imagers the output voltage is ideally directly proportional to the level of irradiation incident to the Photodiode (PD). However, in real devices, circuit noise introduces output variability that leads to degradation of image quality. Although the readout and amplification circuitry lead to noise in CMOS imagers, the light sensing element sets the fundamental limit on image quality in CMOS imagers [4]. Typically, a PD or some variation thereof is used as the light sensing element, and the optimization of such a device can greatly affect the overall imager performance. The dark current is the most significant source of noise during the integration period [5]. Because of this, the mitigation of the dark current in CMOS imagers can lead to substantial improvements in image quality.

1.1 Previous Research

Several strategies have been applied to the fabrication of CMOS imagers with the intention of reducing dark current. In response to the findings that a narrower PD junction results in reduced dark current, Ji and Abshire implemented a pixel biasing technique intended to reduce the PD junction width [6]. Similarly, the pseudo active pixel developed by Shih and Wu attempted to minimize dark current through the use of a PD operating in photoconductive mode and a scheme to bias the PD near 0V [7]. Wuu *et al* report lower dark current and dark signal

non-uniformity (DSNU) associated with the non-silicide source/drain technique applied to PD structures [8]. Takenaka *et al* were able to reduce dark current to <1nA through gas phase GeO_2 passivation of Ge photodetectors in a waveguide geometry [9].

The majority of dark current in pn-junction PDs is generated in the bird's beak formed at the interface between the Field-Oxide (FOX) and the doped region. Wu *et al* proposed two alternative structures to minimize dark current generated at the PD periphery as well as minimize surface damage during implantation [10]. The proposed designs resulted in decreased dark current and improved spectral response as compared to standard PD designs.

Historically, the most successful reduction in dark current in CMOS imagers came from the adaptation of the CCD PPD to CMOS imagers. The PPD uses a thin p^+ layer applied over the n-type doped region to "pin" the PD. The p^+ implant isolates the charge collection region of the PD from the FOX interface and surface traps which results in significant reductions in dark current. Additionally, the PPD improves spectral response and quantum efficiency especially at short (blue) wavelengths [11]. Mheen *et al* report the design considerations of Four Transistor (4T) CMOS imager which require careful design to optimize charge transfer characteristics especially at lower operating voltages [12].

Shcherback, Belenky, and Yadid-Pecht investigated the effect of PD periphery shape on the dark-current [13]. It was found that PD shapes with less acute angles or "rounder" shapes resulted in less dark current than shapes with sharper corners. Sharp corners are more stressed and consequently contain a higher concentration of defects than rounder geometries.

Shin, Park, and Shin modified the shape of the typical square PD to determine how a tapered shape would affect the charge transfer of during imager readout [14]. It was found that a

triangular PD shape created an electric field gradient which assisted charge transfer during readout. The resultant triangular design exhibited 50 percent higher output voltage over the square PD and improved image lag due to faster readout.

1.2 Benchmark

Furtado, Diniz, and de Lima Monteiro published the results of the fabrication of a simple N-type Metal-Oxide-Semiconductor (NMOS) imager with geometries similar to the current design [15]. Although the fabrication process used in the research of Furtado *et al* uses ion implantation (versus spin on dopant in the GVSU process), the presented numbers serve as good benchmark for designs on this scale.

The benchmark design has a minimum feature size of 10µm with 200µmx200µm square PDs and transistors with aspect ratios of 2:1 and 4:1. The PDs have dark current density of 375nA/cm^2 at 5V reverse bias. The pixels are saturated in dark conditions after 48s and the PD has an estimated capacitance of approximately 10pF. The 2:1 transistors a drain current of 705µA (V_{GS}=V_{DS}=V_{DD}) and a cutoff current of 14pA. The transistors have a gate threshold voltage of 0.65V.

1.3 Purpose of Current Research

The purpose of this research was to fabricate a low noise NMOS imager implementing a large-area low-dark-current PD in the GVSU cleanroom. In current imagers, pixel dark current is often reduced using PPDs fabricated in a non-standard CMOS process. However, the GVSU process is designed for NMOS fabrication and alternative methods for implementing a pixel with low dark current were explored. The research of Shcherback *et al* demonstrates dark current improvement in relationship to the angle and number of internal and external corners of the PD. In order to maintain a high FF, only PDs with rounded external corners were designed for the

purposes of reducing pixel dark current in the current research. This technique was then applied to the triangular pixel reported by Shin *et al* to determine if rounded PD corners would maintain the voltage elevating effect of the triangular pixel while minimizing dark current.

To ensure the captured imager output was representative of PD array noise rather than readout noise, a low noise readout circuit (VSAC) was developed. The research suggests pixel performance is dependent upon operating voltage and circuit timing. To allow for flexible control of the operational parameters, an off-chip control circuit was devised. Because of the high noise associated with the readout bus of an embedded output, the circuit was designed to sample and hold the imager output as the data is digitized. Typically two sampling circuits and a differential amplifier are implemented at the imager output to facilitate Delta Difference Sampling (DDS) or Correlated Double Sampling (CDS). However, the small array size of the current design minimizes processing requirements which allows these functions to be implemented programmatically. This removes inherent noise in the processing circuits while allowing for greater device flexibility.

2 Theory

2.1 MOS Imagers

In its most basic form, the MOS imager is an array of pixels made up of a photosensitive element, typically a PD, and a charge transfer mechanism. Each pixel outputs a voltage corresponding to the intensity of light incident to the photosensitive element during integration which can be correlated to a black/white level after charge readout. Various filters and lenses can be applied to yield color imagers and improve the quality of the image.

The Passive Pixel Sensor (PPS) was the first conceptualized type of MOS imager. The PPS circuit contains a single transistor which allows this design to have a higher Fill Factor (FF) than Active Pixel Sensors (APS) created with similar design rules. PPS have been demonstrated with dynamic range (DR) of 10^4-10^5 and noise of 250 electrons root-mean-square (RMS) [16]. The lack of pixel level amplification circuitry in the PPS leads to high readout noise due to noise associated with the capacitance of the column bus.

APS address the noise issues of PPS through the use of amplification, reset, and readout circuitry. The simplest APS designs utilize three transistors; however, more transistors can be added at the expense of FF [17]. Similar to the PPS pixel the Reset (RST) transistor (see Figure 2.1) serves to reset the PD voltage to V_{DD} prior to integration. The Source-Follower (SF) transistor is implemented as a source-follower amplifier with a voltage gain of one which

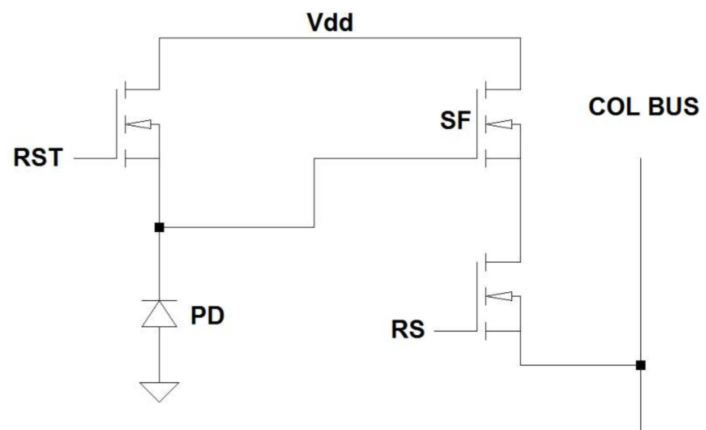


Figure 2.1 - 3T APS Pixel Circuit

improves the current sourcing abilities of the integrating node. The amplified integrated charge at the source of the SF transistor is then transferred to the column bus through the operation of the Row Select (RS) transistor. The inclusion of the SF transistor in the three transistor (3T) pixel significantly improves the signal to noise ratio of the APS over the PPS. The SF amplifier allows for nondestructive readout and buffering at the integrating node.

The 4T pixel (Figure 2.2) further improves the noise characteristics of the 3T APS by implementing a PPD along with a charge transfer (TX) transistor. The PPD improves pixel dark current and spectral response by isolating the charge collection from surface and interface traps while capturing charges generated by short wavelengths. In the standard pn-junction PD of the 3T pixel, photo-generated Electron-Hole Pairs (EHP) typically recombine prior to diffusing to the depletion region.

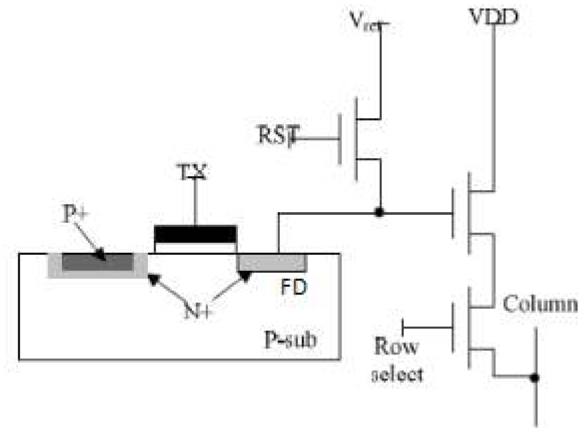


Figure 2.2 - 4T pixel circuit.

The TX transistor in the 4T pixel with a PPD facilitates charge transfer from the high capacitance of the PPD to a lower capacitance of the Floating Diffusion (FD) node. Thus, the conversion gain of the pixel is large as compared to the 3T pixel which improves imager noise performance. If designed properly, the two junctions in the PPD effectively push integrated charge from the integrating node to the FD when the TX transistor is turned on. If the PPD is designed incorrectly and is not fully depleted during TX operation, remaining electrons generate a thermal (kTC) noise component that degrades image quality [12].

Aside from the operation of the TX transistor in 4T pixels, operation of the 3T and 4T pixel are nearly the same. The timing diagram of a typical 3T pixel is shown in Figure 2.3. Initially, the RST transistor is pulsed to return the voltage across the PD capacitance to the reset voltage. As incident light generates EHPs, the voltage across the PD capacitance decreases. The charge stored on the PD capacitance is buffered by the SF amplifier which is then stored as a voltage at the RS node. After the integration period, the RS transistor is pulsed to transfer the charge along the column bus. External to the pixel array, there typically exists sampling circuitry to implement correlated double sampling (CDS) in 4T or delta difference sampling (DDS) in 3T pixels. The sample and hold signal (SHS) and sample and hold reset (SHR) allow for the caputure of two voltage samples which can be fed into a difference amplifier to perform noise cancelling. The final voltage is then digitized via Analog to Digital Converter (ADC) and stored as pixel data.

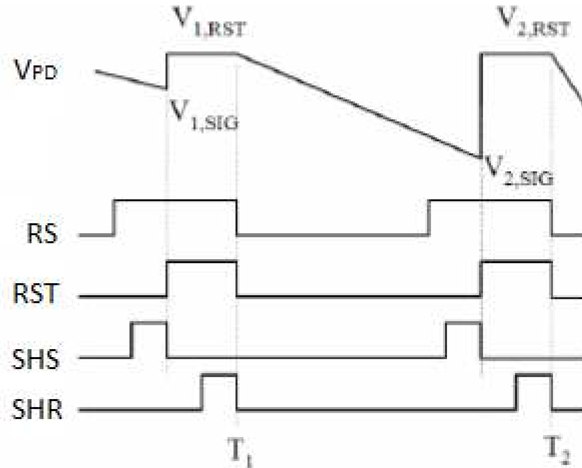


Figure 2.3 - Timing diagram of MOS imager **[30]**.

2.1.1 Photodiode Operation

In CMOS imagers, the PD is operated in one of two modes: photon flux integrating mode or photoconductive mode. The former relies on the PD capacitance to store the integrated charge which is then read at the end of the integration period. In this configuration, the voltage across the PD decreases with respect to integration level. The latter maintains a constant bias across the PD and utilizes the photocurrent to charge an integrating capacitor. This discussion will focus on

photon flux integrating mode as it is most common for MOS imagers and will be utilized in the current research.

In photon flux integrating mode, the PD is first biased to a certain voltage, typically V_{DD}, and then a switch (RST) disconnects the PD cathode from the power supply. A simplified circuit diagram of this configuration is shown in Figure 2.4 where R_{PD} is the series resistance of the PD and C_{PD} is the junction capacitance of the PD.

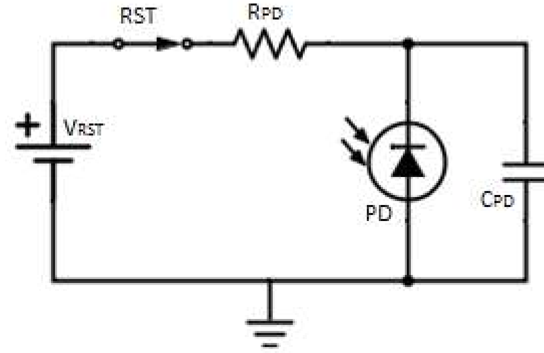


Figure 2.4 - Simplified circuit for photon flux integrating mode operation.

Initially, the switch is closed and the capacitive PD node is charged to V_{RST}. Wekler *et al* explored the operation of such a circuit and the analysis is summarized in the following [18]. At time t=0, the switch opens and the current supplied by the capacitor is equal to the sum of the dark current and photo-generated current in the PD as shown in the expression

$$C_{PD}(v)\frac{d}{dt}V(t) = -I_{PD} \tag{2.1}$$

The junction capacitance changes with the magnitude of the applied reverse voltage due to the decreasing width of the space-charge region. The voltage dependent capacitance of a graded junction is given by

$$C_{PD}(v) = A\left(\frac{qa\varepsilon^2}{12}\right)^{\frac{1}{3}} V^{-\frac{1}{3}} \tag{2.2}$$

In Equation 2.2 a is the junction gradient. The current through the PD is the sum of the dark and optically generated currents which are given by

$$I_d = \frac{Aqn_i}{2\tau_0}\left(\frac{12\varepsilon}{qa}\right)^{\frac{1}{3}} V^{1/3} \quad 2.3$$

$$I_l = I_0 AH \quad 2.4$$

In Equations 2.3 and 2.4, $\tau_0$is the carrier lifetime in the depletion region, $I_0$is the photosensitivity of the junction in amps per unit area per foot-candela, and H is the illumination level in foot-candelas. Combining these four equations yields the following differential equation:

$$V^{-\frac{2}{3}}\frac{dV}{dt} + I_0 HI\left(\frac{12}{qa\varepsilon^2}\right)^{1/3} V^{-\frac{1}{3}} + \frac{n_i}{2\tau_0}\left(\frac{144Q}{\varepsilon a^2}\right)^{\frac{1}{3}} = 0 \quad 2.5$$

An analytical solution for Equation 2.5 does not exist. Through approximation and simulation, Weckler *et al* demonstrated that the integrating voltage is approximately linear regardless of illumination level as shown in Figure 2.5 and Figure 2.6. Figure 2.6 shows the voltage across the junction under no incident illumination. In this case, the curves exhibit slightly less linear behavior which is likely due to the dark current dependence on the width of the space charge region.

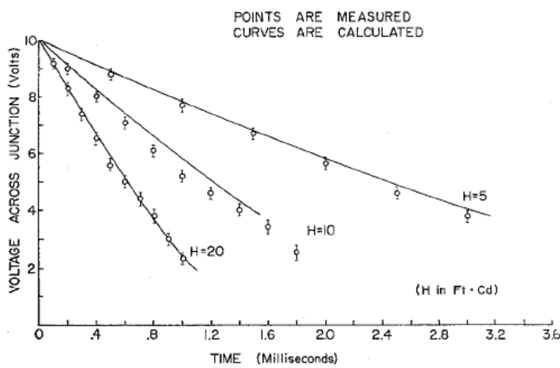


Figure 2.5 - Voltage dependence of illumination level on PD [18].

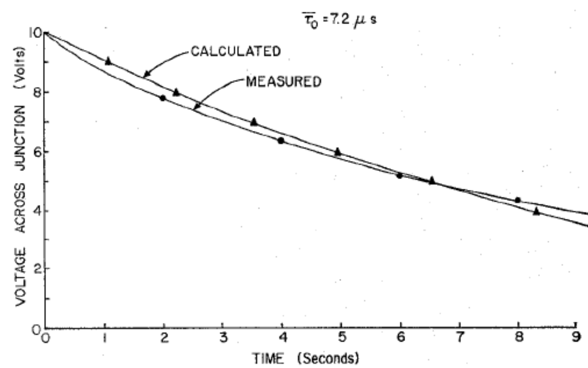


Figure 2.6 - Dark current response of PD in photon flux integrating mode [18].

In this implementation scheme, lower PD voltages represent higher levels of illumination or a "whiter" pixel color. It is important to note the saturation level for these devices. The upper level of the saturation region is determined by the amount of charge that can be stored on the integrating capacitance. A higher capacitance will allow for greater charge storage which can be accomplished through higher doping concentrations, higher reverse bias, and larger PD area. However, higher capacitance will result in poorer conversion gain, and the increase in the width of the space-charge region will result in an increase in the dark signal. The lower level of the saturation region is typically determined by the SF transistors ability to buffer the charge. Thus, at PD voltages below $V_{TH\text{-}SF}$, the pixel will appear white.

2.1.2 Performance Parameters

The characteristics and image quality of CMOS imagers are measured through the application of various parameters. These parameters quantify the imager's response to light, charge transfer characteristics, operational range etc. The following is a brief outline of the most common measurements used to evaluate imager performance.

2.1.2.1 Fill Factor

The pixel FF is the ratio of the area occupied by the photo-sensing element to the area occupied by the pixel. FFs in the range of 30 percent are typical; however, the use of micro-lenses overtop the pixel can increase the effective FF to upwards of 80 percent [16]. High FF captures more incident light which results in a better digital representation of an analog image.

2.1.2.2 Dynamic Range

Dynamic range is the maximum integrated voltage divided by the noise floor. The maximum integrated voltage is determined by the charge storage characteristics of the PD. The noise floor of the pixel is determined by the threshold characteristics of the source-follower

amplifier. Dynamic range can be increased through the reduction of dark current through the effect of lowering the noise floor. Dynamic range is typically measured in dB.

2.1.2.3 Dark Current

Dark current, also known as leakage current, is a measure of generated charge carriers under no incident illumination. Dark current in CMOS imagers decreases the integration voltage in dark conditions which leads to a misrepresentation of pixel color. In highly illuminated scenarios, dark current has little effect on overall image quality. However, as illumination levels drop the dark current occupies a larger percentage of the pixel output which leads to poorer image quality. According to Pain *et al*, dark current sets the performance limit of CMOS imagers [19].

Dark current is presented as a voltage at the integrating node with respect to integration time, a current density with respect to the photo-sensitive element, or as the root-mean-square of non-photogenerated electrons. The measured voltage at the integrating node is dependent upon the conversion gain and size of the PD. For this reason, dark current measurements are often standardized and presented in terms of current/cm^2.

2.1.2.4 Conversion Gain

Conversion gain refers to the output voltage fluctuation per integrated electron and serves as a measurement of the responsivity of the pixel. High conversion gain is desirable to allow for more accurate ADC capture. Conversion gain is calculated as

$$CG = \frac{q}{c} G_{SF} \tag{2.6}$$

In Equation 2.6, G_{SF} is the gain of the source follower (ideally 1), and c is the total parasitic capacitance at the integrating node. Conversion gain can be used to estimate the total parasitic capacitance by injecting a known charge into the integrating node and measuring the output. The parasitic capacitance in a 3T pixel is comprised of the junction capacitance of the PD, C_{gs} of the RST transistor, C_g of the SF transistor, the sidewall capacitance of the PD, and other parasitic components [20].

2.1.2.5 Well Capacity

The well capacity is the maximum amount of charge that can be stored on the integrating node. The upper limit is determined by the capacitance at the integrating node and the reset voltage prior to integration. The empty well voltage is determined by the minimum amount of charge the SF transistor is able to buffer which is often significantly higher than the fully depleted level of the integrating node. Thus, conversion gain can be maximized by increasing the operating voltage at the expense of noise and power consumption or by optimizing the behavior of the SF transistor.

2.1.2.6 Dark Signal Non-Uniformity

Dark signal non-uniformity (DSNU) is a measure of the uniformity of pixel dark currents in the imager. Pixel dark current is usually noisy which necessitates statistical characterization of the dark signal. DSNU is the reason dark current cannot simply be subtracted from the integrated voltage for image correction. DSNU is calculated according to the following:

$$DSNU = \frac{\sigma_{DM}}{S_{DM}} \qquad 2.7$$

In Equation 2.7, σ_{DM} is the square root of the variance of the mean of various dark signal values, and S_{DM} is the average dark signal value [21].

2.1.3 Noise in NMOS Imagers

Noise in a circuit refers to any deviations in circuit signals that are caused by the non-ideal behavior of circuit components. In a MOS imager pixel, the sources of noise include reset noise, readout noise, fixed pattern noise, and PD noise which are outlined in the following sections.

2.1.3.1 Reset Noise and Image Lag

Reset noise is defined by the mode of operation, either hard reset or soft reset. Hard reset refers to the case in which the PD capacitance is reset to V_{DD} by applying a sufficiently high voltage to the gate of the reset transistor such that the transistor operates in saturation regardless of the rising voltage at the capacitive node. According to Pain *et al*, the higher driving voltages associated with hard reset lead to hot-carrier stress and possible breakdown [22]. For this reason the saturation voltage is usually decreased below V_{DD} in order to reduce noise. This has the effect of decreasing the voltage range at the integrating node which can result in poor dynamic range.

To improve the dynamic range loss and high noise associated with hard reset, the RST transistor is often operated in soft reset mode. In this case, the voltage level the integration node reaches is dependent on the integration level of the previous frame. If the previous frame was exposed to sufficient illumination, the gate to source voltage across the RST transistor may be high enough for the transistor to operate in saturation. As the voltage at the integration node rises, the RST transistor will begin to operate in the subthreshold regime. The voltage at the integration node will have a logarithmic response, and the maximum voltage reached is dependent on the amount of time the circuit is in reset mode as well as the residual voltage from the previous frame.

According to Pain *et al,* when a small amount of charge is restored to the integration node during reset, the noise on the signal is dominated by shot noise [22]. In the case where a large amount of charge is restored to the pixel, thermal noise becomes the dominating noise factor. When the pixel is operated in hard reset, the noise is $\sqrt{\frac{kT}{C}}$. When thermal noise is the dominant source of noise during soft reset, the noise is $\sqrt{\frac{kT}{2C}}$ [23]. The implication is that the noise will be lower when operated in soft reset; however, with soft reset, it is common for the integration node to remain below V_{DD} after the reset period resulting in image lag.

2.1.3.2 Readout Noise

During the readout phase the pixel noise sources include RS, SF, and the SF biasing transistor external to the pixel. Because RS is operated in switch mode, its contribution to the noise is negligible in the readout phase. Thus, the SF and biasing transistor are the main components of signal noise during readout. The noise analysis performed by Brouk *et al* suggests that thermal noise and 1/*f* noise are the dominant sources of noise in these transistors [5]. The variance of the voltage from the thermal noise contribution of SF and the biasing transistor is given by

$$\sigma_{TH}^2(t_{read}) = \frac{2}{3}\frac{kT}{C_L}\frac{\left(g_{m,1}(1+\eta_1)+g_{m,2}\right)}{C_L\omega_0} \qquad 2.8$$

In Equation 2.8, C_L is the load capacitance external to the pixel used during readout, g_m is the transconductance of the respective MOSFET, $\eta = g_{m,bs}/g_m$, and $\omega_0 = (r_{sF_out}C_L)^{-1}$ where r_{SF_out} is the output impedance of the source-follower [5].

As is shown in Equation 2.8, a large load capacitance at the readout node will reduce the effect of thermal noise. According to Van Zeghbroek, the transconductance of a MOSFET is proportional to $C_{ox}W/L$ which implies the thermal noise during readout can be reduced by decreasing the MOSFET aspect ratio and gate capacitance [24].

The 1/*f* noise variance during readout can be found according to the following:

$$\sigma_{\frac{1}{f}}^2(t_{read}) = \frac{\rho_0}{2}\left(\frac{I_{DC,n}}{N_{eff,n}C_L\omega_0}\right)^2 \qquad 2.9$$

In Equation 2.9, ρ_0 is the density of traps per unit depth of the oxide, $I_{DC,n}$ is the current through the channel of transistor M_n, and $N_{eff,n}$ is the effective number of charges in the MOSFET channel [5]. The dependence on the channel current implies that 1/*f* noise will be lower for longer channel devices. Similar to thermal noise, a higher load capacitance will reduce the effect of noise.

2.1.3.3 Fixed Pattern Noise

The individual devices within a pixel array will have varying characteristics which result in slightly different response from pixel to pixel. These differences are manifest as FPN which is typically constant from frame to frame but varies from pixel to pixel. The primary sources of fixed pattern noise are due to device mismatch; however, the majority of this noise can be reduced by the implementation of correlated double sampling in 4T cells and delta difference sampling in 3T cells [25]. The remaining source of fixed pattern noise in the pixel is PD dark current. The mismatched dark response from pixel to pixel results in FPN; however, minimizing the dark current in the PD will also improve FPN due to dark current.

2.1.3.4 PD Noise

During integration the primary source of noise is shot noise due to the PD dark current and PD photo-generated current. The noise voltage on the PD sampled at the end of integration is given by the following [23]:

$$\sigma_{PD}^2(t_{int}) = \frac{q\left(i_{ph} + i_{dc}\right)}{C_{ph}^2\left(v_{ph}(0)\right)} t_{int} \left(1 - \frac{1}{2\left(v_{ph}(0) + v_{bi}\right)} \frac{i_{ph} + i_{dc}}{C_{ph}^2\left(v_{ph}(0)\right)} t_{int}\right)^2 \qquad 2.10$$

Equation 2.10 takes into account the varying PD capacitance during integration. It is important to note the dependence of PD noise on the integration time. This suggests that as integration time is extended to accommodate for lower light conditions, there is less signal fidelity. Thus, to minimize PD noise during integration, the integration time should be as short as possible. Also, a higher PD capacitance and higher bias voltage will result in less PD noise.

2.2 Photodiode Dark Current

In a MOS imager pixel circuit, the dark current continues to lower the voltage at the integrating node which results in a non-black pixel in dark conditions. As the illumination level decreases, the dark signal occupies a greater portion of the readout signal which results in poor imager quality in low light environments. The DSNU of the imager from pixel to pixel prevents the dark signal from simply being subtracted from each pixel. Thus, a reduction in pixel dark current has a strong implication on improving picture quality in low light scenarios.

2.2.1 Mechanisms

Dark current generation is typically attributed to four different sources in CMOS devices: charge carrier generation and diffusion in the neutral bulk, charge generation due to surface states at the Si-SiO_2 boundary, charge generation in the depletion region, and charge generation

at interface traps at the diode perimeter [26]. The dark current components produced at the Si-SiO_2 interface and the diode perimeter are similar in that they are both the result of a high concentration of lattice defects at interfaces. The dark current components in the bulk and space-charge region are the effect of buried traps in the substrate. Research suggests that the net G/R rate can be controlled through the dopant concentration and trap concentration [27]. Because the dopant concentrations are set for device operation, the trap concentration must be reduced in order to reduce dark signal. Deep level traps are often the result of impurities introduced to the substrate during wafer fabrication. The number of interface traps is typically much larger than deep level traps, so contribution of deep level traps to dark current is often neglected.

2.2.2 Influence of Charge Traps on Dark Current

Impurities and defects in a silicon lattice contribute to a band gap dividing phenomenon in which impurities and defects act as intermediate generation/recombination centers inside the forbidden gap. The Fermi distribution allows the concentration of holes and electrons to be determined for a trap energy level. Trap energy levels that result in equal probability of electron and hole concentrations contribute most to the charge carrier generation and recombination [27]. For this reason, impurities that create energy states near the midgap of the forbidden region contribute most to an increase in the dark signal.

2.2.3 Effect of PD Shape on Dark Current

A higher concentration of defects is typically found in areas of the PD that are exposed to high stress. These areas are typically junctions and sharp edges. For this reason Shcherback, *et al* investigated the effect of PD shape on the dark signal of a 3T pixel [13]. In this research it was found that the PD with external angles ranging from 90 to 135 degrees contributed to a

reduction in dark current from 8.5nA/cm^2 to 7nA/cm^2. The reduction in dark current indicates a reduction in trap concentration at the perimeter of the PD.

Shin *et al* explored a tapered PD design to facilitate charge transfer from the PD during the readout of a 4T pixel [14]. It was found that when the size of the PD was tripled, the voltage output only increased 20 percent. This is due to incomplete charge transfer in large PDs. The tapered design establishes a lateral electric field gradient due to the charge concentration gradient (Figure 2.7). An angle of 26.1 degrees results in a triangular shape and optimum charge transfer characteristics. This design leads to a reduction in reset noise and readout noise due to the field assisted charge transfer. The mitigation of dark current is not mentioned in the article; however, it can be assumed that the 26.1 degree angle used in the design would introduce a higher stressed region in the PD and lead to a comparatively higher dark current. However, the introduction of rounded corners may reduce dark current while maintaining the higher output voltage.

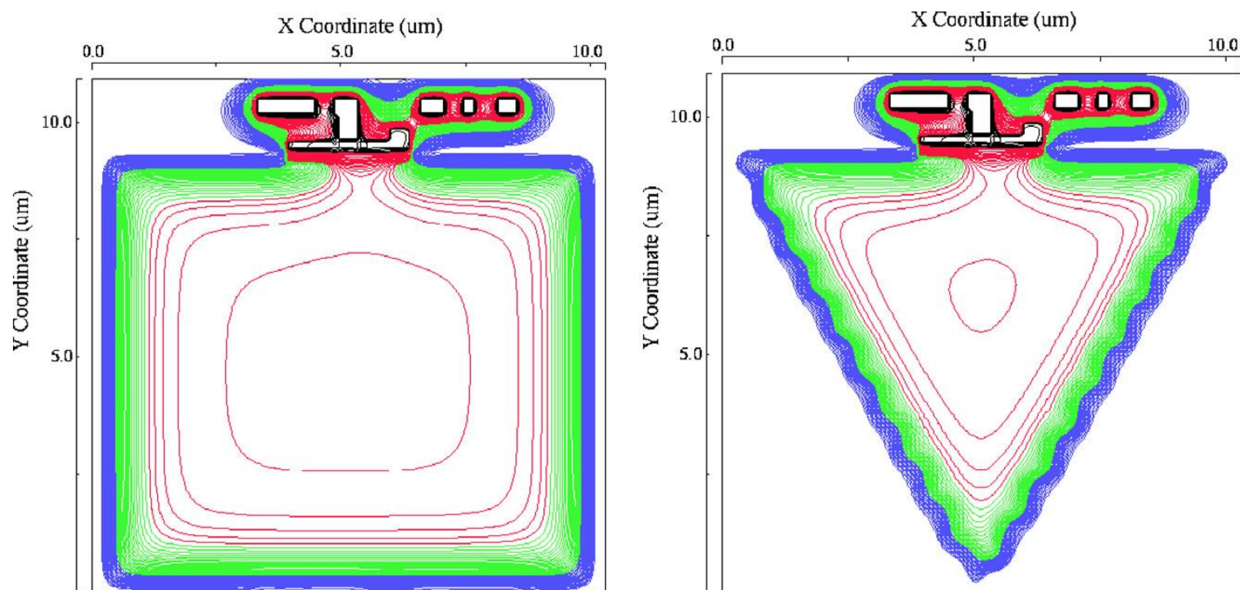


Figure 2.7 - Tapered PD design and E-field gradient [14].

The methods of dark current response and improved charge transfer presented in [13] and [14] are easily applied to the large area PDs that can be fabricated in the GVSU cleanroom. More sophisticated techniques of dark current reduction are beyond the scope of the GVSU cleanroom. For this reason, these two methods were used to form the basis of designing a reduced noise NMOS imager in the GVSU cleanroom.

3 Experimental Method

The purpose of this research was to fabricate a low noise NMOS imager in the GVSU Cleanroom with a focus on the reduction of pixel dark current. Dark current reduction was attempted through the use of alternative PD designs. The readout circuitry attempted to maintain signal integrity through sample and hold circuitry and ADC sample averaging. Also, the Voltage and Sample and Acquisition Controller (VSAC) was designed for flexible control of the timing and voltage parameters of the control circuitry for imager optimization.

3.1 Integrated Pixel Array Design

3.1.1 Functional Requirements

The pixel arrays should implement the following characteristics:

Table 3.1 - Functional requirements of the integrated PD arrays.

Functional Requirements	
Requirement	**Description of requirement**
8x8 pixel array.	The 8x8 pixel interface allows easy interface with common eight I/O circuit components.
Sensitivity to illumination level	The PD arrays should respond to incident illumination.
Output voltage near V_{DD} in dark conditions	Voltages nearer V_{DD} represents darker pixel color. Under zero illumination the voltage increase is mainly due to dark current.
Output voltage near $V_{TH,SF}$ under high intensity illumination	Under high intensity illumination, voltages nearer the lower bound of the readout circuit result in better dynamic range.
Implement one PD shape per array.	Limit PD test shapes to one per array to allow for simple comparison between shapes.
Individually accessible pixels	Each pixel should be accessible one by one through operation of row and column elements.
Current source for SF transistor	To achieve appropriate gain, a current bias (biasing transistor) is necessary for the SF amplifier.
Compatibility with GVSU fabrication process	Only devices capable of being fabricated in the GVSU cleanroom are included in IC layout.

Additionally, the fabrication of a 4T pixel requires the ability to implant various doping concentrations of both P and N type which is beyond the scope of the GVSU fabrication process. For this reason, 3T pixels were used in the current research. Because the readout circuitry is not

integrated, the array size was kept small. This allows the readout circuitry to be hardwired to the interface board housing the fabricated IC. The pixel arrays were designed such that each array contained a single PD shape so that developed imagers implementing each type of PD can be compared. To maximize dynamic range, the output voltage should vary between V_{DD} and $V_{TH,SF}$. The SF amplifier requires a current source for proper operation. A biasing transistor is included on each column bus for this purpose. The NMOS imager was designed with standard pn-junction PDs and a minimum feature size of 10µm for compatibility with the GVSU fabrication process. The fabrication process is outlined in more detail in section 3.3.

3.1.2 Integrated Circuit Layout

Five PD geometries were designed to test the influence of PD shape on the dark signal. These designs are adapted from the findings of Shcherback *et al* and Shin *et al* [13] [14] . The integrated circuit layout along with the FF of each pixel is shown in Figure 3.1. Pixel One is the test bench with which the altered designs will be compared. The PD of Pixel One occupies the greatest area and yields the best FF. Shcherback *et al* tested the influence of the number of corners and corner angle on the pixel dark response. Only the angles of the four corners in the rectangular shape were modified in this research in order to maintain a high FF. For this reason, pixels two and three are rectangular in shape with increasingly rounder corners.

Pixel Four serves as a benchmark to test the output voltage elevating effect demonstrated in the research of Shin *et al* [14]. The sharp corners of the triangular design are areas of high stress. The corners will have high concentrations of interface defects which will lead to elevated dark current. The sharp corners of Pixel Four were rounded as seen in Pixel Five with the hope of maintaining the voltage elevating effect while reducing dark current. The PD of Pixel One is

300 µm x 250µm and each subsequent design is based off this size. The corners of Pixel Two and three are 135 and 150 degrees respectively. The corners of Pixel Five are 120 degrees.

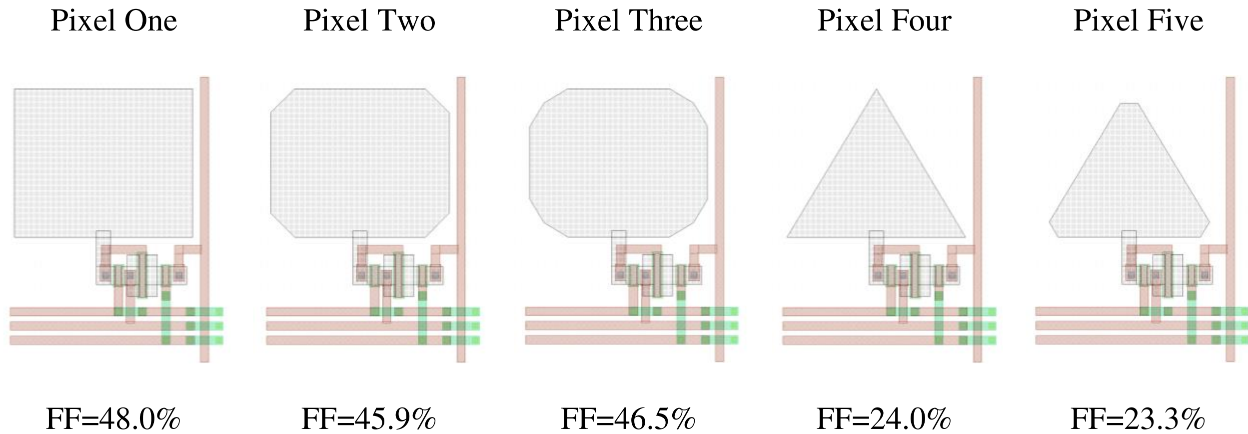


Figure 3.1 - Five PD designs to determine effect of PD shape on dark current.

Pixel One is shown in Figure 3.2 with the devices and traces identified. The transistors are formed by creating two diffusion regions separated by the transistor channel with width equal to the minimum feature size; in this case 10µm. A gate oxide layer is grown on top of the transistor channel. A metal layer is then formed above the gate oxide to form the MOS capacitor which is the gate of the FET. Voltage applied at the gate attracts electrons in the n-type FET which creates a conductive path from the source to drain of the transistor. Control signals are routed to the transistors through use of the RST, V_{DD}, and RS traces. The output of the pixel is transferred to the column bus using the RS transistor.

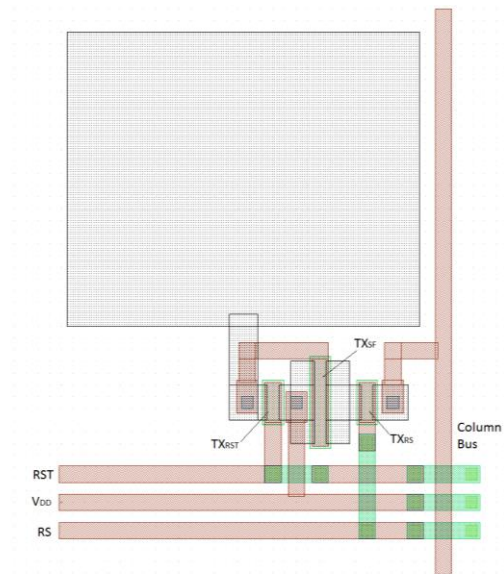


Figure 3.2 - Pixel layout with identified devices and traces.

Each pixel contains three transistors. The RST and RS transistors have aspect ratios of 3:1 while the SF and biasing (not shown) transistors have aspect ratios of 7:1. The research suggests minimizing MOSFET aspect ratio will result in improved thermal noise performance during readout [5] [24]. The MOSFETs that source small currents (RST and RS) were designed with 3:1 aspect ratios for this reason. The amplifier transistors require a larger aspect ratio to improve the current sourcing abilities. Thus, the SF and biasing transistors were designed with an aspect ratio of 7:1.

A sample die containing the rectangular PD array is shown in Figure 3.3. The 8x8 PD array consists of row and column readout busses as well as a biasing transistor for proper operation of the SF transistor in each pixel. The interface pads are 200x200μm and are used to supply control signals to the array as well as capture the array output. The array is designed for a single diffusion layer, gate oxide, two aluminum interconnect layers, and two via layers for a total of six layers. The array including readout pads occupies a 4.86mm by 5.00mm area.

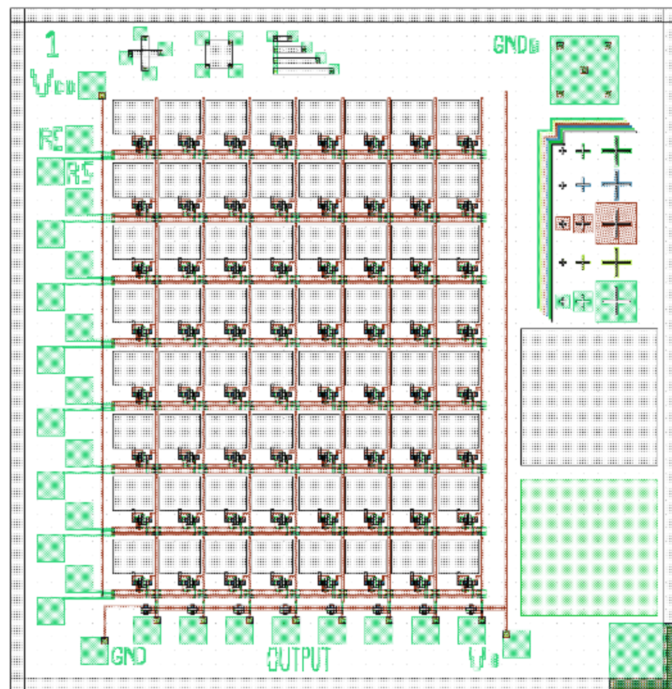


Figure 3.3 - Imager die with type one PDs.

An n-type isolation barrier was designed to surround each die with the intention of preventing bulk currents from interfering with the PD current. The isolation border encapsulates the PD array with a pn-junction. Biasing the border with a positive voltage creates a reversed

biased diode condition. This prevents currents from flowing into the die region from the areas of the bulk external to the PD array.

Designs with the source and bulk connected and disconnected have been designed to accommodate the likelihood that bulk biasing may need to be employed to obtain positive threshold operation with the transistors. The GND_B pad in the upper right corner of the die is used to apply a voltage to the bulk of the die in designs where the transistor sources are not shorted to the bulk.

The five rows of cross structures and thin traces in Figure 3.3 are alignment features for use in the fabrication process. Each row compares the current layer to the previous layer. During the alignment process these structures are used to ensure proper alignment from row to row. If the layers are not aligned the devices will not operate correctly.

The three Van der Pauw structures at the top of Figure 3.3 are used for measuring the resistivity of the diffusion layer. Resistivity measurements help characterize the uniformity of the diffusion layer.

The two large squares on the right of the die are used for sheet resistance and gate oxide (from top to bottom) measurements. The large area of the windows was designed to allow the four point probe and ellipsometer to capture measurements from individual die. The measurement of sheet resistance and gate oxide thickness from dummy wafers serves the same purpose as these regions.

3.1.3 Calculations and Simulations

The MOSFET threshold voltage calculations outlined in Appendix A.3.1 were used to estimate behavior of the 3:1 and 7:1 MOSFETs in the imager pixels. The values presented in

Table 3.2 were used in estimating the threshold voltage. The acceptor doping concentration is a function of the wafer resistivity and the hole mobility in the substrate. The interface charge is an estimate of the concentration of mobile ionic impurities at the Si-SiO_2 interface. The thickness of the gate oxide is estimated from previous fabrication results. The work function difference is a function of the substrate doping. Based on the estimated substrate doping, Streetman suggests a value of approximately -1V for the work function variation [28]. Based on these preliminary numbers, the MOSFET threshold voltage is likely to be in the range of 1-2V.

Table 3.2 - MOSFET threshold parameter estimates.

(Bold value is the result of the calculation.)

Parameter	Value
$\boldsymbol{N_a}$	1.30x10^{18} [cm^{-1}]
$\boldsymbol{Q_i}$	3.50x10^{12} [qC/cm^2}
$\boldsymbol{d}$	70.0 [nm]
$\boldsymbol{\phi_{ms}}$	-1.00 [V]
V_{TH}	**1.65 [V]**

PD size is typically 15-20 times the minimum feature size [16]. To maximize FF in the current design the PD dimensions were increased to approximately 25 times the minimum feature size. Using the PD equations in Appendix A.1, PD characteristics were estimated for simulation purposes. The parameters used and values calculated are shown in Table 3.3. The junction width and area of the photodiode are used to estimate a PD capacitance of 3.4pF. The carrier lifetime (τ_0) in the depletion region is an empirical estimate suggested by [18]. The photo current is estimated to be 1.16μA. The magnitude of the PD current and the size of the PD

capacitance are the primary mechanisms controlling the speed at which the voltage across the PD junction decays.

Table 3.3 - Parameters for estimating PD photocurrent.

(Bold values are the results of the calculations.)

Parameter	Value	Parameter	Value
A	7.50x10^{-4}[cm^2]	L_n	35.2 [μm]
$\boldsymbol{N_A}$	9.00x10^{15} [cm^{-1}]	L_p	59.1 [μm]
$\boldsymbol{N_D}$	1.43x10^{15} [cm^{-1}]	$\boldsymbol{C_j}$	**3.40 [pF]**
$\boldsymbol{V_{bi}}$	0.759 [V]	τ_0	7.20 [μs]
V	-5 [V]	g_{op}	10^{18} [(cm^{3}s)$^{-1}$]
W	2.28 [μm]	$\boldsymbol{I_{PD}}$	**1.16 [μA]**

Figure 3.4 and Figure 3.5 show the schematic and simulation of the 3T APS respectively. The PD is modelled as a diode in parallel with a capacitance and current source. The effective capacitance during charge integration is the junction capacitance of the PD combined with parasitic RST and SF capacitances. The RST transistor contributes charge stored on the source-bulk and source-gate capacitors. The SF transistor contributes charge stored on the gate capacitance. The voltage across the PD capacitance after reset decreases due to the photocurrent modelled by the current source. Using the calculated parameter values, the 3T APS was simulated.

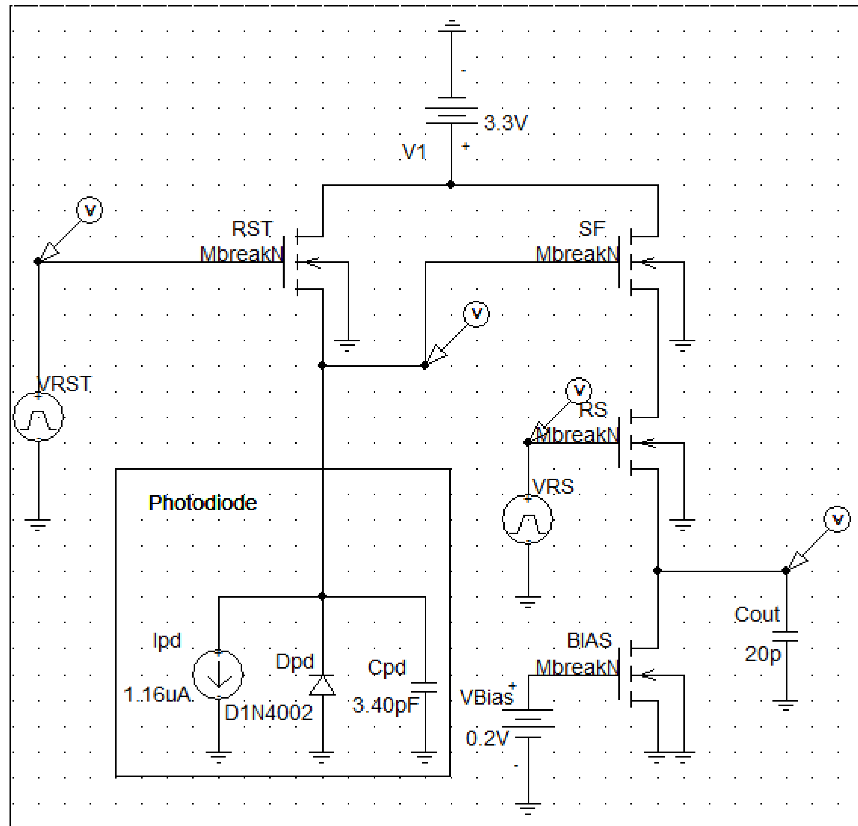


Figure 3.4 - Pixel simulation circuit

The following simulation results demonstrate the operation of the 3T APS. The gate of the RST transistor was overdriven at 5V during operation such that PD capacitance could be fully charged to V_{DD} before RST enters subthreshold operation. Because the fabricated transistors are likely to exhibit thresholds in the 1-2V range, a conservative ~1.5V_{DD} pulse was applied to the RST gate to ensure adequate reset as suggested by Ji and Abshire [6]. After the reset pulse, the voltage across the PD rises to V_{DD} and slowly decreases proportional to the photocurrent. Because the SF transistor loses its buffering ability when the PD voltage decreases below the threshold voltage, operation of the RS transistor should occur prior to this point. When the gate to source voltage of the RS transistor is set to V_{DD}, the charge stored at the drain of the RS transistor is transferred to the output node modelled by a 20pF capacitance. The

simulation shows that the output voltage decreases with time due to leakage currents and the current through the bias transistor. However, in the circuit implementation, the output node will be captured by a sample and hold circuit to minimize losses during readout. Based on the values of the integrating capacitance and the photocurrent estimate, an integration time of roughly 8μs is appropriate.

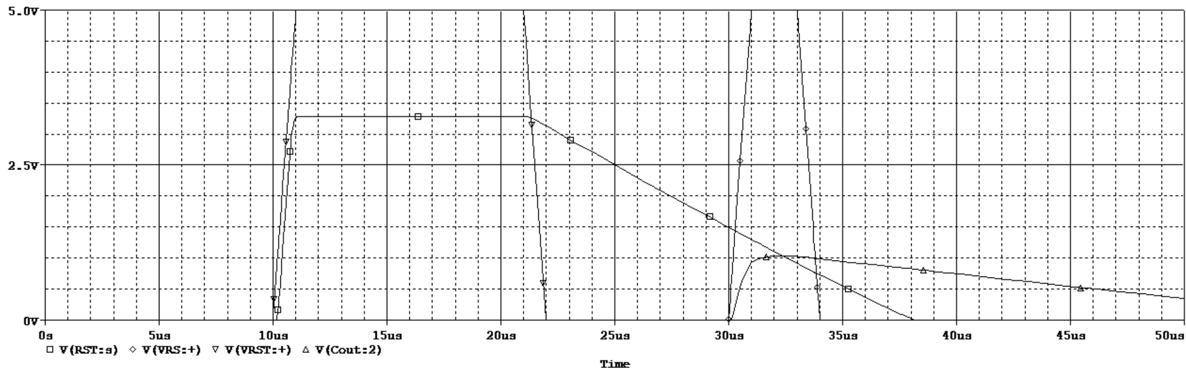


Figure 3.5 - Simulation results of 3T pixel.

3.1.4 IC Testing

Each wafer layout contains several test die which will assist in the characterization of process fidelity. The test die is shown in Figure 3.6. Various alignment features are present on each test die. These features were visually inspected after each processing stage to ensure proper alignment from layer to layer. The test die has been designed with an n-type isolation border to test the influence of currents in the bulk on the operation of the device. The isolation border can be biased to prevent currents external to the structure from contributing to measured currents. The die also contains a bulk biasing pad which enables access to the substrate in order to test the effect of bulk potential on device operation. A Micromanipulator Company Inc. Model 6000 Probe Station is used to probe the IC test points.

The capacitance of the PDs was measured using the Agilent E4980A Precision LCR Meter. This is used to characterize the voltage decay during the integration period as compared to the simulation.

The test die contains two different transistor arrays with aspect ratios of 7:1 and 3:1. These arrays can be tested for correct transistor operation including threshold verification, the effect of body biasing, and drain current characterization. MOSFET and PD characteristics are captured using the HP4145A semiconductor parameter analyzer. An enclosure was built to house the ICs so dark conditions could be tested.

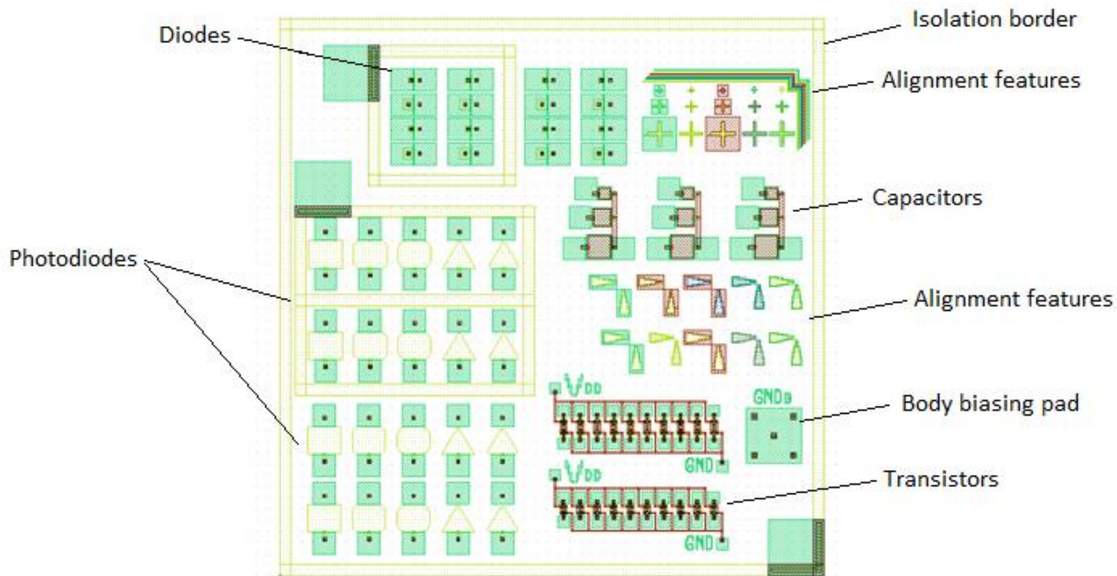


Figure 3.6 - Test die for fabrication characterization.

The test die will be utilized to obtain an average dark signal for each PD type as well as identify fabrication variations due to die position on the wafer. The GVSU fabrication process often exhibits performance variability with respect to die location. Thus, the test die can be used to identify regions likely to contain functional imagers.

3.2 Control Circuit Design

The readout circuitry captures the voltage output of the Imager IC and transfers that information to a PC for data analysis. The following sections outline the developed system used to capture image data.

3.2.1 Functional Requirements

The diagram shown in Figure 3.7 shows the necessary components of the VSAC. The two shift registers, RST Select and Row Select blocks are used to index and control the RST and RS transistors of each row. The RST Gate Driver allows a logic level output from the RST shift register to supply a wide range of analog voltages to be used as the RST transistor gate to source voltage. This allows the gates of the RST transistors to be overdriven to prevent image lag. The voltage regulators must be able to supply voltages in the range of 0.2 to 10V to various parts of the imager IC; so, BK Precision Model 1762 DC power supplies were used as the voltage regulators. The column sampling needs to sample the imager IC output with low noise and must maintain the signal level as the 8:1 multiplexor sequentially processes the parallel outputs. The ADC needs to be high resolution and low noise. The ADC is a peripheral of the TI LM326965 development board with 10-bit resolution. The development board is used to programmatically control the hardware and capture imager data. The UART peripheral of the microcontroller is used to send the data to a PC for processing and storage.

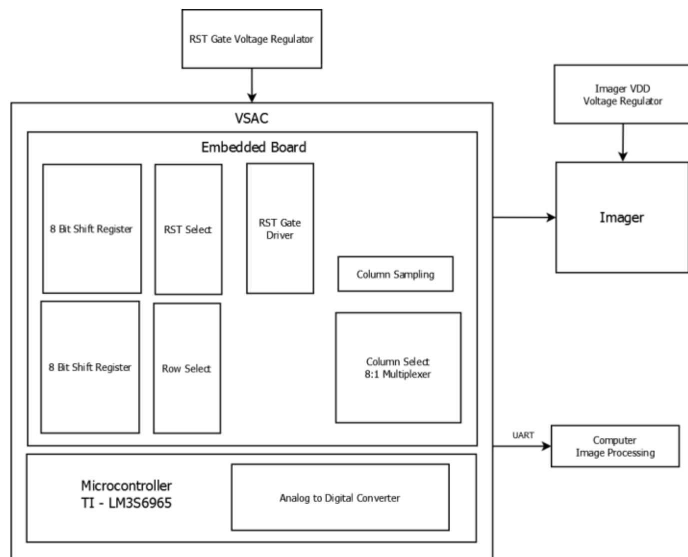


Figure 3.7 - Block diagram of the VSAC.

During transmission the 10 bit pixel values are byte extended to 16 bits and passed along the UART. The system is designed to capture and transmit the 64 pixel samples so for each image, the system should be capable of transmitting 128 bytes of image data.

3.2.2 Hardware and Simulations

The following sections outline the design decisions regarding the interface between the IC and PC. The schematic and board designs can be found in Appendix B.

3.2.2.1 TI Development Board

The TI LM3S6965 was used in this project to communicate between the developed embedded system and a PC, as well as convert the analog voltages at the imager output to digital. The LM3S6965 is a 32-bit microcontroller implementing an ARM Cortex M3 processor. The LM3S6965 was chosen for this project because it contains onboard ADC and UART peripherals which simplify the design of the developed PCB.

The LM3S6965 contains a 10-bit four channel ADC with hardware oversampling capability. This gives a voltage resolution of 2.93mV. Oversampling aids in noise reduction by sampling the analog voltage several times during a short period. The samples are then averaged together which effectively reduces the noise manifest in the reading. Hardware oversampling was used in this project to improve the noise performance during the readout stage.

3.2.2.2 VSAC

The VSAC is comprised of two shift registers, a voltage driver for the RST transistors, sample and hold circuitry, and multiplexor. Because the LM3S6965 does not have 16 extra outputs for the RS and RST transistors in each of the 8 rows, shift registers (74AHC595D) are used to expand the output size of the microcontroller. Using only four outputs from the

LM3S6965, each shift register can index eight outputs. Also, the clock functionality on the shift register allows a single pulse to swap control from one imager row to the next making programming the circuit simple.

The RST transistors need driving circuitry such that the gate can be overdriven to prevent image lag. An n-type transistor coupled with a pull up resistor at the transistor drain is used to supply a wide range of voltages to the RST gate. This configuration inverts the signal from the shift registers; so, the RST shift register is programmed opposite to that of the RS shift register.

The sample and hold circuitry was designed to capture the analog voltage at the output pad of the imager IC and store the value as the data is serialized through the Multiplexor (MUX). The analog voltage at the output pads of the IC is subject to the bias current and other leakage which will result in significant voltage drops during serialization. The sample and hold ICs (LF398) are simultaneously triggered to sample the imager output with a single control signal from the LM3S6965. The use of a high quality polypropylene holding capacitor allows the sample and hold circuitry to maintain a steady voltage with a droop rate of less than 5mV per minute while the data is serialized through the MUX. Based on the capacitor choice for the sample and hold circuit, the LF398 datasheet suggests an acquisition time of roughly 20µs. Significant noise and quality degradation is not expected due to the sample and hold circuitry.

The LF398M sample and hold IC has a differential threshold voltage of 1.4V with a minimum to maximum of 0.8V to 2.4V. PD voltages below the logic threshold will appear as the logic threshold during readout. Characterization of the sample and hold circuits shows a differential threshold of 1.55V. This value should not limit the dynamic range of the imager as the SF transistors were designed for a threshold between 1-2V. The SF transistor sets the lower bound for the dynamic range.

The schematic and simulation results in Figure 3.8 and Figure 3.9 show the noise simulation performed on the sample and hold circuitry. It is necessary that the sample and hold circuitry exhibit low noise characteristics so that captured samples are representative of the imager IC and not the readout circuitry. The capacitor at the positive terminal of op-amp U1 is the holding capacitor which is modelled with series and parallel parasitic resistances.

Figure 3.8 - Schematic designed for testing noise performance of sample and hold circuits.

The simulation results show that the input voltage suffers slight amplification between 10 and 100KHz; however, this amplification is less than 0.05dB and will not result in noticeable quality degradation. Due to the presence of the holding capacitor, high frequency noise is filtered from the output node.

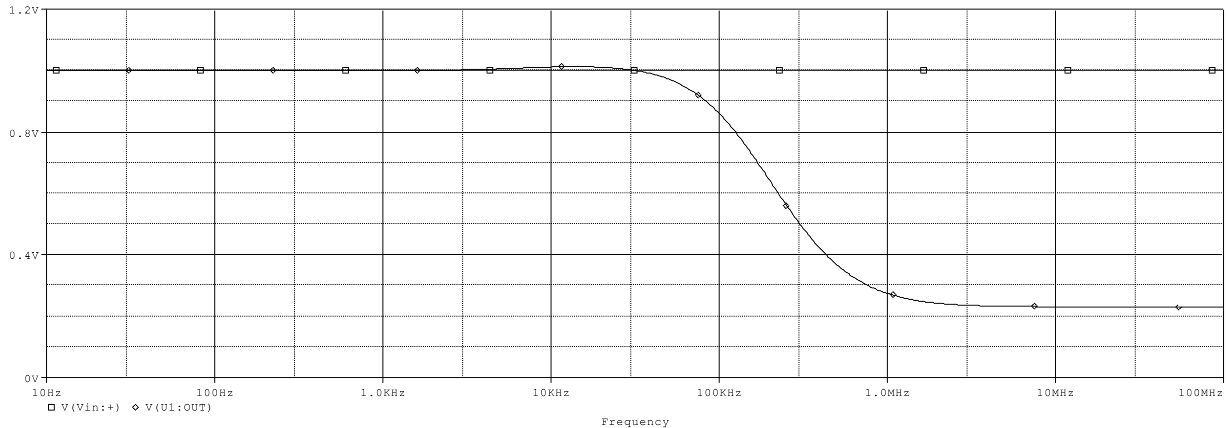


Figure 3.9 - Noise response of sample and hold simulation.

The MUX circuitry consists of a MUX and four bit counter (CD74HC4051NSR and SN54LV163A respectively). The MUX acts as a switch between one of the eight inputs to the single output where the analog voltage is digitized. The MUX is a high speed CMOS logic analog multiplexor which allows the IC output to be sampled quickly; thus, reducing the effective voltage droop at the holding node. The connected input is determined by the four bit counter. Only three of the counter's bits are used. The active bits between 000 and 111 are used to determine which of the eight MUX inputs is to be sampled at the output.

Several filtering and decoupling capacitors are also included on the circuit board near the power pins of each IC as well as the power lines of the board. This will help reduce noise due to changes in circuit current draw. Pin headers are also included on the circuit board which allows the LM3S6965, the VSAC, and the IC interface to be connected.

3.2.2.3 IC to PCB Interface

Due to limited space and probes, the probe station is only used to test individual devices. For this reason, an embedded board was developed for IC wafer bonding so that the developed imagers could be tested. Appendix B.2 contains the schematic and board layout of the developed

interface board. The pads on the interface board needed to have an Electroless Nickel Immersion Gold (ENIG) finish in order for wire bonding to work. Similar to the VSAC, the interface board was designed with filtering capacitors to improve the noise performance on the power supply lines.

3.2.3 Testing

The interface board, VSAC, and the LM3S6965 can be connected to test the imager performance. The timing and voltage parameters of imager operation are controlled by the LM3S6965 and power supplies respectively. The average dark signal can be calculated by measuring the voltage change with respect to time across the PD in dark conditions. This test can performed by connecting the LM3S6965 and the VSAC to discreet PDs using the probe station or testing imager output in dark conditions.

The minimum voltage the SF transistor can buffer must be determined for dynamic range calculation. To measure this, the RS transistor will be turned on during integration. When the output voltage levels off under these conditions the buffer threshold for the SF buffer is found. PD well capacity is then determined through the difference between V_{DD} and the minimum buffer voltage and effective capacitance of the integrating node. This will help determine appropriate timing for the integration period based on sensitivity at different levels of illumination.

After the performance parameters are optimized, image capture will take place and the voltage readout transferred to PC. Based on the well capacity of the imager circuit, the captured voltages will be mapped to black/white levels. Due to the small pixel array size and lack of optics, the imager output will likely not result in a discernable image. However, the voltage

output of the imager will demonstrate the ability of the imager to respond to the level of incident illumination.

The operation of the VSAC is confirmed through the use of the Salea eight bit 24MHz logic analyzer. The noise performance of the readout circuitry will be characterized by applying a known DC voltage to the readout pins of the VSAC. The variation in the VSAC readout will determine the noise injection of the readout circuitry.

The imager is tested by connecting the control signals of the VSAC to the interface board and LM3S6965. The integration period, reset period, and control voltages can be varied to accommodate the results of the IC testing. The imager output is digitized and sent to the PC for analysis to determine appropriate signal timing. The VSAC can be used to determine the average dark performance of each pixel shape through collection of imager output. This method will yield high volumes of comparable data for overall PD performance analysis.

3.3 Fabrication Process

The GVSU fabrication process is a nonstandard single diffusion, metal gate, two metal process with a minimum feature size of 10μm. The steps in Table 3.4 outline the fabrication process. It should be noted that the GVSU fabrication process uses a spin on dopant of type P509 from Filmtronics. Also, the insulating layer between the metal one and metal two layers is a Spin on Glass (SOG) of type B20 from Filmtronics. The SOG deposits a thin layer of SiO_2 to isolate trace routing on the two metal layers.

Table 3.4 - Processing stages in imager fabrication in the GVSU cleanroom.

Step	Description
1	Standard RCA cleaning

2	Wet oxidation (1100°C, 5000Å)
3	First photolithography process and wet oxide etch – definition of source and drain
4	Phosphorous diffusion and drive in (~1µm junction depth)
5	Field oxide growth (1100 °C, 2000Å)
6	Second photolithography and wet oxide etch – gate definition
7	Dry oxidation for high quality gate oxide (1100 °C, 1000Å)
8	Third photolithography and wet oxide etch – definition of source and drain vias
9	Aluminum evaporation deposition (~5000-6000Å)
10	Fourth photolithography and aluminum etch – definition of aluminum routing
11	Spin on glass deposition
12	Fifth photolithography and wet oxide etch – definition of metal two to metal one vias
13	Aluminum evaporation deposition (~5000-6000Å)
14	Sixth photolithography – definition of aluminum routing
15	Annealing - (300-400°C for 10 minutes)

3.3.1 Limitations of the GVSU Fabrication Process

Some devices fabricated in the GVSU cleanroom exhibit non-ideal behavior. The following sections highlight common issues and how they were addressed for the purposes of the current research.

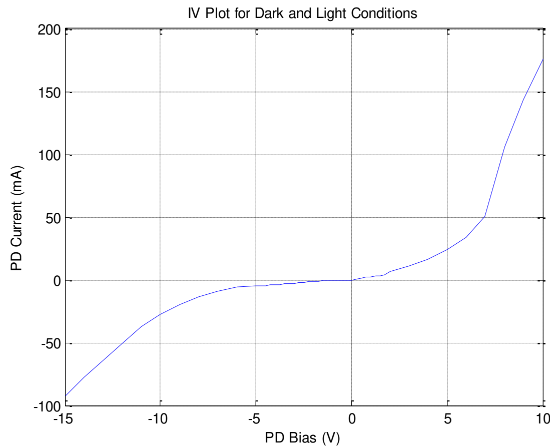
3.3.1.1 MOSFET Limitations

It is common for MOSFETs fabricated in the GVSU cleanroom to exhibit depletion mode operation with a negative threshold voltage. This phenomenon is likely due the presence of mobile ionic impurities, poor bulk grounding, or poor junction formation. Enhancement mode

MOSFETs have been successfully fabricated in the GVSU cleanroom. Although working MOSFETs have been fabricated with channels lengths as small as one micron, the trends of previous fabrications indicate that larger channel lengths improve the probability of fabricating enhancement mode MOSFETs. To improve the likelihood of fabricating enhancement mode (rather than the commonly seen depletion mode) MOSFETS the minimum feature size has been set at a less aggressive size of 10μm. In case the fabricated imagers exhibit this type of response, a pixel has been designed that will allow threshold manipulation through the body biasing effect of the bulk.

3.3.1.2 PD Limitations

Previously fabricated pn-PDs were tested to assess the capability of the GVSU fabrication process to yield functioning photosensitive pixels. The pn-junctions were fabricated by doping the surface of a two inch wafer with Filmtronics P508 n-type dopant. Various aluminum contact patterns were then deposited on the surface of the substrate in $4x4mm^2$ cells to test the charge transfer of different aluminum finger layouts. Figure 3.10 and Figure 3.11 show the response of a fabricated PD under dark conditions and illumination, respectively. The dark curve shows a turn on voltage in the range of 1V and a reverse breakdown of approximately -8.3V. The slope of the curves after both forward and reverse breakdown indicate a large series resistance that is due to the formation of a poor PD junction.



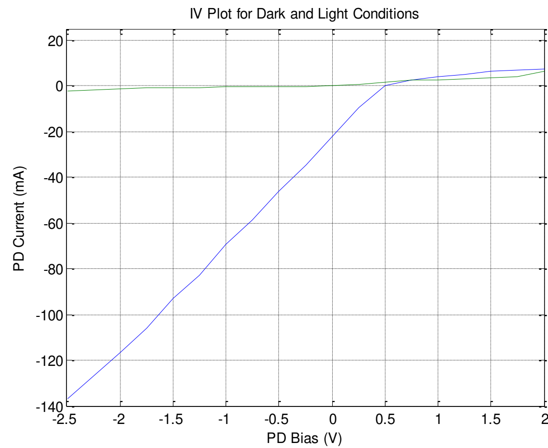


Figure 3.10 - IV characteristics of dark pn junction.

Figure 3.11 - IV characteristics of illuminated pn junction.

Figure 3.11 shows the shift in the diode current under illumination. The slope of the illuminated curve in reverse bias implies a parasitic shunt resistance on the order of 1KΩ. The illuminated junction causes the IV curve to shift which appears to force the PD in to reverse bias breakdown. This characteristic will have the effect of causing the pixel to exhibit non-linear behavior.

The tested PDs exhibited a high degree of variability regarding the magnitude of the leakage current and reverse bias breakdown. Breakdown voltages as low as one volt were observed. It was common for the tested PDs to show resistive behavior under reverse bias with no breakdown, similar to that of the illuminated junction curve of Figure 3.11. These results indicate the formation of a low-quality and non-uniform junction which will lead to a high degree of performance variability in the fabricated imagers. The P509 type dopant has a higher concentration of phosphorous than the P508. This was used in the current research to minimize resistive qualities of fabricated PDs. Also, the amount time the wafers are subject to high temperature processes has been reduced to ensure a more abrupt junction gradient.

3.3.2 Testing

The thickness of SiO_2 films is measured using a Rudolph AutoEl 3 Ellipsometer. The growth of the field oxide (FOX), gate oxide, and SOG layers will require measurement during the fabrication process. These layers are characterized through the use of dummy wafers which are included in the oxide growth process. This allows for a large area to be covered by the oxide which can be measured using the ellipsometer.

The photoresist development, oxide and metal etching, and gate formation are inspected with both an optical microscope with 4, 10, 40, and 63x magnification and Hitachi S-3400N Scanning Electron Microscope (SEM). The inspection takes place after feature fabrication and allows the integrity of the process step to be characterized visually. The optical microscope and SEM are also used to ensure proper alignment after photoresist development.

After the diffusion process, the sheet resistance of the wafers is measured using the Jandel RM3 four point probe.

The thickness of the aluminum layer is measured using the Trovato aluminum evaporator. During deposition the crystal detectors present in the evaporator record the thickness of the deposited layer.

4 Results

4.1 Fabrication Results

The fabrication process is documented in the following sections. Six wafers were processed during the fabrication. Prior to any processing the wafers were scribed with an identification number (1-6) along with two dummy wafers used for layer characterization. The resistivity and die layout of each wafer are documented in the following table. Wafers three and six were fabricated as test circuits instead of imagers so that device parameters could be better determined.

Table 4.1 - Wafer resistivity and circuit pattern.

Wafer	Resistivity (Ωcm)	Die
1	0.01-0.02	Imager
2	0.01-0.02	Imager
3	0.01-0.02	Test Circuits
4	0.1-0.3	Imager
5	0.1-0.3	Imager
6	0.1-0.3	Test Circuits
Dummy 1	0.01-0.02	None
Dummy 2	0.1-0.3	None

4.1.1 Diffusion

The wet oxidation was performed at 1100°C for 70 minutes. When the furnace temperature reached 950°C, the wafers were inserted into the mouth of the furnace and were slid to the center of the furnace over a five minute period. The wafers were exposed for five minutes

to an oxygen ambient. This facilitates the growth of a dense oxide at the surface of the FOX which improves oxide characteristics. The hydrogen was then engaged. After a 70 minute wet oxidation, the wafers were subjected to another five minute dry oxidation in the oxygen ambient.

The temperatures of the furnace were then ramped down 100°C every five minutes and the wafers were removed when the furnace temperature reached 900°C. After cooling, the thickness of the grown oxide was measured with the Rudolph AutoEl 3 Ellipsometer. The results of the oxide growth are shown in the following tables. The FOX thickness is useful in determining the etch time for each wafer.

Table 4.2 - Fabrication two wet oxide thicknesses (Å) after initial oxidation.

Wafer	Center	Top	Bottom	Left	Right	Average
1	6552	6696	6408	6459	6483	6519.6
2	6517	6656	6341	6399	6428	6468.2
3	6376	6551	6222	6285	6289	6344.6
4	6244	6238	6103	6194	6185	6192.8
5	6050	6294	5940	6044	6034	6072.4
6	5808	6070	5742	5828	5840	5857.6

After growth of the wet oxide, the wafers were coated with the photoresist primer and photoresist using the Specialty Coating Systems Spincoater Model 6700. The wafers were then exposed to the diffusion pattern using the Karl Suss MJB 3 Mask Aligner. The photoresist development process consists of exposure to a 5:1 solution of water to Microposit 351 for ~50s.

Figure 4.1 shows the diffusion pattern after 55s development of wafer five. This image is representative of the pixel pattern after diffusion development. The image shows distinct pattern shapes with defined isolation between the sources and drains of the three pixel transistors. The smallest dimension in the design occurs in the channel of the transistors; so, these areas are the most subject to over-development and over-etching. The pixel pattern appears blue while the surrounding photoresist appears pink. This distinct color variation indicates development is complete.

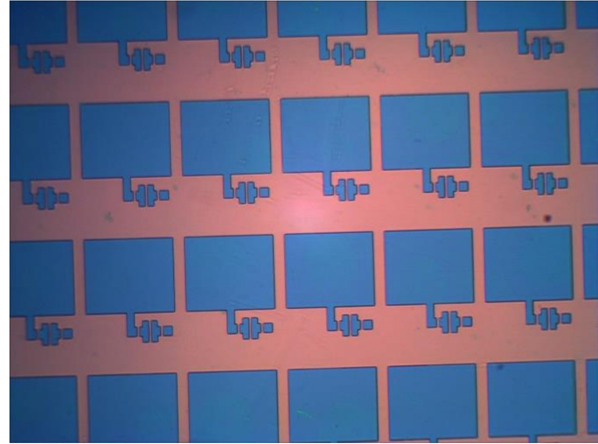


Figure 4.1 - Diffusion pattern of W5 for 55s under 10x optical magnification.

After development, the diffusion pattern is etched to expose the substrate. The etch rate was found to be approximately 500Å/min in undiluted Buffered Oxide Etch (BOE). The wafers exhibited slightly different etch rates; so, the wafers were inspected visually to ensure the oxide had been fully etched.

Figure 4.2 shows wafer two after nine minutes and 45 seconds of etch time. The etched regions appear white which indicates the substrate has been reached. The transistor channel appears distinct which indicates there is no over-etching.

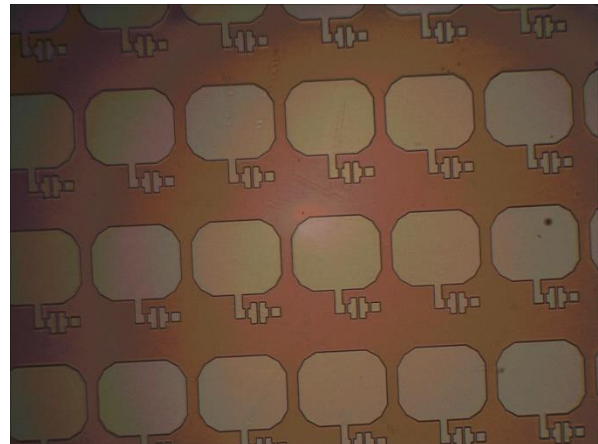


Figure 4.2 - W2 diffusion pattern after 9min 45s etch time.

Figure 4.3 and Figure 4.4 show SEM images of a single pixel and the source and drain of two transistors respectively. Inspection of

the pixel shows defined edges to the etched regions suggesting a mostly anisotropic etch. The sharp contrast at the edges of the etched regions suggests the interface of two different layers; i.e., the silicon substrate and oxide. The transistors shown in Figure 4.4 were designed with a channel length of 10μm. The SEM measurement indicates a channel length of 6.75μm which indicates slight isotropic etching. The sharp boundary suggests the diffusion pattern was not over-etched.

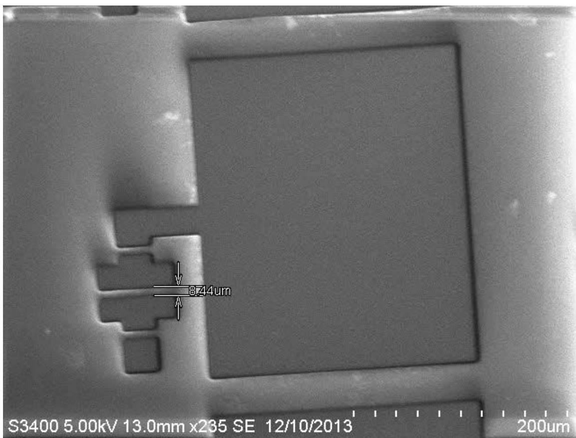


Figure 4.3 - SEM image of rectangular pixel after diffusion etch.

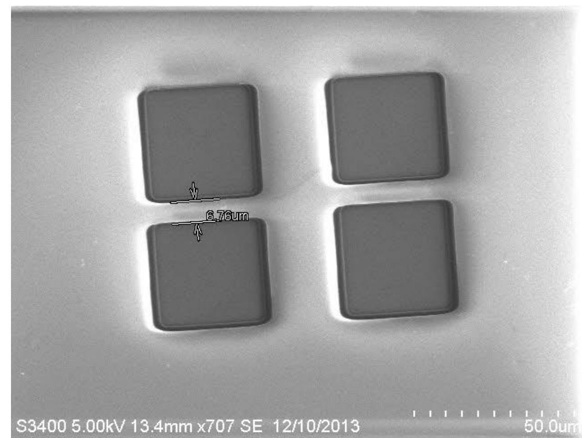


Figure 4.4 - Transistor source and drain patterns after diffusion etch.

During diffusion, the wafers were subjected to 25 minutes at 1100C. Previous fabrication results indicated that the time in the furnace for the wafers was too long and the junctions did not form properly. For this reason, the wafers were inserted into the furnace at a more aggressive 933°C to shorten the thermal exposure as the furnace heated to 1100°C.

The dummy wafers were etched to the substrate and dopant was applied to the entire surface. This creates a large area so that the sheet resistance can be measured after the diffusion process. The wafers exhibited average sheet resistances 2.955Ω/□ respectively. These values corroborate the Filmtronics P509 application notes.

4.1.2 Gate Oxidation

After the diffusion process, the gate oxide is grown over the transistor channels. The optical microscope image shown in Figure 4.5 shows the gate development on wafer two. The edges of the transistor sources and drains appear white as they were previously etched to the substrate during the diffusion etch. The gates in both the images shown appear fully devleoped due to the uniform color of the devleoped areas.

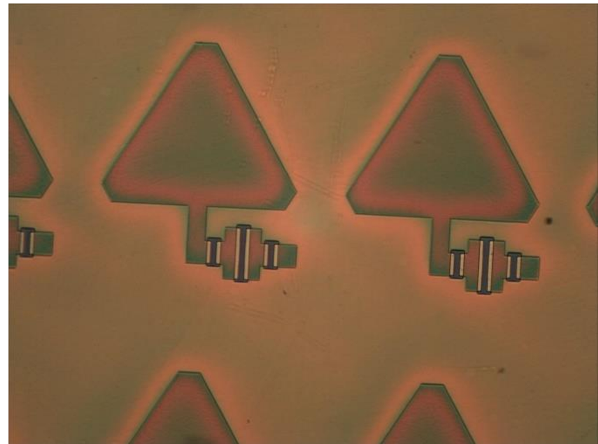


Figure 4.5 - W2 Gate development under 10x magnification.

The image shown in Figure 4.6 shows the gate etch of wafer one. The gate pattern was under-cut at the tops and bottoms of the gates due to the previously etched diffusion pattern. This should not lead to significant quality degradation so long as the under-cut gates are not connected.

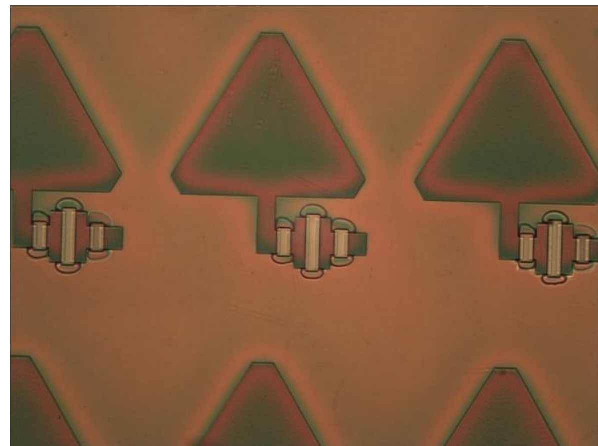


Figure 4.6 - W2 Gate etch after five minutes.

Figure 4.7 shows a SEM image of the pixel transistor gates after the gate etch. The under-cutting at the top and bottom of the transistors is more apparent in these images. Each gate region appears isolated from the adjacent gate so the transistor performance should not be affected. The under-cutting likely

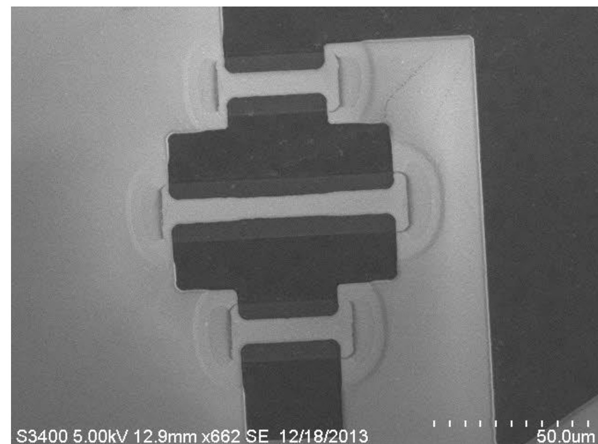


Figure 4.7 - W1 gate pattern after gate etch.

occurred due to the lack of the additional FOX after diffusion. The exposed areas at the intersection of the gate and source/drain were likely undercutting as the oxide was removed from the center of the channel.

The photoresist was then removed and the wafers were cleaned according to the RCA cleaning procedure and piranha solution (3:1 H_2SO_4 to H_2O_2) at 110°C for 10 minutes. The wafers were then arranged in the quartz boat and inserted into the furnace at 950°C. The furnace temperature was ramped up to 1100°C, and the wafers were oxidized for 25 minutes in an oxygen ambient. After 25 minutes oxidation, the oxygen flow was turn off and the wafers were annealed at 1100°C for 15 minutes in a nitrogen ambient. The temperature was then ramped down and the wafers removed at 950°C.

After the wafers cooled, the dry oxide thickness was measured using the ellipsometer on the dummy wafers. The dry oxide thicknesses are shown in Table 4.3. The target thickness for the dry oxidation process is 1000Å. The wafer closest to the oxygen flow (dummy 1) during the oxidation process exhibits the thickest oxide and is nearest the target thickness. The measurements on dummy two demonstrate the variability of the oxide thickness from the front of the wafer boat to the rear. The oxide thickness plays a significant role in determining threshold voltage and based on the measurements the fabricated transistors will likely exhibit non-uniform threshold characteristics.

Table 4.3 - Measured gate oxide thicknesses Å.

Wafer	**Center**	**Top**	**Bottom**	**Left**	**Right**	**Average**
Dummy 1	958	941	943	939	933	942.8
Dummy 2	706	801	690	693	699	717.8

4.1.3 Via One

The via layers allow electrically insulated layers to be electrically connected. Wafer six after via one development is shown in Figure 4.8. The vias exhibit a uniform color which indicates development is complete.

Oxide etching at this stage is subject to over/under-etching due to via etching through two different oxide layers. The vias above the source and drain of the transistors have to be etched through the denser gate oxide. Vias through the anode of the PDs must etch through the first grown oxide ~6000Å thick. A highly anisotropic etchant is desirable for this stage in the fabrication process to minimize undercutting.

Figure 4.9 shows wafer six from fabrication two after two minutes and 30 seconds of etching. The vias to the diffusion layer are nearly complete; however the via to the undoped substrate is not. This wafer required an additional three and a half minutes after the vias to the doped substrate were etched to complete the remaining vias. During this time, the nearly complete vias to the doped substrate are subject to over-etching.

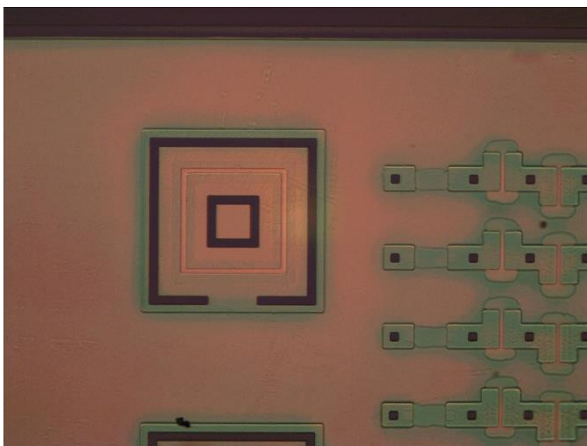


Figure 4.8 - W6 via one development.

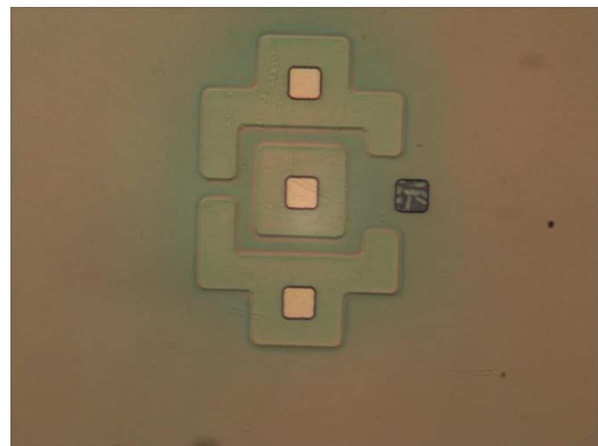


Figure 4.9 - W6 completed dry oxide etch and incomplete FOX etch after two min 30s etch

The left and right vias of the PD in the SEM image shown Figure 4.10 are vias to the doped substrate of wafer six. The top via is etched to the undoped substrate. As is shown in the image both types of vias appear to be completely etched with no visible undercutting.

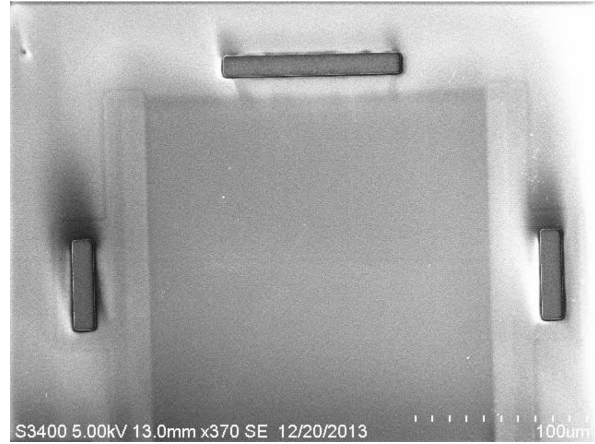


Figure 4.10 - W6 PD via etch showing completed vias.

The via shown in Figure 4.11 was designed at 10µm. It measures at 12.4µm. This suggests some lateral etching due to the prolonged exposure to the etchant; however, the connections to the vias were designed with a minimum of 4µm between the via and edges of the pad. Thus, with proper alignment, the larger vias will not overlap undesirable boundaries.

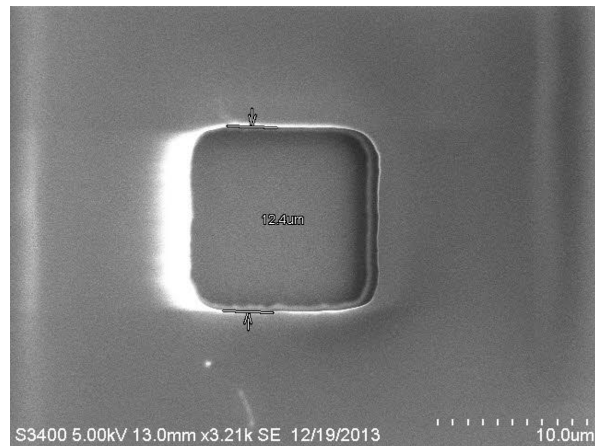


Figure 4.11 - W6 via one measurement.

4.1.4 Metal One

After the via one etch, the wafers were loaded into the evaporation chamber and aluminum deposition took place. The aluminum deposition process resulted in 5802Å thick layer of aluminum. The development of the metal one layer on wafer two is shown in Figure 4.12. The image shows good alignment at the termianls of the MOSFET which are the most cricitcal

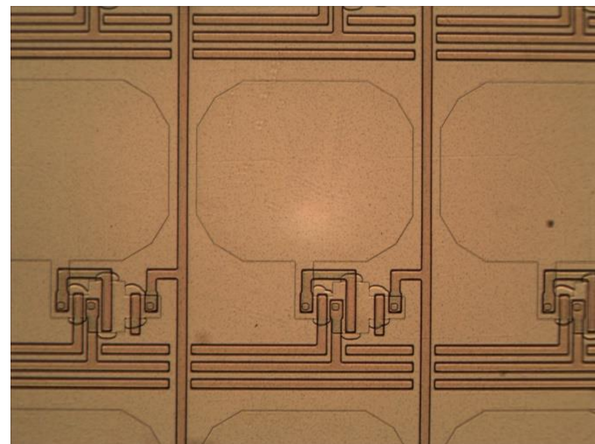


Figure 4.12 - W2 metal one development.

dimensions during the metal one alignment process. Any overlap of the gate contact to the source and drain will effectively short the gate to the connected terminal resulting in device failure.

The etched metal one layer of wafer two is shown in Figure 4.13. The mask pattern of the metal layers are inverted from the other masks. This is because the un-etched pattern is the metal routing. For this reason, the pattern at this stage is subject to over-etching which can result in thin traces or open circuits. There are no open circuits shown in Figure 4.13 which suggest good development of this layer.

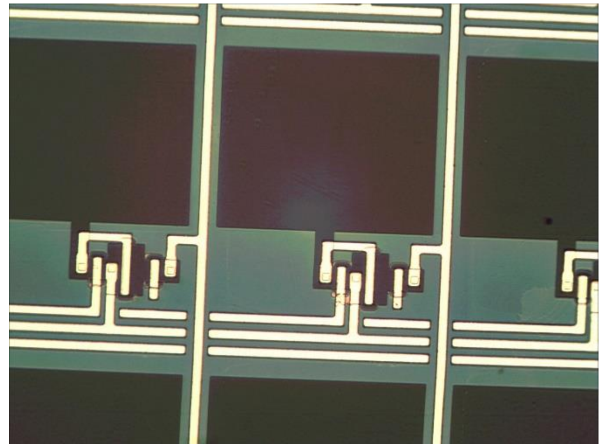


Figure 4.13 - W2 metal one etch.

4.1.5 Spin on Glass

To isolate the metal one and metal two routing layers, a thin film of SiO_2 (Filmtronics B20) was spin-coated on the wafers. The wafers were cured according to the Filmtronics application notes and a thickness of ~600Å was measured.

4.1.6 Via Two

After the SOG cure, the wafers were coated with photoresist and patterned with the via two mask. Wafer five from after via two ethcing is shown in Figure 4.14. The vias appear to be slightly off-center which indicates some variation in alignment; however, the vias connect to the corresponding metal traces and suggest contact will be made as designed.

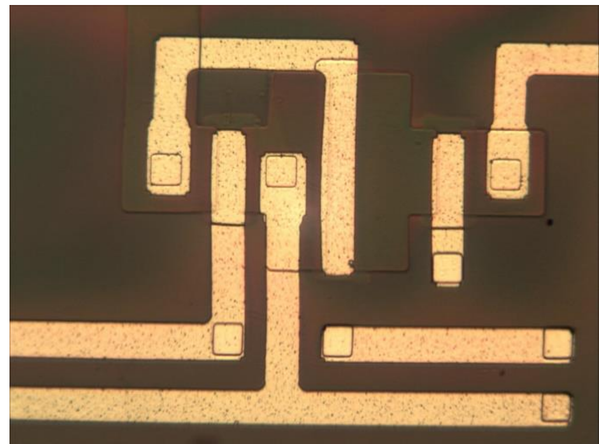


Figure 4.14 - W5 via two pattern.

4.1.7 Metal Two

The aluminum thickness of the metal two layer was 5311Å. The image in Figure 4.15 shows the metal two routing of wafer one. On wafers one and two, there appeared to be an issue with the photoresist development. The image shown in Figure 4.16 shows that regardless of etch time certain areas of these wafers did not etch. This indicates incomplete development of the photoresist which was preventing the aluminum etchant from reacting with the aluminum layer in these areas. The development time for the metal two layer in fabrication two was kept short to ensure adequate trace width; however, it appears the time was too short. A slightly longer development would likely improve the etching in these areas. Despite the incomplete etch in these areas, there were correctly developed die on these wafers.

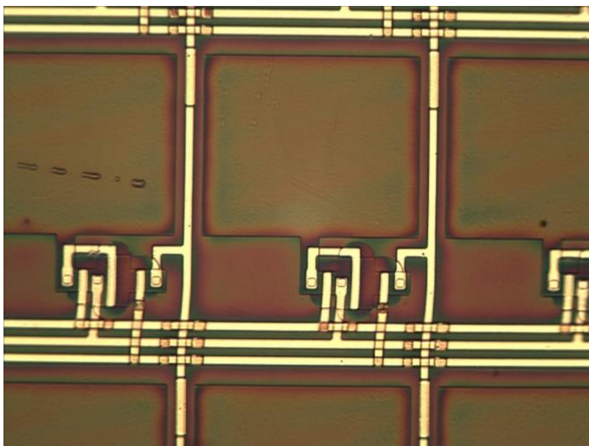


Figure 4.15 - W1 metal two formation. Traces exhibit no open circuits.

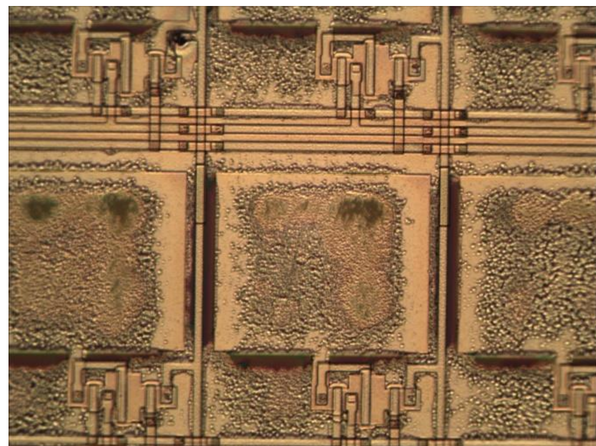


Figure 4.16 - W1 unremoved aluminum.

4.2 Photodiode Characteristics

The preliminary calculations suggested a transistor threshold in the range of 1-2V. For this reason, the imager circuits were operated with a logic voltage of 3.3V and the dark current was measured at 3.3V reverse bias. Ideally, VSAC controlled operation of the PD arrays would have allowed for efficient quantization of PD responses. However, the fabricated arrays were non-functional due to transistor characteristics (Section 4.3). For this reason, the PD measurements

were obtained manually, and the sample size is small. The results are inconclusive but indicate the rounder geometries of the rectangular design improve PD dark response; however, the samples presented are only indicative of the PDs on the test die.

4.2.1 Dark Currents

The average dark current of all diodes of a particular shape is not indicative of overall relationship between the PD shape and the dark response due to device variations. For this reason, the dark response of each diode shape must be compared to PDs on the same die. Typical dark currents were in the range of tens to hundreds of microamps; however, wafer two from fabrication two exhibited dark currents as low as a few nanoamps. In the nanoamp range, circuit noise played a large role in the measured currents so the recorded values are presented as the averages of the RMS current density of 30 dark current measurements corresponding to a single PD. The measurements are taken from the discreet PDs on the test die.

To compare the diodes exhibiting dark current in the microamp range, the dark current density measurements were normalized using the dark current average and standard deviation of each die. The normalized data was then averaged according to PD shape and the results are presented in Table 4.4. According to the normalized values, the rounded square shape of PD three exhibited the lowest dark current characteristics. This suggests the rounded corners improve the dark current response of the rectangular PD. The rounded corners of the triangle shape do not appear to improve the dark response of the triangular pixel. It is possible that the charge gradient created by the triangular shapes facilitates the transfer of dark current in PD shapes four and five.

Table 4.4 - Normalized value of dark current density from wafer one fabrication two.

PD Number	**1**	**2**	**3**	**4**	**5**
Normalized DC Average	-0.39	-0.33	-0.64	0.48	0.84

The dark currents of wafer two from were measured in the nanoamp range. Figure 4.17 shows the characteristic diode curve of a diode from wafer two in dark conditions. The breakdown voltage of the diode appears at -7.1V and the turn on voltage at 0.7V. The PDs from wafer one exhibited a reverse breakdown at -6.35V and a turn-on voltage at 0.65V. The differences in the breakdown and turn-on voltages from wafer one to two indicates inconsistencies in the junction formation between the two wafers which are likely due to ionic contamination during fabrication.

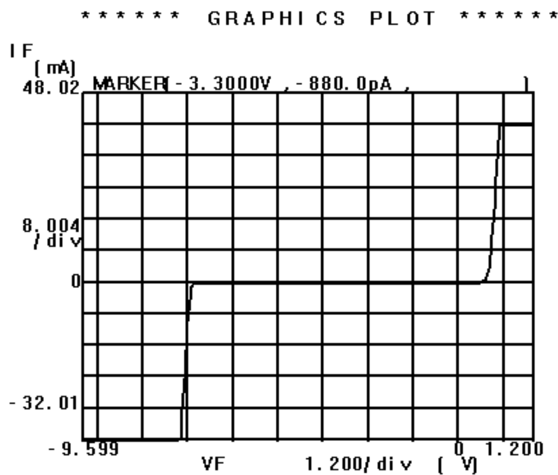


Figure 4.17 - Diode dark current with respect to bias voltage of a square PD on W2.

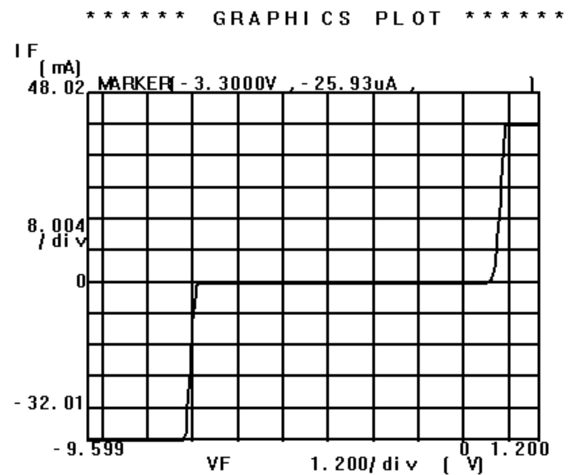


Figure 4.18 - Diode illuminated current with respect to bias voltage of a square PD on wafer two.

The dark current measurements obtained from wafer two were consistent from die to die. For this reason the measurements are presented as the average RMS value of the dark current density. The RMS values of the dark current and dark current density measurements of wafer two are presented in Table 4.5. The dark current measurements indicate improved dark response

for the rounded triangular pixel shape of PD five; however, the reduced dark current measurement is the result of the smaller PD area. The dark current density measurements suggest the square shape of PD one performs the best on wafer two.

Table 4.5 - Dark current and Dark Current Density Averages from W2.

PD Shape	**1**	**2**	**3**	**4**	**5**
R.M.S. Dark Current (nA)	6.94	8.09	7.53	6.61	5.62
R.M.S. Dark Current Density (μA/cm^2)	9.25	11.27	10.93	17.63	15.46

The results are characteristic of a small sample size of tested PDs. It appears the pixel dark current may be improved by the rounded geometries of pixels two and three. The rounded triangular shape of Pixel Five appears to improve the PD dark response over Pixel Four. The measured dark current densities are significantly higher than the 0.375μA/cm^2 reported in the research of Furtado *et al* which is due to the use of spin-coating rather than ion implantation in the current research. [15].

4.2.2 Illuminated Currents

The PDs were tested in illuminated conditions to characterize the photo-generated current characteristics. To test the illuminated response of the PDs, a UV lamp was positioned at a distance from the wafer surface such that the incident irradiation was equivalent to the AM 1.5 Spectrum. The photocurrent was then measured. Figure 4.18 shows the same diode as that of Figure 4.17 under illumination and exhibits an illuminated current of -25.93μA at -3.3V reverse bias. The measured illuminated current is much higher than anticipated. This suggested the optical generation rate under the UV light are higher than the simulated values. The elevated illuminated current would depleted the charge stored on the PD capacitance quicker than the

simulation results suggest. The UV lamp emits a wavelength spectrum different from the AM 1.5 Spectrum which may contribute to the high illuminated current.

The illuminated current measurements and RMS values of the dark current were used to characterize the dynamic range of the PDs. This measurement is not the same as imager dynamic range because the ability of the SF transistor to buffer the integration voltage sets the lower end of the imager output. However, the dynamic range of the PDs is set by the maximum and minimum current outputs of the PDs. The PD's of wafer two exhibited an average dynamic range of 68.3dB. The PDs of wafer one exhibited a dynamic range of 43.2dB. This suggests the PDs of wafer two are more suitable for imager operation.

4.3 Transistor Operation

The parallel MOSFET structures on the test die with common source and common drain on the test die were not used for MOSFET parameter characterization. The individual MOSFET characteristics varied significantly. If a single MOSFET in the transistor array operated in depletion mode or exhibited a short at the junction, the entire array appeared to operate incorrectly. Also, the parallel drain to source resistance of the MOSFETs in this configuration led to high measured currents which made individual MOSFET contribution indistinguishable.

The MOSFET threshold voltage was measured by plotting the square root of the drain current with respect to the gate to source voltage. Lines were fitted to the curve in the cutoff and saturation regions of the drain current. The point at which these lines intersected was determined to be the threshold voltage. Typically, the intersection of a line of best fit in the saturation region of the transistor curve and the x-axis indicates the threshold. However, the cutoff current was usually measured in the range of a few microamps which led to a skewed threshold when extrapolating to the x-axis.

The characteristic curve of a biasing MOSFET on wafer two of an imager die near the center-bottom of the wafer is shown in Figure 4.19. The plot shows a drain to source voltage of roughly 6V results in about 19µA drain current in saturation. The MOSET exhibits a cutoff current of 5.68µA. The MOSFETs fabricated in the research of Furtado *et al* exhibit a saturation current of approximately 700µA with a 5V drain to source voltage and a cutoff current of 14pA [15]. The low saturation current and high cutoff current of the fabricated MOSFETs lead to non-functioning imagers due to an indistinguishable difference between the cutoff and saturation states of the transistors.

Figure 4.20 shows the transfer curve of the same MOSFET measured in Figure 4.19. The transfer curve indicates a threshold voltage of roughly 4.5V when V_{DS} is 5V. The VSAC was designed for 3.3V operation, and the ADC cannot sample voltages above 3.3V. This suggests the readout circuitry will be incompatible with imagers containing MOSFET's with these characteristics.

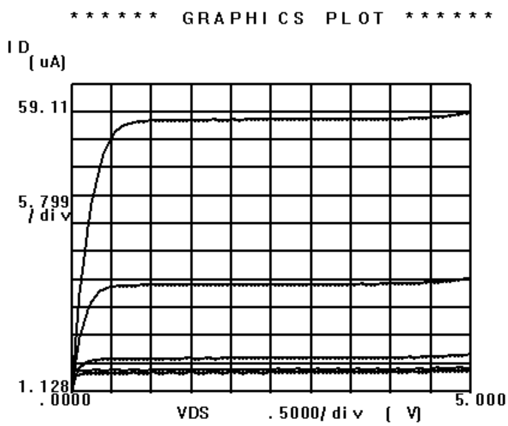


Figure 4.19 - MOSFET characteristic curve obtained from wafer two.

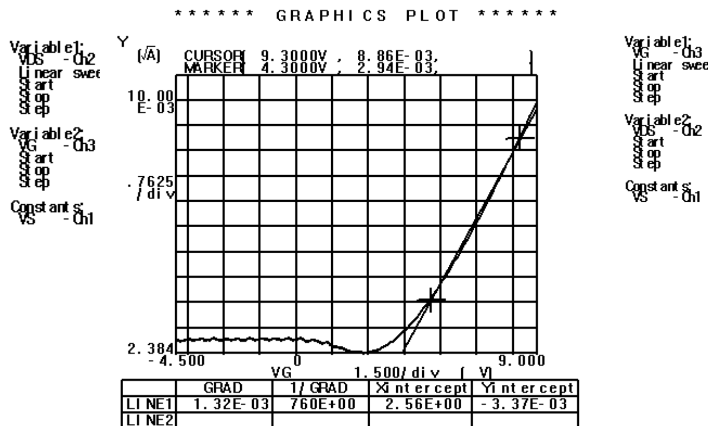
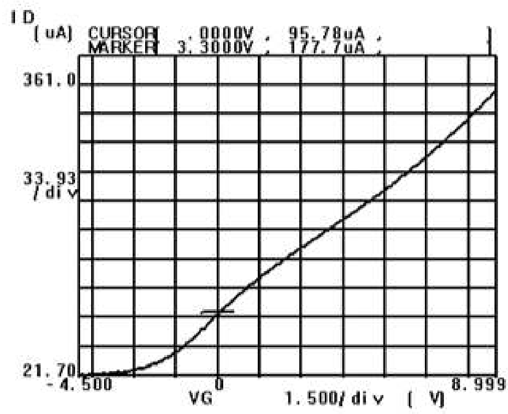
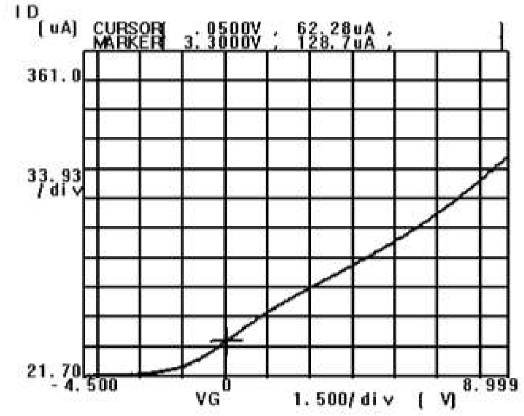


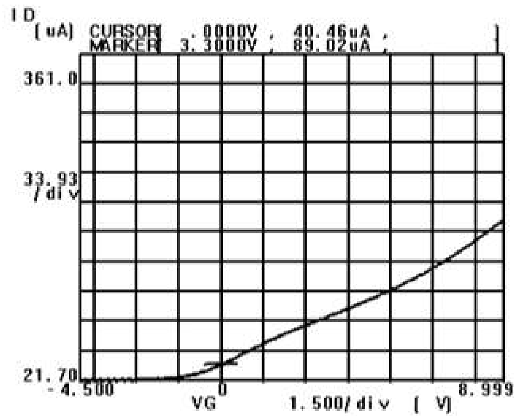
Figure 4.20 - MOSFET transfer curve obtained from wafer two.

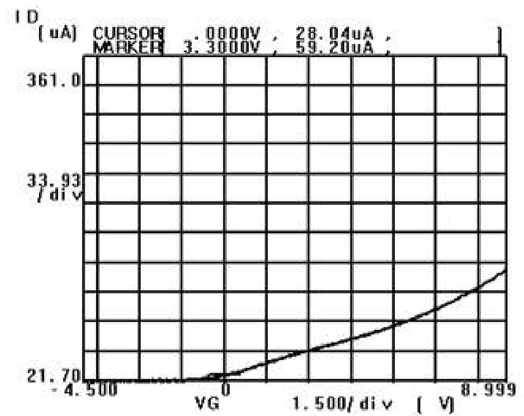
The transistors from wafer one exhibit an average threshold of -1.91V. To drive the threshold into the positive regime the body-biasing effect was employed. The effect of the body-

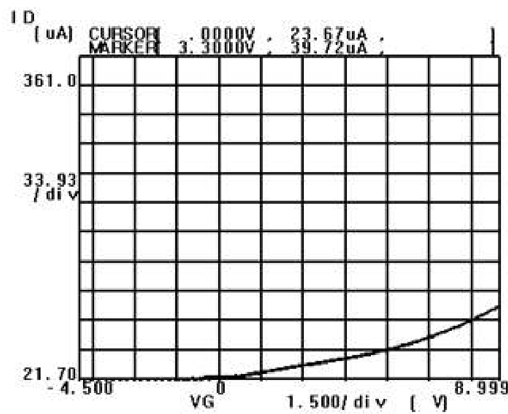
biasing effect on a MOSFET near the center-bottom of a die on wafer one is shown in Figure 4.21. Each consecutive image shows an increase in the source to bulk voltage of 0.1V. The images are left unscaled to better demonstrate the shift of the transfer curve. The first image shows a threshold voltage in the range of -1.5V with a 0V bias between the source and bulk. The threshold of the final image with a 0.5V bias applied show a threshold of ~5.2V. Thus, the 0.5V bias difference leads to a threshold shift of ~6.7V which is about 2.6 times the expected magnitude of the shift. Ideally, the shifted curves would exhibit thresholds in the range of 1-2V; so, the MOSFET shown in the figures would need an applied source to bulk bias of approximately 0.2V.











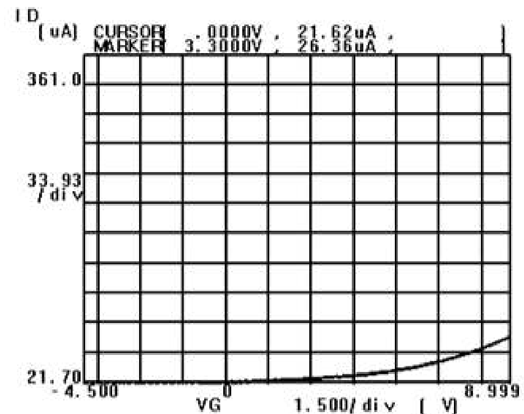


Figure 4.21 - Effect of bulk biasing in 0.1V increments on a transistor from wafer one fabrication one.

Figure 4.22 is the scaled view of the 0.5V bulk biased transistor. The figure shows the transistor threshold has been shifted into the positive regime. The drain current at voltages below threshold seem to exhibit increased noise. This may be due to the widened junction between the source and bulk of the transistor collecting an increased number of thermally generated carriers. The high cutoff current compared to the saturation current shows a dynamic range of only 10dB whereas the MOSFETs of Furtado *et al* exhibit a dynamic range of 154dB [15].

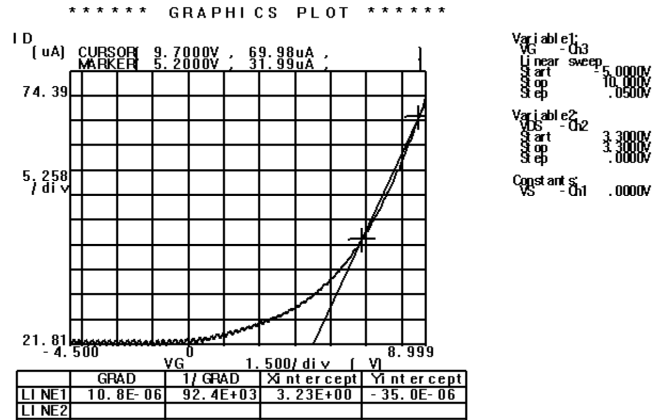


Figure 4.22 - Scaled view of 0.5V bulk biased TX.

4.4 VSAC Verification

The VSAC was verified prior to the attempted image readout. The Salea eight channel 24MHz logic analyzer was used to obtain timing diagrams of the circuit operation. The program code for imager operation can be found in Appendix C. The VASC was designed to send an overdriven reset pulse, wait for the integration period, and then perform charge transfer through the use of the row select transistors. The transferred charge was then sampled at the eight output nodes and serialized through the MUX through the use of the three bit counter. The timing diagram shown in Figure 4.23 shows this iteration pattern over each of the eight rows and columns of the imager circuit. The timing diagram shows correct operation of the controlling circuitry.

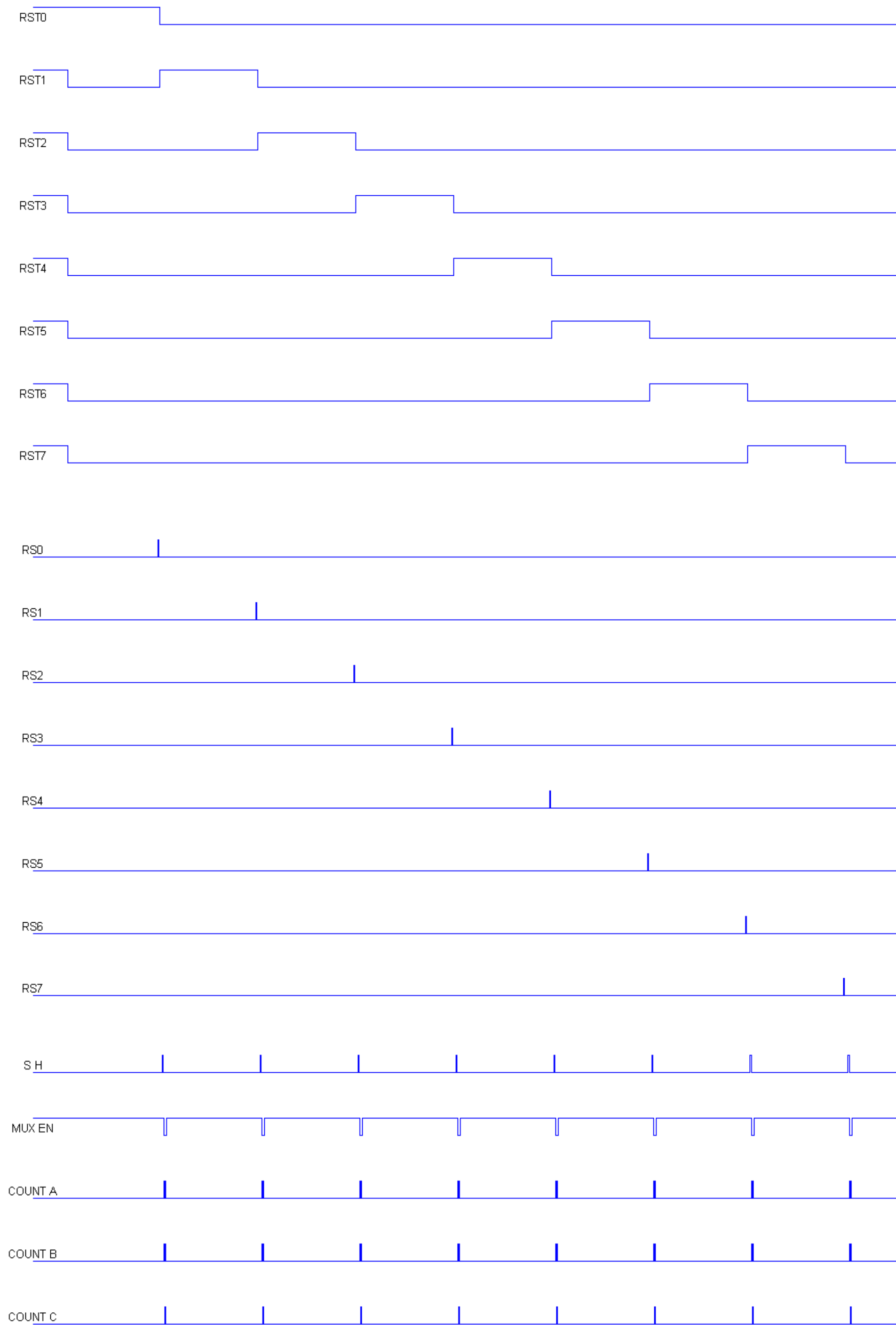


Figure 4.23 - Logic capture of readout circuitry operation.

A close up view of the RST0 and RS0 timing pulses along with the sample and hold pulse is shown in Figure 4.24. The integration time is the time between the end of the reset period and the beginning of charge transfer to the column bus. The integration period shown in the image is 27µs. The integration time is controlled through the use of the SysTick peripheral on the LM3S696 which functions as a timer. The period of the timer can be set and upon reaching a predetermined value the system will interrupt and trigger the appropriate changes in the outputs. Due to overhead in the code, the minimum possible integration time with the designed system was 27µs while operating on an 8MHz clock.

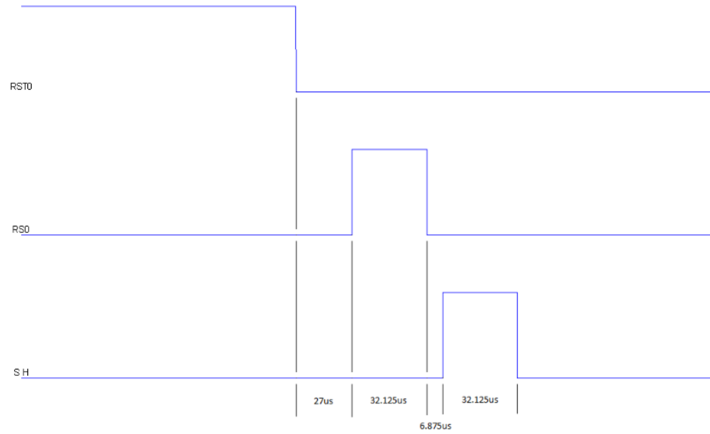


Figure 4.24 - RST0, RS0, and SH pulse details

Operation of the counter is detailed in Figure 4.25. The counter is used to select the active input to the MUX which is then sampled by the ADC. The figure shows the counter iterating over all eight outputs of the imager, which causes each MUX input to be sampled sequentially. As shown in Figure 4.23, the MUX and counter are only active during the sampling period. The sampling period is 67.875µs after which point the serialized data is sent via UART to the PC.

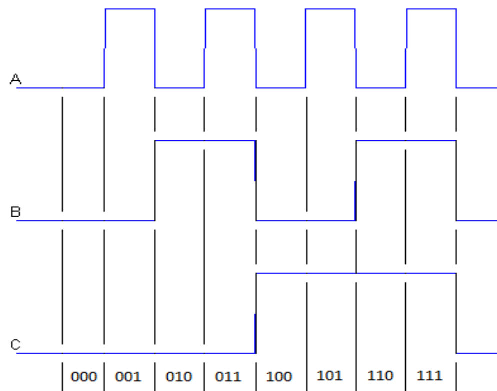


Figure 4.25 - Counter operation during readout.

4.4.1 Image Readout

The company performing the wafer bonding was unable to achieve bonding between the IC pads and the bonding wires, as the aluminum peeled from the wafers. Wafer bonding would have enabled interface between all IC inputs and outputs. Because wafer bonding was unsuccessful, image readout was attempted by probing the RST0, RS0, Output0, GND, V_{DD}, and V_{Bias} pads on several imager die with the probe station. Using the probe station, the VSAC can only communicate with one pixel rather than the entire array. The transistor sources were shorted to the bulk and V_{DD} was set to 3.3V. The imager output was consistent at the lower bound of the sample and hold threshold (1.55V) regardless of light intensity, integration time, bias voltage, and operational voltage.

To assess the PD performance on the IC, a 2N7000 N-FET was connected to the readout circuitry and a standalone rectangular PD from a wafer two test die. Using a breadboard the circuit was connected as shown in Figure 4.26 creating a PPS pixel. The RST transistor was overdriven with 5V, and the voltage decay on the PD was captured using an oscilloscope. The use of the breadboard and probe station to capture the PD response introduces stray capacitance that was not accounted for during the simulation. The result of the increased capacitance will be a slower voltage decay as compared to the simulation.

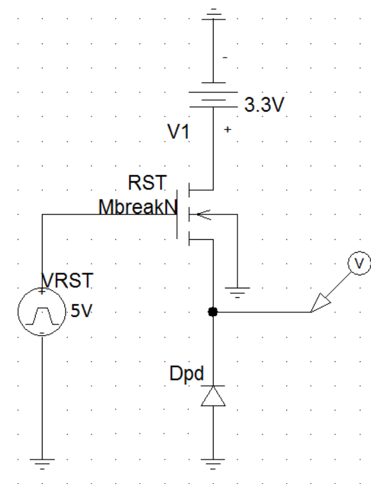


Figure 4.26 - Test circuit for PD characterization.

The oscilloscope capture of the voltage decay after reset is shown in Figure 4.27 and Figure 4.28 for light and dark conditions respectively. The dark current of this particular PD was measured at 9.52nA RMS and ambient light current was 771.5nA. As shown in the figures, the illuminated and dark current fall times are 152µs and 192µs respectively. The faster fall time of the illuminated current is indicative of faster PD capacitance discharge as a result of the higher photocurrent. As suggested by Weckler, the voltage decay should be approximately linear [18]. The voltage decay of the curves is nearly linear between 1.4 and 3.3V. An ambient light source was used instead of the high intensity light used to test the PDs in the preliminary characterization. This was done because the high intensity UV lamp yielded photocurrents in the microamp range. This led to voltage decays of less than 27µs which was the minimum achievable integration time of the VSAC. An alternative Dolan-Jenner Fiber-Lite MI 150 light was used as the high intensity light source for further device characterization.

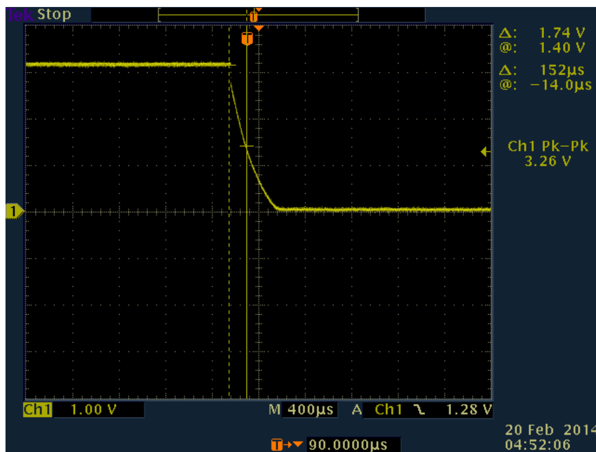


Figure 4.27 - Square PD voltage decay while illuminated.

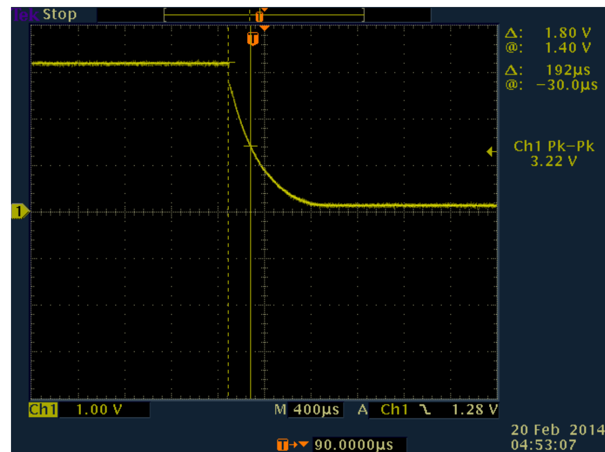


Figure 4.28 - Square PD voltage decay in dark conditions.

The calculations suggested a PD capacitance of 3.40pF for PD One which led to a simulated voltage decay in the range of 10µs. The capacitance of the various PD shapes was measured with a 3.3V reverse bias using the probe station and Agilent LCR meter. The

measurements are presented in Table 4.6. The discrepancy between the measured capacitance and calculated capacitance are likely the result of stray capacitance in the wire leads used to probe the PD terminals. The increased capacitance results in a slower voltage decay during charge integration as compared to the simulation. The measurements shown in Table 4.6 indicate that with the discrete test circuit shown in Figure 4.26, the necessary integration times will be longer than the simulation predicted.

Table 4.6 - Measured PD capacitance at 3.3V reverse bias.

PD Shape	**1**	**2**	**3**	**4**	**5**
Capacitance (pF)	133	129	126	75	72

ADC voltage capture was then performed using the VSAC at the output node shown in Figure 4.26. The PD voltage output was dependent upon integration time and light intensity and the numbers are presented in the following section. The proper operation of the VSAC and PD suggest the non-functioning imager is the result of inoperational MOSFETs. The MOSFET testing results exhibited cutoff drain currents consistently in the microamp range. The high currents would discharge the small capacitances of the PD and output nodes too quickly. For this reason, if any integrated charge was transferred to the output node during imager operation, it would likely only be manifest for very short periods of time. The voltage would likely decay before the VSAC could obtain a reading.

4.4.2 Readout Characterization

The goal in designing the imager and readout circuitry was low-noise performance. The readout circuitry was tested to ensure minimal noise injection to the measured PD signal. To test the noise performance of the readout circuitry, 1.5, 2.5, and 3.0V DC voltages were applied to the input of the sampling circuitry using the BK Precision Model 1762 power supply. The power

supply has <100mV variation on the DC output. The VSAC input was then sampled 64 times at each voltage to determine the variability of the output signal. The results are summarized in Table 4.7. The results show accurate readout at 2.5 and 3.0V. The 4.22% deviation at 1.5V is due to an input voltage below the differential logic threshold of the LF398 sample and hold ICs. The standard deviation of the output voltage is a measure of the magnitude of random voltage fluctuations present at the VSAC output. A minimal standard deviation demonstrates decreased voltage fluctuations due to circuit noise. The measured values exhibit standard deviation with less than 4mV in all cases. The 100mV ripple of the input signal is not manifest in the output signal which further suggests excellent noise performance as a result of the ADC hardware averaging. Every recorded sample is the average of eight samples which effectively averages the noise in the input signal.

Table 4.7 - Input and Output voltage readings of readout circuitry.

Input (V)	**1.5000**	**2.5000**	**3.0000**
Output Average (V)	1.5633	2.4859	2.9681
Standard Dev. (V)	0.0019	0.0020	0.0036
Deviation (%)	4.22	-0.56	-1.06

Using the test circuit shown in Figure 4.26, the five PD shapes on the test die were tested. Initially PD shape 4 was used to calibrate the integration time as it yielded the lowest voltage reading under illumination. A Dolan-Jenner Fiber-Lite MI 150 light was used to supply a high intensity light to the PD, and the voltage output was measured under illuminated and dark conditions. The dark readings reach a maximum level of ~2.7V. Although the PD is initially reset to 3.2V through the operation of the RST transistor, the dark current lowers the integrated voltage before sampling. The integration time was then characterized such that the high intensity

light resulted in nearly full depletion of the PD node which is the same as the differential threshold of the LF398 of 1.55V. An integration time of 27µs was found to be suitable for the integration period.

The PDs were then measured in high light, ambient light, and dark conditions. The average voltage output in each scenario are shown in Figure 4.29. Figure 4.29 shows the voltage decay of each PD in varying light conditions after a 27µs integration time. A higher average voltage correlates to a blacker pixel while a lower voltage correlates to a whiter pixel. Thus, a PD with a higher voltage in dark conditions would yield a better quality image. Only PDs from wafer two were measured. The high dark and illuminated currents of the PDs on wafer one caused a voltage decay across the PD faster than the circuitry could sample. Initial PD readings exhibited significant image lag with a reset period of 100µs. The first sample would result in a higher output than consecutive samples as the PD voltage was not reaching V_{DD} before the subsequent integration period. A reset period of 5ms with a RST gate voltage of 5V was found to be suitable to prevent image lag.

The results of the dark condition test agree with the dark currents measured from wafer two. PD One yields the highest integrated voltage during dark conditions suggesting better dark current performance in this shape. PD One also exhibits the highest voltage in the high light scenario. This suggests the PD One exhibits the best dynamic range and the integration time could be increased for this shape which would lead to better voltage resolution and more accurate pixel coloring.

The faster voltage decay of the rounder and triangular shaped PDs is likely due to the faster discharge of the smaller PD capacitances. A smaller PD capacitance results in a decreased PD well capacity which requires less charge transfer for voltage fluctuation. These diodes would

require a shorter integration time as compared to the rectangular PD. The research suggests shorter integration time would yield lower dark current manifestation as suggested by Equation 2.10.

PDs four and five exhibit the most significant voltage decay in the high and ambient light scenarios. The faster voltage decay is most likely mainly caused by the decreased PD capacitance. However, the faster decay of the triangular shape in particular may be the result of shape assisted charge transfer. Triangularly shaped PDs with the same capacitance as the square test bench would determine if the effect is due to PD capacitance or assisted charge transfer.

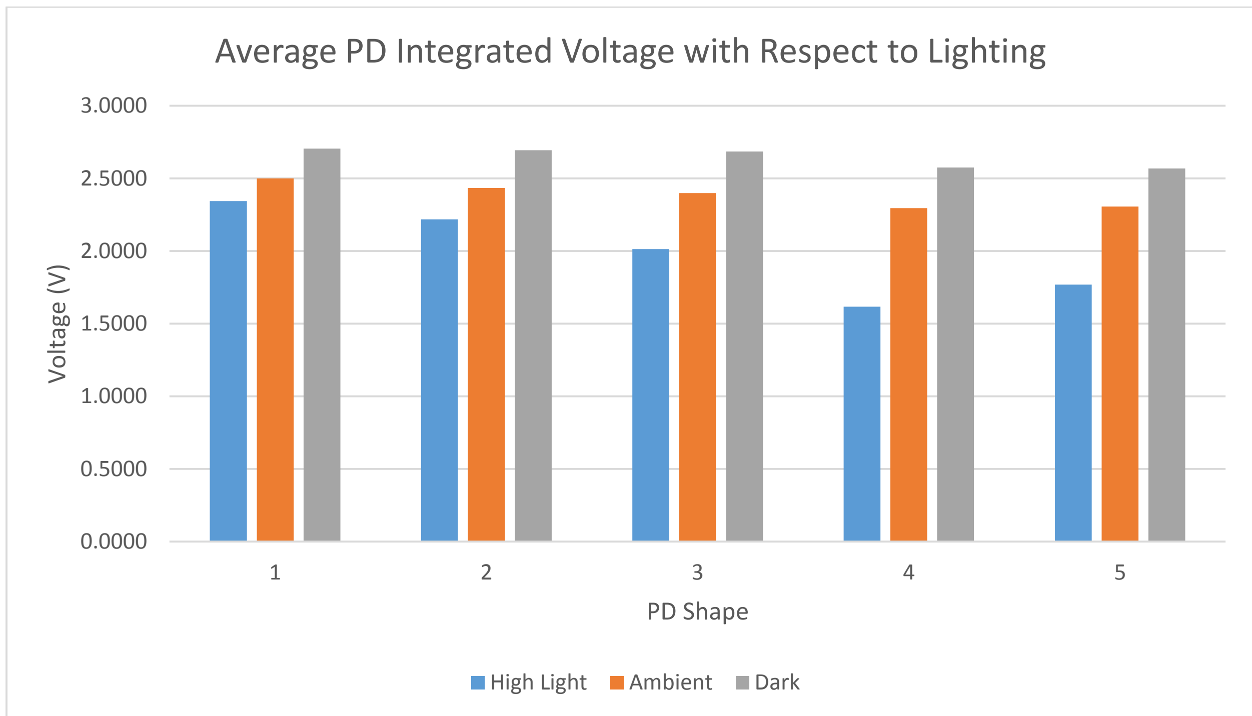


Figure 4.29 - Voltage response of PD shapes with respect to light intensity.

Table 4.8 shows the magnitude of the voltage decay of the PD shapes based on the difference between V_{DD} and the measured voltage in dark conditions over the 27μs integration period. The research of Furtado *et al* suggests a voltage decay in dark conditions of 48s [15].

The values presented in Table 4.8 show the PDs charge well would be depleted in ~140µs. The research of Furtado *et al* utilized ion implantation which results in a more uniform and predictable junction than spin-on application [15]. This partly explains the performance difference of the benchmark and current research.

Table 4.8 - Voltage decay in dark conditions of PD shapes.

PD Shape	**1**	**2**	**3**	**4**	**5**
PD Voltage Decay in Dark Conditions (V/ms)	22.07	22.47	22.74	26.86	27.05

Figure 4.30 shows the standard deviation of the voltage readings with respect to light intensity. The standard deviation is indicative of the magnitude of PD noise. It appears the PDs exhibit the highest noise characteristics when exposed to high light intensity. This may be the result of thermally injected carriers from the higher currents experienced at high illumination. Characterization of the VSAC showed a <4mV standard deviation. To demonstrate the PDs are inherently noisier than the readout circuitry the data in figure 4.30 is presented. The standard deviation of the voltage output is, at its smallest, is approximately three times larger than the noise of the VSAC. The figure justifies the assertion that reducing pixel dark current would significantly improve imager quality.

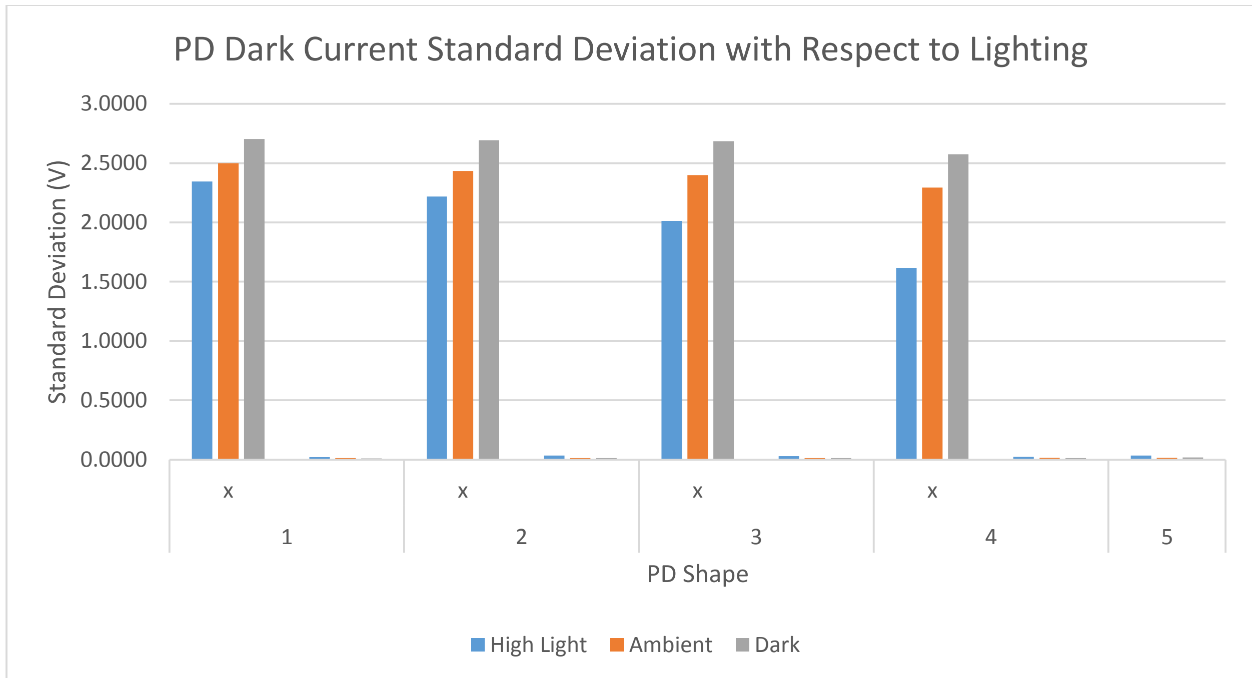


Figure 4.30 - Standard Deviation of voltage response of PD shapes with respect to light intensity.

The improved charge transfer reported by Shin *et al* is suggested by the dark current densities of PDs four and five as well as the elevated voltage decay rate [14]. The triangular shapes of PDs four and five were meant to assist in charge transfer and result in increased voltage readout. The higher dark currents measured in these shapes may be the result of improved charge transfer acting on charge generated in dark conditions. The output voltage elevating effect may be masked by the higher dark currents and lower PD capacitances associated with PDs four and five.

5 Conclusions

The hypothesis that rounder corners in the PD shapes would improve dark current performance in NMOS imagers was suggested but not confirmed by this research. The improved charge transfer resulting in elevated voltage output of the triangular pixel was not observed; however, this behavior was likely offset by the higher dark currents and lower PD capacitances observed in PD shapes four and five. The higher dark currents observed in these shapes may be the result of improved charge transfer characteristics acting on the generated charge carriers. The results suggest improved performance of the rounder PD geometries; however, due to small sample size, the results are inconclusive.

The PDs of wafer two in fabrication two exhibited good operational characteristics with dark current densities in the range of 9-18μA/cm^2. These PDs were interfaced with a makeshift PPS pixel circuit to confirm the design of the VSAC. The VSAC exhibited excellent noise performance while allowing for easy alteration of the control signals. The hardware sample averaging led to high precision during readout with a one percent deviation in output accuracy between output voltages of 1.55 to 3V.

The fabricated transistors exhibited high cutoff currents and low saturation currents as well as threshold voltage non-uniformity. The non-functioning imagers are attributed to the performance of the fabricated MOSFETs due to confirmed operation of the VSAC and PDs. Had the MOSFETs operated correctly, the imagers most likely would have been operational.

6 References

[1] P. P. Suni, "CCD Wafer Scale Integration," *Proceedings., Seventh Annual IEEE International Conference on Wafer Scale Integration,* vol. 123, no. 133, pp. 18-20, 1995.

[2] M. Bigas, E. Cabruja, J. Forest and J. Salvi, "Review of CMOS Image Sensors," *Microelectronics Journal,* vol. 37, pp. 433-451, 2006.

[3] A. J. Theuwissen, "CMOS Image Sensors: State-of-the-Art," *Solid-State Electronics,* vol. 52, pp. 1401-1406, 2008.

[4] K. Murari, R. Etienne-Cummings, N. Thakor and G. Cauwenberghs, "Which Photodiode to Use: A Comparison of CMOS-Compatible Structures," *IEEE Sensors Journal,* vol. 9, no. 7, pp. 752-760, July 2009.

[5] I. Brouk, A. Nemirovsky, K. Alameh and Y. Nemirovsky, "Analysis of noise in CMOS image sensor based on a unified time-dependent approach," *Solid-State Electronics,* vol. 54, pp. 28-36, 2010.

[6] H. Ji and P. A. Abshire, "A CMOS image sensor for low light applications," in *Circuits and Systems*, 2006.

[7] Y.-C. Shih and C.-Y. Wu, "A new CMOS pixel structure for low-dark-current and large-array-size still imager applications," *IEEE transactions on circuits and systems--I: Regular papers,* vol. 51, no. 11, November 2004.

[8] S.-G. Wuu, H.-C. Chien, D.-N. Yaung, C.-H. Tseng, C. S. Wang, C.-K. Chang and Y.-K. Hsaio, "A high performance active pixel sensor with 0.18um CMOS color imager technology," in *Electron Devices Meeting*, 2001.

[9] M. Takenaka, K. Morii, M. Sugiyama, Y. Nakano and S. Takagi, "Ultralow-dark-current Ge photodetector with GeO2 passivation and gas-phase doped junction," in *International Conference on Group IV Photonics*, 2011.

[10] C.-Y. Wu, Y.-C. Shih, J.-F. Lan, C.-C. Hsieh, C.-C. Huang and J.-H. Lu, "Design, optimization, and performance analysis of new photodiode structures for CMOS active-pixel-sensor (APS) imager applications," *Sensors Journal, IEEE,* vol. 4, no. 1, pp. 135-144, February 2004.

[11] Z. Huiming, W. Tingcun and Z. Ran, "Modeling of pinned photodiode for CMOS image sensor," in *2011 IEEE International Conference on Signal Processing, Communiations and Computing.*, 2011.

[12] B. Mheen, M. Kim, S. Y.-J. and S. Hong, "Operation Principles of 0.18-um Four-Transistor CMOS Image Pixels with a Nonfully Depleted Pinned Photodiode," *IEEE Transactions on*

Electron Devices, vol. 53, no. 11, November 2006.

[13] I. Shcherback, A. Belenky and O. Yadid-Pecht, "Empirical Dark Current Modeling for Complementary Metal Oxide Semiconductor Active Pixel Sensor," *Optical Engineering,* vol. 41, no. 6, pp. 1216-1219, December 2001.

[14] B. Shin, S. Park and H. Shin, "The Effect of Photodiode Shape on Charge Transfer in CMOS Image Sensors," *Solid State Electronics,* vol. 54, pp. 1416-1420, 2010.

[15] A. Furtado, J. Diniz and D. de Lima Monteiro, "Fabrication and characterization of active pixel sensors (APS) using simple metal gate nMOS technology," *ECS Transactions,* vol. 23, no. 1, pp. 461-467, 2009.

[16] E. R. Fossum, "CMOS Image Sensors: Electronic Camera on a Chip," *Electron Devices Meeting,* vol. 17, no. 25, pp. 10-13, 1995.

[17] Teledyne DALSA, "Image Sensor Architectures for Digital Cinematography," [Online]. Available: http://www.teledynedalsa.com/public/corp/PDFs/papers/4K_Workflow_Whitepaper_03-70-00209-00.pdf. [Accessed 22 July 2013].

[18] G. P. Weckler, "Operation of p-n junction photodetectors in a photon-flux integrating mode," *IEEE Journal of Solid-State Circuits,* Vols. sc-2, no. 3, pp. 65-73, September 1967.

[19] B. Pain, T. J. Cunningham and B. R. Hancock, "Noise Sources and Noise Suppression in CMOS Imagers," *Focal Plane Arrays for Space Telescopes,* vol. 5167, pp. 111-120, August 2004.

[20] C.-C. Wang, "A study of CMOS technologies for image sensor applications," Massachusetts Institute of Technology, 2001.

[21] A. Godbeer, "Investigation of 4T CMOS Image Sensor Design and the Effects of Radiation Damage," Surrey, 2010.

[22] B. Pain, G. C. T. J. Yang, C. Wrigley and B. Hancock, "An enhanced-performance CMOS imager with a flushed-reset photodiode pixel," *IEEE Transactions on Electron Devices,* vol. 50, no. 1, pp. 48-56, January 2003.

[23] H. Tian, B. Fowler and A. E. Gamal, "Analysis of temporal noise in CMOS Photodiode Active Pixel Sensor," *IEEE Journal of Solid-State Circuits,* vol. 36, no. 1, pp. 92-101, January 2001.

[24] B. Van Zeghbroeck, "Principles of Electronic Devices," 2011. [Online]. Available: http://ecee.colorado.edu/~bart/book/book/chapter7/ch7_3.htm. [Accessed 2013].

[25] X. Wang, P. R. Rao and A. J. Theuwissen, "Fixed-Pattern Noise Induced by Transmission

Gate in Pinned 4T CMOS Image Sensor Pixels," in *Proceeding of the 36th European*, 2006.

[26] A. E. Gamal and H. Eltoukhy, "CMOS Image Sensors," *Circuits and Devices Magazine, IEEE,* vol. 21, no. 3, pp. 6-20, May/June 2005.

[27] H. Foll, "Shockley-Read-Hall Recombination," University of Kiel Engineering, [Online]. Available: http://www.tf.uni-kiel.de/matwis/amat/semi_en/kap_2/backbone/r2_3_3.html. [Accessed 7 August 2013].

[28] B. G. Streetman and S. K. Banerjee, Solid State Electronics, 6 ed., New Belhi: Prentice-Hall Inc., 2009.

[29] S. K. Mendis, S. E. Kemeny and E. R. Fossum, "A 128 x 128 CMOS Active Pixel Image Sensor for Highly Integrated Imaging Systems," in *International Electron Devices Meeting*, Washington DC, 1993.

[30] S. U. Ay, "Electrical Property Modelling of Photodiode Type CMOS Active Pixel Sensor (APS)," *Circuits and Systems, 48th Midwest Symposium on,* vol. 1, pp. 371-375, 7-10 Aug 2005.

[31] Keithley Instruments Inc., "Four-point resistivity and Hall voltage measurements with the Model 4200-SCS," Cleavland, 2011.

[32] H. Diesinger, A. Bsiesy and R. Herino, "In situ measurement of the optical absorption coefficient of porous silicon," *Journal of Applied Physics,* vol. 89, no. 1, pp. 221-225, January 2001.

[33] S. Sze, Physics of Semiconductor Devices, vol. New York, John Wiley and Sons, Inc, 1969.

[34] OSI OptoElectronics, "OSI OptoElectronics," [Online]. Available: http://www.osioptoelectronics.com/application-notes/AN-Photodiode-Parameters-Characteristics.pdf. [Accessed January 2014].

Appendix A Semiconductor Physics Highlights

A.1 PN Junctions

A.1.1 Built in Potential

A pn junction is formed by interfacing n-type and p-type semiconductor regions. The junction is typically formed by diffusing or implanting a p-type substrate with an n-type dopant or vice versa. Because a concentration gradient of the dopants is present at the metallurgical junction, electrons and holes will diffuse into the p-type and n-type regions respectively. As the charge carriers diffuse across the junction, an electric field gradient develops. The electric field, also known as the built in potential, is in the direction of the p-type to the n-type and its magnitude is given by

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) \qquad \text{A.1}$$

In Equation A.1, $\frac{kT}{q}$ is the thermal voltage, N_A and N_D are the acceptor and donor dopant concentrations, and n_i is the intrinsic carrier concentration of the semiconductor. The built in potential typically ranges from 0.6 to 0.8V.

A.1.2 Junction Width

The built in potential sweeps free carriers from a region of size proportional to the square root of the magnitude of the built in potential at no applied bias. This region is called the space-charge or depletion region and the width of this region is given by

$$W = \left[\frac{2\varepsilon_r \varepsilon_0}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)(V_{bi} - V)\right]^{\frac{1}{2}} \qquad \text{A.2}$$

In Equation A.2, ε_r is the relative permittivity of the semiconductor, and ε_0 is the permittivity of free space. As shown in Equation A.2, the width of the depletion region is dependent on the externally applied voltage. Under reverse bias the depletion region becomes larger and the converse is true for forward bias. This phenomenon forms the basis of operation for the diode. Equation A.2 predicts the width of the space charge region for a pn-step junction. The GVSU fabrication process utilizes a diffusion process to create the junction; however, Equation A.2 gives a good approximation for the size of the space-charge region. The size of the depletion region in the PD of an imager pixel directly affects the amount of light converted into image data. Because the electric potential across the depletion region sweeps free charge carriers from the depletion regions a wider depletion region will result a more captured electrons as the result of incoming photons.

Similar to the depletion region the size of the diffusion length affects the number of captured charge carriers as a result of photo-generated charge. The diffusion length is the distances that generated charge carriers, also called electron-hole pairs (EHPs) can travel prior to the recombination of electrons and holes. The diffusion length can be determined as

$$L_{n,p} = \sqrt{D_{n,p}\tau_{n,p}} \qquad \text{A.3}$$

In Equation A.3, $D_{n,p}$ is the diffusion constant for electrons and holes respectively, and $\tau_{n,p}$ is the carrier lifetime which will be discussed more in the following sections. If a charge carrier is generated within one diffusion length of the space-charge region, the generated charge carriers can diffuse to the space-charge region where they are swept by the electric potential across the junction; thus, contributing to the magnitude of accumulated charge.

A.1.3 Junction Capacitance

The amount of charge that can be integrated on the PD is a function of the junction capacitance characteristic of the pn-junction. The depletion region formed at the pn-junction acts as a dielectric layer for a parallel plate capacitor. Integrated charge as the result of converted photon energy accumulates on the PD capacitance and forms the mechanism for determining incoming light intensity. The size of the capacitor determines the upper limit to the amount of irradiation converted to image data; therefore, accurate characterization of the PD capacitance is a necessity in the fabrication of a CMOS imager pixel. The junction capacitance of a pn-junction can be estimated as

$$C_j = \frac{\varepsilon A}{W} \qquad \text{A.4}$$

It is important to note the dependence of the width of the space-charge region, and hence the junction capacitance, on the voltage across the space-charge region. The implication is that the junction capacitance will decrease with decreasing reverse bias (Figure A.1). Regarding this effect in the operation of a CMOS pixel, the PD capacitance sets the fundamental limit on the conversion gain of the 3T pixel [26]. Higher capacitance implies lower conversion gain, less variation in integrated voltage, and lower imager quality in dark environments.

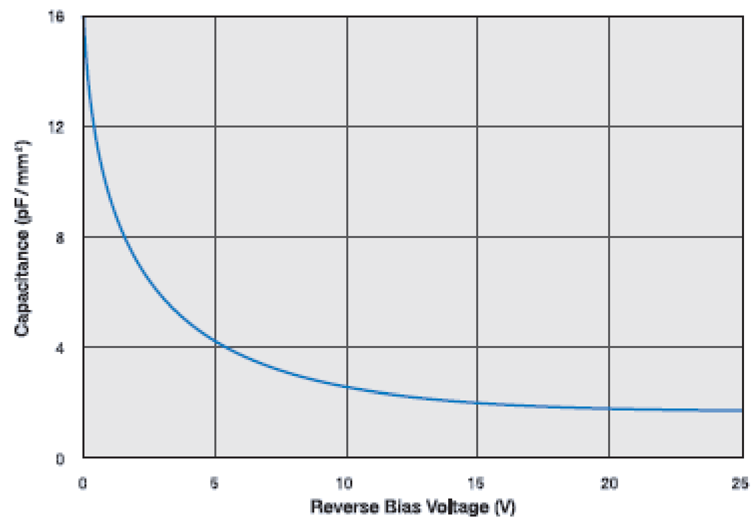


Figure A.1 - PD Capacitance with respect to reverse bias voltage **[34]**.

A.1.4 Diode Current

When reversed biased, the current in the PD is the combination of the thermally and optically generated currents. When the PD is used as an optical sensor, the thermal current is also known as the dark current. Because the thermal current will continue to flow in the absence of light it leads to misrepresentation in the integrated pixel voltage. The diode can be calculated as shown in Equation A.5 where p_n and n_p are the minority carrier concentrations for non-equilibrium conditions given by

$$I_D = qA\left(\frac{L_p}{\tau_p}p_n + \frac{L_n}{\tau_n}n_p\right)\left(e^{\frac{qV}{KT}} - 1\right) \quad \text{A.5}$$

$$p_n = p_{n0}e^{\frac{eV_a}{kT}} \quad \text{A.6}$$

$$n_p = n_{p0}e^{\frac{eV_a}{kT}} \quad \text{A.7}$$

Equation A.5 is the Shockley ideal diode equation. This equation neglects the generation of charge carriers in the space-charge width assuming the concentration will be small. However, in this research, an accurate representation of non-ideal current estimation is desired so the thermal generation in the space-charge region is of interest. According to Weckler, the thermal current component of the space charge region can be estimated according to the following [18]:

$$I_{D,SC} = \frac{Aqn_i}{2\tau_0}W \quad \text{A.8}$$

The intrinsic carrier concentration is given by

$$n_i = \sqrt{N_C N_V}e^{\frac{E_g}{2kT}} \quad \text{A.9}$$

In Equation A.9, N_C and N_V are the effective density of states in the conduction and valence bands and τ_0 is the effective carrier lifetime in the space charge region. Weckler suggests a value of 7.2µs for τ_0 based on experimental observation [18]. Substituting Equations A.8 and A.9 into equation A.5 yields an estimated diode current of

$$I_D = qA\left(\left(\frac{L_p}{\tau_p}p_n + \frac{L_n}{\tau_n}n_p\right)\left(e^{\frac{qV}{KT}} - 1\right) + \frac{n_i}{2\tau_0}W\right) \qquad \text{A.10}$$

The current contribution of the space charge region is not multiplied by the exponential factor due to the built in dependence of the space charge width on the junction bias.

A.2 Optoelectronics

The operation of an imager PD is based on the photovoltaic effect. A photon has energy proportional to its frequency given by

$$E = h\nu \qquad \text{A.11}$$

In Equation A.11, h is Plank's constant and ν is the frequency of the photon.Upon collision with the semiconductor, the photon is capable of exciting an electron in the valence band to the conduction band if the photon energy is greater than the work function of silicon; thus generating an EHP. The carrier lifetime, also known as the recombination lifetime, characterizes the amount of time the average free carrier can exist in the semiconductor before recombining with an opposite charge carrier. When an EHP is generated in the space-charge region or within one diffusion length of the space-charge region, the charge carriers are swept from the junction, where the generated charge is stored on the junction capacitance. Ideally, all photo-generated EHP's are generated within the depletion region or one diffusion length from the depletion

region. Any photo-generated charge generated outside of these regions does not contribute to the photo-current.

A.2.1 Absorption Coefficient and Penetration Depth

For application in CMOS imagers, PDs should be optimized to collect and convert as many photons as possible within the visible light spectrum. This requires the junction depth of the PD to be positioned such that the majority of photo-generated carriers are generated within the depletion region. Visible light ranges from roughly 400 to 800 nm with absorption coefficients (α) as shown in Figure A.2. The absorption coefficient of a material corresponds to the inverse of the average penetration depth of a photon before being absorbed as a function of wavelength. The shallow penetration depth of short wavelength photons often leads to optically generated carriers outside the space-charge region; so, in order to ensure adequate blue response, the space-charge region should be located within 0.5μm from the silicon surface.

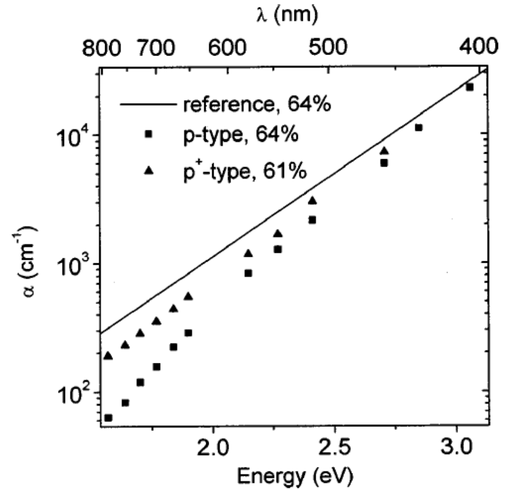


Figure A.2 - Absorption coefficient of various wavelengths in Silicon **[32]**.

A.2.2 Optical Generation Rate

The optical generation rate is a measure of the average number of optically generated charge carriers per unit area. The optical generation rate of a pn-junction PD can be estimated as

$$g_{op} = \frac{P'\lambda}{hc}\alpha e^{-\alpha z} \qquad \text{A.12}$$

In Equation A.12, P is the optical power impinging on the junction, λ is the optical wavelength, and z is the penetration depth [20]. Integration of the optical generation rate with respect to

wavelength and depth for a given power will yield the total number of optically generated carriers in the PD.

A.2.3 Photo-generated Current

The optically generated current component of the PD current is given by

$$I_{op} = qAg_{op}\left(L_p + L_n + W\right) \tag{A.13}$$

In Equation A.13, g_{op} is the concentration of optically generated charge carriers. The sum of the thermal and optical components yields the total expected current from the reversed bias PD which is given by

$$I_{PD} = qA\left(\left(\frac{L_p}{\tau_p}p_n + \frac{L_n}{\tau_n}n_p\right)\left(e^{\frac{qV}{KT}} - 1\right) + \frac{n_i}{2\tau_0}W\right) - qAg_{op}\left(L_p + L_n + W\right) \tag{A.14}$$

Equation A.14 shows that a smaller reverse bias will decrease the dark current, but also the number of optically generated carriers that contribute to the optical current. Thus, it is not sufficient to simply reduce operating voltage in the CMOS imager to reduce dark current. According to Wang, the minority carrier concentrations are often set based on doping parameters designed to give the device proper conductivity characteristics, so the carrier lifetime is often the parameter of interest regarding the reduction of dark current [20].

A.3 MOSFET Parameter Estimation

A.3.1 Threshold Estimation

According to Streetman *et al* the threshold voltage of a MOSFET can be calculated according to

$$V_T = \phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_d}{C_i} + 2\phi_F \tag{A.15}$$

In Equation A.15, $\phi_{ms}$is the variation in the metal-semiconductor work function which is dependent upon doping, $Q_i$is the effective interface charge, Q_d is the effective depletion charge, $C_i$is the interface capacitance, and ϕ_F is the potential difference between the Fermi level and the intrinsic bulk. Streetman suggests a typical interface charge in the range of $4\text{x}10^{10}$qC/cm^2; however, the oxidation and diffusion processes in the GVSU cleanroom will likely introduce a higher concentration of defects. For this reason, $3.5\text{x}10^{12}$ was used as the effective interface charge for the purposes of calculating the threshold voltage. The interface capacitance given by

$$C_i = \frac{\epsilon_i}{d} \tag{A.16}$$

In Equation A.16, ϵ_i is the permittivity of the the interface layer and d is the thickness of the interface. The capacitance is given in terms of F/cm^2. Using a value of 3.9 as the relative permittivity of silicon and a target oxide thickness of 100nm, the interface capacitance was predicted to be 34.5pF. The work function difference for an n-type transistor is given by

$$\phi_F = \frac{kT}{q} \ln \frac{N_a}{n_i} \tag{A.17}$$

Equation A.17 is based on the ratio of the concentrations of acceptors in the bulk to the intrinsic carrier concentration of silicon. Based on a 0.01Ωcm resistivity and a typical hole mobility of 480cm^2/(Vs), the work function difference was 0.473eV. The effective depletion charge is the product of the electron charge, bulk doping, and maximum width of the depletion region give by

$$Q_d = -qN_A W_m \tag{A.18}$$

The maximum width of the depletion region is calculated as

$$W_m = 2\left[\frac{\varepsilon_s \phi_F}{qN_a}\right]^{\frac{1}{2}} \quad \text{A.19}$$

Based on the previous calculations, the maximum width of the depletion region is estimated to be 3.08µm. This yields a depletion charge of -6.42x10^{-7}C/cm^2. Based on these parameter estimates the threshold voltage of the fabrication MOSFETs is estimated to be in the range of 2.32V.

A.3.2 Body biasing

Because the transistors in the GVSU cleanroom often exhibit depletion mode operation, the body-biasing effect can be used to drive the threshold voltage into the positive regime. The body-biasing effect is achieved by introducing a reverse bias between the bulk substrate and the doped source of the MOSFET. The reverse bias increases the charge required at the gate to drive the MOSFET channel into inversion. The magnitude of the threshold shift is determined according to the following [28]:

$$\Delta V_T = \frac{\sqrt{2\epsilon_s q N_a}}{C_i}\left[(2\phi_F - V_B)^{\frac{1}{2}} - (2\phi_F)^{\frac{1}{2}}\right] \quad \text{A.20}$$

Based on the parameters calculated in the threshold estimation, the threshold changes associated with various biases are presented in Table A.1. Thus, using the body bias effect, MOSFETs exhibiting negative threshold can be fashioned to act as enhancement mode FETs.

Table A.1 - Predicted threshold shift with respect to applied source to bulk bias.

Applied Bias	**-0.1**	**-0.2**	**-0.3**	**-0.4**	**-0.5**	**-0.6**	**-0.7**	**-0.8**	**-0.9**	**-1**
ΔV_T (V)	0.550	1.075	1.577	2.060	2.525	2.974	3.409	3.830	4.240	4.639

Appendix B Schematics and Board Layouts

B.1 VSAC

Figure B.1 - VSAC schematic layout.

Figure B.2 - VSAC embedded board layout.

B.2 IC Interface Schematic

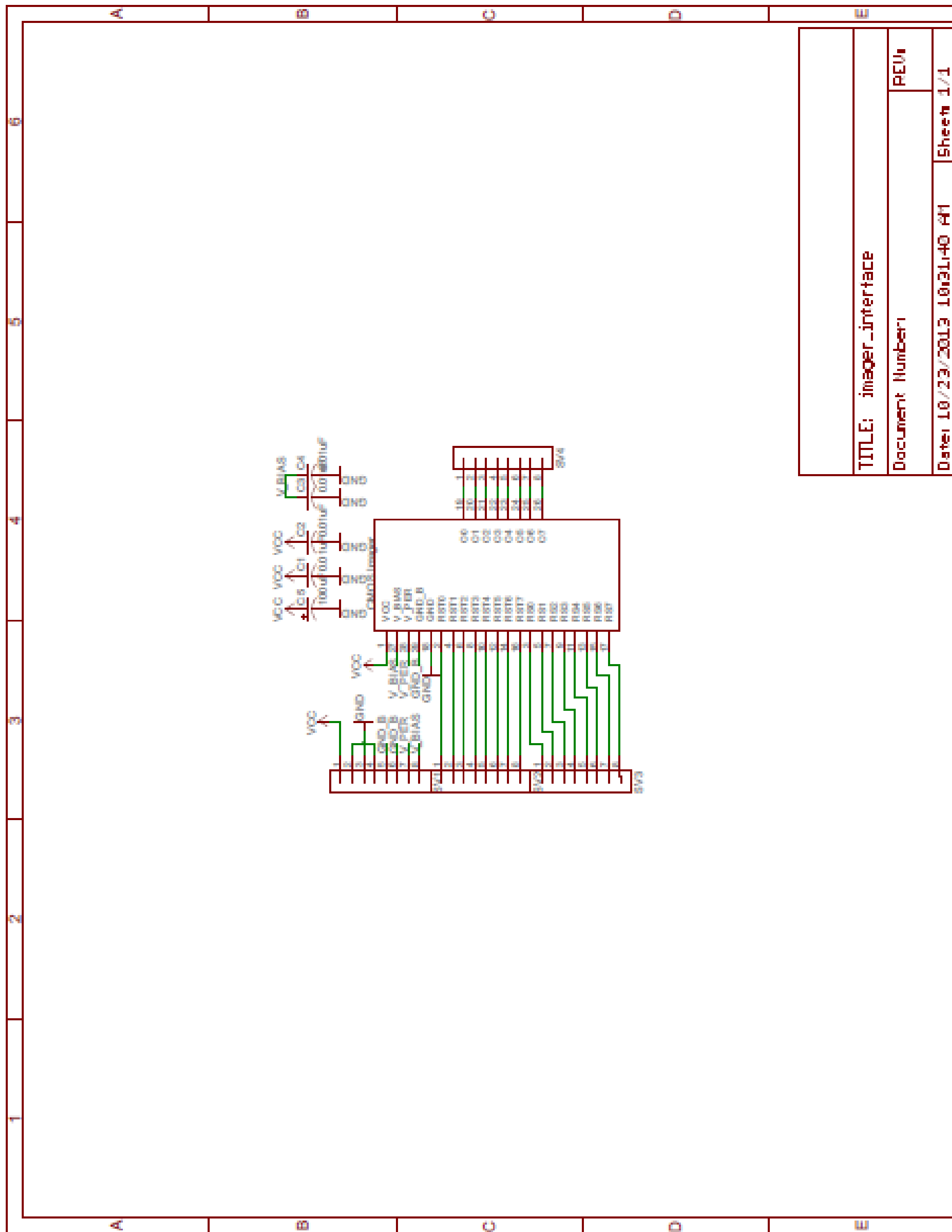


Figure B.3 - IC interface schematic layout.

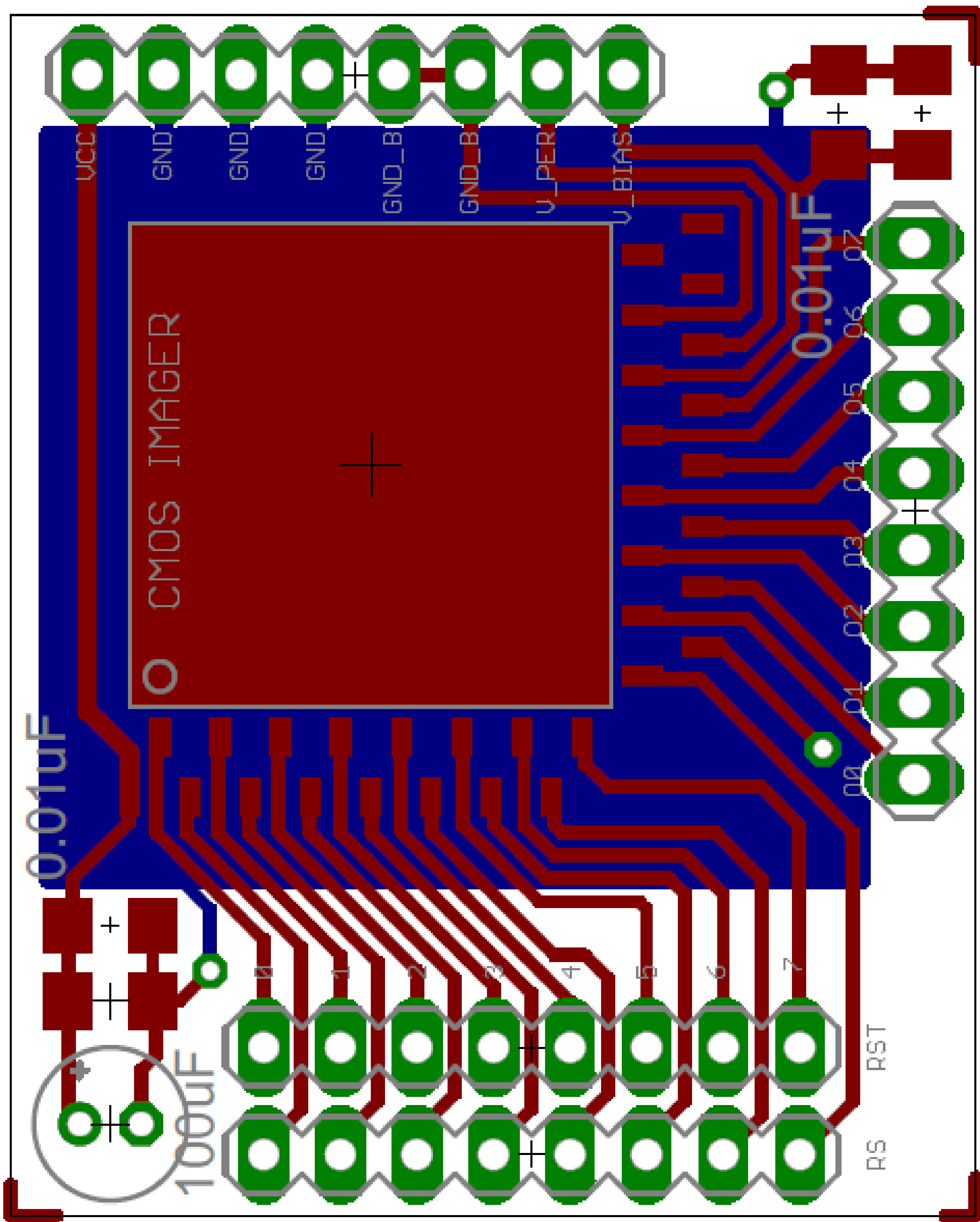


Figure B.4 - IC interface board layout.

Appendix C Code

C.1 main.c

```
#include <stdint.h>

#include "inc/hw_ints.h"
#include "inc/hw_memmap.h"
#include "inc/hw_types.h"
#include "inc/lm3s6965.h"
#include "driverlib/debug.h"
#include "driverlib/gpio.h"
#include "driverlib/interrupt.h"
#include "driverlib/sysctl.h"
#include "driverlib/systick.h"
#include "driverlib/uart.h"
#include "driverlib/adc.h"
#include "drivers/rit128x96x4.h"

#include "pin_functions.h"
#include "common_variables.h"
#include "custom_functions.h"

//*****************************************************************************
//
// The error routine that is called if the driver library encounters an error.
//
//*****************************************************************************
#ifdef DEBUG
void
__error__(char *pcFilename, unsigned long ulLine)
{
}
#endif

//
// External variable declarations
// ADCIntHandler
//
extern unsigned long g_ulAverage;
extern volatile unsigned long g_sampleCount;
extern volatile unsigned long g_adcRead[64];
//
// SystickIntHandler
//
extern volatile int gSysTickDelayBlock;
```

```
int main(void){
   //
   // Set the clocking to run directly from the crystal.
   //
   SysCtlClockSet(SYSCTL_SYSDIV_1 | SYSCTL_USE_OSC | SYSCTL_OSC_MAIN |
                SYSCTL_XTAL_8MHZ);

   //
   // Initialize the OLED display and write status.
   //
   RIT128x96x4Init(1000000);

   // Pushbuttons
   SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOE);
   GPIOPinTypeGPIOInput(GPIO_PORTE_BASE,0x000F);

   //
   // Configure pushbuttons to have pull up resistor.
   // 2MA strength does nothing with input configuration.
   //
   GPIOPadConfigSet(GPIO_PORTE_BASE, 0x000F, GPIO_STRENGTH_2MA,
GPIO_PIN_TYPE_STD_WPU);


   //
   // Enable UART Pins
   //
   SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOA);
   SysCtlPeripheralEnable(SYSCTL_PERIPH_UART0);

   //
   // Set GPIO A0 and A1 as UART pins.
   //
   GPIOPinTypeUART(GPIO_PORTA_BASE, GPIO_PIN_0 | GPIO_PIN_1);

   //
   // Configure the UART for 115,200, 8-N-1 operation.
   //
   UARTConfigSetExpClk(UART0_BASE, SysCtlClockGet(), 115200,
                  (UART_CONFIG_WLEN_8 | UART_CONFIG_STOP_ONE |
                   UART_CONFIG_PAR_NONE));

   //
   // Initialize ADC Operation
   //
   SysCtlPeripheralEnable(SYSCTL_PERIPH_ADC0);
```

```
    //
    // Initialize the ADC to oversample channel 1 by 8x using sequencer 0.
    // Sequencer will be triggered by processor interrupts.
    //
    ADCSequenceConfigure(ADC_BASE, ADC_SEQUENCE, ADC_TRIGGER_PROCESSOR,
0);
    ADCHardwareOversampleConfigure(ADC_BASE,8);
    ADCSequenceStepConfigure(ADC_BASE, ADC_SEQUENCE, 0,(ADC_CTL_CH1 \
    | ADC_CTL_IE | ADC_CTL_END));

    //
    // Enable ADC sequencer and its interrupt (in both the ADC and NVIC)
    //
    ADCSequenceEnable(ADC_BASE, ADC_SEQUENCE);
    ADCIntEnable(ADC_BASE, ADC_SEQUENCE);
    IntEnable(INT_ADC1);

    //
    // Enable processor interrupts.
    //
    IntMasterEnable();

    //
    // Configure Peripherals
    //
    ConfigureSampleHold();
    ConfigureMUX();
    ConfigureCounter();
    ConfigureRSTShift();
    ConfigureRSShift();

    ClearRSTShift();
    ClearRSShift();
    HoldOutput();
    DisableMUX();
    DisableRSTShift();
    DisableRSShift();

    int once = 0;
    gSysTickDelayBlock = 0;

    RIT128x96x4StringDraw("Press Button",        20,  60, 15);

    while(1){
      //Monitors input buttons - Active low
```

```
    while(!GPIOPinRead(GPIO_PORTE_BASE, BUTTON_UP) ||
!GPIOPinRead(GPIO_PORTE_BASE, BUTTON_DOWN)
    || !GPIOPinRead(GPIO_PORTE_BASE, BUTTON_LEFT) ||
!GPIOPinRead(GPIO_PORTE_BASE, BUTTON_RIGHT)){

        if(!once){

            LoadRSShift();
            LoadRSTShift();

            int row;
            for (row=0;row<8;row++){
                DisableMUX();

                //
                // Wait for reset period
                // 1ms = 8000
                ChangeSysTickPeriod(20000);
                SysTickIntEnable();
                //Block program for reset delay
                while(gSysTickDelayBlock==0);
                gSysTickDelayBlock = 0;

                //
                // Integration
                // Incrementing RST shift will reset currentNode+1 and float the current PD row
                //
                IncrementRSTShift();

                //
                // Wait for integration period
                // 40us = 320
                ChangeSysTickPeriod(50);
                SysTickIntEnable();
                while(gSysTickDelayBlock == 0);
                gSysTickDelayBlock = 0;

                EnableRSShift();
                ChangeSysTickPeriod(120);
                SysTickIntEnable();
                while(gSysTickDelayBlock == 0);
                gSysTickDelayBlock = 0;
                DisableRSShift();
                IncrementRSShift();

                SampleOutput();
```

```
            //
            // Wait for sampling
            //
            ChangeSysTickPeriod(120);
            SysTickIntEnable();
            while(gSysTickDelayBlock == 0);
            gSysTickDelayBlock = 0;
            HoldOutput();

            CountReset();
            EnableMUX();
            int col;
            for(col=0;col<8;col++){
              ADCProcessorTrigger(ADC_BASE, ADC_SEQUENCE);
              CountIncrement();
            }
            DisableMUX();


          }
          UARTSend((unsigned char *)g_adcRead,256);
          IntMasterDisable();

          RIT128x96x4StringDraw("Data Sent",          20,  60, 15);

          once = 1;
        }
      }
      once = 0;
    }
}
```

C.2 common_variables.h

```
#ifndef __COMMON_VARIABLES_H__

#define __COMMON_VARIABLES_H__

#define ADC_SEQUENCE 1

#define ACTIVE_NODE 0

//-------------------------------------------------
// Up = PE0/PWM4
```

```
// Down = PE1/PWM5
// Left = PE2/PhB1
// Right = PE3/PhA1
//--------------------------------------------------
#define BUTTON_UP 0x0001
#define BUTTON_DOWN 0x0002
#define BUTTON_LEFT 0x0004
#define BUTTON_RIGHT 0x0008

//
//ADCIntHandler
//
unsigned long g_ulAverage;
volatile unsigned long g_sampleCount;
volatile unsigned long g_adcRead[64];

//
//SystickIntHandler
//
//int gSampleTime;
volatile int gSysTickDelayBlock;

#endif
```

C.3 custom_functions.c

```
#include "inc/hw_ints.h"

#include "inc/hw_memmap.h"
#include "inc/hw_types.h"
#include "inc/hw_nvic.h"
#include "driverlib/debug.h"
#include "driverlib/gpio.h"
#include "driverlib/interrupt.h"
#include "driverlib/timer.h"
#include "driverlib/sysctl.h"
#include "driverlib/systick.h"
#include "driverlib/adc.h"
#include "driverlib/uart.h"
#include "drivers/rit128x96x4.h"

#include "common_variables.h"

//****************************************************************************
*
//
// Send a string to the UART.
```

```
//
//***************************************************************************
*
void UARTSend(const unsigned char *pucBuffer, unsigned long ulCount){
   //
   // Loop while there are more characters to send.
   //
   while(ulCount--)
   {
      //
      // Write the next character to the UART.
      //
      UARTCharPut(UART0_BASE, *pucBuffer++);
   }
}

//
// Set SysTickPeriod effective immediately
// SysTickPeriodSet updates period after next interrupt.
// ulPeriod max value = 16777216
//
void ChangeSysTickPeriod(unsigned long ulPeriod){
   //Disable Systick so no interrupts occur during period reset
   SysTickDisable();
   //Set new period - 8MHz clock reference
   SysTickPeriodSet(ulPeriod);
   //Any write to the NVIC_ST_CURRENT register resets period to new value
   HWREG(NVIC_ST_CURRENT) &= 0x00000000;
   //Reenable to start new period.
   SysTickEnable();
}

//***************************************************************************
*
//
// Sample ADC and store result in g_ulAverage buffer.
//
//***************************************************************************
*
extern unsigned long g_ulAverage;
extern volatile unsigned long g_sampleCount;
extern volatile unsigned long g_adcRead[64];

//
// Analog Digital Conversion Interrupt Handler
//
```

```
void
ADCIntHandler(void)
{
   //
   // Clear the ADC interrupt
   //
   ADCIntClear(ADC_BASE, ADC_SEQUENCE);

   //
   // Get averaged data from the ADC
   //
   ADCSequenceDataGet(ADC_BASE, ADC_SEQUENCE, &g_ulAverage);

   g_adcRead[g_sampleCount]=g_ulAverage;
   g_sampleCount++;
}

//
// Systick Interrupt Handler
//
//int gSampleTime=0;
extern volatile int gSysTickDelayBlock;
void
SysTickIntHandler(void)
{
   SysTickIntDisable();
   gSysTickDelayBlock = 1;
   //gSampleTime = 1;
   //RIT128x96x4StringDraw("Systick Int Handle",          20,  60, 15);
}
```

C.4 pin_functions.c

```
#include "inc/hw_ints.h"

#include "inc/hw_memmap.h"
#include "inc/hw_types.h"
#include "driverlib/debug.h"
#include "driverlib/gpio.h"
#include "driverlib/sysctl.h"
#include "drivers/rit128x96x4.h"
#include "inc/hw_nvic.h"
#include "driverlib/gpio.h"
#include "driverlib/sysctl.h"

//------------------------------------------------------------
//------------------------------------------------------------
```

```
//
// RESET pins
// DS - A2
// CLK - A3
// CLR - A4 - active low
// OE - A5 - active low
//
//--------------------------------------------------------
//--------------------------------------------------------
void ConfigureRSTShift(void){

   SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOA);
   SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOD);
   SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOG);
   GPIOPinTypeGPIOOutput(GPIO_PORTA_BASE,0x0080);
   GPIOPinTypeGPIOOutput(GPIO_PORTD_BASE,0x0050);
   GPIOPinTypeGPIOOutput(GPIO_PORTG_BASE,0x0002);
   GPIOPadConfigSet(GPIO_PORTA_BASE, 0x0080, GPIO_STRENGTH_8MA,
GPIO_PIN_TYPE_STD);
   GPIOPadConfigSet(GPIO_PORTD_BASE, 0x0050, GPIO_STRENGTH_8MA,
GPIO_PIN_TYPE_STD);
   GPIOPadConfigSet(GPIO_PORTG_BASE, 0x0002, GPIO_STRENGTH_8MA,
GPIO_PIN_TYPE_STD);
}

void EnableRSTShift(void){
   //
   // Enable output
   //
   GPIOPinWrite(GPIO_PORTD_BASE, 0x0040, 0x0000);
}


//
// Disabling sets all RST_X pins to Vrst due to pull up resistors
// at drain of inverting MOSFETS.
//
void DisableRSTShift(void){
   //
   // Disable output
   //
   GPIOPinWrite(GPIO_PORTD_BASE, 0x0040, 0x0040);
}

void IncrementRSTShift(void){
```

```
    // Pulse clock
    GPIOPinWrite(GPIO_PORTG_BASE, 0x0002, 0x0002);
    GPIOPinWrite(GPIO_PORTG_BASE, 0x0002, 0x0000);

}

void ClearRSTShift(void){

    DisableRSTShift();

    //
    //Pulse CLR
    //
    GPIOPinWrite(GPIO_PORTD_BASE, 0x0010, 0x0000);
    GPIOPinWrite(GPIO_PORTD_BASE, 0x0010, 0x0010);

    //
    // RST GATE TX Drivers act as inverters so to have RST
    // transistors on Imager to be "OFF" we need to fill shift
    // register with 1's.
    //
    GPIOPinWrite(GPIO_PORTA_BASE, 0x0080, 0x0080);

    int i = 0;
    for(i=0; i<9; i++){

        IncrementRSTShift();
    }
}

void LoadRSTShift(void){
    //
    // Disable output
    //
    DisableRSTShift();

    //
    // Set DS to low
    //
    GPIOPinWrite(GPIO_PORTA_BASE, 0x0080, 0x0000);

    //
    // Pulse clock twice to get DS to out
    //
    IncrementRSTShift();
```

```
    //
    // Set DS to high
    //
    GPIOPinWrite(GPIO_PORTA_BASE, 0x0080, 0x0080);

    IncrementRSTShift();

    EnableRSTShift();
}

void ResetPDNode(int node){
    //
    // Disable output
    //
    DisableRSTShift();

    //
    // Set DS to low
    //
    GPIOPinWrite(GPIO_PORTA_BASE, 0x0080, 0x0000);

    //
    // Pulse clock twice to get DS to output 0
    //
    IncrementRSTShift();

    //
    // Set DS to high
    //
    GPIOPinWrite(GPIO_PORTA_BASE, 0x0080, 0x0080);

    int i;
    for(i=0;i<node;i++)
        IncrementRSTShift();

    EnableRSTShift();
}

//
// Disabling RSTShift sets 0's on RSTShift output so RST Tx is constantly at 3.3V
// To float RST Tx source during integration period it is necessary to set a 1 at the RSTShift
Output
//
void FloatPDNode(int node){
    //
    // Disable output
```

```
    //
    DisableRSTShift();

    //
    // Set DS to high
    //
    GPIOPinWrite(GPIO_PORTA_BASE, 0x0080, 0x0080);

    //
    // Pulse clock twice to get DS to out
    //
    IncrementRSTShift();

    int i;
    for(i=0;i<node;i++)
        IncrementRSTShift();

    //
    // Set DS to low
    //
    GPIOPinWrite(GPIO_PORTA_BASE, 0x0080, 0x0000);

    EnableRSTShift();
}

//---------------------------------------------------------
//---------------------------------------------------------
//
// Row Select pins
// DS - C4
// CLK - C5
// CLR - D2 - active low
// OE - D3 - active low
//
//---------------------------------------------------------
//---------------------------------------------------------
void ConfigureRSShift(void){

    SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOC);
    SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOD);
    GPIOPinTypeGPIOOutput(GPIO_PORTC_BASE,0x0030);
    GPIOPinTypeGPIOOutput(GPIO_PORTD_BASE,0x000C);
    GPIOPadConfigSet(GPIO_PORTC_BASE, 0x0030, GPIO_STRENGTH_8MA,
GPIO_PIN_TYPE_STD);
    GPIOPadConfigSet(GPIO_PORTD_BASE, 0x000C, GPIO_STRENGTH_8MA,
GPIO_PIN_TYPE_STD);
```

```
}

void EnableRSShift(void){
   //
   // Enable output
   //
   GPIOPinWrite(GPIO_PORTD_BASE, 0x0008, 0x0000);
}

void DisableRSShift(void){
   //
   // Disable output
   //
   GPIOPinWrite(GPIO_PORTD_BASE, 0x0008, 0x0008);
}

void IncrementRSShift(void){

   // Pulse clock
   GPIOPinWrite(GPIO_PORTC_BASE, 0x0020, 0x0020);
   GPIOPinWrite(GPIO_PORTC_BASE, 0x0020, 0x0000);
}

void ClearRSShift(void){

   DisableRSShift();

   //
   // Pulse CLR
   //
   GPIOPinWrite(GPIO_PORTD_BASE, 0x0004, 0x0000);
   GPIOPinWrite(GPIO_PORTD_BASE, 0x0004, 0x0004);

}

void LoadRSShift(void) {


   //DisableRSShift();
   ClearRSShift();

   //
   // Set DS to high
   //
   GPIOPinWrite(GPIO_PORTC_BASE, 0x0010, 0x0010);
```

```
    //
    // Pulse clock to get DS to out 1
    //
    IncrementRSShift();

    //
    // Set DS to low
    //
    GPIOPinWrite(GPIO_PORTC_BASE, 0x0010, 0x0000);

    IncrementRSShift();

    //EnableRSShift();
}

void SetRSNode(int node){
    //
    // Disable output
    //
    DisableRSShift();

    //
    // Set DS to high
    //
    GPIOPinWrite(GPIO_PORTC_BASE, 0x0010, 0x0010);

    //
    // Pulse clock twice to get DS to out
    //
    IncrementRSShift();

    //
    // Set DS to low
    //
    GPIOPinWrite(GPIO_PORTC_BASE, 0x0010, 0x0000);

    int i;
    for(i=0;i<node;i++)
        IncrementRSShift();

    EnableRSShift();
}

//----------------------------------------------------------
//----------------------------------------------------------
//
```

```
// Counter pins
// CLK - B2
// CLR - B6 - active low
//
//---------------------------------------------------------
//---------------------------------------------------------

void ConfigureCounter(void){
   SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOB);
   GPIOPinTypeGPIOOutput(GPIO_PORTB_BASE,0x0044);
   GPIOPadConfigSet(GPIO_PORTB_BASE, 0x0044, GPIO_STRENGTH_8MA,
GPIO_PIN_TYPE_STD);
}

void CountIncrement(void){
   //
   // Pulse CLK
   //
   GPIOPinWrite(GPIO_PORTB_BASE, 0x0004, 0x0004);
   GPIOPinWrite(GPIO_PORTB_BASE, 0X0004, 0X0000);

}

void CountReset(void){
   //
   // Pulse CLR
   //
   GPIOPinWrite(GPIO_PORTB_BASE, 0x0040, 0x0000);

   //
   // Clear operation is synchronous so pulse clock for reset.
   //
   CountIncrement();

   GPIOPinWrite(GPIO_PORTB_BASE, 0X0040, 0X0040);
}



//---------------------------------------------------------
//---------------------------------------------------------
//
// MUX pins
// EN - B3 - Active low
// Output - C0
//
```

```
//----------------------------------------------------------
//----------------------------------------------------------
void ConfigureMUX(void){
   SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOB);
   GPIOPinTypeGPIOOutput(GPIO_PORTB_BASE,0x0008);
   GPIOPadConfigSet(GPIO_PORTB_BASE, 0x0008, GPIO_STRENGTH_8MA,
GPIO_PIN_TYPE_STD);
}

void EnableMUX(void){
   //
   // Set EN pin low
   //
   GPIOPinWrite(GPIO_PORTB_BASE, 0X0008, 0X0000);
}

void DisableMUX(void){
   //
   // Set EN pin high
   //
   GPIOPinWrite(GPIO_PORTB_BASE, 0X0008, 0X0008);

}

//----------------------------------------------------------
//----------------------------------------------------------
//
// Sample and Hold - B0
// Sample - high
// Hold - Low
//
//----------------------------------------------------------
//----------------------------------------------------------
void ConfigureSampleHold(void){
   SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOB);
   GPIOPinTypeGPIOOutput(GPIO_PORTB_BASE,0x0001);
   GPIOPadConfigSet(GPIO_PORTB_BASE, 0x0001, GPIO_STRENGTH_8MA,
GPIO_PIN_TYPE_STD);
}

void SampleOutput(void){
   //
   // Set B0 high
   //
   GPIOPinWrite(GPIO_PORTB_BASE, 0X0001, 0X0001);
```

```
}

void HoldOutput(void){
   //
   // Set B0 low
   //
   GPIOPinWrite(GPIO_PORTB_BASE, 0X0001, 0X0000);
}
```