Low-Noise Sigma-Delta Capacitance-to-Digital Converter for Sub-pF Capacitive Sensors with Integrated Dielectric Loss Measurement

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Abstract

A sigma-delta capacitance-to-digital converter (CDC) with a resolution down to 19.3 aF at a bandwidth of 10 kHz, corresponding to a noise level of 0.2 aF/$\sqrt{Hz}$, is presented. An integrated dielectric loss measurement circuit by means of two parallel channels with different integration times offers a complex permittivity measurement in a single-chip solution. The achieved dielectric loss angle resolution is as low as 0.3 $^\circ$ for a material density ratio of 0.55 %. A test chip with two converter blocks including two 2nd order and two 4th order modulators has been produced in the austriamicrosystems AG C35B3C0 0.35 μm DPTM CMOS process, operating at a single 3.3 V supply. Applications of this circuit include mass measurement and analysis of material compositions.

1. Introduction

CDCs are analog-to-digital converters (ADCs) with a sensor capacitance as the measuring variable of the converter. The sigma-delta CDC described in this paper is dedicated for measuring a relative capacitance, therefore using a fixed reference capacitor and a variable sensor capacitor. The sensor and the reference capacitances can be implemented on-chip as well as off-chip. The application of this work uses external capacitors for measuring material characteristics.

Disregarding flicker noise, the resolution of a sigma-delta ADC in switched-capacitor (SC) technology is mainly limited by the $\frac{kT}{C}$-noise on the switched capacitors, which results from the thermal noise of the switches [1]. Therefore, large sampling capacitors are desirable. In a capacitive sensor interfacing scheme, where the sensor capacitance directly serves as sampling capacitor [2], small front-end capacitors are desirable to increase the signal gain. Despite the increased thermal noise, a higher signal-to-noise ratio (SNR) can be achieved using smaller capacitors.

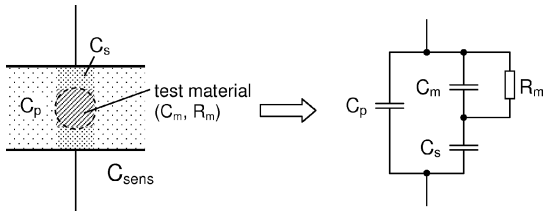

Figure 1. Equivalent circuit of the sensor capacitance

A switched-capacitor sigma-delta CDC interfacing capacitive sensors in the range of some hundred fF is discussed here.

The use of two converter channels with different integration times during the discharge phase of the sensor capacitor allows the measurement of both the capacitance and the dielectric loss angle of test materials.

2. Measuring Principle

A model of the sensor capacitance including test material is shown in Fig. 1. The face of the test material can be approximated by a square profile. In this consideration,

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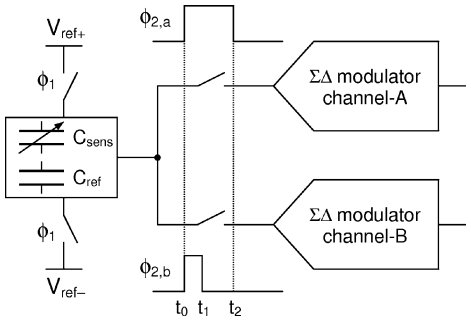


Figure 2. Functional measuring principle

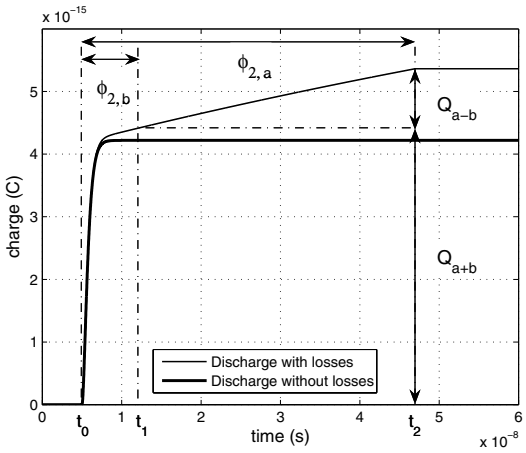


Figure 3. Sensor charge transfer over time

the frequency dependent properties of the test material are unaccounted for, and the equations hold only for static conditions. Nevertheless, this model is suitable to describe the functional measuring principle shown in Fig. 2.

C_{sens} and C_{ref} are connected in a differential configuration, where C_{sens} is the sensor capacitor and C_{ref} is the reference capacitor. During clock phase ϕ_1, the capacitors are charged to $V_{ref+} - V_{ref-}$. During clock phase ϕ_2, the difference sensor discharge $Q_{sens} - Q_{ref}$ is apportioned over two channels. The charge transfer over time is shown in Fig. 3. For an integration time t_0 to t_1, both channels share the transferred charge. The charge Q_{a+b} is integrated in channel-A and channel-B. The pulse width of $\phi_{2,b}$ is set larger than the time constant defined by the sensor capacitor and the on-resistance of the CMOS switches. At t_1, channel-B is disconnected from the sensor capacitor and channel-A continues integration. During $t_2 - t_1$, the remaining charge Q_{a-b}, which was trapped in C_m and C_s by the dielectric losses, is integrated in channel-A.

The dielectric loss angle φ of a test material is given by (1), where f is the sampling frequency of the sensor capacitors. The material density ratio p is given by (2).

$$\varphi = \arctan \frac{1}{2\pi f C_m R_m} \quad (1)$$

$$p = \frac{volume\ of\ test\ material}{overall\ measuring\ capacitance\ volume} \quad (2)$$

3. Architectural Design

3.1. Block Diagram

The block diagram of the sigma-delta modulator architectures is shown in Fig. 4. The modulator topology is a cascade of integrators with feedback (CIFB). A MASH 2-2 structure is used for the 4th order modulator.

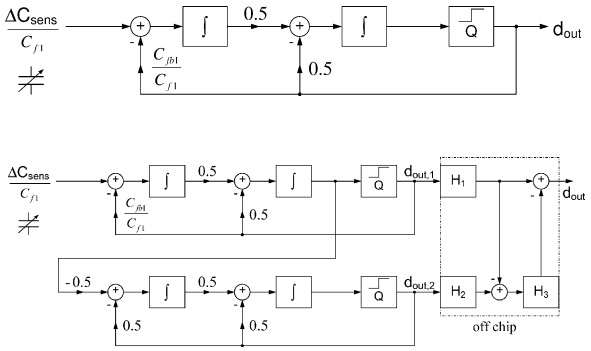


Figure 4. Block diagram of the 2nd and 4th order sigma-delta modulators

3.2. Noise Analysis

The noise contributions of the second and subsequent integrators are neglected in this noise analysis, since the overall noise budget is dominated by the first integrator. In the following, thermal and flicker noise of the first integrator stage are considered.

The thermal noise of the switches is sampled on the feedback capacitor C_{fb1}, the sensor capacitor C_{sens}, and the parasitic capacitor $\frac{C_{para}}{2}$. C_{para} is the sum of the sensor and circuit parasitics at the sensor interface. The sampling switches generate $\frac{kT}{C}$-noise contributions with mean square noise voltages of $\frac{kT}{C_{fb1}}$, $\frac{kT}{C_{sens}}$, and $\frac{kT}{C_{para/2}}$ on the capacitors respectively. Considering the thermal noise and the flicker noise of the main contributing input transistors of the op-amp, a total mean square noise voltage $\overline{V^2_{out,noise}}$ at the output or on the feedback capacitor of the first integrator according to (3) results. f_l is the lowest frequency of interest and $f_s/(2OSR)$ is the signal bandwidth. f_s is the sampling frequency and y (6) is the op-amp factor with the switch

on-resistance R_{on} and the transconductance g_{m1} of the op-amp input transistors. In $\frac{4kT}{C}$, a factor of 2 is caused by switching in both the sampling phase ϕ_1 and the integration phase ϕ_2. A second factor of 2 results from the differential design, where uncorrelated noise from the n- and p-side sampling capacitors are added [3][4]. $H_{thermal}$ (4) is the thermal noise transfer factor, given by the square root of the ratio of the input capacitances to the feedback capacitance plus the transfer factor of the feedback capacitance itself.

The flicker noise of the first integrator stage is expressed by the flicker noise of the noise-equivalent transistors at the input of the op-amp. W and L are the width and length of the op-amp noise-equivalent transistors. $K_{flicker}$ is the flicker noise coefficient, which is a process constant, and C''_{ox} is the specific oxide capacitance per unit area of the transistors. $H_{flicker}$ (5) is the flicker noise transfer factor, which depends on the integration capacitance C_{f1} and the feedback capacitance C_{fb1} of the first integrator.

$$\overline{V^2_{out,noise}} = |H_{thermal}|^2 \cdot \frac{4kT}{C_{fb1}\,OSR} \cdot y + |H_{flicker}|^2 \cdot \frac{2 \cdot K_{flicker}}{C''_{ox} WL} \cdot \ln \frac{\frac{f_s}{2OSR}}{f_l} \quad (3)$$

with

$$|H_{thermal}| = \sqrt{1 + \frac{C_{sens} + \frac{C_{para}}{2}}{C_{fb1}}} \quad (4)$$

$$|H_{flicker}| = 1 + \frac{C_{f1}}{C_{fb1}} \quad (5)$$

$$y = 1 + \frac{1}{6\,(1 + 2R_{on}g_{m1})} \quad (6)$$

y can be omitted for $2R_{on}g_{m1} >> 1$.
In this work y = 1.04.

The signal-to-noise ratio is given by the square of the signal voltage $V_{out,signal}$ at the output according to (7) divided by $\overline{V^2_{out,noise}}$. V_{ref} is the reference voltage of the sensor capacitors and ΔC_{sens} is the sensor capacitance variation to be measured. Using a low-frequency noise cancellation method, flicker noise can be shifted out of the signal frequency band, hence the thermal noise becomes dominant [5]. Neglecting flicker noise, the thermal noise dependent SNR in (8) is obtained. The resolution can be increased by reducing the feedback, sensor, and parasitic capacitances for a constant sensor signal charge, OSR and reference voltage.

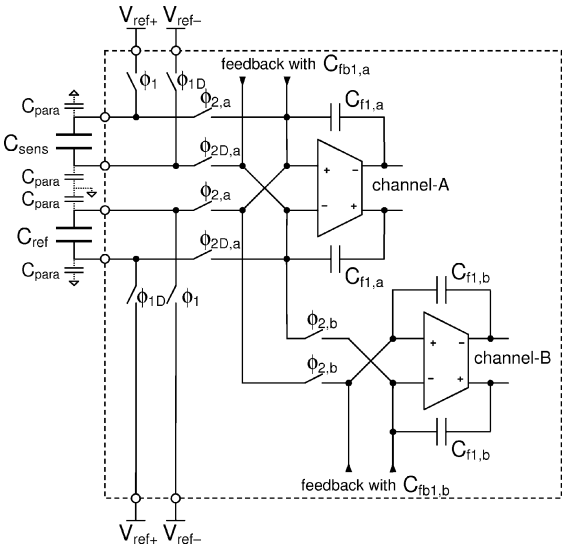


Figure 5. Sensor front-end

$$V_{out,signal} = V_{ref} \cdot \frac{\Delta C_{sens}}{C_{fb1}} \quad (7)$$

$$SNR_{thermal} = \frac{V^2_{ref} \cdot \Delta C^2_{sens} \cdot OSR}{4kT\left(C_{fb1} + C_{sens} + \frac{C_{para}}{2}\right) \cdot y} \quad (8)$$

4. Implementation

The capacitive sensor consists of a reference and a signal capacitor located close to each other in order to minimise parasitic influences. In the sensor front-end, these two capacitors serve as sampling capacitors in a fully differential input stage as shown in Fig. 5. The sensor front-end includes the input stage for channel-A and channel-B.

The offset calibration is done by adjusting one of the external sensor reference voltages.

Folded-cascode operational transconductance amplifiers (OTAs) are used in this design with a n-channel input stage in order to benefit from the lower white noise level compared to p-channel transistors. The input transistors are large to reduce the flicker noise. The common-mode feedback of the amplifiers is realised in switched-capacitor technique. The OTAs have an open-loop gain of 70 dB, a gain-bandwidth product of 2.9 GHz and a slew-rate of 1.25 kV/μs in order to allow sufficient settling in the sampling phases. The integrated capacitors are of polysilicon-to-polysilicon type placed on a grounded n-well. For range selection, the feedback capacitors C_{fb1} and the integration capacitors C_{f1} of the first integrator are adjustable in four steps, from 60 fF to 240 fF for C_{fb1} and from 120 fF to

480 fF for C_{f1}. The second and the following integrator stages have values of C_{fb}=100 fF and C_f=200 fF.

The modulator cells are placed and routed manually in a fully symmetrical arrangement to reduce cross-talk. Separately connected shield lines guard the sensitive wires of the switched-capacitor circuits. The transmission gate switches are realised complementary with half-sized dummy transistors to reduce charge injection and clock feedthrough. A delayed clock driving scheme reduces charge injection and other interferences into the signal path. The single-bit data streams of the converters are recorded and analysed offline.

A 4th order modulator with the same measurement functionality as the 2nd order modulator is implemented on the test chip. With the 4th order modulator working at a second sampling frequency, different frequency dependent test material compositions can be analysed.

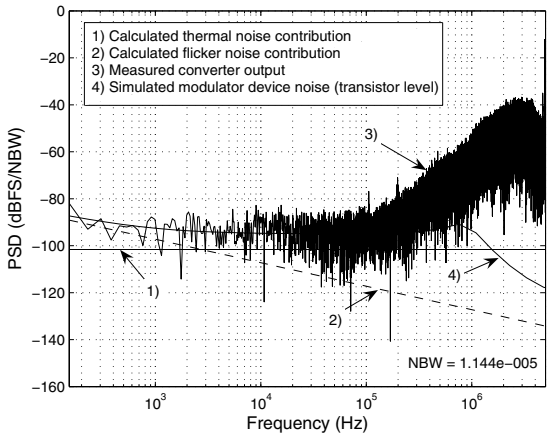
The simulation of the modulator device noise is performed on a transistor-level circuit design. The applied simulation methodology for a discrete-time closed-loop second-order sigma-delta ADC is described in [6]. The simulation results are compared to the calculated estimation as shown in Fig. 6.

5. Experimental Results

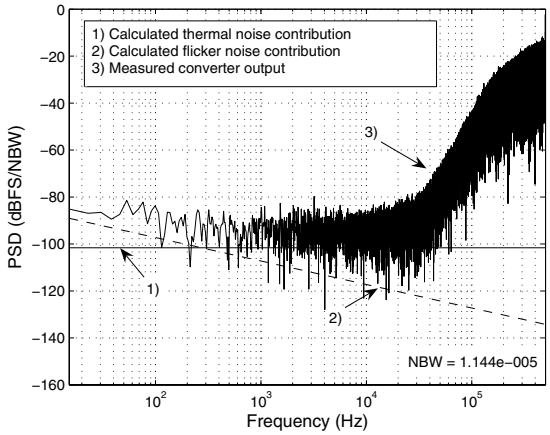
The test chip is characterised on a custom printed circuit board in a CQFP44 package. The single-bit modulator output data stream is analysed in the frequency domain using a 128 kS FFT with a Hanning window. The SNR is calculated by integrating the power spectral density (PSD) over the signal bandwidth. The noise level is 0.2 aF/$\sqrt{\text{Hz}}$ for the 2nd order modulator and 0.52 aF/$\sqrt{\text{Hz}}$ for the 4th order modulator. The peak SNR is measured on a configuration with the lowest gain setting of the first integrator, which gives a larger full-scale range. The full-scale capacitive range is quantified statically for lack of adequate dynamic test equipment. The results of the noise measurements are shown in Fig. 6. The noise bandwidth (NBW) is the normalised unit bandwidth used for the FFT scaling. The plots display the product of the noise density and the noise bandwidth.

The calculated resolution according to (8) is 5.1 aF if only thermal noise is considered and 9.5 aF if flicker noise is included. The measured value of 19.3 aF includes additional contributions caused by circuit non-idealities and noise from the references and the measurement environment.

The dielectric loss angle φ is derived from the output data values $d_{A,out}$ of channel-A and $d_{B,out}$ of channel-B. To calculate the dielectric loss angle difference $\Delta\varphi$ between two test materials, the dielectric loss angles of material 1 and material 2 are measured and compared. The formula used for this approximation is given in (9) and the measured results are shown in Fig. 7.



(a)



(b)

Figure 6. Calculated vs. measured noise power spectral density (PSD) plots of the (a) 2nd and (b) 4th order modulator

$$\Delta\varphi = \arctan\left(\frac{d_{A,out}-d_{B,out}}{d_{A,out}+d_{B,out}}\right)_{material1} - \arctan\left(\frac{d_{A,out}-d_{B,out}}{d_{A,out}+d_{B,out}}\right)_{material2} \quad (9)$$

The summary of the test chip performance is given in Table 1. Theoretical, a 10 dB difference in the SNR between the 2nd and 4th order modulator occurs due to the OSR ratio of 10 between the modulators. The actual difference is 6.6 dB which deviation is stated to come from measuring influences. The value of 0.86 ° of the dielectric loss angle resolution for the 2nd order modulator compared to 0.3 ° for the 4th order modulator is due to a missing offset adjustment circuit between channel-A and channel-B.

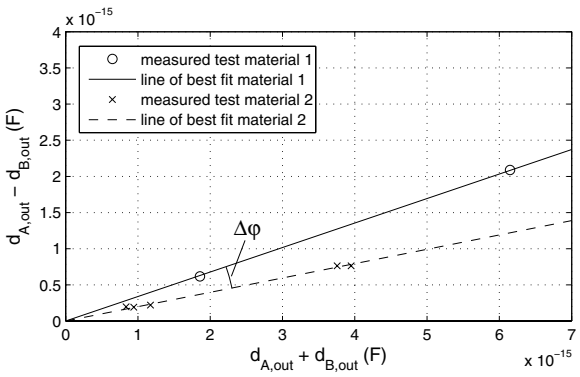


Figure 7. Measured dielectric loss data $d_{A,out} - d_{B,out}$ vs. $d_{A,out} + d_{B,out}$ and resulting dielectric loss angle difference $\Delta\varphi$ of the 4th order converter

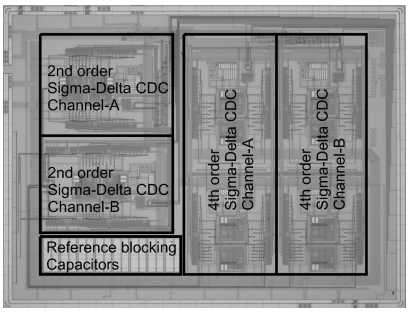


Figure 8. Test chip foto (without pads)

Table 1. Test chip performance summary

	2nd Order Mod.	4th Order Mod.
Supply Voltage	3.3 V	
Power Dissip. (Channel Pair)	64 mW	116 mW
Sampling Frequency	10 MHz	1 MHz
Oversampling Ratio	500	50
SNR_{max} (BW=10kHz)	73.4 dB	66.8 dB
Resol. Cap. (BW=10kHz)	19.3 aF	51.3 aF
Resol. Diel. Loss Angle[1] at p = 0.55 %[3] (BW=10kHz)	0.86 °[2]	0.3 °
Sensor Capacitance	305 fF	
Technology	*austriamicrosystems AG* C35B3C0 0.35 μm CMOS DPTM	
Silicon Area without Pads	0.9 x 1.2 mm^2	1.2 x 1.5 mm^2

6. Conclusion

A switched-capacitor sigma-delta capacitance-to-digital converter for capacitive sensors in the sub-pF range has been presented. This noise optimised circuit yields a noise level of 0.2 aF/$\sqrt{\text{Hz}}$ at an OSR of 500, compared to 1.5 aF/$\sqrt{\text{Hz}}$ given for the 2nd order CDC in [2].

A new scheme in switched-capacitor technique to simultaneously measure the capacitance and the dielectric loss angle of test materials has been introduced. The resolution of the dielectric loss angle is as low as 0.3 °.

Calculations and transistor-level simulations of the thermal and flicker noise contributions have been performed and are in good agreement with the measured results.

Power dissipation of the circuits can be improved, mainly for the 2nd, 3rd and 4th integrators due to the noise shaping characteristic of the modulator. Using correlated double sampling (CDS) will further reduce the flicker noise and the offset drift of the OTAs [7]. This will result in a SNR limited by $\frac{kT}{C}$-noise. An improved offset adjustment between the parallel connected channel pairs will be required to guarantee a dielectric loss angle resolution of at least 0.3 ° at a material density ratio of 0.55 % in production.

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[1] experimentally determined

[2] lower value due to a missing offset adjustment circuit between the parallel connected dielectric loss angle measuring channels

[3] material density ratio $p = \frac{volume\ of\ test\ material}{overall\ measuring\ capacitance\ volume}$