Low-Overhead Design of Soft-Error-Tolerant Scan Flip-Flops with Enhanced-Scan Capability

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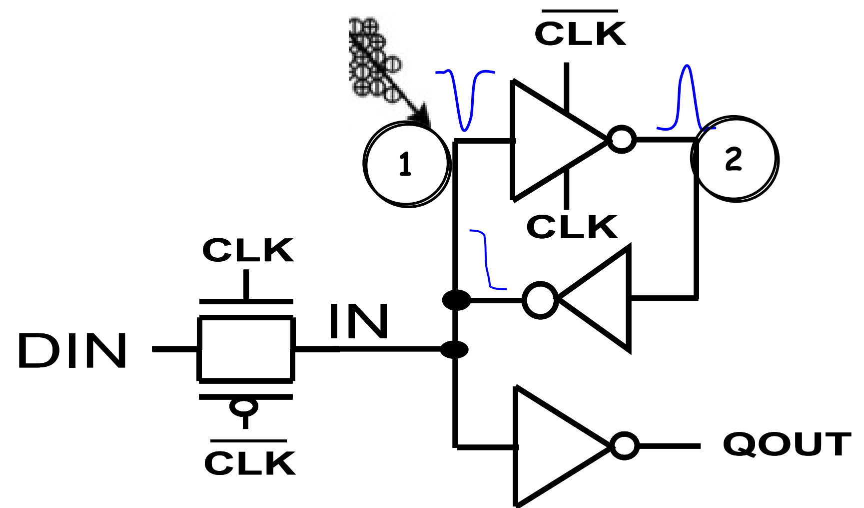
Motivation

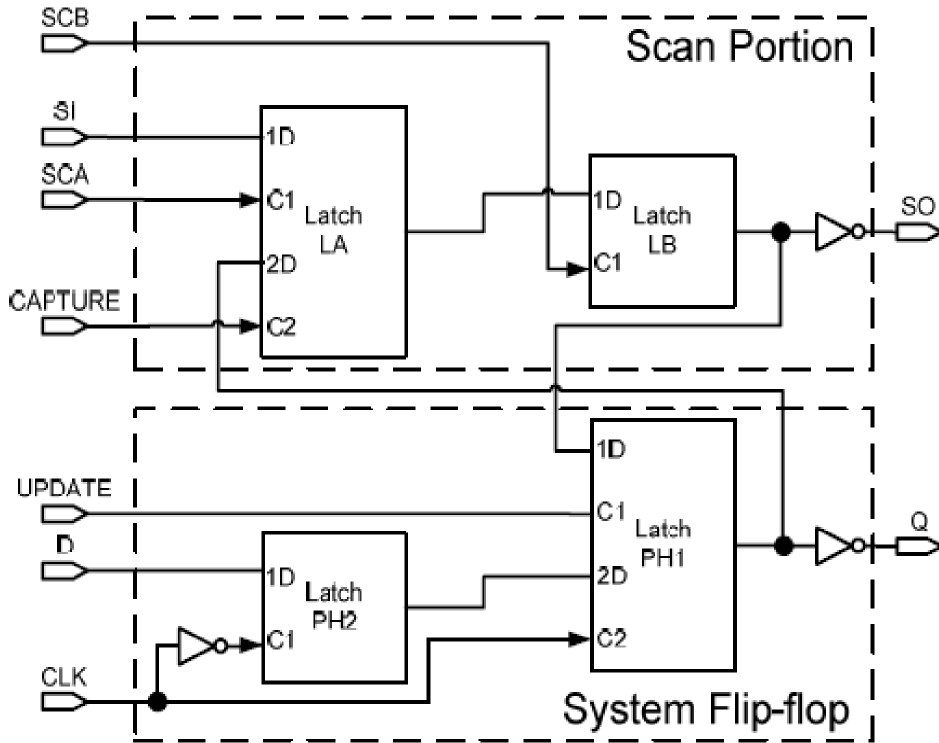
- Critical charge: Qc
- Scaling: C↓, V↓, Qc↓
- Unlike memories flip flops not protected by parity and ECC



Static Latch Cell

- **Cross-coupled inverters**
- **Feedback increases soft error vulnerability**

Motivation

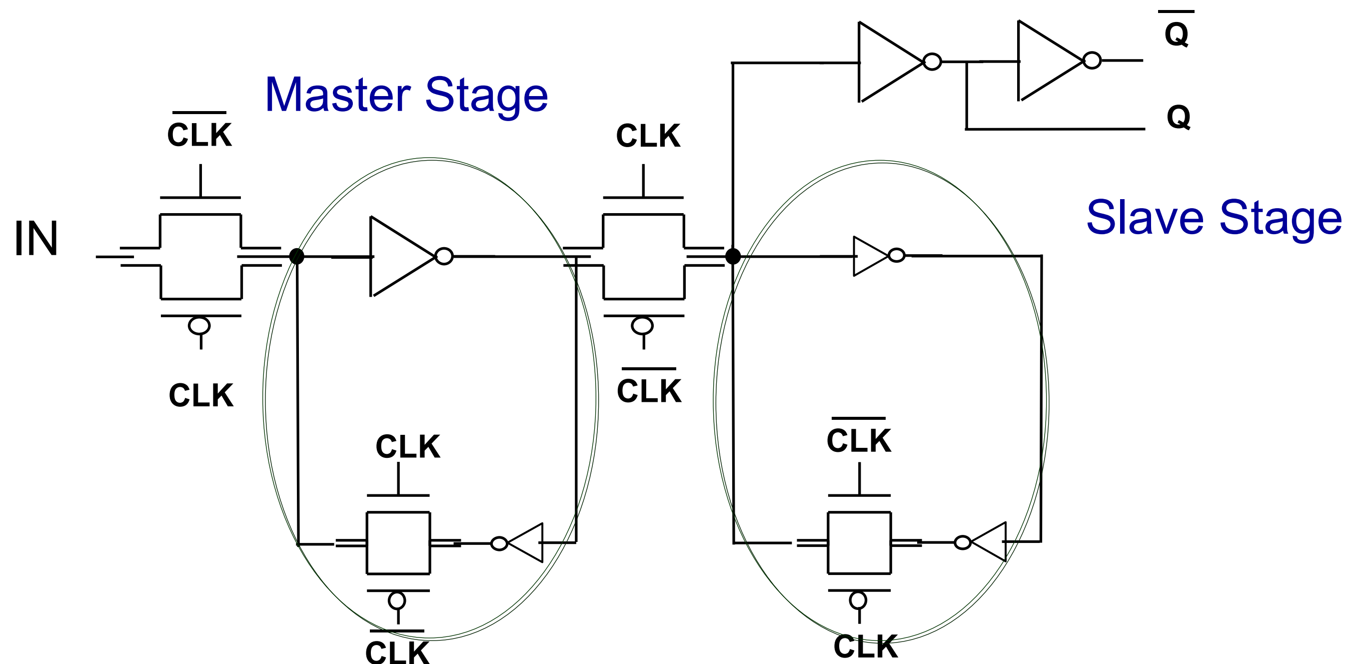


Scan Flip-flop design of a Microprocessor*

- **Reuse of on chip scan design-for-testability (DFT) resources to reduce overhead**
- **Integration of soft error tolerant flip-flops into the scan path**

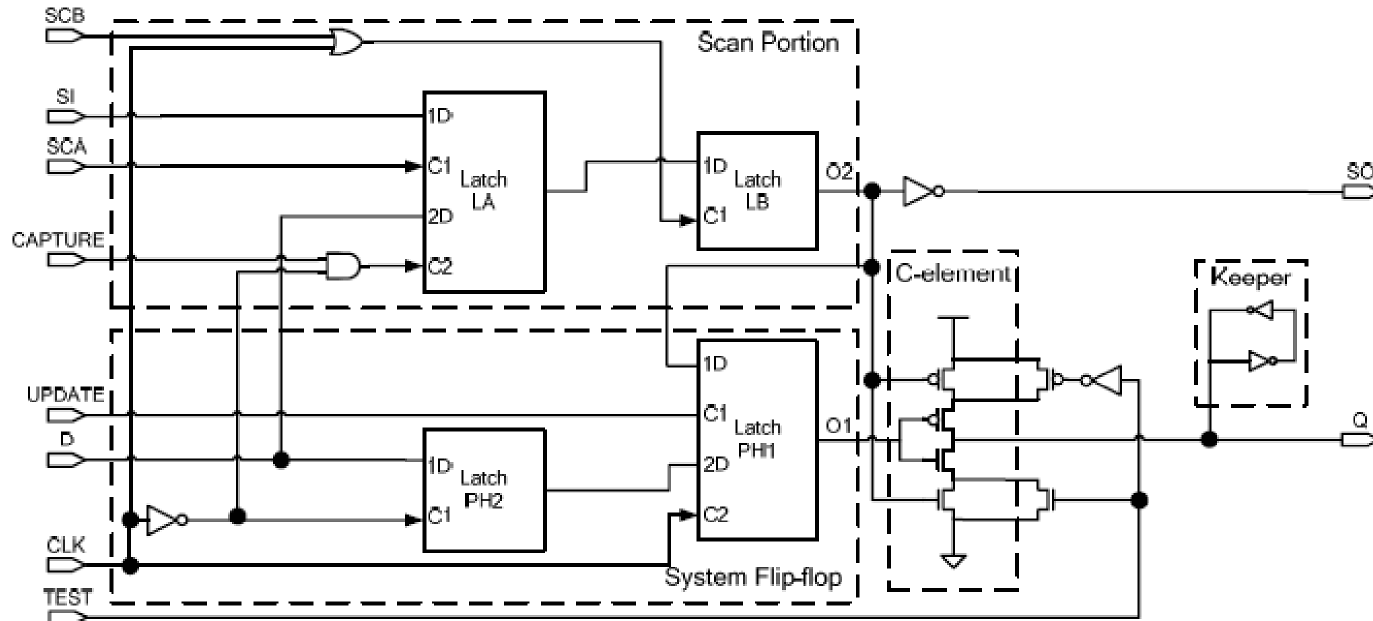
S. Mitra,N. Seifert, M. Zhang, Q. Shi, K. Kim, "Robust System Design with Built-In Soft Error Resilience," *Computer*, vol. 38, No. 2, Feb. 2005, pp. 43-52

Soft Error in Transmission Gate Flip-Flop



- Clk = 1, Master Stage susceptible
- Clk = 0, Slave Stage susceptible
- Need a redundant copy for soft error detection / correction

Reuse of On Chip Scan DFT resources

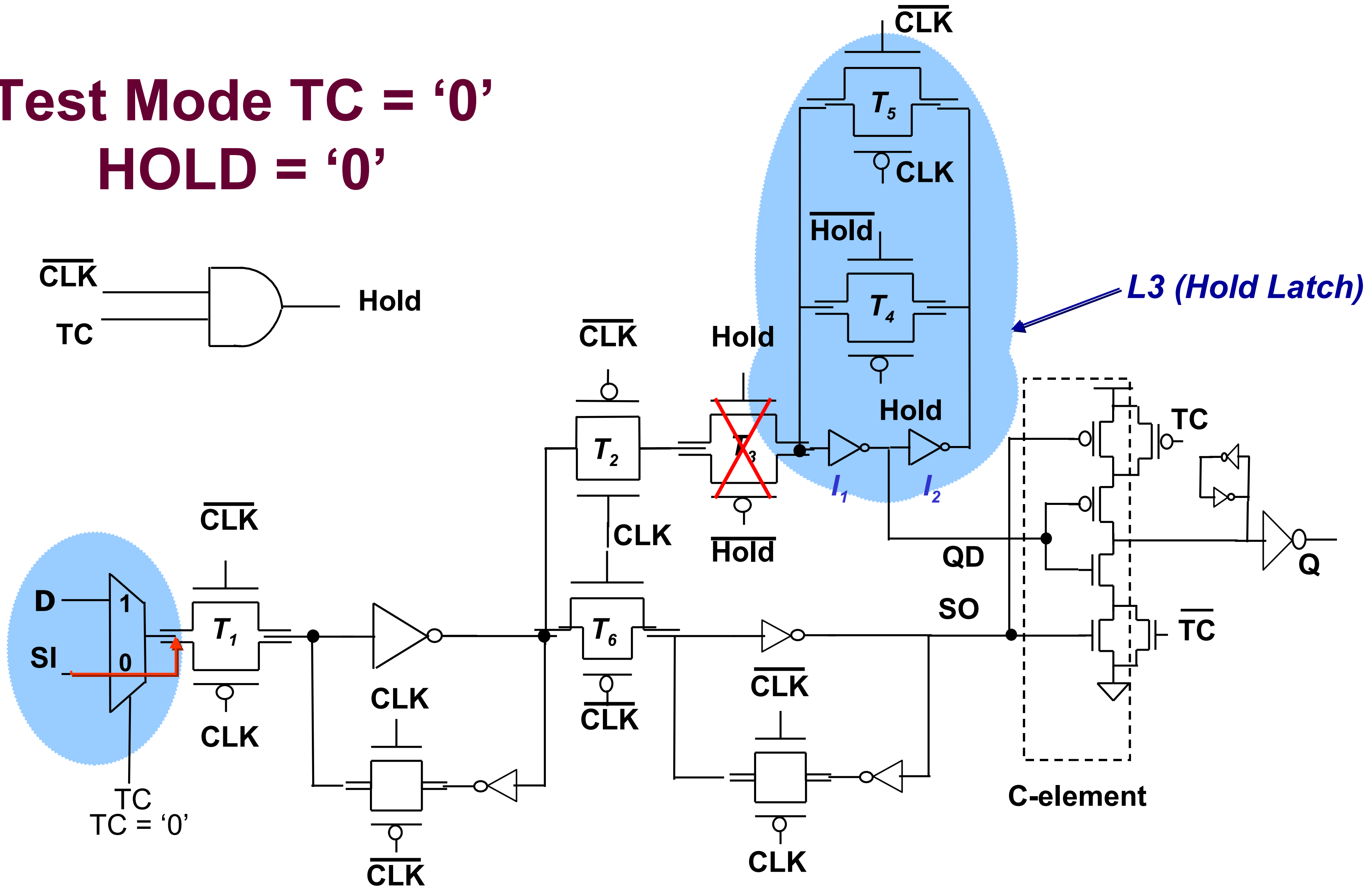


Scan Reuse for Soft Error blocking* (ISR)

- Scan latches sized up to store a copy of data, increases area and power overhead
- Four latches required to store the two copies of the data_

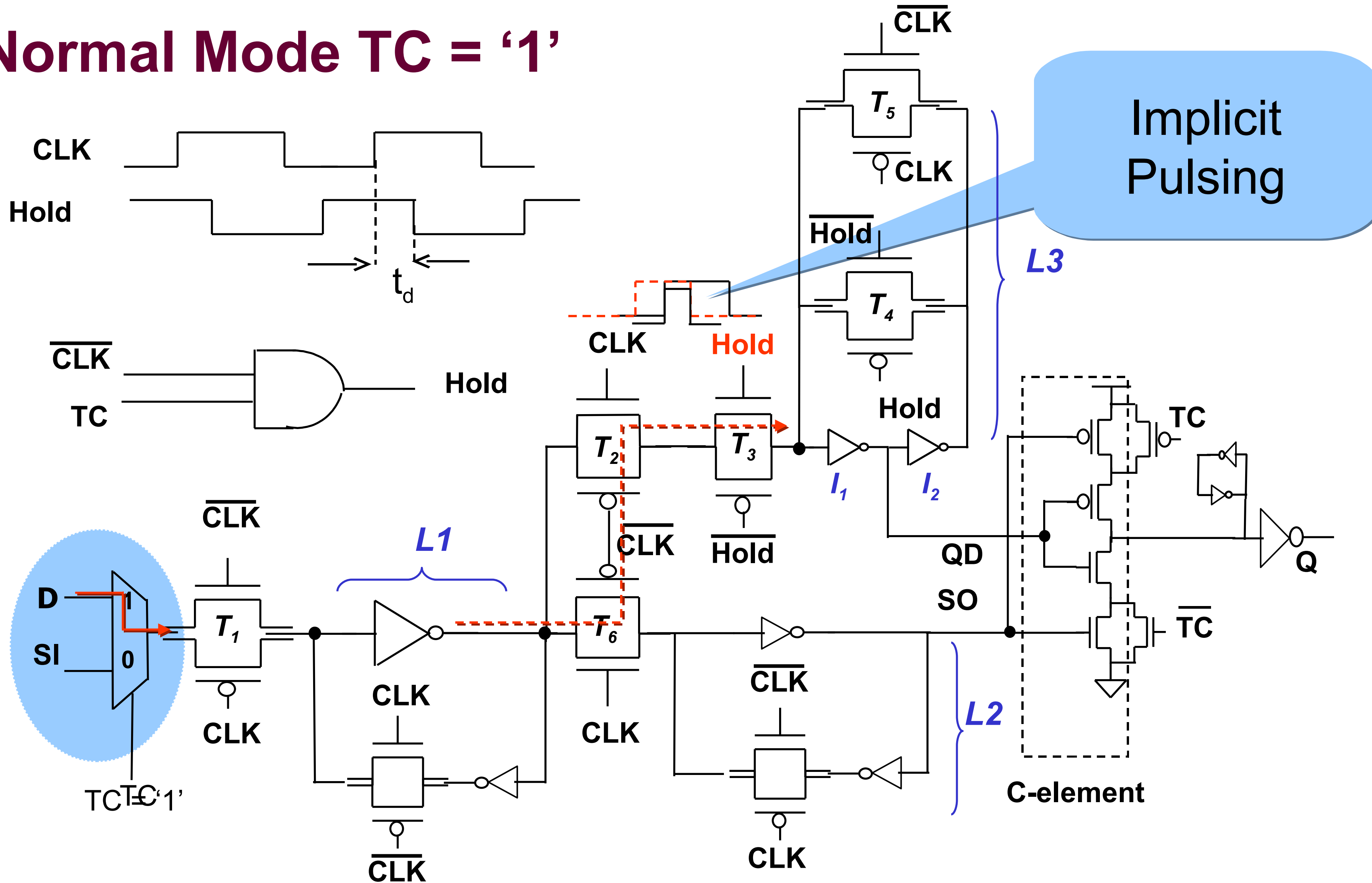
S. Mitra, N. Seifert, M. Zhang, Q. Shi, K. Kim, "Robust System Design with Built-In Soft Error Resilience," *Computer*, vol. 38, No. 2, Feb. 2005, pp. 43-52

Proposed Design for Enhanced Scan and Soft Error Correction (ESFF-SEC)



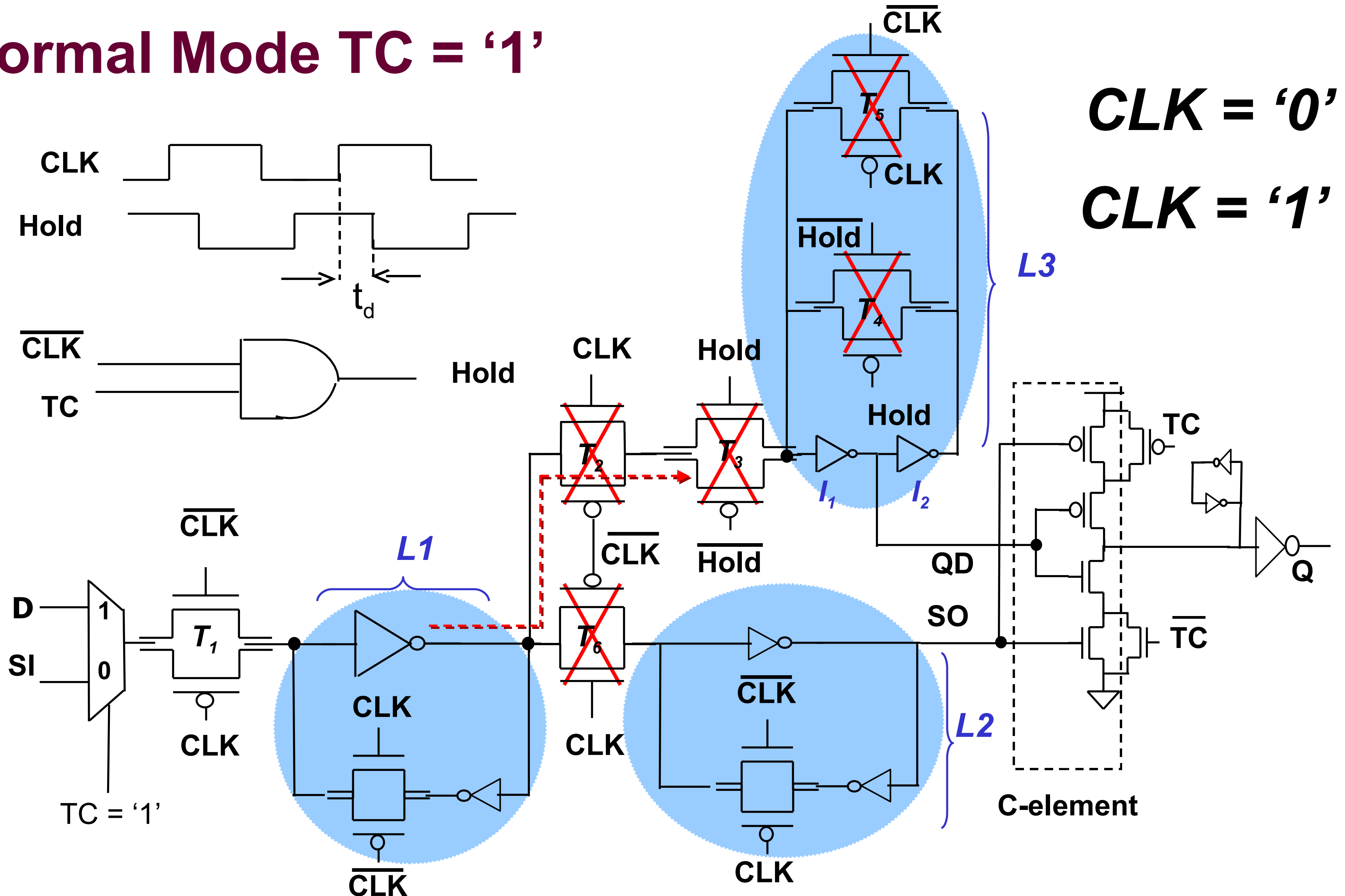
Proposed Design (Contd.)

Normal Mode TC = '1'



Proposed Design (Contd.)

Normal Mode TC = ‘1’

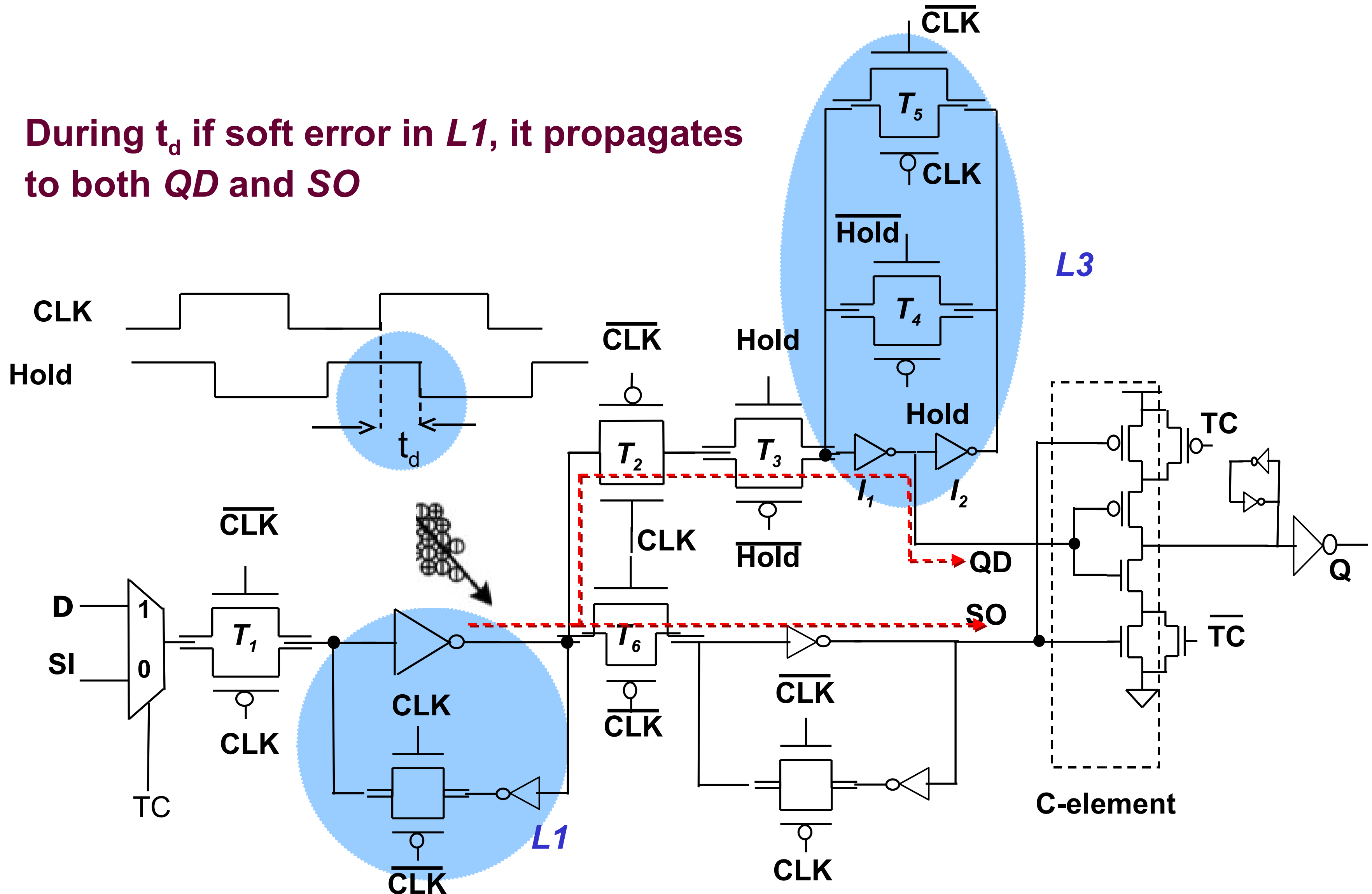


ESFF-SEC vs. ISR

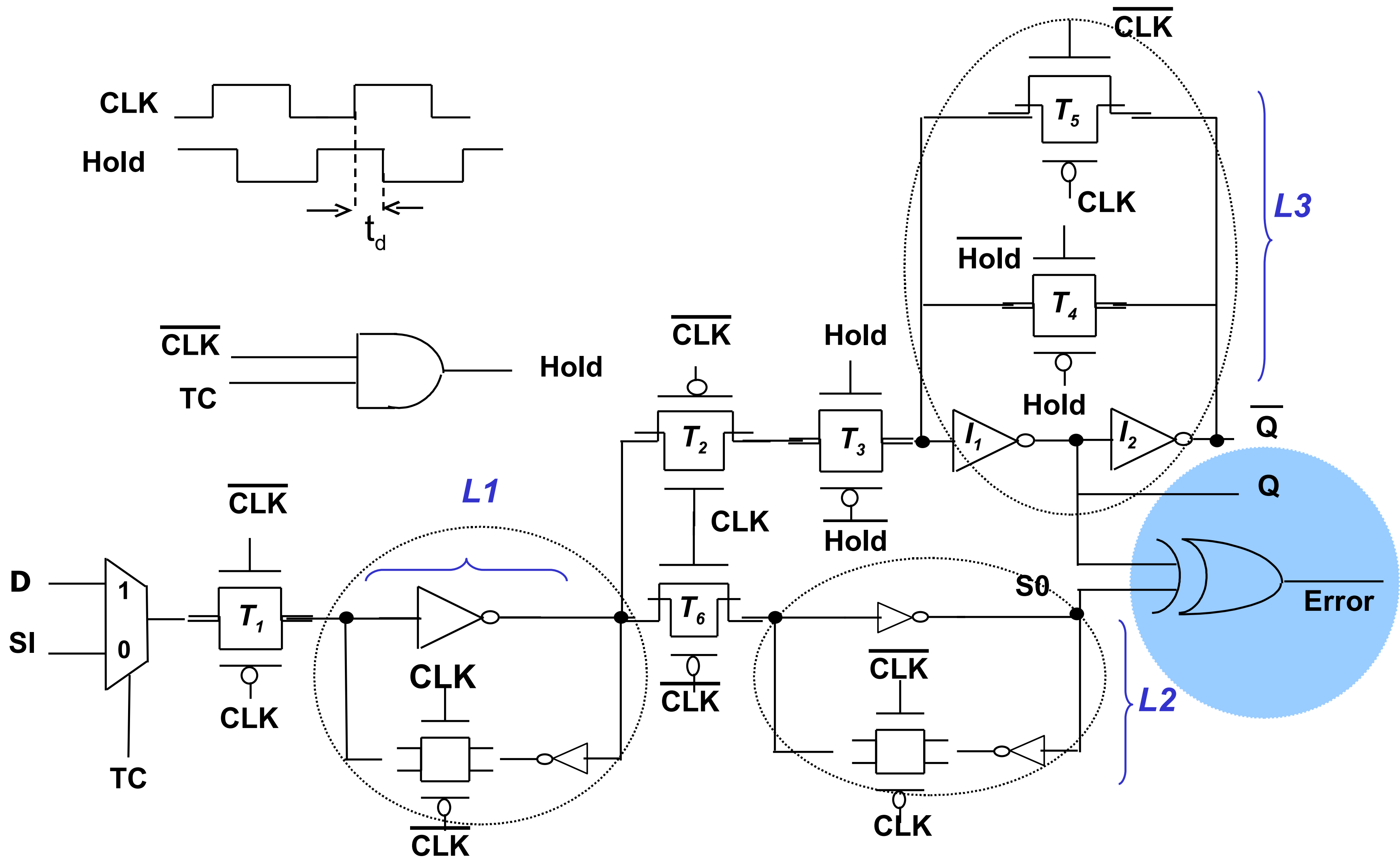
	ESFF-SEC	ISR
Power	1.0	1.26
Area	1.0	1.61
Setup Time	1.0	1.70
C-to-Q Delay	1.0	1.00

- **Power and Area - Reduction in the number of latches from four to three**
- **Setup time - Scan Latch is sized up in ISR, more load on the data driver**

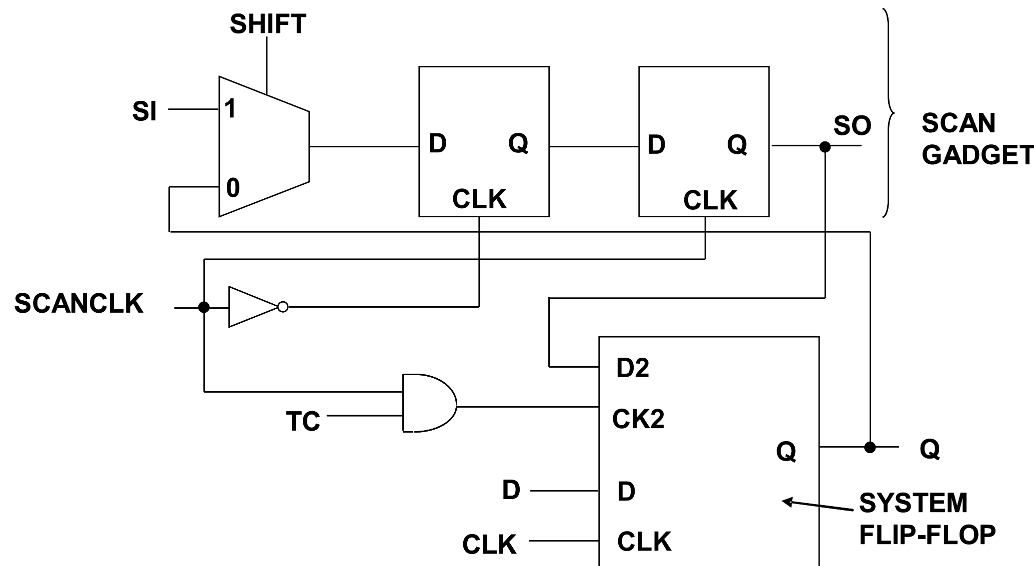
Proposed Design (Contd.)



Proposed Design for Enhanced Scan and Soft Error Detection (ESFF-SED)



Enhanced Scan Approach to Delay Testing

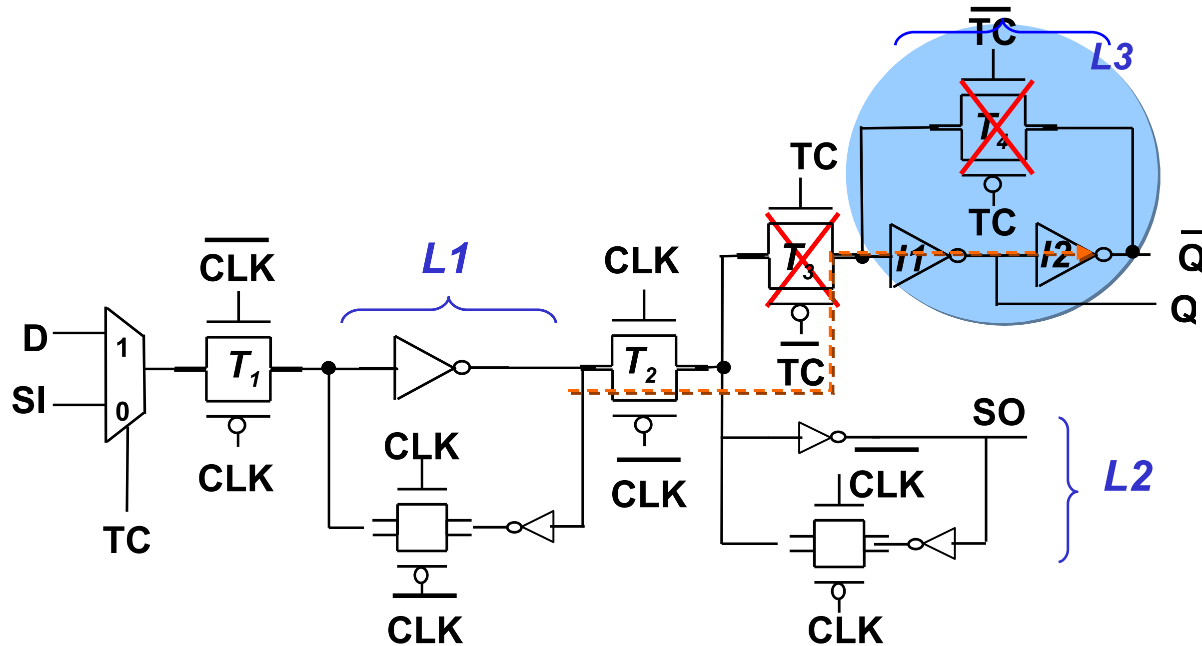


Scan Gadget Scheme (HSSG)*

- **Scan Gadget Scheme (HSSG) – uses a Scan Gadget along with system latch to scan in and hold test vector**
- **Overhead – extra latch, complicated design of system flip-flop requiring two clocks and extra timing signals required (SCANCLK, SHIFT)**

R. Kuppuswamy et al., "Full Hold-Scan Systems in Microprocessors: Cost/Benefit Analysis," *Intel Technology Journal*, Vol.8, Issue 1, Feb. 2004

Proposed Design for Enhanced Scan Delay Testing (ESFF)



- Drivers I_1 and I_2 converted into latch *L3* using T_3 and T_4
- Normal Mode, TC = ‘1’, T_4 is OFF and T_3 is ON
- Test Mode, TC = ‘0’, T_3 is OFF and T_4 is ON, *L3* disconnected from *L2* and *L1*, acts as a hold latch
- No extra timing control signals required

Results

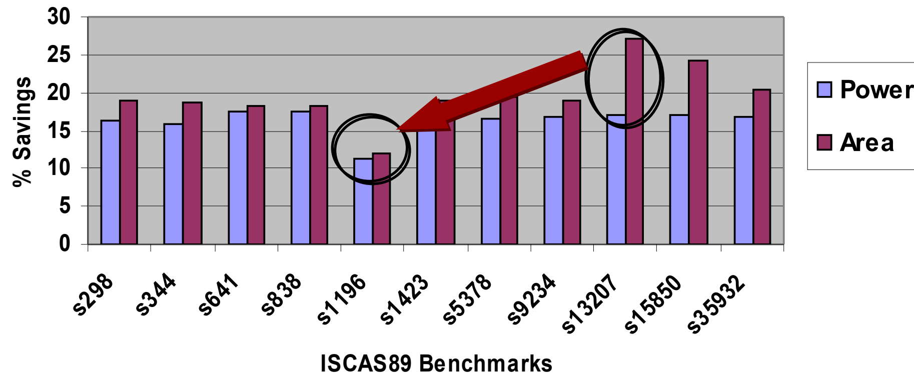


Figure. 1

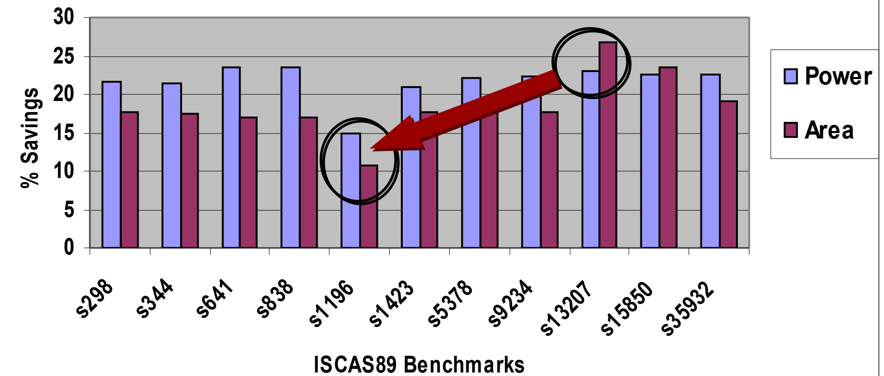


Figure. 2

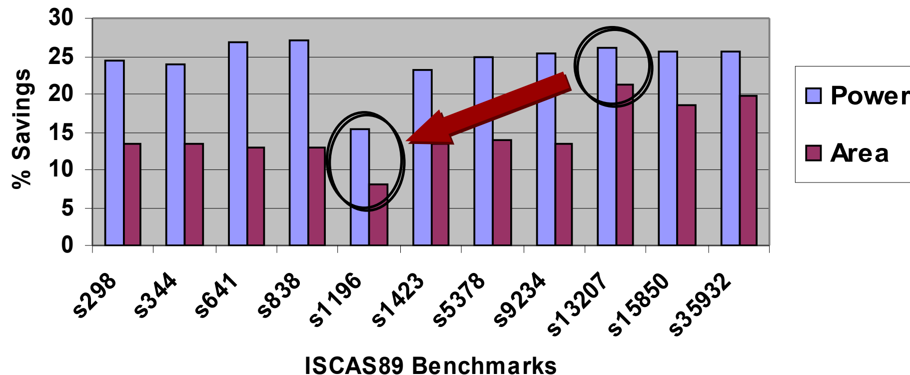


Figure. 3

- HSPICE simulation of ISCAS89 benchmarks in BPTM 70nm node
- 16% power and 17% area reduction on average at no delay overhead
- % of sequential elements in the benchmark decrease from 74% in s13207 to 22% in s1196, hence total savings decrease

Conclusion

- **Novel Flip-Flop designs are proposed having soft error detection/correction capability along with enhanced scan based delay fault testing**

- A simplified version having enhanced scan delay fault testing capability is proposed

- Low area and power overhead due to reuse of existing hardware resources

Thank You!

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C-element and Keeper

O1	O2	Q
0	0	1
1	1	0
1	0	Previous Value
0	1	Previous Value

- **Keeper is used to retain the previous value when O1 and O2 are different from each other**