Low-Pass Filtering SC-DAC for Reduced Jitter and Slewing Requirements on CTSDMs

Dries Vercaemer, Johan Raman, and Pieter Rombouts

***Abstract*— In this paper, a technique is introduced that improves the performance of one-bit continuous-time sigma delta modulators (CTSDMs) using a low-pass filtering switched capacitor digital to analog converter (LPSC-DAC). This DAC effectively combines an infinite impulse response filter with a switched capacitor resistor DAC (SCR-DAC). The resulting DAC is inherently immune toward inter-symbol interference. Moreover, by filtering the feedback signal in the discrete-time domain, the jitter robustness of the modulator is greatly improved and most importantly the slewing requirements on the OpAmps in the modulator's loop filter are greatly relaxed up to a level that the OpAmps can be scaled down toward their ultimate noise limited power level. Furthermore, this LPSC-DAC does not suffer from the SCR-DAC's disadvantageous trade-off between the modulator's jitter, slewing, and anti-aliasing performance. We also show how to compensate for the extra pole of the LPSC-DAC, such that the CTSDM's loop filter, noise- and signal-transfer function remains unchanged. As a result, this technique is completely transparent to the system level designer and established system-level design techniques for sigma delta modulators remain applicable.**

***Index Terms*— Analog-to-digital conversion, pulse-width modulation, small area ADC, CTSDM, low power, SC-DAC.**

I. Introduction

ONE-BIT continuous-time sigma delta modulators (CTSDMs) have gained renewed attention over their multi-bit counterparts thanks to their small size and simplicity [1]–[5]. These advantages come from the fact that multi-bit CTSDMs need a multi-bit quantizer and a linear multi-bit feedback digital to analog converter (DAC). Due to the reduced voltage headroom (inherent to today's ultra deep sub-micron technology), it is difficult to design reliable multi-bit quantizers. Today, linearizing a multi-bit DAC is mature (e.g. through dynamic element matching or calibration) but still introduces a considerable silicon area overhead. One-bit CTSDMs don't need these multi-bit blocks whereas they fully exploit the fact that the devices in modern ultra deep sub-micron technology are very fast.

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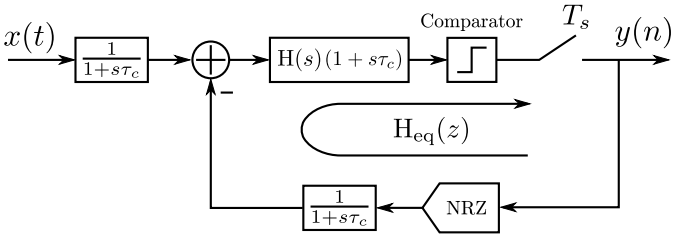


Fig. 1. Low-pass filtering and compensation scheme of [3].

This allows for high over sampling ratios (OSRs), such that good performance can easily be obtained with one-bit modulators. All these elements shift the balance in favor of one-bit CTSDMs.

Nevertheless, one-bit modulators also face challenges. High OSR means that one-bit designs drive their loop filter with high-frequency full scale DAC-pulses, resulting in stringent slew rate requirements on the OpAmps. Furthermore, using full scale pulses increases the errors caused by jitter or inter-symbol interference (ISI) at the DAC. A possible solution to the slew rate problem is filtering the DAC signal. Here we can consider two families of techniques. The first are finite impulse response DAC (FIR-DAC) techniques, which have been studied in [5]–[11]. In this work we will focus on a second family: i.e. analog filtering techniques. As will become clear later on, the proposed approach is in every aspect competitive with the FIR-DAC approach. Moreover, the technique is orthogonal to the FIR-DAC approach and hence these techniques could be combined if needed.

First variants of the analog filtering approach were proposed in [3] and [11]–[13]. It consists of adding a passive low-pass filter in front of the first OpAmp in the loop filter. This reduces the voltage swing and required slew rate of the first OpAmp in the loop. Unfortunately, adding this filter to the loop puts constraints on the modulator's noise transfer function (NTF) such that the noise shaping is affected. Solutions for this problem have been proposed in [3] and [12]. In the former, an extra zero is added to the loop filter after the first OpAmp to cancel the pole introduced by the low-pass filter, leading to the system of Fig. 1. As a result, the technique of [3] is completely transparent on the system level, leaving the loop filter, noise transfer function (NTF) and signal transfer function (STF) unchanged. Unfortunately this approach does not improve errors introduced at the DAC, like jitter or ISI. This is because the filtering happens in the continuous-time

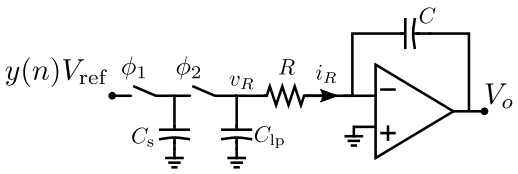


Fig. 2. LPSC-DAC and integrator.

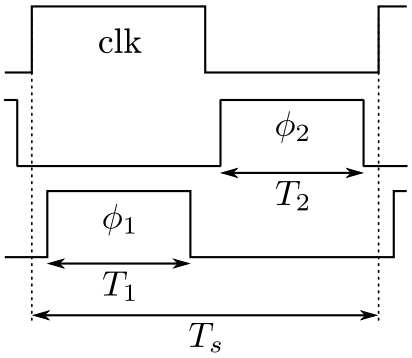


Fig. 3. Clock phases.

domain *after* the DAC and hence errors introduced at the DAC have already entered the system and will directly affect the modulator's performance. Inspiration for an improved analog filtering technique can be found in [4]. Here, a passive-active modulator without OpAmps is presented. Instead, switched capacitors and passive RC-filters are used to implement (lossy) integrators, while the gain is provided by differential pairs and the 1-bit quantizer. In this work we elaborate the core switch-capacitor-RC circuit of [4] and show that it actually performs its filtering in the discrete-time domain. This means it can reduce DAC-errors such as jitter or ISI. We will denote this DAC structure as a low-pass filtering switched capacitor DAC (LPSC-DAC). However, similar as in other filtering techniques [3], the loop's noise- and signal transfer functions are again affected and we explain how this can be solved by a compensation scheme similar to the one of [3].

Below, the resulting LPSC-DAC CTSDM is analyzed extensively with respect to the modulator's noise, slewing, jitter and anti-aliasing performance. It is found that the resulting structure has very good performance on each of these aspects.

II. Switched Capacitor Low-Pass Filtering DAC

Fig. 2 shows the proposed low-pass filtering switched capacitor DAC embedded in an RC-integrator as would be the case at the input of a CTSDM. ϕ_1 and ϕ_2 are non-overlapping clock signals with the same period as the sampling clock, T_s, and a duty cycle slightly smaller than 50 %, as shown in Fig. 3. To simplify the following analysis, we will however neglect the time of non-overlap between ϕ_1 and ϕ_2, such that $T_s = T_1 + T_2$. During ϕ_1, the capacitor C_s is either charged to the reference voltage V_{ref}, or discharged to ground, depending on the value of the bit $y(n)$. We will assume that V_{ref} equals unity to simplify the following analysis. During ϕ_2, this capacitor is placed in parallel with the capacitor C_{lp}, and their charge is redistributed. The charge on C_{lp} constantly leaks through the resistor R into the nullator node of the OpAmp. This results in a current which is integrated onto the feedback capacitor C. We will consider this current, i_R on Fig. 2, as the output signal of the LPSC-DAC.

In order to analyze the behavior of this structure, we start by examining what happens with the voltage v_R, during switching. If we define $v_R(0-, n)$ as the value of v_R at the instant just before the n'th rising edge of ϕ_2, and $v_R(0+, n)$, as the voltage just after, we can write down the following relationship, assuming ideal switches and using conservation of charge:

$$v_R(0+, n) = \frac{C_s y(n) + C_{lp} v_R(0-, n)}{C_{lp} + C_s} \tag{1}$$

$$= \alpha y(n) + (1-\alpha) v_R(0-, n) \tag{2}$$

$$\alpha = \frac{C_s}{C_s + C_{lp}} \tag{3}$$

During clock phase ϕ_2, $v_R(t)$ exponentially decays, with time constant $R(C_s + C_{lp})$. During ϕ_1, the time constant is RC_{lp}. Note that the charge on C_{lp} does not change on the falling edge of ϕ_2. This behavior is illustrated in Fig. 4a (bold black line). The total decay over one clock period is then given by:

$$\gamma = e^{-\frac{T_1}{RC_{lp}}} e^{-\frac{T_2}{R(C_s + C_{lp})}} \tag{4}$$

Combining this with Eq. (2) results in the following relationships:

$$v_R(0-, n) = \gamma\, v_R(0+, n-1) \tag{5}$$

$$v_R(0+, n) = \alpha y(n) + (1-\alpha)\gamma\, v_R(0+, n-1) \tag{6}$$

To ease notation we will rename the sequence $v_R(0+, n)$ as $v(n)$. Now, this sequence $v(n)$ depends in a linear time-invariant way on the input sequence $y(n)$. And hence, we can write down the corresponding Z-domain transfer function, $\mathrm{H_{lp}}(z)$:

$$\frac{V(z)}{Y(z)} = \mathrm{H_{lp}}(z) = \frac{\alpha}{1 - (1-\alpha)\gamma\, z^{-1}} \tag{7}$$

Clearly, this transfer function corresponds to a discrete-time first-order low-pass filter.

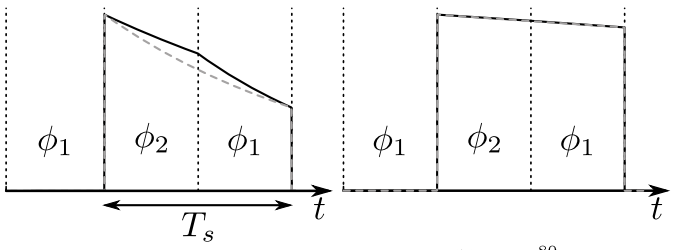
The continuous-time waveform $v_R(t)$ is the convolution of the discrete-time signal $v(n)$ with the exponentially decaying pulse shown on Fig. 4a (bold black line). As explained above, the exponential decay has a slightly different time constant during ϕ_1 than during ϕ_2. In practice this can be accurately approximated as one effective time constant, chosen to result in the same total exponential decay during a clock cycle:

$$\tau = -\frac{T_s}{\ln(\gamma)} = RC_{lp} \frac{T_s}{T_s - \alpha T_2} \tag{8}$$

As will become clear later on, in a practical sizing α will normally be quite small. In this case, the equation can be simplified into:

$$\tau \approx RC_{lp} \tag{9}$$

Since the exponential pulse starts on the rising edge of ϕ_2, it is delayed for a duration T_1 with respect to the rising edge



(a) $\tau = \frac{1}{\omega_s}$ (b) $\tau = \frac{80}{\omega_s}$

Fig. 4. Actual pulse (solid black) and its single exponential approximation (dashed gray) for (a) an unrealistically small value of the time constant τ and (b) for a typical value of the time constant.

of the clock signal. This leads us to the following expression for the exponential pulse in the Laplace domain:

$$\mathrm{P}(s) = \frac{1 - \gamma\, e^{-sT_s}}{1 + s\tau} \tau e^{-sT_1} \tag{10}$$

The impulse response of Eq. (10) is illustrated on Fig. 4 for two different sizings, together with the actual pulse with varying time constant. For Fig. 4a the value of τ was chosen very small to clearly illustrate the difference in pulse shape. As will be explained in section IV, in an actual design τ will be made quite large to optimally benefit from the filtering of the DAC. A pulse with such a sizing ($RC_{lp} = \frac{80}{\omega_s}$) is shown in Fig. 4b. ω_s represents the angular sampling frequency: $\omega_s = \frac{1}{2\pi T_s}$. In both sizings, C_s was equal to $\frac{T_s}{R}$. As can be seen on Fig. 4b, the exponential pulse is very well approximated if C_{lp} is much higher than C_s.

The output signal of the LPSC-DAC, the current i_R (annotated in Fig. 2), is simply v_R divided by R, assuming that the OpAmp is ideal. Using this observation, we obtain the transfer function DAC(s) from $y(n)$ to i_R:

$$\mathrm{DAC}(s) = \frac{1}{R}\,\mathrm{P}(s)\,\mathrm{H_{lp}}(z)|_{z=e^{sT_s}} \tag{11}$$

Eq. (11) represents the product of a discrete-time low-pass filter and a delayed exponential DAC-pulse. This justifies the name for this circuit (see Fig. 2): low-pass filtered switched capacitor DAC, or LPSC-DAC.

The discrete-time impulse response of $\mathrm{H_{lp}}(z)$ is illustrated in Fig. 5. Here again the sizing motivated in section IV is used: $RC_{lp} = \frac{80}{\omega_s}$ and $C_s = \frac{T_s}{R}$. The total impulse response of the LPSC-DAC is shown on Fig. 6, where the black dots represent the output samples of the discrete-time filter, while the gray lines show the exponential pulses, approximated with the constant time constant of Eq. (8). It is clear that the DAC-pulse is spread out over several clock periods due to the filtering operation. This reduces the peak value of the pulse, which is beneficial for slewing considerations. Lastly we also expect this LPSC-DAC to be immune against inter-symbol interference (ISI), similarly to a switched capacitor DAC (SC-DAC [14]). Parasitic effects, such as charge injection, happen every clock cycle and do not depend on the derivative of the digital input signal as is the case with an NRZ-DAC. Simulations on a modulator with an LPSC-DAC, implemented with transistor switches, confirmed mismatch and charge injection did not result in ISI.

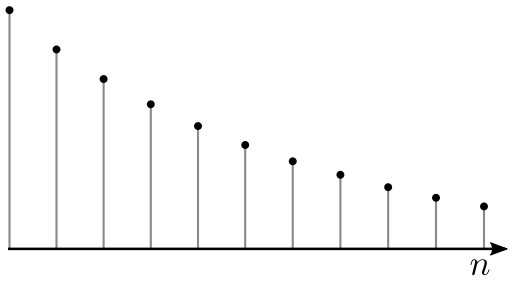


Fig. 5. Impulse response of $\mathrm{H_{lp}}(z)$.

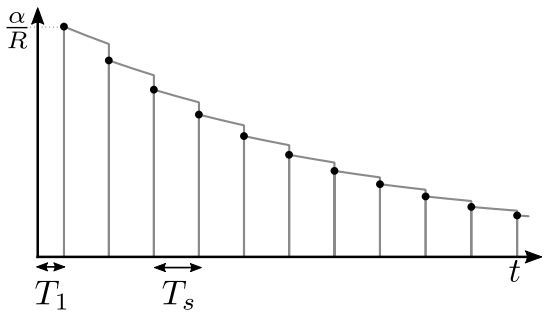


Fig. 6. Impulse response of the overall LPSC-DAC.

III. SDM With LPSC-DAC and Compensation

It is our goal to use the LPSC-DAC in the first stage of a CTSDM. However, from the analysis above we know that the LPSC-DAC operation consists of the combination of a discrete-time first-order low-pass filter effect and a delayed exponentially decaying pulse. Due to this, incorporating the LPSC-DAC in a CTSDM will increase the order of the SDM's total loop filter by one. This effect is undesired because it puts limitations on the modulator's NTF and STF, impeding a typical top-down design of the modulator (with a first NTF synthesis step and a mapping of the NTF to modulator structure in a second step). To make the technique transparent on the system level, we need to restore the loop filter's order. To achieve this, we propose to add an extra compensating zero to the modulator's loop, somewhat similar to established excess loop delay (ELD) compensation techniques [15], [16]. Like with ELD-compensation, this zero can be implemented in several ways. However, for maximal generality, we add the zero to the forward loop filter H(s) as the factor $(1 + s\tau_c)$ shown in Fig. 7. Unfortunately, adding the zero in the forward filter path will still not suffice to preserve the system level behavior, since it will change the STF. As will become clear later on in section IV, the introduced compensating zero can be a lot lower than the clock frequency, which would significantly change the filtering characteristic of the STF. For full compensation, it is therefore necessary to add a low-pass filter in front of the loop, as was also done in [3] for a system with an NRZ-DAC. Fig. 7 shows the resulting proposed system. R_{in} represents the impedance level of the input branch. H(s) is the continuous-time loop filter of the modulator, which is conventionally implemented as a cascade of integrators with feedforward and/or feedback paths. $\mathrm{H_{eq}}(z)$

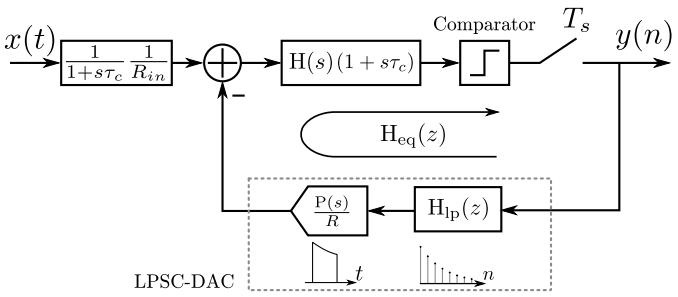


Fig. 7. System level diagram of CTSDM with LPSC-DAC and compensation.

is the corresponding equivalent discrete-time loop filter. In a typical top-down design of the modulator, first a desired NTF is synthesized, which leads to a desired $\mathrm{H_{eq}}(z)$ [17], [18]. Then, in a subsequent step the continuous-time filter $\mathrm{H}(s)$ needs to be calculated such that the loop with the DAC and the sampling implements the discrete-time filter $\mathrm{H_{eq}}(z)$. For the LPSC-DAC, the integrator coefficients of $\mathrm{H}(s)$ and the value of the zero τ_c are found by solving the following equation:

$$\mathrm{H_{eq}}(z) = [\mathrm{H}(s)(1 + s\tau_c)\,\mathrm{DAC}(s)]^* \tag{12}$$

Here the notation $[\ ]^*$ is used to represent the sampling operation as in [19] and [20]. The s-domain filter coefficients corresponding to the solution of this equation can be found by some numerical routine e.g. using the c2d and d2c functions in Matlab. It is also possible to derive exact closed form expressions for τ_c and the s-domain integrator coefficients, however these expressions are quite long even for moderate orders of $\mathrm{H_{eq}}(z)$. However, in practice, the value of τ should be relatively large (see below). In this case, we found that τ_c does almost not depend on $\mathrm{H_{eq}}(z)$, and can be well approximated as:

$$\tau \gg T_s, \quad T_1 \approx \frac{T_s}{2} \Rightarrow \tau_c \approx \tau \frac{1}{RC_s f_s + 1} \tag{13}$$

f_s is the sampling frequency: $f_s = \frac{1}{T_s}$. Fig. 8 shows a plot of τ_c together with the approximation of Eq. (13) for two different sizings of the loop filter as a function of the normalized analog filter bandwidth $\frac{T_s}{2\pi\tau}$. Here, the exact value of τ_c was calculated by numerically solving Eq. (12). Both considered loop filters were third order filters designed using the sigma delta toolbox [17] but with different values for the maximum NTF gain, H_∞: i.e. $H_\infty = 1.5$ and $H_\infty = 2$. C_s was chosen equal to $\frac{T_s}{R}$. Fig. 8 shows excellent correspondence between the approximation Eq. (13) and the exact value of τ_c, except for very high values of the normalized analog filter bandwidth. On the figure we have also indicated the practically useful range which corresponds to the range where the normalized analog filter bandwidth is smaller than $1/40$. As we will see below, this corresponds to oversampling ratios that are larger than 20, which is almost always the case for single bit $\Sigma\Delta$ modulators. For values of τ inside this range, the maximum error is within 1.5 %.

To understand this result, it is helpful to consider Fig. 9. It is a low frequency approximation of the circuit of Fig. 2, where the switched capacitor C_s has been replaced by its equivalent

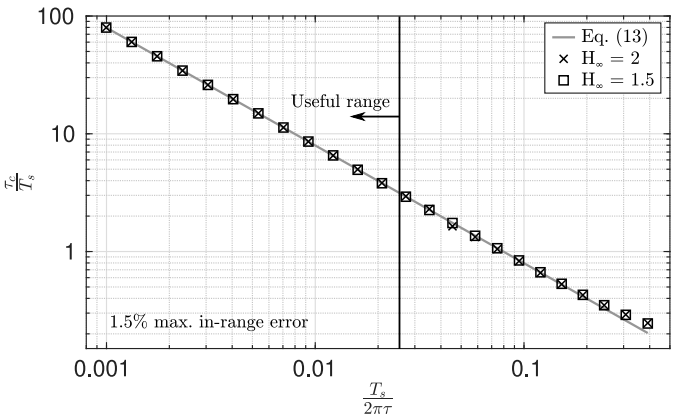


Fig. 8. Exact value of τ_c normalized to T_s and its approximation of Eq. (13) as a function of the normalized analog filter bandwidth $\frac{T_s}{2\pi\tau}$ for two different sizings of the loop filter.

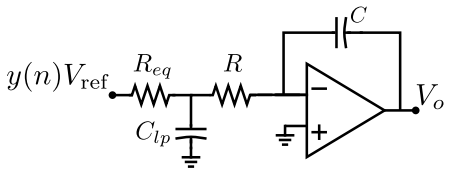


Fig. 9. Low frequency approximation of the circuit of Fig. 2.

resistor R_{eq} [21]:

$$R_{eq} = \frac{T_s}{C_s} \tag{14}$$

It is clear that R, R_{eq} and C_{lp} form a passive low-pass filter. Hence, in this approximation, the circuit collapses to the system of [3], shown on Fig. 1, where τ_c must be equal to the time constant τ_{eq} formed by R, R_{eq} and C_{lp}. This leads to:

$$\tau_c = \tau_{eq} = C_{lp}\frac{RR_{eq}}{R + R_{eq}} \tag{15}$$

Combining this with the approximation of Eq. (9) leads to Eq. (13).

It is important to note that the equivalent resistor analysis is only approximate: it helps in the intuitive understanding of the expression for τ_c but in reality the LPSC-DAC circuit of Fig. 2 performs its filtering in the discrete-time domain in front of the DAC. As a result, contrary to the system of Fig. 1, errors introduced at the DAC are reduced, as we will show in the following sections.

To complete the system level design, we need to find a sizing strategy for the LPSC-DAC's time constant τ. Ideally we would like an aggressive filter with a very large value of τ. As we will show in the next section however, if τ is chosen too large, the modulator's thermal-noise level will increase. To explore this trade-off, we need to look at the circuit level of the CTSDM.

IV. Circuit Implementation

Fig. 10 shows the single-ended representation of a circuit level implementation of the modulator of Fig. 7. The inverting

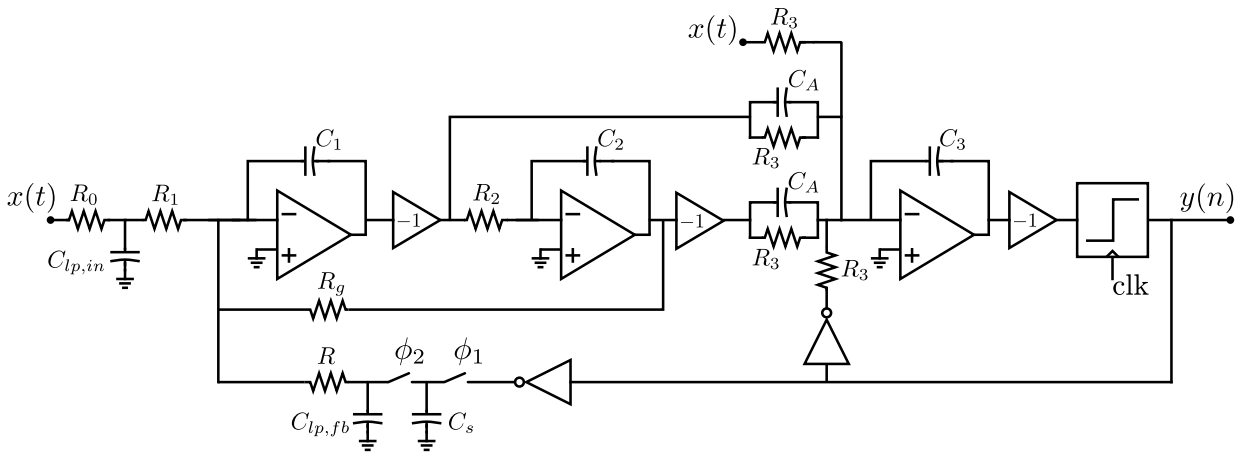


Fig. 10. 3rd order 1-bit CIFF-FB CTSDM with LPSC-DAC and compensation.

buffers represent the crossing of two differential wires. The modulator has a CIFF-FB loop filter, but it has the same STF as a CIFF-modulator because of the feed-in path to the third integrator. The signal swing at the output of the first integrator is also identical to the swing of the corresponding signal in a CIFF-loop filter. The additional low-pass filter in front of the modulator is implemented using the resistance of the first integrator and an additional capacitor $C_{lp,in}$. The extra zero $\frac{-1}{\tau_c}$ in the loop filter is realized with two extra capacitors at the input of the third integrator, labeled C_A on Fig. 10.

A. Noise

For the noise analysis we will focus on the resistors in the input branch, the LPSC-DAC and on the OpAmp of the first integrator. We will assume that the input referred contribution of all noise sources further in the loop filter are adequately suppressed by the gain of the first integrator. Also, we will neglect the contribution of the local feedback resistor R_g, since it is always much larger than R_{in}. Furthermore, we will assume that the modulator's STF has unity in-band gain. To guarantee this, the following requirement needs to be fulfilled:

$$R_{in} = R_0 + R_1 = R + R_{eq} \tag{16}$$

The switch driven by ϕ_1 on Fig. 10 introduces noise with a spectral density of $\frac{kT}{C_s \frac{f_s}{2}}$. From the perspective of the other switch, driven by ϕ_2, the capacitors C_s and C_{lp} are in series, which under the assumption that $C_s \ll C_{lp}$ means it introduces noise with the same spectral density as the first switch. As a result, the switched capacitor C_s introduces the same baseband noise as its equivalent resistance R_{eq}. We can therefore approximate the in-band mean square noise voltage, by replacing the switched capacitor C_s with its low frequency equivalent resistance R_{eq}, which greatly simplifies the following analysis. This also means that we neglect aliasing of out-of-band OpAmp or resistor noise, but as we will show in section VI, the LPSC-DAC is quite robust against aliasing such that this approximations is justified.

For frequencies above the low-pass filter cut-off frequency, the input referred noise contributions of R_1, R and the OpAmp are amplified, because these noise components are injected after the low-pass filter. Hence, the low-pass filter's bandwidth should not become too small, to avoid that the modulator's thermal in-band noise would increase. We will assume $\tau \gg T_s$ to obtain accurate and concise analytical expressions for the noise behavior. This corresponds to the expected worst case noise behavior and it allows to make use of Eq. (13).

After a straightforward calculation, the following expression can be found for the in-band noise voltage variance, from the input resistors and the LPSC-DAC (in a differential design):

$$\overline{V^2}_{R,LPSC} = 4kTB4R_{in}\left[1 + \frac{(2\pi B\tau_c)^2}{3}\left(\frac{R_{in}}{2R_1} + \frac{R_{in}}{2R}\right)\right] \tag{17}$$

T represents the temperature in Kelvin, k is Boltzmann's constant, and B stands for the modulator's bandwidth. The modulator's in-band, input referred mean square noise voltage due to white noise of the OpAmp can be approximated as follows, again assuming $\tau \gg T_s$ and provided the first integrator has high in-band gain:

$$\overline{V^2}_{OA,LPSC} \approx \frac{4}{3}\frac{4kTB}{g_m}\left[4 + \frac{(2\pi B\tau_c)^2}{3}\left(\frac{R_{in}}{R_1} + \frac{R_{in}}{R}\right)^2\right] \tag{18}$$

Here, we assumed that two differential pair transistors with transconductance g_m dominate the OpAmp's noise. For ease of comparison, we also present the noise for a reference modulator with the same impedance level, but using a regular switched resistor NRZ-DAC:

$$\overline{V^2}_{R,ref} = 4kTB4R_{in} \tag{19}$$

$$\overline{V^2}_{OA,ref} \approx 4\frac{4}{3}\frac{4kTB}{g_m} \tag{20}$$

Again we assumed high in-band gain for the first integrator and a noise dominant transistor pair in the OpAmp.

To verify these analytical results, we performed a case study on a typical SDM designed using Schreier's $\Delta\Sigma$-toolbox [17], [18], for an over-sampling ratio of 50 and an NTF H_∞ value of 1.5. The resulting discrete-time loop

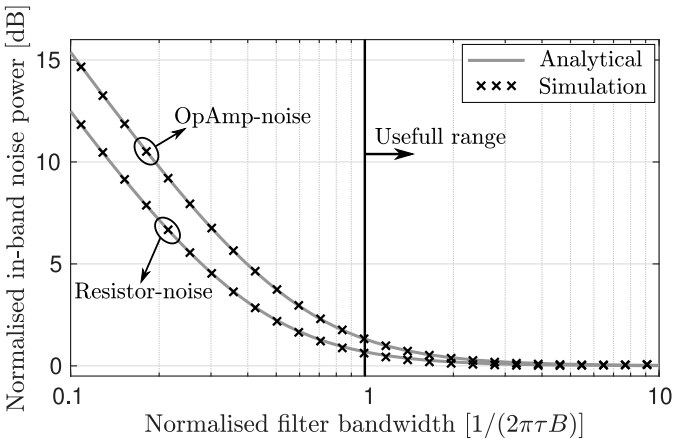


Fig. 11. In-band noise power generated by the first OpAmp and the input resistors of the circuit of Fig. 10, for swept LPSC-DAC bandwidth. Normalized to corresponding noise power in a modulator using NRZ-DAC.

filter $\mathrm{H_{eq}}(z)$ is shown in table I. For this modulator prototype, we investigated the noise performance over a range of varying values of τ. For every value of τ, the corresponding loop filter parameters ($\mathrm{H}(s)$ and τ_c) were calculated by numerically solving Eq. (12). Here, all input resistors (R_0, R_1, R and R_{eq}) were chosen equal to minimize the size of $C_{lp,in}$ and $C_{lp,fb}$. The results are summarized in Fig. 11 which shows the contribution to the total in-band noise power of both the input resistors as well as the first OpAmp, as a function of τ. Both contributions are normalized to their corresponding level in a conventional CTSDM with NRZ-DAC, i.e. Eqs. (19) and (20). As can be seen, the analytical approximations match perfectly with the simulations. It is also clear that choosing the LPSC-DAC's bandwidth too low will dramatically increase the noise level of the modulator. However for this OSR there is a large range for τ, where the noise level remains unchanged and remains identical to the noise level for an NRZ-DAC.

Based on this analysis, we decided to choose the value of τ such that the resulting increase of thermal noise is not more than 1 dB. For this, we define $g_{m,min}$ as the noise optimal g_m value which is such that the OpAmp generates the same amount of noise as the input resistors. This leads to the following noise limited sizing:

$$g_m = g_{m,min} = \frac{4}{3}\frac{1}{R_{in}}, \quad R = R_1 = \frac{R_{in}}{2}, \quad \tau = \frac{1}{\frac{5}{4}2\pi B} \tag{21}$$

The total noise increase with this sizing is only 0.93 dB. With regard to finding the value of the compensation time constant τ_c, we found that the approximation of Eq. (13) is very accurate for this sizing of τ. All the corresponding modulator parameters are listed in table I, and will be used for the remaining simulations.

B. Slewing

Even though the bandwidth of the low-pass filter is limited by noise considerations, it is still very effective in reducing the required output current. Fig. 12 shows a first simulation result for the output current of the first OpAmp in the loop filter, both for a modulator with an LPSC-DAC and a modulator with an

TABLE I

PARAMETERS OF THE THIRD ORDER CTSDM USED IN THE SIMULATIONS AND DEPICTED ON FIG. 7

$\mathrm{H_{eq}}(z) = 0.7998\frac{z^2-1.31z+0.5556}{(z^3-2.998z^2+2.998z+1)}$	$\tau_c \approx \tau\frac{R_{eq}}{R+R_{eq}}$	$\mathrm{OSR} = 50$
$\mathrm{H}(s) = \frac{0.6745f_s}{s}\frac{s^2+0.3617f_s s+0.068f_s^2}{s^2+0.0024f_s^2}$	$\tau = \frac{80}{2\pi f_s}$	$H_\infty = 1.5$

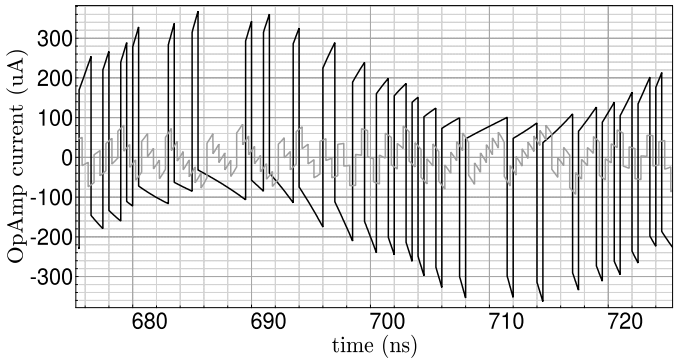


Fig. 12. OpAmp output current for modulator with NRZ (black) and LPSC-DAC (gray).

NRZ-DAC. The OpAmps were ideal for this simulation and the input signal was a -3 dBfs sine wave with a frequency at the edge of the modulator's bandwidth, $\frac{f_s}{100}$. Both modulators had the discrete-time equivalent loop filter shown in table I. The simulation clearly shows that the total current level at the output of the first OpAmp is heavily reduced by using an LPSC-DAC.

For better comparison with existing filtering techniques, we also designed a modulator with a FIR-DAC [5], [6], [8], [9]. We choose a FIR-filter with four equal taps, and its effect on the loop filter has been compensated such that the equivalent discrete-time loop filter $\mathrm{H_{eq}}(z)$ remains unchanged.

This required adding a FIR-DAC in the inner feedback path of the modulator and recalculating the integrator coefficients. For a second set of simulations, we implemented the OpAmp of the first integrator of both modulators (FIR-DAC and LPSC-DAC) using a macro-model of a single stage OpAmp, whose output current is a non-linear function of its differential input voltage according to the well-known square law Fet-model:

$$\begin{cases} I_{out} = -I_d & \frac{g_m V_{in}}{I_d} < -\sqrt{2} \\ I_{out} = g_m V_{in}\sqrt{1-\left(\frac{V_{in}g_m}{2I_d}\right)^2} & \left|\frac{g_m V_{in}}{I_d}\right| < \sqrt{2} \\ I_{out} = I_d & \frac{g_m V_{in}}{I_d} > \sqrt{2} \end{cases} \tag{22}$$

We also added an output impedance equal to $\frac{100}{g_m}$, to ensure a fixed 40 dB DC-gain. To assess the efficiency of our technique, we investigated the case where the OpAmp is squeezed into its ultimate noise limited sizing. Two quite extreme sizings of g_m were examined: i.e. $g_{m,min}$ and $2g_{m,min}$. The loop gain of the feedback OpAmp circuit is very low at such a low value of g_m. This affects the time constant of the integrator and the input impedance at the OpAmp inverting terminal.

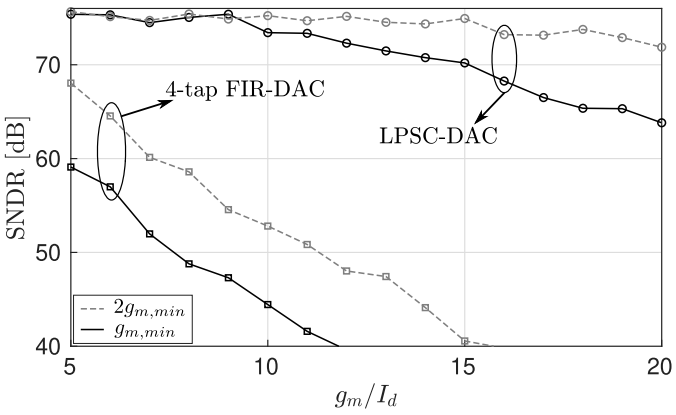


Fig. 13. Simulated SNDR for a modulator with an LPSC-DAC and another modulator with a four-tap FIR-DAC. Both modulators where sized to have the Z-domain loop filter of table I. The first OpAmp is a macro-model of a simple differential pair with varying g_m and g_m/I_d and fixed 40 dB DC-gain.

To correct these effects, we rescaled the integrating capacitor, such that the poles and zeros of the modulator's loop filter remain unaffected [22], [23]. This also required rescaling the low-pass capacitors $C_{lp,fb}$ and $C_{lp,in}$, and adding a resistor in series with the integrating capacitor to cancel the feed-forward zero of the integrator. We ran a batch of simulations on this circuit. The input signal frequency was set at a fourth of the modulator's bandwidth. The quantizer was dithered to reduce limit cycles. We varied the $\frac{g_m}{I_d}$ of the transistors in the differential pair, and for all values the SNDR of the two modulators was simulated with a -3 dBfs input signal. The results are shown on Fig. 13. The top two lines represent the simulated SNDR values of the LPSC-DAC modulator, for both g_m values. It can be observed that the LPSC-DAC modulator's performance is only degraded for high values of $\frac{g_m}{I_d}$ (and hence very small current levels). This illustrates the relaxed slew rate requirement of the LPSC-DAC, as well as its ability to cope with a high impedance nullator node.

The bottom two lines on Fig. 13 show the results for the modulator with a four-tap FIR-DAC. It is clear that the SNDR is heavily limited by slewing, and all SNDR values are worse than the values for the modulator with the LPSC-DAC. This indicates that a four-tap FIR-DAC is not as efficient as an LPSC-DAC in reducing slewing requirements. One could think of increasing the number of FIR-DAC taps to improve the FIR-DAC performance, but this also increases several undesirable effects as described in [8]. The two most important issues are the following. First, the number of resistors in the FIR-DAC goes up with the order n, as do the size of these resistors, such that their combined chip area increases as n^2, as well as their total parasitic capacitance on the nullator node of the integrator. Second, increasing the order of a FIR-DAC also increases the signal swing of the modulator's input signal related component at the output of the first integrator in the loop filter. The reason for this is that the FIR filter adds phase shift in the feedback path, which leads to reduced cancellation of the modulator's input signal with the input signal component in the modulator's feedback signal. A modulator with an LPSC-DAC and the proposed compensation technique does not suffer from this drawback since it filters in both the feedback and the input branch. To asses this effect, we investigated our test vehicle modulator of table I for the case of a FIR-DAC. We found that for a full scale input signal, the signal swing at the output of the first OpAmp, was more than double when using a four-tap FIR-DAC compared to an LPSC-DAC implementation. Moreover, this signal swing was even further increased for FIR-DACs with more than four taps, as the reduction in quantization noise due to increased filtering was not enough to compensate for the increased swing of the input signal component. At this point we should note that the LPSC-DAC also suffers from an area penalty. This is mainly due to the added low-pass capacitors $C_{lp,in}$ and $C_{lp,fb}$. Actually in practice these additional capacitors will typically be the largest capacitors in the overall circuit. Therefore, in a differential design they should be implemented as fully differential capacitors between the differential lines, which saves a factor 4 relative to implementing each of them as 2 separate capacitors to ground in each of the differential branches. To give a numerical idea of the actual area overhead we can refer to our previous work [3], which is a 3rd order single bit design (of similar complexity as Fig. 10), with 12-bit resolution and 20 MHz bandwidth in 65 nm CMOS. If we would modify this design to incorporate the proposed LPSC-DAC, we estimate that the resulting circuit would have a total active area around 0.01 mm^2. The low-pass filtering capacitors, $C_{lp,in}$ and $C_{lp,fb}$, would occupy around 15 % of this area.

Finally, an important side comment is that the FIR-DAC approach is orthogonal to the proposed LPSC-DAC approach. Hence, it is relatively straightforward to combine them, which could be beneficial (e.g. at a different OSR than the one used for our simulations). Note that to implement an n-tap FIR filter with LPSC-DACs, n low-pass filtering capacitors are needed, whose size is n times smaller compared to a single LPSC-DAC, meaning that the total capacitor area to implement the LPSC-DAC technique is essentially independent of the FIR-DAC order.

Lastly, we also simulated a modulator with an NRZ-DAC, without any filtering technique. All SNDR values were lower than 50 dB and heavily limited by slewing, confirming that some kind of filtering or current reducing technique is necessary in 1-bit modulators to obtain a power efficient design.

C. Variability

Eq. (15) shows that the proposed compensation technique consists of matching an RC time constant with a time constant implemented with both a switched capacitor and an ordinary resistor. Since PVT-variations [12], [23], [24] have a different impact on the switched capacitor than on the resistors, they will result in mismatch between these time constants. PVT-variations will also cause a mismatch between the equivalent resistance of the two input branches of the first integrator. If the equivalent resistor formed by the switched capacitor C_s no longer matches the other resistors, Eq. (16) will no longer be fulfilled. As a result, the DC-gain of the STF will no longer be unity. We performed simulations on the design of table I

TABLE II
PEAK SNDR FOR SEVERAL CORNERS FOR THE MODULATOR OF FIG. 7 WITH PARAMETERS IN TABLE I, AS WELL AS A COMPARABLE MODULATOR WITH AN NRZ-DAC

	Nominal	Fast	Slow
Peak SNDR LPSC	75.5 dB	69.45 dB	72.29 dB
Peak SNDR NRZ	75.5 dB	1.2 dB	68.47 dB

to illustrate the sensitivity of the compensated LPSC-DAC scheme to PVT-variations. R and R_{eq} were chosen equal. As well as the nominal case, a fast and a slow corner were simulated, meaning that all RC time constants were respectively decreased and increased with 30 %. The peak SNDR was determined for every corner by simulating with several input signal amplitudes. For reference, a conventional CTSDM with a switched-resistor NRZ-DAC but the same discrete-time loop filter, was also simulated under fast and slow corners. Table II shows the results. The simulations show that the modulator with LPSC-DAC is actual more robust against time constant variations than the reference modulator with NRZ DAC. In fact for this design the reference modulator is unstable in the fast corner, while the modulator with LPSC-DAC remains functional. This can be explained by again referring to Fig. 9, showing the low frequency approximation of the LPSC-DAC together with the first integrator. The time constant of the integrator in this circuit is given by

$$\tau_{int} = \frac{C(1 + RC_s f_s)}{C_s f_s} \tag{23}$$

In a conventional RC-integrator, a change of 30 % in RC time constants directly translates into a 30 % change of the time constant in the loop filter. However because half of the resistance is implemented as a switched capacitor in this design, a 30 % change of RC-time constants results in only 15 % deviation on the integrator's time constant. This inherent compensation effect seems to be more important than any negative effect on the modulator's stability caused by mismatch between the LPSC-DAC's pole and the compensating zero.

V. JITTER

Jitter is an important issue in one-bit CTSDMs. Since one-bit DACs have full scale pulses, deviations in the pulse-widths result in large error signals. It is therefore necessary to analyze this behavior. We start by examining the effect of jitter on an isolated LPSC-DAC, after which we will consider a CTSDM in its entirety.

A. Jittered LPSC-DAC

Consider a jittered clock signal, whose rising edges occur at the following time instants:

$$t_r(n) = (n + j(n))T_s, \quad n \in \mathbb{N} \tag{24}$$

Where $j(n)$ is a stochastic process whose power spectral density (PSD) is not necessarily white. In fact, a clock signal generated by a PLL usually has low-pass jitter [25]. We assume $j(n)$ has a variance σ_j^2 and a zero mean, such that T_s represents the effective clock period. If a DAC, with a given input signal $y(n)$, is driven by a jittered clock, its output pulses will be different from those generated by the same DAC driven by an ideal jitterless clock. We call the difference between those two outputs the "jitter-caused error", and we will model it as an additive error.

To determine this error, we will again assume that $C_{lp} \gg C_s$ such that the exponential decay of the LPSC-DAC pulses is constant during one clock cycle (see discussion in section II). This means that only jitter on the rising edge of ϕ_2 results in an error. Jitter will change both the width and the timing of the exponential pulses. The pulses without jitter have a fixed exponential decay, γ, but by changing the pulse-width, the decay now varies from cycle to cycle. We call this jitter dependent decay $\gamma_j(n)$:

$$\gamma_j(n) = \gamma\, e^{-T_s \frac{j(n)-j(n-1)}{\tau}} \tag{25}$$

The discrete-time filter $\mathrm{H_{lp}}(z)$, becomes a time-varying filter because of jitter. We examine its output $v(n)$ (defined in section II), assuming $y(n)$ and $j(n)$ are zero for $n < 0$:

$$v(n) = \alpha \sum_{k=0}^{n} y(n-k)(1-\alpha)^k \prod_{l=0}^{k-1} \gamma_j(n-l) \tag{26}$$

$$= \alpha \sum_{k=0}^{n} y(n-k)[\gamma\,(1-\alpha)]^k e^{-T_s \frac{j(n)-j(n-k)}{\tau}} \tag{27}$$

Taking into account the effect of jitter on the timing and exponential decay of the pulses leads to the following expression for the output current of the jitter affected LPSC-DAC:

$$i_R(t) = \frac{1}{R} \sum_{n=0}^{\infty} \big(v(n) - \gamma_j(n) v(n-1)\big)\, p_e(t - (n + j(n))T_s) \tag{28}$$

$$p_e(t) = H_e(t - T_1) e^{-\frac{t-T_1}{\tau}} \tag{29}$$

$H_e(t)$ represents the Heaviside function. i_R is the current injected in the first integrator by the LPSC-DAC (see Fig. 2). Similar to the approach in [26], we will approximate the jitter-caused error with a first-order Taylor series. This is accurate, since jitter is typically small, and it allows us to model the effect of jitter as an additive error. This results in:

$$i_R(t) \approx i_R(t)|_{j=0} + \sum_{k=0}^{\infty} j(k) \left.\frac{d i_R(t)}{d j(k)}\right|_{j=0} \tag{30}$$

$$= i_{R,0}(t) + i_{R,j}(t) \tag{31}$$

$i_{R,j}(t)$ represents the jitter caused error, while the LPSC-DAC's output in the absence of jitter is represented by $i_{R,0}(t)$. Combining Eqs. (27), (28) and (30) gives us an expression for $i_{R,j}(t)$, as shown at in Eq. (32) at the bottom of the next page. $p_e'(t)$ represents the derivative with respect to time of the exponential pulse $p_e(t)$ and $v_0(n)$ is the output signal of the discrete-time filter $\mathrm{H_{lp}}(z)$ in the absence of jitter. Fig. 14 shows a signal flow diagram of Eq. (32).

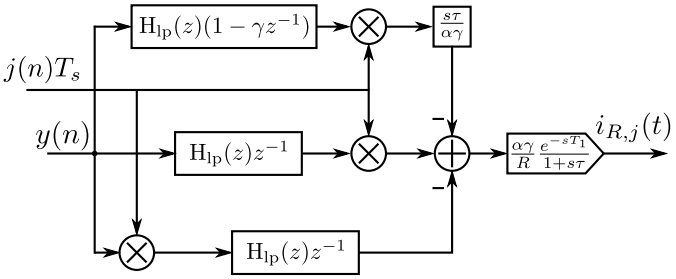


Fig. 14. Graphical representation of Eq. (32), the approximated jitter error at the output of the LPSC-DAC.

B. Jittered Modulator

If a CTSDM is driven by a jittered clock, this will result in errors at the sampler and at the DAC. Errors introduced at the sampler are usually neglected during jitter analysis, since they are shaped out of band by the NTF, in a similar manner as quantization noise [26]–[31]. Errors introduced at the DAC however are shaped by the STF, since they are injected at the modulator's input, and they can cause a significant error component in the modulator's output signal:

$$y(n) = y_j(n) + y_0(n) \tag{33}$$

$y_j(n)$ represents the jitter-caused error component in the modulator's output signal, while $y_0(n)$ is the output signal of the modulator driven by a perfect jitter-less clock. Since the jitter caused error introduced at the DAC itself depends on $y(n)$, finding the jitter noise at the modulator's output requires solving a non-linear equation. However, the jitter induced error at the DAC is quite small, so we can neglect higher order contributions to the jitter noise $y_j(n)$, and assume that $i_{R,j}(t)$ only depends on $y_0(n)$. This linearizes the problem and allows us to consider the effect of jitter on the CTSDM as an additive error. The same approach has been followed in previous publications considering NRZ-DACs [29]–[31]. By referring the jitter-induced error current to the input of the modulator of Fig. 7, and filtering by the STF, we obtain the following expression for $y_j(n)$:

$$y_j(n) = i_{R,j}(t) \circledast \mathcal{L}^{-1}\left\{R_{in}(1+s\tau_c)\,\mathrm{STF}(s)\right\} \tag{34}$$

$\circledast$ stands for the convolution operator, while $\mathcal{L}^{-1}$ indicates the inverse Laplace-transform. Using this expression, we arrive at the power spectral density (PSD) of the jitter caused error at the modulator's output:

$$S_{y_j}(\omega) \approx \frac{1}{2\pi}\int_{-\pi}^{\pi}\left[S_{y_0}(\nu)S_j(\omega-\nu)\left|\mathrm{TF}(\omega,\nu)\right|^2\right]d\nu \tag{35}$$

$S_{y_0}(\omega)$ is the PSD of $y_0(n)$, the modulator's output in the absence of jitter. $S_j(\omega)$ represents the PSD of $j(n)$. $\mathrm{TF}(\omega,\nu)$ is shown page wide in Eq. (36), as shown at the bottom of the page. We approximated the STF as unity, since we are only interested in the in-band jitter-caused noise. If $S_j(\omega)$ and $S_{y_0}(\omega)$ are known, this expression allows us to accurately calculate the jitter caused noise at the modulator's output.

In the conventional linearized model of a CTSDM, $y_0(n)$ consists of two components; shaped quantization noise and an input signal related component. Similarly, modulation due to jitter will cause two additional error components in the modulator's output signal; one related to modulation of the quantization noise, $y_{j,q}(n)$ and an input signal related component, $y_{j,x}(n)$.

$$y_j(n) = y_{j,q}(n) + y_{j,x}(n) \tag{37}$$

The input signal modulation, $y_{j,x}(n)$, is fundamentally tied to sampling with jitter, and it causes a skirt around the input tone, regardless of the shape of the DAC pulse [27], [28]. We will therefore focus on the modulated quantization noise component. If we assume that the quantization noise and the input signal are uncorrelated, we can calculate the PSD of the modulated quantization noise component in the CTSDM's output signal in a straightforward way by replacing $S_{y_0}(\omega)$ in Eq. (35) with the PSD of the shaped quantization noise, leading to:

$$S_{y_{j,q}}(\omega) = \frac{\sigma_q^2}{2\pi}\int_{-\pi}^{\pi} S_j(\omega-\nu)\left|\mathrm{TF}(\omega,\nu)\,\mathrm{NTF}(z)\right|^2_{z=e^{j\nu}}d\nu \tag{38}$$

σ_q^2 represents the variance of the white quantization noise. For a modulator with a high OSR, the in band jitter error related to the quantization noise can be well approximated by its value at DC:

$$\begin{aligned} S_{y_{j,q}}(\omega) &\approx S_{y_{j,q}}(0) \\ &= \frac{\sigma_q^2}{2\pi}\int_{-\pi}^{\pi}\left[S_j(\nu)\left|\mathrm{TF}(0,\nu)\,\mathrm{NTF}(z)\right|^2\right]_{z=e^{j\nu}}d\nu \end{aligned} \tag{39}$$

Here,

$$\mathrm{TF}(0,\nu) = \frac{\gamma\,R_{in}}{R}\alpha\gamma\left[\mathrm{H_{lp}}(z)z^{-1} - \mathrm{H_{lp,DC}}\right]_{z=e^{j\nu}} \tag{40}$$

$$\begin{aligned} i_{R,j}(t) = -\frac{T_s}{R}\sum_{n=0}^{\infty}\left(v_0(n)-\gamma\,v_0(n-1)\right)j(n)\,p_e'(t-nT_s) \\ +\frac{\alpha^2\gamma\,T_s}{R\tau}\sum_{n=0}^{\infty}\sum_{k=0}^{n-1}y(n-k-1)(\gamma\,(1-\alpha))^k(j(n)-j(n-k-1))\,p_e(t-nT_s) \end{aligned} \tag{32}$$

$$\mathrm{TF}(\omega,\nu) = \frac{R_{in}}{R}\frac{1+j\omega\tau_c}{1+j\omega\tau}\left[\mathrm{H_{lp}}(z)(z^{-1}\alpha\gamma\,-(1-\gamma\,z^{-1})j\omega\tau) - \alpha\gamma\,H_{lp}(e^{j\omega})e^{-j\omega}\right]_{z=e^{j\nu}} \tag{36}$$

We can further simplify Eq. (39) by observing that the NTF is very small at in-band frequencies. This means that the integration over ν in Eq. (39) will mainly be determined by out of band values of ν. We can use this to further simplify TF(0, ν) by its high frequency value. Since the factor H_{lp} is a first-order low-pass filter with cut-off angular frequency $1/\tau_c$, the factor $[\mathrm{H_{lp}}(z)z^{-1} - \mathrm{H_{lp,DC}}]$ can be considered constant above $1/\tau_c$.[1] This means that in the expression of Eq. (39), the following approximation can be made:

$$\mathrm{TF}(0,\nu) \approx \frac{\gamma R_{in}}{R}\alpha\gamma\left[\mathrm{H_{lp}}(z)z^{-1} - \mathrm{H_{lp,DC}}\right]_{z=-1} \tag{41}$$

Now, by using, $\alpha \approx \frac{T_s R}{\tau R_{eq}}$ and $\gamma \approx 1 - \frac{T_s}{\tau}$, and neglecting lower order terms in τ, we obtain:

$$\mathrm{TF}(0,\nu) \approx \frac{T_s R}{\tau R_{eq}} \tag{42}$$

Which allows to establish the following simplified expression for the in band jitter induced noise spectral density:

$$S_{y_{j,q}}(\omega) \approx \left|\frac{T_s R}{\tau R_{eq}}\right|^2 \frac{\sigma_q^2}{2\pi}\int_{-\pi}^{\pi} S_j(\nu)\left[\left|\mathrm{NTF}(z)\right|^2\right]_{z=e^{j\nu}} d\nu \tag{43}$$

We can compare the approximation of Eq. (43) with the modulated quantization noise of a CTSDM using a conventional NRZ-DAC [30], [31]:

$$S_{y_{j,q},NRZ}(\omega) = \frac{\sigma_q^2}{2\pi}\int_{-\pi}^{\pi} S_j(\omega-\nu)\left|(1-z^{-1})\,\mathrm{NTF}(z)\right|^2_{z=e^{j\nu}} d\nu \tag{44}$$

For an NRZ-DAC, the NTF is differentiated before modulation. This differentiation has gain for the frequencies where the NTF is high, leading to increased jitter noise. By compensating this differentiation with low-pass filtering, the LPSC-DAC reduces quantization noise modulation. It is clear that the LPSC-DAC will strongly reduce the total amount of in-band jitter-caused modulated quantization noise for large τ. Lastly, the power spectral density of the jitter-modulated quantization noise of a modulator with a FIR-DAC is given by:

$$S_{y_{j,q},FIR}(\omega) = \frac{\sigma_q^2}{2\pi}\int_{-\pi}^{\pi} S_j(\omega-\nu)\left|F(z)(1-z^{-1})\,\mathrm{NTF}(z)\right|^2_{z=e^{j\nu}} d\nu \tag{45}$$

Here $F(z)$ represents the FIR-DAC's transfer function. We have only taken into account the jitter noise of the outer FIR-DAC, and neglected the contribution of the inner compensating FIR-DAC.

C. Simulation

We performed comparative simulations for our prototype 3rd order modulator (see table I), both for the LPSC-DAC version of Fig. 10 as well as for a similar circuit with a four-tap FIR-DAC with inner compensating FIR-DAC. For these simulations, we only applied jitter at the outer DAC (either LPSC or FIR). We considered first-order shaped jitter with bandwidth f_j, similar as in [31]. The jitter standard deviation was chosen (unrealistically) high, $\sigma_j = 4.5$ %, so the jitter noise dominates over the quantization noise. We applied a very small input signal so that the modulator's in-band noise is dominated by the jitter-modulated quantization noise rather than the jitter-modulated input signal, the former being the main focus of the above analysis. We swept the bandwidth of the clock jitter, $j(n)$, while keeping the jitter variance constant, and calculated the modulators' dynamic range, both through simulation and analytically. In the simulation, as before, we added dither to get rid of limit cycles. For the modulator with an LPSC-DAC, we used the analytical expressions of both Eq. (35) as well as the more simplified approximation of Eq. (43) to calculate the dynamic range. For the modulator with a FIR-DAC, the analytical expression of Eq. (45) is used.

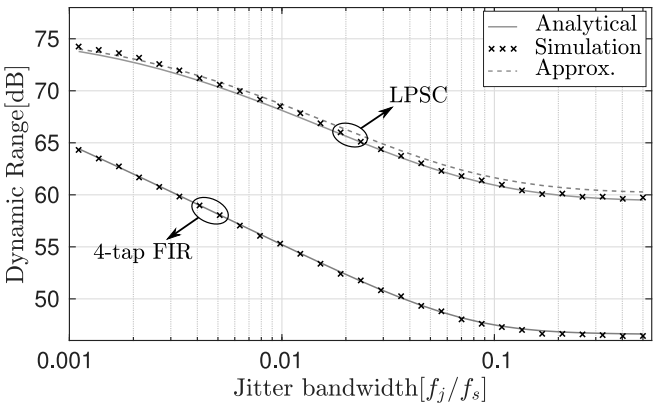


Fig. 15. Simulated and analytically derived Dynamic range for modulators with four-tap FIR-DAC & LPSC-DAC for several jitter-bandwidths.

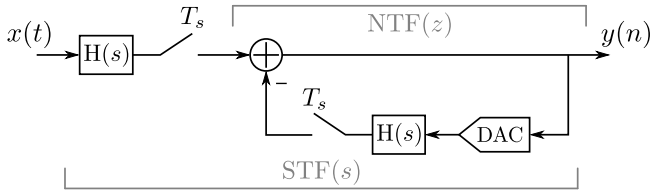


Fig. 16. Linearized CTSDM without quantization noise.

The resulting plot, Fig. 15, shows excellent correspondence between the simulation results and the analytically derived values. The simple approximation is also quite accurate. From Fig. 15 it is clear that the considered LPSC-DAC modulator has less jitter caused-modulation of the quantization noise, over all simulated jitter bandwidths, than the example design using a four-tap FIR-DAC. Of course the jitter performance of the FIR-DAC will improve as the number of taps goes up, but as we stated in section IV, there are limitations on the order of the FIR filter. Again, for certain designs with stringent jitter requirements, it might be interesting to combine an LPSC-DAC with an FIR-DAC.

VI. Anti-Aliasing Filtering

A. Analysis

CTSDMs are known to exhibit good anti-aliasing filtering. This can be explained by considering Fig. 16. It shows a model of a CTSDM where the sampler and the loop filter have been shifted in front of the summation. This transformed diagram

[1]This can be understood by using the following omega domain approximations $H_{lp} \approx \mathrm{H_{lp,DC}}/(1 + j\omega\tau_c)$ and $1 - z^{-1} \approx j\omega T_s$

is strictly equivalent to the original diagram because filtering and sampling are linear operations. The only non-ideality is the omission of the quantizer, which we have simply linearized as a unity gain. This is justified because in this analysis, we focus on the STF and hence quantization noise is not taken into account.

The system of Fig. 16 contains two samplers, one in front of the loop, and one in the feedback path. The sampler, filter and DAC in the feedback path form a system with a digital input and a digital output. The corresponding loop filter is the modulator's equivalent discrete-time loop filter $\mathrm{H_{eq}}(z)$. By inspection, we immediately obtain for this system the following well known expression:

$$Y(z) = [\mathrm{H}(s)X(s)]^* \frac{1}{1+\mathrm{H_{eq}}(z)} = [\mathrm{H}(s)\,\mathrm{NTF}(z)X(s)]^*$$

Here, as before the notation $[\ ]^*$ is used to represent the sampling operation [19]. This can be interpreted in the sense that the input signal is filtered by the signal transfer function STF and subsequently is sampled:

$$\mathrm{STF}(s) = \left.\frac{\mathrm{H}(s)}{1+\mathrm{H_{eq}}(z)}\right|_{z=e^{sT_s}} = \mathrm{H}(s)\,\mathrm{NTF}(z)|_{z=e^{sT_s}} \quad (46)$$

Since the NTF, has notches around integer multiples of the sampling frequency f_s, the STF will also have these notches, which means it provides excellent anti-aliasing filtering.

It is well known that using a switched capacitor digital to analog converter (SC-DAC [14]) in combination with unavoidable OpAmp non-idealities degrades this anti-aliasing behavior [32]. With an SC-DAC, the loop filter $\mathrm{H}(s)$ will become a linear periodically time-varying filter, which causes aliasing. Since the SC-DAC is connected to the input of the loop filter, aliasing will occur *before* the input signal enters the loop. These in-band aliased components enter the modulator directly at its input and therefore appear (unsuppressed) at the output. As a result, this aliasing mechanism is virtually independent of the rest of the modulator loop filter, as long as the STF has a signal band gain close to unity. Only the loop filter's input circuit is important. In [32], this aliasing mechanism is analyzed extensively and it is shown that the anti-aliasing performance of a CTSDM with a straight SC-DAC is catastrophically affected. For this reason, and also to limit the slew-rate of the DAC-pulse, a resistor should be added in series with the switched capacitor to improve anti-aliasing filtering, resulting in a switched capacitor resistor-DAC (SCR-DAC). Unfortunately this deteriorates the jitter performance in an unfavorable trade-off.

We expect the LPSC-DAC to offer far improved anti-aliasing performance compared to an SC(R)-DAC, when used in a CTSDM. The reasons are as follows. Firstly the input signal is filtered by a simple passive low-pass filter before it is connected to the time-variant LPSC-DAC. Secondly, the switched capacitor C_s is separated from the loop filter with the relatively large resistor R, which is not switched. Furthermore, C_s is placed in parallel with the large fixed capacitor C_{lp}, hence the total capacitance variance over time remains limited.

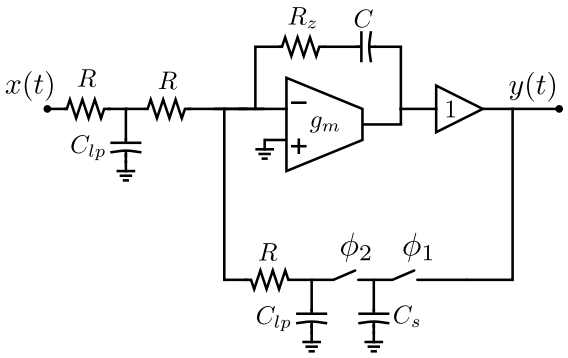


Fig. 17. The linearized first-order modulator with LPSC-DAC used to analyze aliasing.

Based on the state-space analysis techniques explained in [32], we performed an approximate analytical study of the aliasing from f_s to DC, for the case of our LPSC-DAC. As explained above, for the considered aliasing mechanism only the input stage matters and the overall modulator architecture is not so important. We therefore performed our study on the greatly simplified circuit shown on Fig. 17. Here, as in [32], the modulator is simplified into a first-order version and the quantizer is linearized. Moreover the sampler in the forward path is removed to reduce the number of states. Instead the output signal is directly sampled on C_s at the falling edge of ϕ_1, which also removes the feedback delay of the modulator. The resistors in the LPSC-DAC are chosen equal and a large value of τ is assumed. The OpAmp is modeled as a simple transconductance g_m as in [32]. In this circuit, the compensating zero τ_c is implemented through the feedback resistor R_z. We chose $C = \frac{1}{f_s R_{in}}$, to further simplify the analysis. Our test vehicle's sizing is summarized as:

$$R_{in} = 2R, \quad C_s = \frac{1}{Rf_s}, \ \tau_c \approx \frac{RC_{lp}}{2}, \ R_z = \frac{\tau_c}{C} \quad (47)$$

After a straightforward application of the state-space technique described in [32], we obtain the following expression for the direct aliasing from f_s to DC:

$$\left|\frac{\mathrm{STF}(f_s)}{\mathrm{STF}(0)}\right| \approx \frac{1}{2}\frac{1}{(g_m\frac{R_{in}}{4}+1)(2\pi RC_{lp}f_s)^2} \quad (48)$$

Examining this result, we see that the aliased components are suppressed by the loop gain of the feedback OpAmp circuit implementing the first integrator. This loop gain (at high frequency) is given by $g_m\frac{R_{in}}{4}$. Additionally, aliasing is heavily suppressed by the *square* of the high-frequency attenuation of the passive low-pass filter.

B. Simulation

We performed circuit level simulations on three CTSDMs; one with an LPSC-DAC another with an SCR-DAC and a third with a FIR-DAC. Again all modulators have the equivalent discrete-time loop filter shown in table I. The modulators with FIR-DAC and LPSC-DAC are identical to those used for the simulations in section IV and V. The time constant of the SCR-DAC was chosen to be $0.2T_s$. For this value, the SCR-DAC modulator has a comparable jitter performance as the LPSC-DAC modulator, and markedly worse slewing

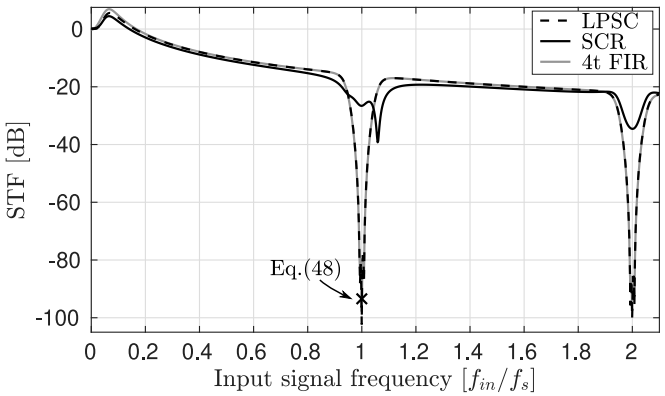


Fig. 18. Simulated STF of three modulators with different DACs, with $g_m = 10g_{m,min}$ in the first OTA. The approximation of Eq. (48) is also shown.

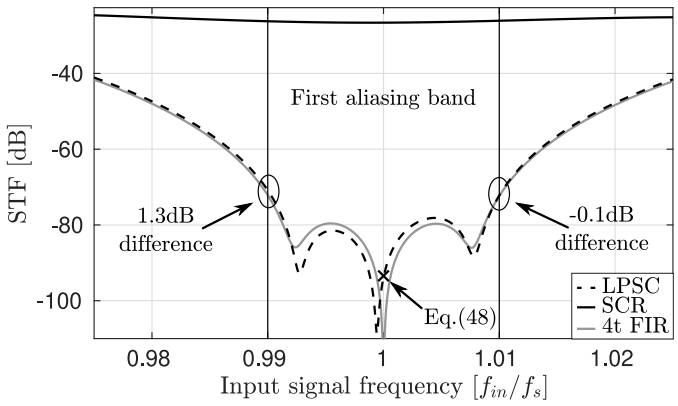


Fig. 19. Detail of simulated STF of three modulators with different DACs, with a simple $g_m = 10g_{m,min}$ in the first OTA.

behavior. The comparator for both systems was shorted to allow for a simulation using linear periodic analysis. The first OpAmp in all three loop filters was implemented as a single transconductance, g_m, with an output impedance $\frac{100}{g_m}$ for 40 dB DC-gain. The second and third OpAmps are ideal with quasi-infinite amplification. Again the low-pass filtering capacitors and the feedback capacitors of the first integrators were scaled to compensate for the effect of low g_m values, as we did in section IV. Fig. 18 shows the simulated STF of the modulators for $g_m = 10g_{m,min}$. The calculated value of the STF at f_s according to the approximate expression of Eq. (48) is indicated as well. It is clear that a modulator with an SCR-DAC has awful anti-aliasing filtering, particularly around f_s. This is partly because the first notch in the STF is shifted out of band, an effect that is also discussed in [32]. The modulator with a four-tap FIR-DAC shows slightly more peaking than the other modulators [8]. Apart from this, on this scale, the FIR-DAC's STF is almost indistinguishable from the LPSC-DAC's STF.

To illustrate the LPSC-DAC's effect on the modulator's aliasing behavior, we have to look at the detail of the modulators' STF in the first aliasing band which is centered around f_s. This is shown on Figs. 19 and 20 for two different values of g_m. Again, the calculated value of the STF at f_s according to Eq. (48) is indicated, and it matches the simulation very well. However, it is also clear that the worst case aliasing frequency does not correspond to f_s but instead to the edges

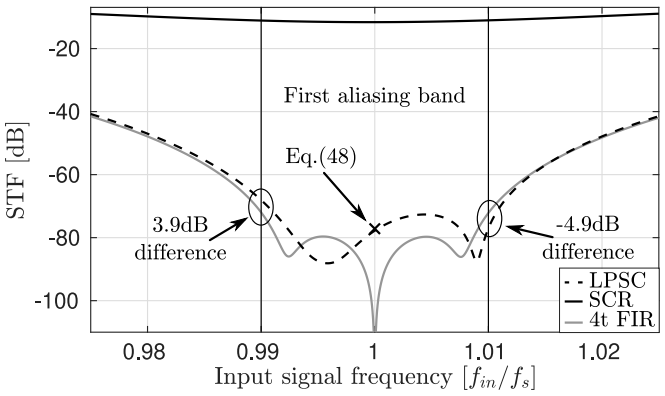


Fig. 20. Detail of simulated STF of three modulators with different DACs, with a simple $g_m = g_{m,min}$ in the first OTA.

of the alias band. For $g_m = 10g_{m,min}$, this worst case anti-aliasing filtering is virtually the same for the LPSC-DAC as for the FIR-DAC with a difference of only 1.3 dB on a total of 70.9 dB. For the case of $g_m = g_{m,min}$, the worst case anti-aliasing filtering of the LPSC-DAC is slightly more affected, but it is still within 4 dB from that of the the FIR-DAC modulator. For both considered values of g_m the anti-aliasing performance of the SCR case is catastrophically affected.

VII. Conclusion

We proposed to introduce a low-pass filtering switched capacitor DAC into the loop of a CTSDM. It was shown that this circuit filters the modulator's feedback signal in the discrete-time domain. We have shown that by adding a compensating zero in the loop, the effect of this filter toward the equivalent discrete-time loop filter can be removed entirely. Additionally by adding an extra low-pass filter, the STF can be restored. This way, the technique is transparent on the system level and compatible with any existing system-level modulator synthesis technique.

The advantage of the technique is that the requirements on the OpAmps in the loop are greatly relaxed up to a level that the OpAmp power can be cut down toward its bare white noise limited value. To achieve this, the time constant of the LPSC-DAC should be suitably sized. For this we have analyzed the noise behavior of the LPSC-DAC and we have defined optimal design guidelines for the time constant of the LPSC-DAC which should be set appropriately such that the modulator's in-band noise level remains unaffected.

Furthermore, we have analyzed the jitter sensitivity and anti-aliasing filtering of the LPSC-DAC modulator, and we have derived simple but accurate analytical expressions, which are confirmed by simulation results. The conclusion of the analysis is that our technique offers excellent jitter sensitivity and maintains very good anti-aliasing filtering, even for the most interesting case where the OpAmp power is cut down to its bare limit.

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