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NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
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(NASA-Case-NPO-11569) : LOW PHASE NOISE N73-26229
DIGITAL FREQUENCY DIVIDER Patent (Jet
Propulsion Lab.) 9 p CSCL 09C

REPLY TO
ATTN OF: GP

Unclas
00/10 06466

TO: KSI/Scientific & Technical Information Division
Attention: Miss Winnie M. Morgan

FROM: GP/Office of Assistant General Counsel for
Patent Matters

SUBJECT: Announcement of NASA-Owned U.S. Patents in STAR

In accordance with the procedures agreed upon by Code GP and Code KSI, the attached NASA-owned U.S. Patent is being forwarded for abstracting and announcement in NASA STAR.

The following information is provided:

U.S. Patent No. : 3,737,676
CALTECH
Government or Corporate Employee : Pasadena, CA
Supplementary Corporate Source (if applicable) : JPL
NASA Patent Case No. : NPO-11569

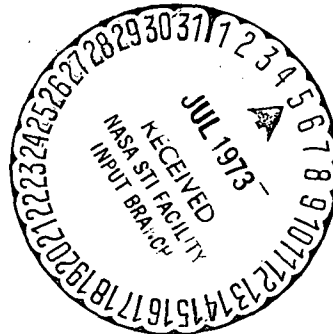
NOTE - If this patent covers an invention made by a corporate employee of a NASA Contractor, the following is applicable:

Yes No

Pursuant to Section 305(a) of the National Aeronautics and Space Act, the name of the Administrator of NASA appears on the first page of the patent; however, the name of the actual inventor (author) appears at the heading of column No. 1 of the Specification, following the words ". . . with respect to an invention of . . ."

Elizabeth A. Carter

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Enclosure
Copy of Patent cited above



[54] **LOW PHASE NOISE DIGITAL FREQUENCY DIVIDER**

[76] Inventors: **James C. Fletcher**, Administrator of the National Aeronautics and Space Administration with respect to an invention of; **George F. Lutes, Jr.**, South Gate, Calif.

[22] Filed: **Nov. 18, 1971**

[21] Appl. No.: **199,957**

[52] U.S. Cl. **307/220, 307/233**

[51] Int. Cl. **H03k 21/00**

[58] Field of Search **307/167, 220, 225, 307/226, 232, 233, 240; 328/25, 30, 37-39, 42, 15**

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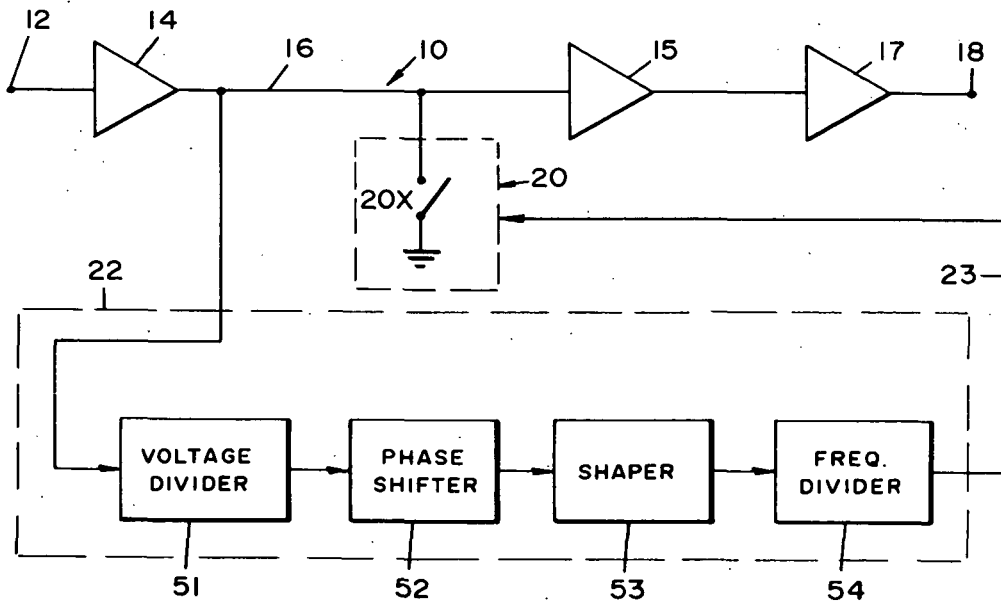
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[57] **ABSTRACT**

A low phase noise frequency divider is disclosed comprising a gating arrangement which supplies selected portions of an input reference signal to be divided to a tuned circuit without any phase noise due to the gating action. The arrangement which in one embodiment consists of a FET is connected to the tuned circuit input to short out the input except when the input reference signal amplitude crosses ground level in a positive direction and a gate enabling signal is present at the gate electrode of the FET. The gate-enabling signal alone does not decouple the tuned circuit input from ground, therefore phase noise, due to the leading and trailing edges of each gate-enabling signal, is substantially eliminated.

5 Claims, 7 Drawing Figures



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FIG. 1

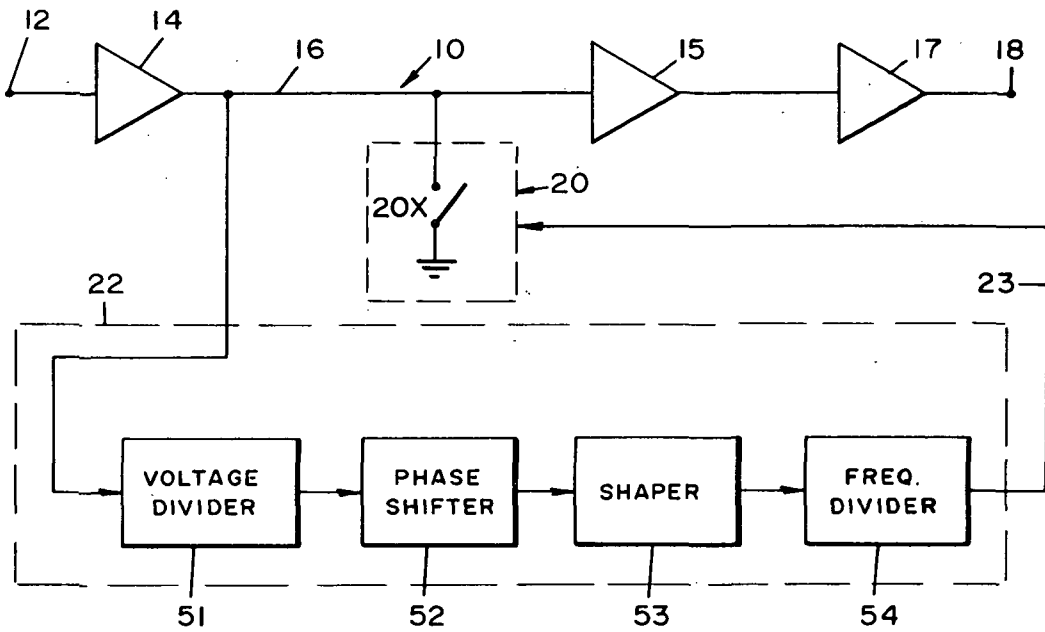
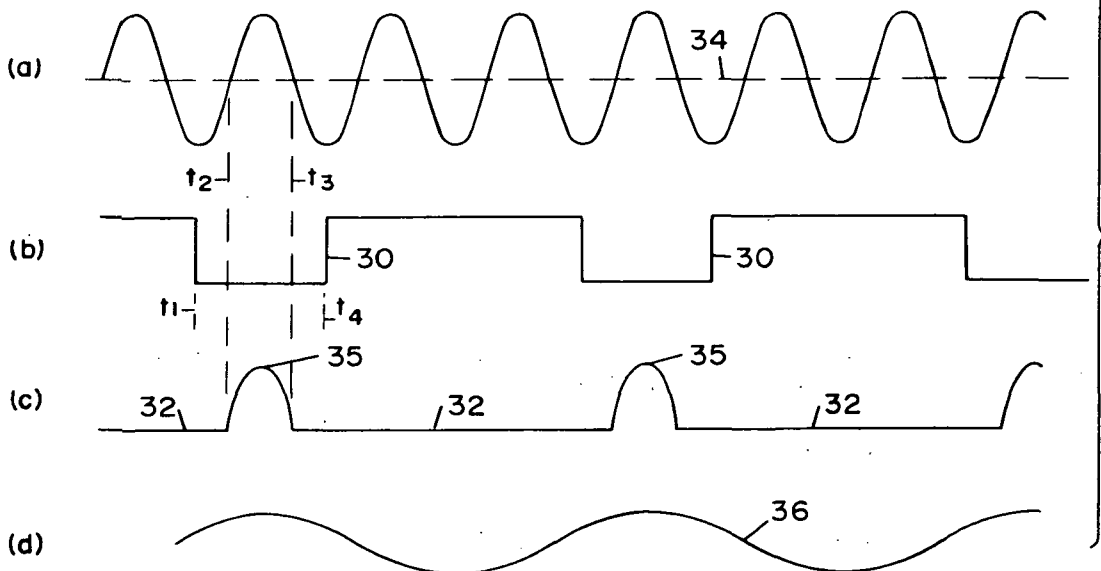


FIG. 2



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FIG. 3
PRIOR ART

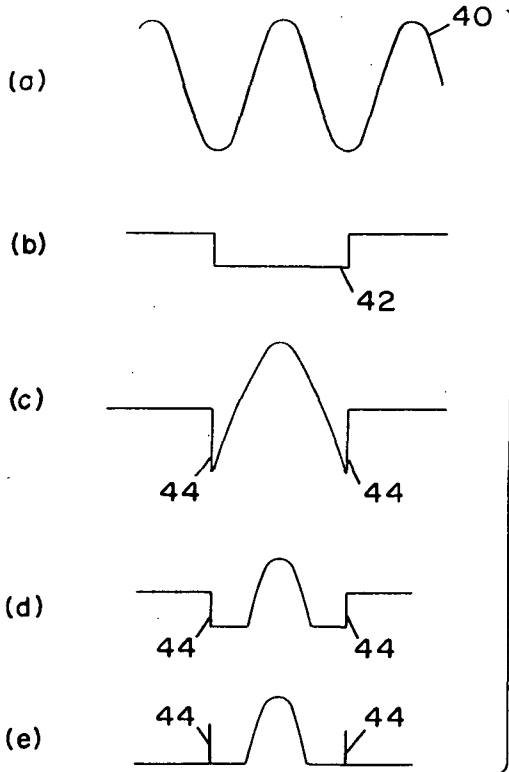


FIG. 4

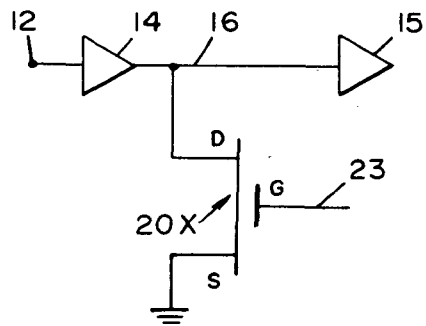
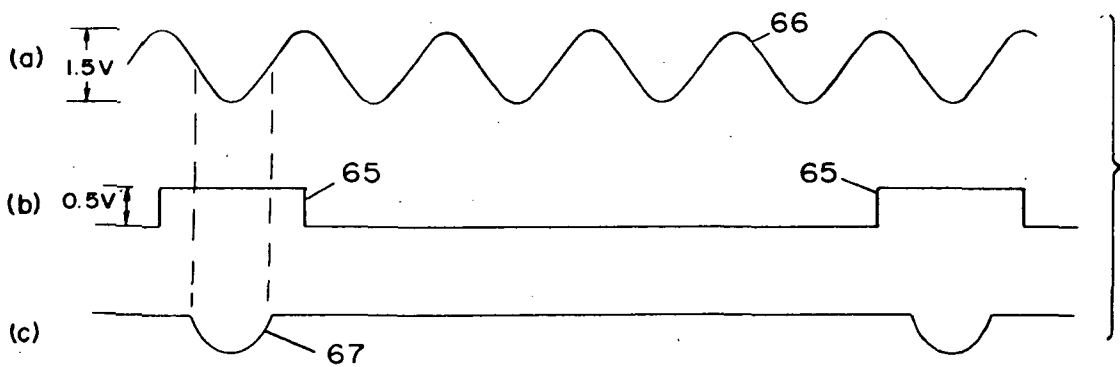


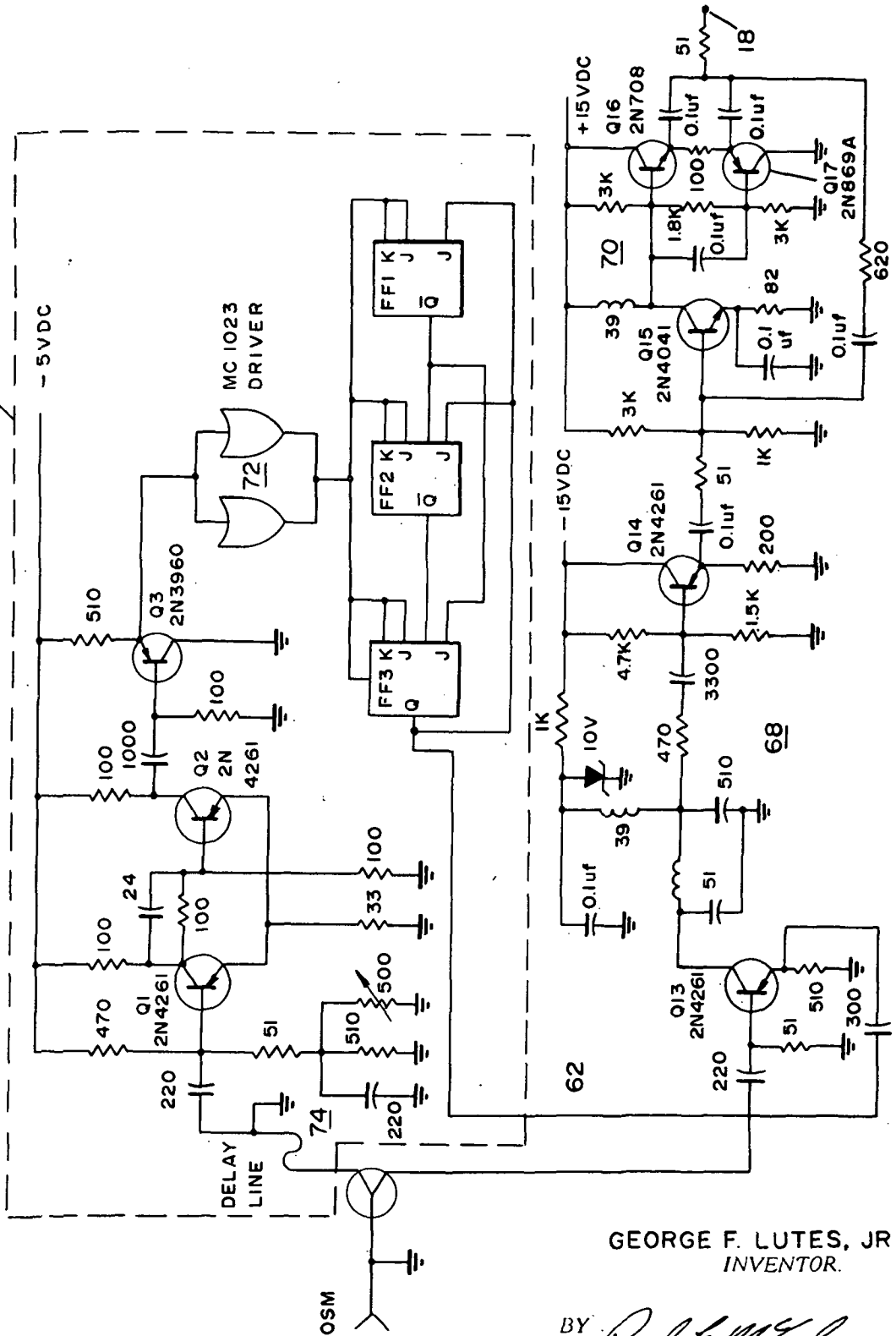
FIG. 7



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FIG. 6



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LOW PHASE NOISE DIGITAL FREQUENCY DIVIDER

ORIGIN OF INVENTION

The invention described herein was made in the performance of work under a NASA contract and is subject to the provisions of Section 305 of the National Aeronautics and Space Act of 1958, Public Law 85-568 (72Stat. 435; 42 U.S.C. 2457).

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to a frequency divider and, more particularly, to a digital frequency divider with low phase noise.

2. Description of the Prior Art

Stable frequency sources are being used for a variety of purposes, including ranging, by which the precise distance from earth of a spacecraft can be determined. Range resolution depends largely on the purity and stability of the frequency sources, used in the receivers. As distances of further space exploration missions increase, the need for very pure and stable frequency sources increases to insure accuracy of ranging.

Scientific research in recent years has led to the development of hydrogen masers, which are still in the process of further development. One of the most important properties of a hydrogen maser is the stability and purity of its output frequency. However, the signal produced by a hydrogen maser is in the range of over 1,000 MHz, e.g., 1,420+MHz. The maser's signal is generally used to control the stability and purity of a reference signal from a crystal oscillator.

Although the reference signal is extremely clean and stable, it is also at a very high frequency region, e.g., 100MHz. Therefore, for many applications, such as ranging receivers, it must be divided down to lower frequencies, such as 20MHz, 10MHz, etc. In being divided down, noise, in the form of amplitude noise and phase noise, is added to the reference signal by the dividers which are inherently noisy devices. Thus, whereas the reference signal is clean and stable, the same is not true for the divided signals at the lower frequencies.

Amplitude noise can be controlled by various amplitude limiting arrangements. However, controlling phase noise or jitter is a more difficult problem, and one which has a significantly greater, objectionable effect on the resolution capabilities of the receiving and measuring equipment, since ranging receivers and telemetry systems employ phase modulation. For example, doppler shifts in phase over the long distances of space exploration are used to determine target distance and the effect of the local phase jitter, present in the divided signals, tends to insert a degree of uncertainty in the range or distance measurements.

To date various attempts were made to eliminate the phase jitter produced by the frequency dividers which are used to divide the clean and stable reference signal to lower frequencies. However, although some of these attempts reduced phase jitter, none has succeeded in eliminating or reducing the phase jitter to acceptable levels. Thus, a need exists for a frequency divider with very low phase noise or jitter.

OBJECTS AND SUMMARY OF THE INVENTION

It is a primary object of the present invention to provide a new frequency divider.

Another object of the present invention is to provide a highly reliable frequency divider with low phase noise.

A further object of the invention is the provision of means in a frequency divider to substantially eliminate phase noise due to the dividing process.

These and other objects of the invention are achieved by providing a digital frequency divider with a novel gating arrangement. The arrangement includes a gate which effectively is connected at the input of a tuned amplifier, whose output represents the divided signal. The gating arrangement is such that the relatively noisy output of the digital divider does not add appreciable noise to the signal passing through the gate. The gate acts as a switch which shorts out the undesired portion of the input reference signal. The gate, which is supplied with gating signals, is primed by each gating signal to open the short. However, the short is not removed until the desired portion of the reference signal arrives. Thus, only when the gate is primed and the desired reference signal portion arrives is the short removed, to permit passage of the desired portion of the reference signal to the tuned amplifier. The frequency of the gating signals is related to the reference signal frequency by the factor by which the reference signal is to be divided.

The novel features of the invention are set forth with particularity in the appended claims. The invention will best be understood from the following description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a general block diagram of the novel divider of the present invention;

FIG. 2 is a multiline waveform diagram useful in explaining the basic operation of the novel divider;

FIG. 3 is a multiline waveform diagram useful in describing disadvantages of the prior art;

FIG. 4 is a diagram of a gating arrangement using a field effect transistor;

FIG. 5 is a complete schematic diagram of one embodiment of the invention;

FIG. 6 is a complete schematic diagram of another embodiment of the invention; and

FIG. 7 is a multiline waveform diagram useful in explaining the operation of the embodiment shown in FIG. 6.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference is now made to FIG. 1 which is a block diagram of the novel divider of the present invention. The divider, designated by numeral 10, is shown comprising an input terminal 12 at which a clean and stable input reference signal is applied at a frequency which is to be divided down by divider 10 without adding appreciable phase noise. The input signal is amplified in an isolation amplifier 14 whose output is supplied to a tuned amplifier 15, on line 16. The latter's output passes to a broadband amplifier 17 whose output is applied to the divider's output terminal 18.

The output of amplifier 14 on line 16 is also supplied to a novel gating arrangement 20 and to a division-control unit 22. As shown in FIG. 1, the gating arrangement 20 is represented by a switch or gate 20x, which shorts the line 16 to a reference potential, such as

ground, whenever the switch is closed. Thus as long as the gate is closed and the short is present, the input of tuned amplifier 15 is grounded and therefore no portion of the input reference signal passes to the amplifier 15. Consequently no output signal is produced. However, when the switch is open (as shown), the amplifier reference signal passes to the tuned amplifier.

In accordance with the present invention, the control unit 22 provides gate-enabling signals on line 23 to the switch 20x, at the desired rate or frequency of the output signal. In the absence of an enabling signal the switch is closed, thereby shorting the reference signal to ground. Each gate-enabling signal primes the switch to open. However, the switch remains closed until a desired portion of the reference signal appears coincidentally with the presence of the enabling signal. Only then is the switch opened to enable the desired portion of the reference signal to pass to the tuned amplifier 15 for the purpose of producing the output signal. Such an arrangement inhibits any jitter in the gating arrangement from being coupled to the tuned amplifier which, if not prevented, affects the purity of the output signal.

The advantages of the novel divider of the present invention may be highlighted by referring to FIG. 2, wherein lines *a*, *b*, *c* and *d* are waveform diagrams of the input reference signal at terminal 12, the output unit 22, the input of amplifier 15 and the output of amplifier 17, respectively. In FIG. 2 it is assumed that the control unit 20 provides gate-enabling signals 20 at $\frac{1}{3}$ the rate or frequency of the input reference signal to produce a frequency division by a factor of 3.

The type of switch, chosen for the waveforms shown in FIG. 2, is one which remains closed in the absence of a negative-going enabling signal 30. Thus as seen in FIG. 1, line *c*, in the absence of an enabling signal, the input to amplifier 15 is grounded as represented by straight lines 32. However, even when an enabling signal 30 is present, the input to amplifier 15 remains grounded until the input reference signal crosses a reference voltage level, such as ground represented by dashed line 34, in the positive direction.

This unique property is further highlighted in FIG. 2, wherein it is assumed that an enabling signal 30 is provided between t_1 and t_4 , and that during this interval the input reference signal passes the ground level in the positive and negative directions at t_2 and t_3 , where $t_4 > t_3 > t_2 > t_1$. In accordance with the present invention, the switch 20x remains closed thereby shorting line 16 except during the interval between t_2 and t_3 , when both the enabling signal is present and the reference signal is above the ground level. During the intervals that the switch is open, the desired portions of the reference signal, represented by numeral 35 in FIG. 2, pass to the tuned amplifier. Its output after wideband amplification by amplifier 17 is a sinusoidal signal 36 at the frequency of the desired portions, which in FIG. 2 is $\frac{1}{3}$ the input reference signal frequency.

It should be appreciated that for proper operation, the enabling signals 30 should be in phase with the desired portions of the reference signals. In FIG. 2, the duration of each enabling signal is shown to be 1 full cycle of the reference signal. However, from the foregoing it should be apparent that the enabling signal duration is not critical as long as it is not less than $\frac{1}{2}$ cycle or more than $1\frac{1}{2}$ cycles. The switch remains closed during those intervals when the enabling signal is present but the reference signal is not yet above the zero

level 34. Thus noise from the gate does not pass to the amplifier 15 and consequently its output is clean and stable.

Such an arrangement is unlike the prior art in which noise from the gate and from the digital divider are permitted to pass to a tuned amplifier in an output stage. For comparison purposes FIG. 3 is included to diagram on lines *c*, *d* and *e*, different prior art gated outputs produced when gating an input signal 40, shown on line *a*, with a gate command signal 42, shown on line *b*. In each case the noise passing to the tuned amplifier is represented by the waveforms 44.

Before proceeding to describe a specific implementation of gating arrangement 20, attention is again directed to the division-control unit 22 in FIG. 1. Therein it is shown comprising a voltage divider 51, a phase shifter 52, a shaper 53 and a frequency divider 54. Briefly, divider 51 reduces the peak-to-peak voltage of the amplified reference signal from amplifier 14, and phase shifter 52 adjusts the phase of the enabling signals 30 with respect to the reference signal. The output of the phase shifter, which is sinusoidal, is shaped into a square wave by shaper 53. This square wave at the reference signal frequency activates divider 54 which provides the enabling signals at the desired output signal frequency. To compensate for temperature variation and to insure that the enabling signal duration is not less than $\frac{1}{2}$ cycle of the reference signal in one embodiment a divider 54 was chosen to provide each enabling signal of a duration of 1 full cycle of the reference signal. The frequency of these enabling signals is that of the desired frequency of the output signal.

Herebefore the enabling signals 30 have been shown to have negative polarities with respect to a reference level, such as ground. In practice, the polarities and amplitudes of these signals depend on the specific implementation of the gating arrangement 20 and the particular device, used for switch 20x. One device which is particularly suitable as switch 20x is a field effect transistor, or FET.

As is known, the FET is a device of three terminals or electrodes, often referred to as the drain, source and gate electrodes. The FET conducts current between its drain and source as long as the gate electrode potential is equal to or greater than the potential of either of the other electrodes. Under those conditions the FET is ON and is analogous to a closed switch. However, when the gate is negatively biased with respect to both the drain and source, the FET is cut off, i.e., in an OFF state so that current can't flow between the drain and the source. In this state the FET acts as an open switch.

When employed in the present invention, the gate-enabling signals 30 (FIG. 2, line *b*) on line 23, are applied to the gate electrode of an FET, serving as switch 20x, as shown in FIG. 4. One of the FET's other electrodes, e.g., the source, is grounded. Thus, as long as no enabling signal is applied, the gate electrode is substantially at ground and since the source is grounded, the FET is ON, i.e., the switch is closed irrespective of the potential or amplitude of the reference signal on line 16.

During the period of each gate-enabling signal, which is of a negative polarity, the gate electrode is at a negative potential with respect to ground. However, the FET remains fully conductive, i.e., the switch is closed as long as the gate electrode is less negative than the drain electrode at which the reference signal is applied.

As the potential at the drain becomes more positive than the gate electrode, the FET's resistance across the drain and source electrodes increases. Thus, the current flow decreases and the FET starts switching to its OFF state. It is cut off completely, i.e., the switch is opened when the drain is sufficiently positive with respect to the gate electrode. In the particular application, the amplitude of the enabling signal is chosen so that as the drain potential changes from negative to positive, the FET is fully turned off, i.e., the switch is fully open. When the switch is open line 16 is completely ungrounded and therefore the desired portion of the reference signal passes to the tuned amplifier 15.

It should be stressed again that in the present invention the leading and trailing edges of each gate-enabling signal occur when the FET is already conducting, i.e., shorts out the input of the tuned amplifier. Therefore these leading and trailing edges do not produce any phase noise. It should further be stressed that the FET remains at least partially conductive until the reference signal potential is sufficiently positive with respect to the gate electrode, when full cut off occurs. Only then is the short removed completely, and the desired portion of the reference signal passes to the tuned amplifier. Thus, no phase noise is generated in the gating operation of the reference signal.

Attention is now directed to FIG. 5 which is a complete schematic diagram of an embodiment of the invention which was actually reduced to practice. Therein the switch 20x is represented by a DUAL GATE FET Q2, and the isolation amplifier 14 by transistor Q1. The tuned amplifier 15 is represented by transistor Q3 and the output amplifier 17 by transistor Q4-Q6. Transistor Q7 is part of the phase shifter 52 and transistors Q8-Q10 are part of an amplifier interposed between the phase shifter 52 and the shaper 53. The latter is represented by transistor Q11.

In the particular embodiment the frequency divider 54 (see FIG. 1) was implemented with a conventional digital frequency divider connected to divide by five. One example of such a divider is Type S8280A of Signetics. Since such a unit produces positive going gate-enabling signals, an inverter, consisting of Q12, was incorporated. In FIG. 5, the waveforms at various points are also diagrammed. Therein capacitors are in μf and chokes in μh . The arrangement shown in FIG. 5 is capable of operating satisfactorily at input frequencies up to 10MHz. The following Table A lists values of a few critical components (C1, C2 and L) needed to accommodate various input frequencies within this range.

TABLE A

C1, C2 and L Values for Various Frequencies

Frequency	C1	C2	L (μhs)
5 MHz	200 pf	2000 pf	4.6
2 MHz	510 pf	5100 pf	13
1 MHz	1000 pf	10,000 pf	24
360 KHz	3000 pf	0.033 mfd	67
200 KHz	5100 pf	0.051 mfd	120
100 KHz	0.01 mfd	0.1 mfd	240

The use of an FET as switch 20x is satisfactory up to approximately 10MHz. However, above 10MHz, the inter-electrode capacitance of presently available FETs is too high and therefore at such frequencies the FET is no longer an effective switch at the input of the tuned amplifier. A gating arrangement which is suitable for input frequencies as high as 100MHz is shown schematically in FIG. 6 to which reference is now made.

Basically the gating arrangement 20 includes a bipolar transistor Q13. The reference signal from input terminal 12 is applied to the base of Q13 and the gating or gate-enabling signal which comes from a division control unit 60 on a line 62 is impressed on the emitter. Unit 60 and line 62 are analogous to unit 22 and line 23 of the embodiment, shown in FIG. 1. The transistor Q13 performs the functions performed by the FET in the prior-described embodiment. In the absence of a gate-enabling signal, which in the present embodiment is a positive going signal, designated in line *b* of FIG. 7 by numeral 65, Q13 is cut off irrespective of the amplitude of the reference signal at 1.5 volts peak-to-peak (p-p), which is applied to the base and which is designated in FIG. 7, line *a* by numeral 66. Even when the gate-enabling signal is applied, Q13 remains cut off while the positive going portion of the reference signal is applied to the base. However, as the negative-going portion of the reference signal is applied, while the gate-enabling signal is also present, Q13 is conducting to amplify and pass the negative-going portion 67 (see line *c*, FIG. 7) of the reference signal to a tuned amplifier 68 whose output is connected to the collector of Q13.

In FIG. 6, the tuned amplifier 68 is represented by transistor Q14 and the output amplifier 70 by transistors Q15-Q17. Amplifiers 68 and 70 perform functions analogous to amplifiers 15 and 17 of FIGS. 1 and 5. Actually the tuned amplifier 68 consists of a tuned circuit 68x which drives Q14 which acts as an amplifier.

The particular embodiment of division-control unit 60 shown in FIG. 6 is designed to divide the reference signal by five over a frequency range from 100MHz to 20MHz. The unit includes three transistors Q18-Q20, three flip-flops FF1, FF2 and FF3, and a driver circuit 72. The three flip-flops are of the AC coupled J-K type. To insure the coincidence of the gating signal with the negative portions of the reference signal, unit 60 preferably includes a delay line 74. In FIG. 6, all capacitors are in pf and the inductors or chokes in μh , except as noted.

Although particular embodiments of the invention have been described and illustrated herein, it is recognized that modifications and variations may readily occur to those skilled in the art and consequently it is intended that the claims be interpreted to cover such modifications and equivalents.

I claim:

1. In a frequency divider the arrangement comprising:

a source of an input signal which varies sinusoidally about a reference level at a frequency f , each cycle of said signal having a positive half cycle and a negative half cycle with respect to said reference level; a tuned amplifier tuned to a frequency f/n where n is an integer;

control means for generating a succession of control signals at a frequency f/n , each control signal having a duration between its leading and trailing ends which is greater than $\frac{1}{2}$ cycle and less than $\frac{3}{2}$ cycles of the input signal, said control means including phase shifting means for controlling the phase between said input signal and said control signal so that a selected portion of every n^{th} cycle of said input signal occurs during the duration of a different control signal other than during the leading and trailing ends thereof; and

gating means coupled to the input of said tuned amplifier and responsive to said input signal and each control signal for inhibiting the level at the input of said tuned amplifier to vary from a preselected reference level in the absence of a control signal and during the leading and trailing ends of each control signal and for controlling the level at the input of said tuned amplifier to vary in a manner corresponding to the change of level of the input signal during a selected portion of every n^{th} cycle of said input signal which is in time coincidence with a control signal other than during the leading and trailing ends thereof, said selected portion being not more than one half cycle.

2. In a frequency divider the arrangement comprising:

isolation means for receiving an input signal which varies sinusoidally about a reference level, definable as ground, at an input frequency definable as f , to be divided by a factor n , n being an integer and for providing a corresponding output signal at an output terminal of said isolation means;

division control means for providing a succession of control signals at one n^{th} the frequency of said input signal, each control signal having a duration which is greater than $\frac{1}{2}$ cycle of said input signal and less than $\frac{3}{2}$ cycles of said input signal;

a tuned amplifier tuned to one n^{th} the frequency of said input signal;

gating means coupled between said output terminal and the input of said tuned amplifier and responsive to said control signals and the output signal at said output terminal for grounding the input of said tuned amplifier except during a portion of the duration of each control signal which is in time coincidence with a selected portion of a cycle of said output signal, said selected portion being not more than half a cycle, whereby the input of said tuned amplifier is ungrounded only during the selected portion of every n^{th} cycle of said output signal; and

output means responsive to the output of said tuned amplifier for providing a sinusoidal signal at one n^{th} the frequency of the input signal.

3. The arrangement as described in claim 2 wherein said gating means comprises a field effect transistor with drain source and gate electrodes, means for grounding said source electrode, means for applying said control signal to said gate electrode and means for connecting said drain electrode to the input of said tuned amplifier and said output terminal, each control signal having a negative polarity with respect to ground, whereby said field effect transistor provides a low resistive path for the input of said tuned amplifier to ground during the duration of each control signal except when the level at said drain electrode is positive with respect to the level at said gate electrode, whereby the input of said tuned amplifier is ungrounded only during the positive half cycle of each n^{th} cycle of said output signal.

4. The arrangement as described in claim 2 wherein said division control means include phase shifting means for controlling the relative phase between said control signals and said output signal so that each selected portion of a cycle of said output signal occurs during the duration of another control signal other than at the leading or trailing ends thereof, so as to inhibit said tuned amplifier from sensing said leading or trailing ends.

5. The arrangement as described in claim 4 wherein said gating means comprises a field effect transistor with drain source and gate electrodes, means for grounding said source electrode, means for applying said control signals to said gate electrode and means for connecting said drain electrode to the input of said tuned amplifier and said output terminal, each control signal having a negative polarity with respect to ground, whereby said field effect transistor provides a low resistive path for the input of said tuned amplifier to ground during the duration of each control signal except when the level at said drain electrode is positive with respect to the level at said gate electrode, whereby the input of said tuned amplifier is ungrounded only during the positive half cycle of each n^{th} cycle of said output signal.

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