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Het onderzoek of ontwerp dat in dit proefschrift wordt beschreven is uitgevoerd in overeenstemming met de TU/e Gedragscode Wetenschapsbeoefening.

Contents

List of symbols and abbreviations

Symbol	Description	Unit
SAR	Successive approximation register	
ADC	Analog-to-digital converter	
IoT	Internet of Things	
DAC	Digital-to-analog converter	
VR	Voltage reference	
CR	Charge-redistribution	
CS	Charge-sharing	
TC	Temperature coefficient	ppm/ºC
LS	Line sensitivity	%/V
PSRR	Power supply rejection ratio	dB
ECG	Electrocardiography	
EEG	Electroencephalography	
EMG	Electromyography	
SoC	System-on-Chip	
Gm	Transconductance	S
C_T	Total capacitance at each side of a DAC array	F
LDO	Low dropout regulator	
BJT	Bipolar junction transistor	
V_t	Threshold voltage of MOSFETs	V
V_T	Thermal voltage	V
PTAT	Proportional to absolute temperature	
CTAT	Complementary to absolute temperature	
CMOS	Complementary Metal Oxide Semiconductor	
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor	
ENOB	Effective number of bits	bit
SNDR	Signal-to-noise and distortion ratio	dB
SFDR	Spurious-free dynamic range	dB
THD	Total harmonic distortion	dB

Chapter 1 Introduction

In this introduction, the background of this work is described, the technical challenges in this domain are given and the aim, scope and outline of this thesis are discussed.

1.1. Background

The first recorded semiconductor effect dates back to 1833, when Michael Faraday described the “extraordinary case” of his discovery of electrical conduction increasing with temperature in silver sulfide crystals [1]. However, not until 1940s-1950s, with the invention of the point-contact transistor by William Shockley, John Bardeen and Walter Brattain [2] and the licensing of transistor technology by Bell Labs [1], did the semiconductor technology start a booming development. From then on, people have been witnessing a variety of exciting applications brought to this world one after another by semiconductor technology: smaller electronic devices with better portability, more abundant functionalities and lower price. Nowadays, semiconductor electronics is regarded as the physical foundation of the virtual world and acknowledged as one of the greatest breakthroughs since the invention of the wheel [3].

During the past years, with the rapid development of the semiconductor techniques, Internet of Things (IoT) and biomedical sensors have been very prevailing research topics and have drawn tremendous attention. IoT is the internetworking of physical devices embedded with electronics, software, and network connectivity that enable these objects to collect and exchange data [4]. It can be utilized in a variety of areas such as transportation, smart buildings, automatic manufacturing, and environmental monitoring. Usually, one or more sensors are attached to the IoT nodes to enable abundant functionalities. A biomedical sensor detects quantities like physical, chemical or biological information to be used e.g. for healthcare analysis and diagnosis, enabling a cheap, accurate, convenient and personalized healthcare [5]. For example, flexible biomedical sensors like wearable, portable and implantable biomedical sensors can monitor people’s health condition continuously without interrupting people’s daily life. For IoT sensors and flexible biomedical sensors, durable longevity and low cost are two critical factors for a broad and convenient utilization. In terms of durable longevity, the power consumption of the sensors should be as low as possible since the power is usually fed by battery or energy-harvesting or the combination

of these two, any of which can only provide limited power at a reasonable cost. Consequently, these low-power sensors usually operate at low VDD (sub-1V) to reduce the power consumption. Small chip area will reduce the cost of chip fabrication and also lead to a small volume of the sensor that can be used conveniently. To summarize, IoT sensors and flexible biomedical sensors should occupy small chip area and consume little power operating at sub-1V power supply.

In order to sense and process the environmental or biomedical information, analog-to-digital converters (ADCs) are usually present in a sensor to convert the sensed analog information to the digital domain for the sake of convenient processing, storage, and transmission of digital signals and for the robustness of the system. The required resolution of the ADC is usually no larger than 12 bits and the ADC usually operates at low speed [6, 7, 8, 9, 10, 11, 12, 13] which makes a SAR ADC a perfect choice due to the excellent power-efficiency within this resolution range [14]. For a SAR ADC, an accurate reference voltage needs to be generated that should drive the digital-to-analog converter (DAC) array and might consume significant energy or occupy large chip area. This issue is rarely discussed in SAR ADC publications.

For an optimal design, it is necessary to take into account the system in which the ADC will be utilized. Considering the cost and power requirements from the system level, low-power and area-efficient low-VDD SAR ADCs with on-chip voltage reference are investigated and corresponding techniques are proposed in this thesis.

1.2. Technical challenges

As discussed above, power and cost are two major considerations for IoT sensors and flexible biomedical sensors, where cost is related to the chip area. When combining a SAR ADC with reference-voltage generation, power and chip area form usually a trade-off. For instance, in order to reduce the power consumption, large resistances have to be utilized at the expense of large chip area. Similarly, a large capacitance can be used to stabilize the reference voltage instead of a power-hungry high-bandwidth reference-voltage driver, saving power by sacrificing chip area. Another challenge originates from the low-VDD (sub-1V) operation requirement where some conventional circuit topologies cannot be adopted anymore.

1.3. Aim of the thesis

The aim of this thesis is to develop low-power and area-efficient techniques for SAR ADCs with reference-voltage generation for IoT sensors and flexible biomedical sensors. Specifically, the aim of this thesis is explicated as follows:

- Achieve insight in interrelations and trade-offs between the SAR ADC core and the reference-voltage generation.
- Develop and validate low-power and area-efficient techniques for SAR ADCs and their reference-voltage generation from three aspects:
  - power-efficient SAR ADC;
  - low-power sub-1V voltage reference (VR);
  - overall SAR ADC with VR and reference driver.

1.4. Scope of the thesis

The scope of this thesis is explained below:

- **Low-speed sub-1V moderate-resolution SAR ADCs with capacitive DAC**

  This thesis aims at IoT and flexible biomedical sensor applications that require low-speed and low-VDD ADCs with moderate resolution, making SAR ADCs a perfect choice. Consequently, this thesis focuses on SAR ADCs with no higher than 12b resolution operating at a sampling frequency less than 50 MHz and sub-1V VDD. In terms of DAC topology in a SAR ADC, only capacitive DACs are studied, because of their energy-efficiency thanks to the dynamic operation. Only charge-redistribution (CR) DACs are considered in this case because of their advantages compared with charge-sharing (CS) DACs.

- **Sub-1V VRs with main focus on power and chip-area optimization**

  The VR designs in this thesis are all based on CMOS rather than bipolar transistors, and the main concerns are sub-1V operation, power consumption and chip-area occupation due to the targeted applications.

- **Combination of SAR ADCs with reference-voltage generation**

Besides the reference voltage, a time reference (clock signal) and an input buffer are also required for SAR conversion. For low speed sensors, the clock signal can be easily derived from the system clock with little power and chip area and the clock signal has little impact on the ADC performance. Another important periphery block for SAR ADCs is the input driver. However, compared with the reference-voltage driver, it interacts less with the ADC and is less challenging since it mainly operates during track phase.

On the other hand, the reference-voltage generation is highly interrelated with the ADC performance and usually expensive in power consumption and area occupation. In this thesis, only the reference-voltage generation solution is studied and developed, including the VR design and the reference-voltage driver design.

- **CMOS technology**

  One advantage of SAR ADCs is its agility to technology scaling, thanks to the highly digitized architecture. CMOS technology is the most prevailing semiconductor technology and preferable for digital circuit implementation. Hence, it is a very logical choice to limit our scope to CMOS technology. All simulations and implementations in this thesis are conducted in a 65nm CMOS technology.

1.5. Original contributions

The main original contributions of this thesis are listed below:

- Charge-redistribution DAC energy consumption
  - An analysis of the energy consumption of CR-DACs in SAR ADCs, in switching phase and reset phase respectively.
  - Proposal and verification with measurements of a reset-energy-free 'swap-to-reset' scheme.
- Voltage reference (VR)
  - Investigation and summary of the main challenges in low-VDD low-power low-cost CMOS VR design.
  - Proposal and verification with measurements of a 0.62V-VDD 25nW CMOS VR.
  - Proposal and verification with measurements of a high-efficiency multi-stage

duty-cycling scheme, developed to save energy.

- Proposal and verification with simulations of a low-power CMOS VR utilizing MOS-resistors to reduce chip area.
- Proposal and verification with simulations of a duty-cycled sub-nW resistor-less VR based on switched capacitors, achieving low power and small chip area.
- Proposal and verification with simulations of a low-power CMOS VR based on a single type of transistors, hence compatible with low-cost CMOS technology.

- Integration of a SAR ADC with reference driver
  - Analysis of the trade-offs between chip area and power consumption of SAR-ADC reference driver.
  - Proposal and verification with measurements of a reference driver with off-chip capacitor.
  - Proposal and verification with measurements of a power and area-efficient reference-voltage driving scheme with compensated DAC array.

1.6. Outline of the thesis

The outline of this thesis is explained below and visualized in Figure 1.1.

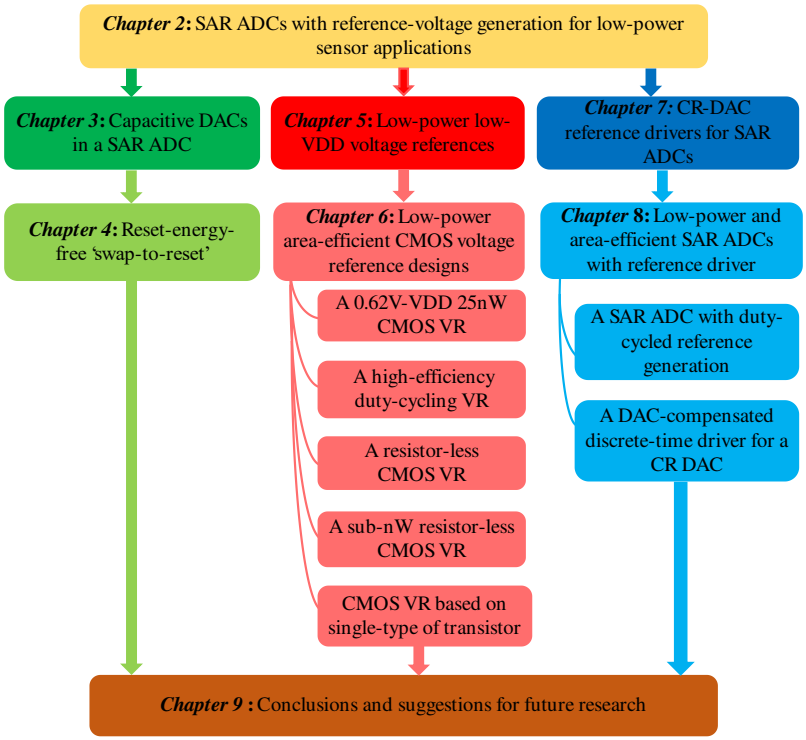


Figure 1.1: The outline of this thesis.

Chapter 2 introduces the technical background of this thesis and indicates the main technical difficulties in detail. In order to overcome above difficulties, solutions are developed from three aspects: SAR ADC, voltage reference, and the combination of SAR ADC with reference-voltage generation.

Chapter 3 to 8 expand and describe the main approaches of this thesis from the three aspects as discussed in the aim in detail.

- CR DAC energy consumption in a SAR ADC
  - In Chapter 3, the CR and CS DACs are first compared and the reason why CR DACs are adopted in the designs of this thesis is given. As one of the dominant energy consumption sources of a CR SAR ADC, the switching and reset energy consumption of a DAC are analyzed for different switching schemes later in Chapter 3.
  - In Chapter 4, a reset-energy-free 'swap-to-reset' scheme applicable to many existing switching schemes is presented and verified by measurements.

- CMOS VR
  - Chapter 5 reviews and compares the prior-art VRs.
  - In Chapter 6, four CMOS VR designs and an efficient duty-cycling technique are introduced, targeting at low power, low VDD, small chip area and portability to low-cost CMOS technology.
- Integration of SAR ADC with reference-voltage driver
  - Chapter 7 introduces the current solutions to SAR ADC reference-voltage driver, which are power hungry or chip-area consuming, or require digital post processing.
  - In Chapter 8, two co-designs of a CR SAR ADC with a reference-voltage driver are presented.

Chapter 9 concludes this thesis.

Chapter 2 SAR ADCs with reference-voltage generation for low-power sensor applications

This chapter explains the periphery circumstances for a SAR ADC in the targeted low-power sensor applications and gives a short review of SAR ADCs. The technical challenges are explicated in detail for SAR ADCs and their reference-voltage generation, and this is followed by some general approaches to deal with these challenges.

2.1 IoT and flexible biomedical sensors

IoT devices are usually embedded with specific types of sensors to enable abundant functionalities. There exist dozens of different IoT sensors such as temperature sensors, pressure sensors, proximity sensors, level sensors, and so on [15]. Depending on the targeted measurement, a sensor requires different specifications for the readout ADC. In general, the required resolution is from 7 to 12-bit ENOB at relatively low speed from DC to a few kS/s for the ADC in IoT sensors [6]. For instance, temperature sensors could be utilized to monitor the temperature in agriculture as shown in Figure 2.1. In order to achieve a maximum output of the plant, the temperature of the soil, the irrigation and the air surrounding the plants should be monitored and controlled. In this application example, 8b or 10b resolution of the ADC is adequate since the required sensing accuracy is not very high. Moreover, the sampling frequency does not need to be high since the temperature changing is a slow process. In the temperature sensor MCP9700 [7] aiming at agriculture applications, an 8b ADC is adopted to read out the temperature, achieving 1℃/bit resolution. In another temperature sensor TC72 [8], a 10b ADC operating at <10Hz is adopted.

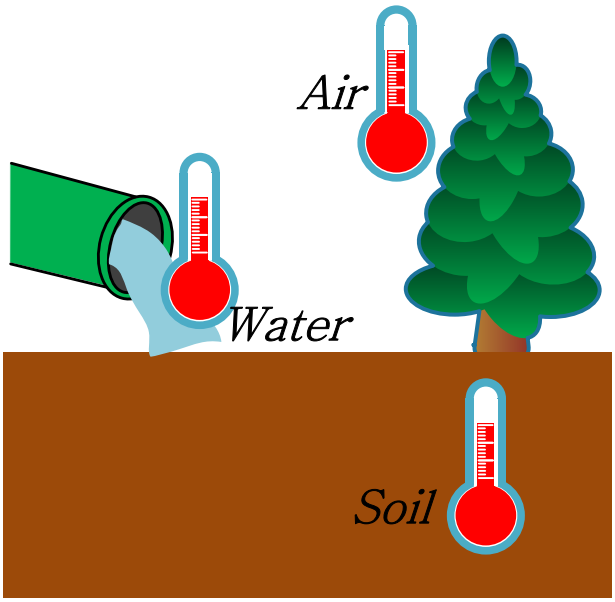


Figure 2.1: Temperature sensors utilized in agriculture.

Biomedical sensors focus on the measurements of biomedical quantities for healthcare analysis, such as blood pressure, ECG (electrocardiography), EEG (electroencephalography), EMG (Electromyography), body temperature, and so on. In order to conduct continuous measurements and monitoring without interrupting people's daily life, flexible biomedical sensors are developed. A flexible wearable ECG sensor system is explicated in Figure 2.2.

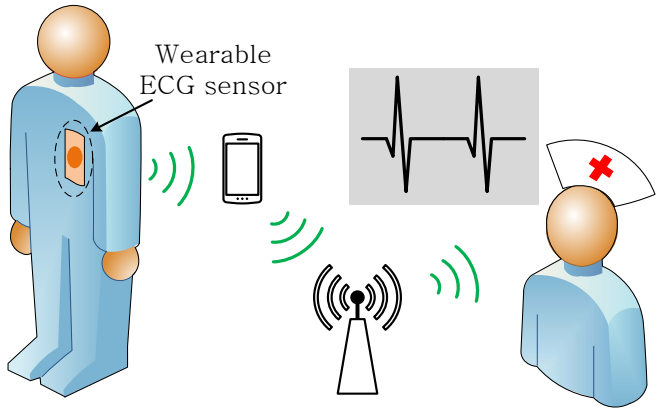


Figure 2.2: Flexible wearable ECG sensor system.

The ECG sensor is attached on the chest of the patient to monitor his/her ECG. The sensed and digitized ECG signal is received by the mobile phone and then transferred to the base station and the hospital. For the ECG sensors [13, 12], 8b to 12b ADCs are adequate operating at a sampling frequency <500Hz.

Just as the above two examples suggest, for most IoT sensors and flexible biomedical sensors, moderate-resolution and low-speed ADCs are capable. More importantly, since massive sensors will be used, cost and longevity are more challenging issues.

2.2 SAR ADCs and the periphery blocks

The SAR ADC is a well-known power-efficient ADC architecture, especially at moderate speed (10k ~ 100MHz) and resolution (6~12bits) [14]. As shown in Figure 2.3, it is based on the efficient binary search algorithm, which is usually realized by 4 components: sampling switches, comparator, DAC, and SAR logic. The inputs are sampled through the sampling switches on the DAC. The comparator then compares the DAC outputs to decide each output bit. SAR logic controls the DAC switching after each comparison and outputs the digital code. Most SAR ADCs utilize a dynamic comparator [16, 17], resulting in a highly digitized hence power-efficient architecture. Besides, the highly digitized architecture is very friendly to technology portability and down scaling. The properties of a SAR ADC make it a perfect choice for IoT and flexible biomedical sensor applications which usually appreciate low power consumption at low speed and moderate resolution.

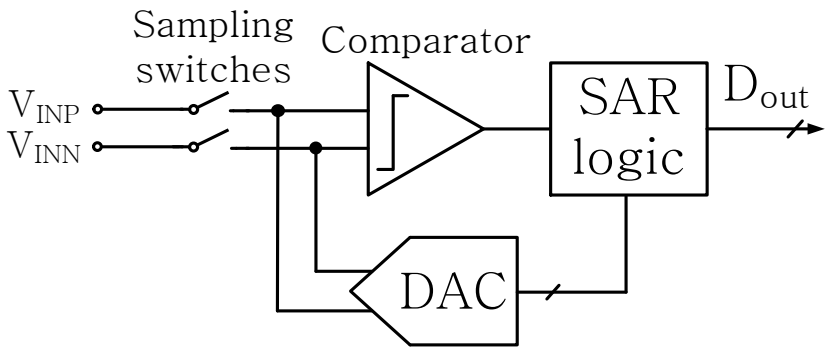


Figure 2.3: Architecture of a differential SAR ADC.

Different from a stand-alone ADC design, the periphery blocks must be taken into account when designing a SAR ADC in a system. As shown in Figure 2.4, for a SAR ADC, an input buffer is required to drive the DAC during the track phase. During the conversion phase,

usually a reference voltage and reference-voltage driver are needed to drive the DAC and support the binary search. Sometimes, a decoupling capacitor is adopted to help stabilize the reference voltage. The track and conversion operations are controlled by a clock signal, whose jitter will cause sampling errors and degrade the ADC performance. As stated in Chapter 1, the main scope of this thesis is the SAR ADC and the reference-voltage generation.

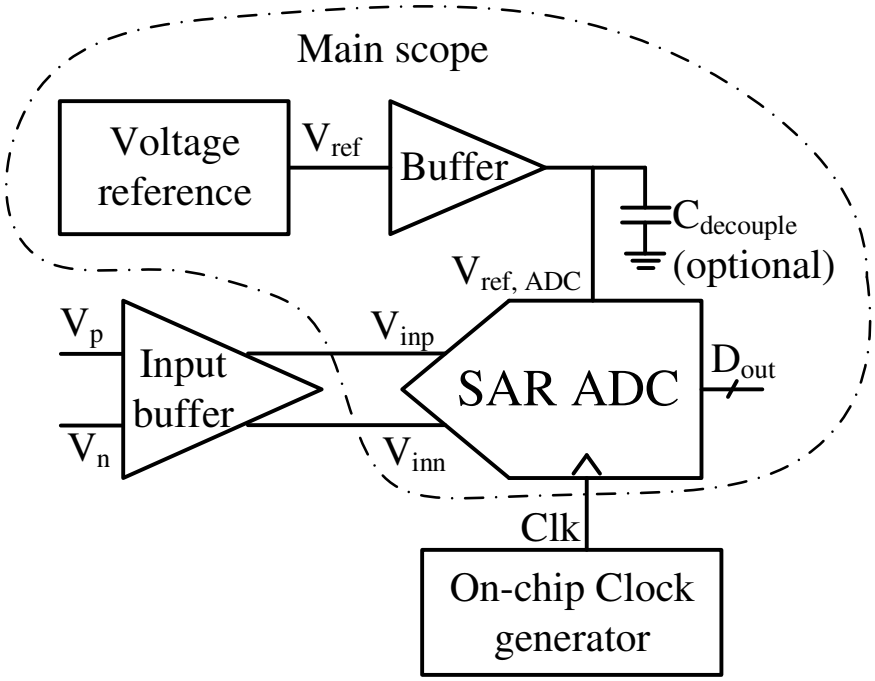


Figure 2.4: SAR ADC with periphery blocks in a system.

2.3 Technical challenges

As discussed above, low power and area efficiency are two vital specifications for IoT and flexible biomedical sensor applications and in order to achieve these two goals, a low power supply (sub-1V) is usually chosen. Consequently, SAR ADCs and their reference-voltage generation in these applications should also be low power and area efficient, operating at low power supply (sub-1V). This sub-chapter discusses the technical challenges in achieving above goals.

2.3.1 Low-power operation

Circuit design is the optimization and trade-off among multiple dimensions. For instance, in order to achieve lower noise performance or higher operation speed, the power consumption has to be increased. In other words, it is a challenge to achieve the targeted low power operation without degrading other performance aspects.

SAR ADC

For SAR ADCs, the energy consumption of the CR DAC is usually a large part of the total energy consumption. DAC energy consumption is proportional to the total capacitance and dependent on the switching scheme. The total capacitance is given by the thermal noise requirement at the sampling and by the matching specification. Consequently, the total capacitance as well as the DAC energy consumption cannot be reduced without any penalty.

VR

In IoT and flexible biomedical sensor devices, sub-1V low-power VRs are required, making the conventional bandgaps based on bipolar devices not applicable, since they operate at a minimum VDD of 1.4V and consume μW-range power [18]. CMOS VRs can achieve sub-1V operation and low power but are usually much more sensitive to process variations [19, 20].

Reference-voltage driver

The DAC of an N-bit SAR ADC has to switch at least (N-1) times during one conversion, requiring the reference-voltage driver to respond accurately at a frequency higher than (N-1) times the sampling frequency. This sometimes results in a reference-voltage driver consuming more than 10x the power of the ADC [21, 22] which means the power optimization of the reference-voltage driver is essential.

2.3.2 Small chip-area occupation

The two main chip-area-consuming components are resistors and capacitors, both in the ADC and the reference stabilization.

Resistors

Resistors are favorable in multiplying a voltage quantity and generating a certain ratio as adopted in the conventional bandgap references [18]. However, according to Ohm's law, in

order to suppress the current flowing through a resistor by 10x, a 10x larger resistor is required. Assuming that 1V is applied to a resistor to generate 1nA current, a 1GΩ resistor is required, which occupies a large chip area (at least 0.5mm^2 in 65nm CMOS).

Capacitors

In order to deal with the fast switching of the DAC, a large decoupling capacitance can be placed at the output of the reference-voltage driver. Reducing this capacitance will require more power consumption of the driver to enhance the loop response [23]. In terms of decoupling capacitance, it is a trade-off between chip area and power consumption, which will be further elaborated in Chapter 7.

Inside the SAR ADC, the total capacitor value inside the DAC is growing exponentially with the resolution N, and also the number of elements could scale (worst case) up to 2^N. Therefore, the switched-capacitor DAC is usually responsible for the largest portion of the area of a SAR ADC.

2.4 Approaches

Here some general approaches will be introduced that deal with the above mentioned challenges. These will be expanded later in this thesis.

2.4.1 Low-power techniques

Three approaches are mentioned here to address the low-power challenge.

Duty-cycling

Duty-cycling operation shuts down the circuits when they are not needed, hence reducing the average power consumption. The operation of a SAR ADC with capacitive DAC and dynamic comparator can be seen as a duty-cycling operation due to the highly digitized architecture. The analog reference voltage and reference-voltage driver are typically always-on. Introducing duty-cycling to these blocks could help saving power, especially in IoT and flexible biomedical sensor systems which are usually duty-cycled in the first place.

Smart operation

Designing the operation of the circuits in a smart way can increase the power efficiency. In [17], a majority-voting technique is presented to reduce the comparator noise in a power-

efficient way. [24, 25, 26] propose smart DAC switching schemes to save DAC power while they only focus on the DAC energy during conversion. In fact, the energy consumed during reset is higher [24, 25, 26] and is seldom optimized hence providing large space to improve.

Co-integration

For an existing SAR ADC, the required specifications for the reference-voltage driver can be derived explicitly and the driver can be designed accordingly. However, this might be an inefficient approach since the ADC and driver are then designed relatively independently. Alternatively, if these two blocks are designed as a combination in the first place, a smart design of one block might relax the requirement for the other one, thus achieving better overall performance.

2.4.2 Chip-area reduction techniques

The chip-area challenge will be addressed as discussed next.

Resistor replacement

In order to replace large poly-resistors, MOS-resistors can be used. The higher sensitivity of MOS-resistors to process and temperature variations needs to be addressed in the design. Switched-capacitors can also be used to replace resistors with smaller area, while providing a smaller temperature dependency given an accurate clock [18]. The dynamic operation of these capacitors will be exploited further to enable duty-cycling, thus achieving low power and occupying small area simultaneously.

Capacitor reduction

As discussed in Section 2.3.2, the decoupling capacitance is a trade-off between chip area and power consumption. In order to reduce the decoupling capacitance and maintain a low power consumption, smart operation will be developed to increase the power efficiency.

2.5 Conclusions

The two critical specifications for SAR ADCs including reference-voltage generation in IoT sensors and flexible biomedical sensors are low power and small chip area, which can be achieved from 3 aspects: the SAR ADC, the VR and the reference-voltage driver. The DAC power consumption of a SAR ADC is defined mainly by the noise and matching requirements hence cannot be simply reduced. In the conventional VR designs, small

currents imply large resistors that occupy a large chip area. Similarly, reference-voltage drivers suffer from a trade-off between power consumption and chip area (decoupling capacitance). Some general approaches have been introduced to deal with the above challenges and these will be utilized in the following chapters after a specific literature review of prior art.

Chapter 3 Capacitive DACs in a SAR ADC

This chapter first compares the two popular capacitive DACs, CR DAC and CS DAC, to explain our choice for a CR DAC, which reveals several strong advantages over the CS DAC, but that also introduces an extra challenge for the design of the reference driver. The CR DAC in a SAR ADC can consume significant energy. This chapter then reviews the CR DAC energy consumption during tracking, conversion and reset phase and points out the reason why reset energy is usually higher than conversion energy. Part of this chapter was published in [27].

3.1 Capacitive DACs

The DAC can be implemented with capacitors, resistors, or current sources. Thanks to the excellent energy-efficiency of the capacitive DAC, it is the most frequently used DAC in SAR ADCs. In this sub-chapter, two popular capacitive DAC solutions, CR (charge-redistribution) DAC and CS (charge-sharing) DAC, are reviewed and compared regarding the DAC performance and the requirements for the reference driver.

3.1.1 CR DAC

Among capacitive DACs, CR (charge-redistribution) DACs [28] are the most common DACs thanks to their simple implementation and their insensitivity to parasitic capacitance. Consequently, CR DACs are adopted in all the presented SAR ADC designs in this thesis. One example of the CR DAC is shown in Figure 3.1, where $C_{1, 2, \ldots K-1}$ are binary scaled and C_a is the attenuation capacitance equal to C_1. All the bottom plates of the binary capacitors are driven by 2 switches (an inverter) to switch between the reference voltage and ground. The CR DAC generates binary voltage steps at the output nodes by switching the binary DAC array causing charge redistribution. As shown in Figure 3.1, when capacitor pair C_i is switched, a differential voltage shift is generated at the two output nodes. According to the conservation of charge, the sum of the charge change at each top plate is zero since all the top plates are floating. Assuming the voltage shift at positive side is ΔV, the charge conservation can be expressed as:

$$(C_T - C_i)\cdot \Delta V + C_i \cdot (\Delta V - V_{REF,ADC}) = 0 \tag{3-1}$$

where C_T is the total capacitance at each side of the DAC. Solving (3-1), ΔV_i can be expressed:

$$\Delta V_i = +\frac{C_i}{C_T}\cdot V_{REF,ADC} \tag{3-2}$$

Similarly, the voltage shift at negative side can also be derived.

(3-2) indicates that an accurate reference voltage has to be present for a CR DAC during conversion, which usually leads to a power-hungry or area-consuming reference driver.

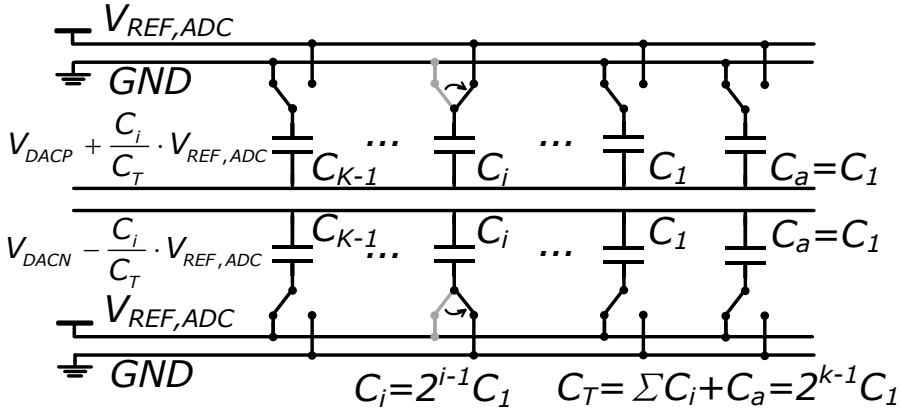


Figure 3.1: Example of a (K-1)-bit CR DAC.

In practice, the switches and the routing of the metal wire will introduce parasitic capacitance to the binary DAC, shown as C_{PS}, C_{PB}, and C_{PT} in Figure 3.2. C_{PS} and C_{PB} have no impact on the charge redistribution of the binary DAC since they do not change the voltage level at the bottom plates. However, extra energy will be consumed when charging these parasitic capacitances during switching. Note that the attenuation capacitor C_a is neglected in Figure 3.2 and replaced with C_{PT} which can be easily larger than C_a. C_{PT} will introduce gain error to the SAR ADCs and affect the energy consumption slightly.

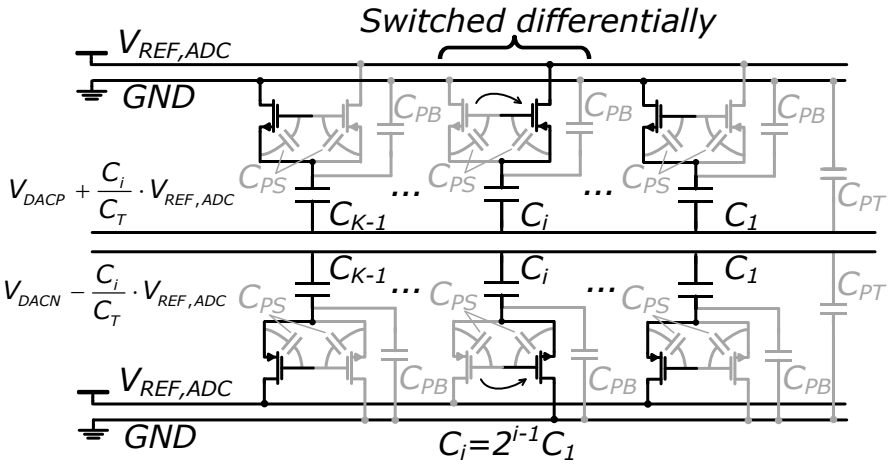


Figure 3.2: CR DAC with parasitic capacitance.

To summarize, the parasitic capacitance in a CR DAC has little impact on the performance of a SAR ADC. It will introduce extra energy consumption and gain error. The gain error is not a severe problem for a SAR ADC.

3.1.2 CS DAC

In order to mitigate the difficulty of reference driving for a CR DAC, the CS DAC has been developed. The CS DAC is based on charge sharing during conversion [29], where the reference driver is only needed during the tracking phase to pre-charge the binary DAC, which makes it easier to design the reference driver for low power and area than in case of a CR DAC.

The operation of a CS DAC is shown in Figure 3.3 where a K-bit ADC is taken as an example. During tracking, the inputs (V_{INP}/V_{INN}) are sampled on the two sampling capacitors (both with value C_S), while the binary CS DAC capacitors (with values C_{K-1}, C_{k-2}, …, C_1) are pre-charged to the reference voltage ($V_{REF,ADC}$). The stored charge on the sampling capacitors can be expressed as:

$$Q_{INP} = V_{INP} \cdot C_S, \quad Q_{INN} = V_{INN} \cdot C_S \tag{3-3}$$

Equivalently, the differential charge on the two sampling capacitors in series can be expressed:

$$Q_S = \frac{Q_{INP} - Q_{INN}}{2} = (V_{INP} - V_{INN}) \cdot \frac{C_S}{2} \tag{3-4}$$

The stored charge on the individual capacitors of the binary DAC can be expressed as:

$$Q_i = V_{REF,ADC} \cdot C_i \tag{3-5}$$

where C_i equals to $2^{i-1} \cdot C_1$ and i ranges from K-1 to 1. The moment each conversion starts, the sampling capacitors are disconnected from the inputs and the binary DAC is disconnected from the reference driver. During conversion, the voltages on the two sampling capacitors are compared, which equivalently detects the polarity of the differential charge as in (3-4). According to the comparison results, the two plates of each capacitor C_i will be successively connected to the sampling capacitors to add or subtract a certain amount of charge and the differential charge will finally approximate zero. For instance, for the MSB, V_{INP} and V_{INN} are compared directly. Assuming V_{INP} is larger, the bottom plate of C_{K-1} will be connected to the positive C_S plate and the top plate of C_{K-1} will be connected to the negative C_S plate as shown in Figure 3.3 (b). Consequently, the differential charge ($Q_{D,1}$) changes to:

$$Q_{D,1} = (V_{INP} - V_{INN}) \cdot \frac{C_S}{2} - V_{REF,ADC} \cdot C_{K-1} \tag{3-6}$$

Note that different from the CR DAC where the total capacitance remains constant all the time, the total capacitance of a CS DAC keeps growing during the conversion. The equivalent total capacitance after the first comparison and switching is:

$$C_{T,1} = \frac{C_S}{2} + C_{K-1} \tag{3-7}$$

As a result, the voltage input seen by the comparator is:

$$V_{D,1} = \frac{Q_{D,1}}{C_{T,1}} = \frac{C_S}{C_S + 2C_{K-1}} \cdot \left[(V_{INP} - V_{INN}) - V_{REF,ADC} \cdot \frac{2C_{K-1}}{C_S} \right] \tag{3-8}$$

Equation (3-8) indicates that a CS DAC can also realize a binary search for a SAR ADC.

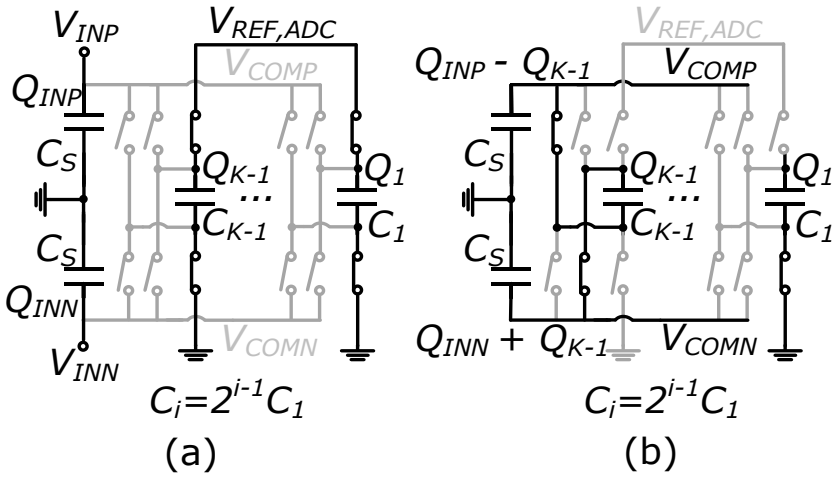


Figure 3.3: A K-bit SAR ADC using a CS DAC: (a) tracking phase; (b) conversion phase after the first comparison.

3.1.3 Comparison between CR and CS DAC

Equation (3-8) gives some more insight in the charge-sharing DAC. The term in the square bracket is the same as for a CR DAC, indicating the same nature of a CS DAC and a CR DAC. It should be noted that in the ideal case, C_S should be $4C_{K-1}$. The coefficient in front of the square bracket (3-8) indicates an attenuated voltage input to the comparator, which is caused by the increasing total capacitance due to the charge sharing, as also indicated by (3-7). As a result, the noise requirement for the comparator is harsher for the CS approach, which will lead to more power consumption for the comparator.

Discussion in the above sub-chapter indicates that the voltage reference driver is only required during the tracking phase in a CS DAC and it does not need to respond to the frequent switching in the conversion phase, leading to a low-cost reference driver. This is an evident advantage of a CS DAC compared to a CR DAC. In terms of DAC energy consumption, a CR DAC consumes energy from the reference voltage source during the conversion due to the charge-redistribution, while a CS DAC only consumes energy during tracking phase to pre-charge the DAC capacitors to the reference voltage. The passive charge sharing during conversion phase consumes no energy.

Compared to a CR DAC, a CS DAC only requires half the amount of binary capacitors, but the total capacitance is larger for the same noise level. Moreover, two additional sampling capacitors need to be present for a CS DAC to operate while the binary CR DAC itself acts

as the sampling capacitors. From the previous discussion it can be noted that for each capacitor plate in the binary CS DAC, there are three possible connections: $V_{REF,ADC}$ or GND during tracking, and V_{COMP} and V_{COMN} during conversion, which requires 6 switches in total for each single-bit sub DAC. Compared to a CR ADC which requires 4 switches for each single-bit DAC (two capacitors in total), the number of switches in a CS DAC is 50% higher.

Moreover, the switches in a CR DAC only connect to the constant voltages $V_{REF,ADC}$ or GND while the switches in a CS DAC also need to connect to a voltage near the changing common mode of the inputs, making it challenging to design the switches, especially when the power supply is relatively low compared to the threshold voltage.

Finally, in a CR DAC, the binary search is realized in the voltage domain, which means the parasitic capacitance introduced by the switches and interconnect has no impact on the binary search since it will not change the voltage. However, in a CS DAC, the binary search is realized in the charge domain so that the parasitic capacitance of the switches and interconnect will influence the charge sharing and degrade the linearity of the DAC.

The comparison between a (K-1)-bit CR DAC and a (K-1)-bit CS DAC is listed in TABLE 3-1. Compared to a CS DAC, a CR DAC requires more capacitor units, but less total capacitance, while the number of switches and the switch requirements are both lower. Moreover, a CR DAC reveals better immunity against parasitics and better linearity, and the requirements for the comparator are lower compared to the signal-attenuating CS DAC. As for the reference driver, a CS DAC relaxes the requirements thanks to the charge sharing during conversion, while a CR DAC requires a high-bandwidth or large-area driver during the entire conversion.

TABLE 3-1: The comparison between a (K-1)-bit CR DAC and a (K-1)-bit CS DAC.

	CR DAC	CS DAC
Sampling capacitors	The DAC itself	2 additional sampling capacitors
No. of binary DAC caps	2(K-1)	K-1
Total capacitance	Low	High
No. of switches	4(K-1)	6(K-1)
Switch requirements	Low	High
Immunity against parasitics/linearity	High	Low
Requirements for the comparator	Low	High
Requirements for the reference driver	High	Low

This comparison substantiates our preference for CR over CS, as already mentioned in Chapter 1.4 (Scope of the thesis), and it also explains why that choice comes with a new challenge with respect to the design of the reference driver.

3.2 CR DAC energy consumption in a SAR ADC

Due to the kT/C noise limitation, the total capacitance of a CR DAC has to be large enough to achieve low enough thermal noise, which usually leads to a significant portion of DAC energy consumption. Moreover, when increasing the resolution of a SAR ADC by 1 bit, the total DAC capacitance has to be quadrupled, resulting in 4x energy consumption, while the energy consumption of the digital (logic) parts in a CR SAR ADC changes linearly with the resolution. As a result, the DAC energy will become strongly dominant in a SAR ADC as the resolution increases. Figure 3.4 shows the CR DAC energy proportion of some recent publications and a rapidly increasing percentage trend can be observed. For low-resolution SAR ADCs, the DAC consumes a small proportion of energy and the digital part (e.g., SAR logic) dominates the total energy consumption, while with increase of resolution, the DAC energy ratio grows rapidly and becomes dominant. At high resolution, it is especially critical to optimize the DAC energy consumption to achieve a low-power SAR ADC overall.

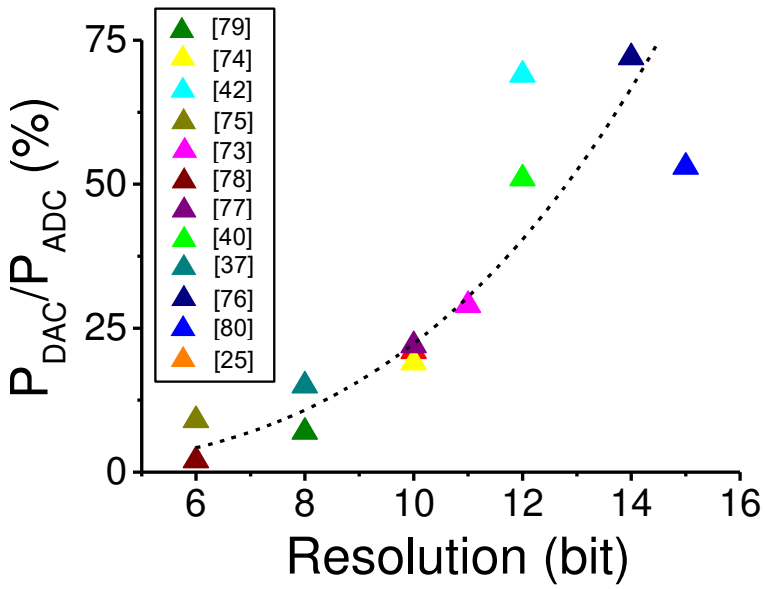


Figure 3.4: A survey of the CR DAC energy proportion in SAR ADCs.

3.3 Comparison of CR switching schemes

In general, the energy consumption of a CR DAC is determined by 3 factors: the total capacitance of the DAC, the reference voltage, and the DAC switching scheme. The CR DAC energy consumption is proportional $C_T V_{REF}^2$, where C_T is the total capacitance and V_{REF} the reference voltage. However, due to thermal noise and matching considerations, the capacitance and reference voltage cannot be reduced unrestrictedly. Moreover, the reference voltage is also constrained by requirements to maintain a large input range, enough speed and consistency with other blocks in the system. Consequently, a lot of work has been presented to develop smart switching schemes to lower the energy consumption of a CR DAC, such as described in [30, 31, 32, 26, 25, 24].

The operation of a SAR ADC can be divided into 3 phases: tracking, conversion, and reset. During tracking phase, the DAC usually consumes no energy from the reference voltage while the input driver has to be present to drive the DAC. During conversion and reset, the DAC consumes energy from the reference voltage, which is the main concern of this chapter. Energy-saving [30] and monotonic [31] approaches save conversion energy but result in a common mode shift of the comparator input. This can introduce a signal-dependent offset to the SAR conversion and cause performance degradation. Another way to save conversion energy is to use more reference voltages other than V_{REF} and GND, e.g., Merged Capacitor Switching (MCS) [32] uses a common mode voltage V_{CM}; however, additional reference voltages require drivers that increase the circuit complexity and consume extra energy. The modified conventional scheme [24], split monotonic scheme [25], and detect-and-skip technique [26] save conversion energy without the above two disadvantages. However, [24, 25, 26] require a reset energy that is close to or even higher than the conversion energy, which diminishes the total energy saving. Figure 3.5 compares the energy consumption of the above schemes to the conventional scheme [28] assuming the same resolution and the same total capacitance at each side (C_T) in order to keep the same thermal noise for a fair comparison. Compared to a conventional scheme, [28, 30, 31, 32] save conversion energy but have the drawbacks as mentioned above. [24, 25, 26] also save conversion energy, but they consume a reset energy that is 0.9x, 1.5x, and 2.2x the conversion energy, respectively. The properties of different switching schemes are further illustrated in Figure 3.6. The designs in Region I do not consume reset energy but require a 3rd reference voltage or suffer from DAC output common mode shift. On the other hand, the designs in Region II use only 2 reference levels and maintain constant output common-mode, but they require a large reset energy. [28] avoids all of the above problems but consumes the largest total energy (Figure 3.5). In terms of reference simplicity and common mode behavior, the schemes in Region II

are more interesting. Although [28] does not consume reset energy, Region II still saves in terms of total DAC energy (Figure 3.5). Furthermore, Region II still has room for improvement as the reset energy can be reduced, as we will show in Chapter 4. Above discussions and comparisons are based on an ideal binary DAC array without parasitics and exclude the logic overhead of different schemes. In reality, the actual energy savings may vary for specific implementations.

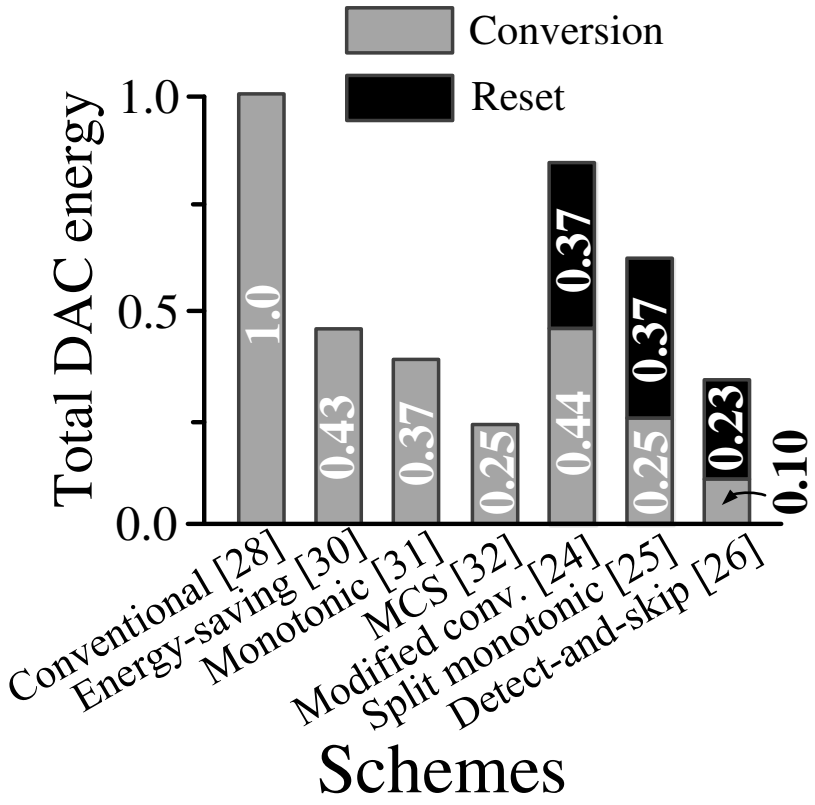


Figure 3.5: Normalized theoretical energy consumption of different switching schemes.

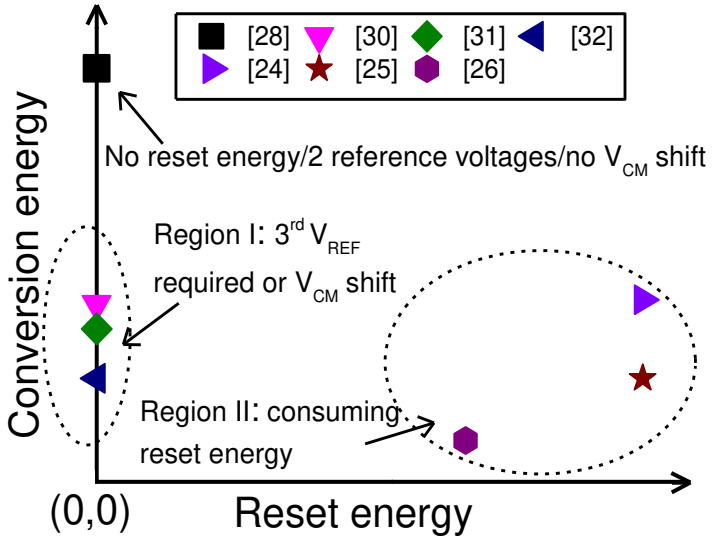


Figure 3.6: Properties of different switching schemes.

3.4 DAC energy consumption of the split monotonic scheme

In order to get a deeper insight about the CR DAC energy consumption, especially the energy consumption comparison between conversion energy and reset energy, the split monotonic [25] scheme is chosen as an example to be investigated further in this sub-chapter.

3.4.1 Conversion energy

The tracking phase of a split monotonic DAC in a SAR ADC is shown in Figure 3.7. For a K-bit SAR ADC, a (K−1)-bit DAC is required and each bit of the DAC comprises two split capacitor pairs, which are reset differentially. C_{K-1}, C_{K-2} … and C_1 are binary scaled and C_{att} is the attenuation capacitor equal to $2C_1$.

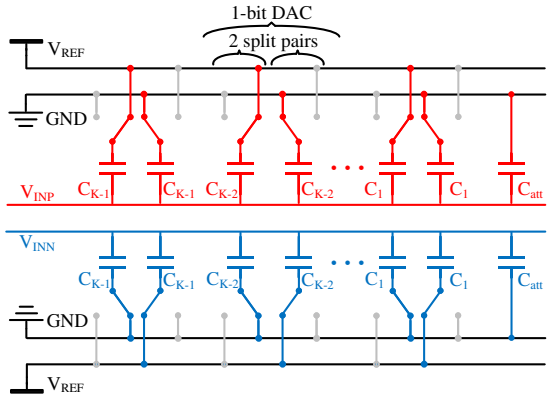


Figure 3.7: Tracking phase of a split monotonic DAC.

During conversion, after the i-th comparison, one pair of C_{K-i} will be switched differentially and the DAC outputs ($V_{P,i}$ and $V_{N,i}$, where $V_{P,1} = V_{INP}$, $V_{N,1} = V_{INN}$) will be shifted by ΔV_{K-i} (= $V_{REF} \cdot C_{K-i} / C_T$ where $C_T = 2 \cdot \sum_{i=1}^{K-1} C_{K-i} + Catt$) according to the comparison result as shown in Figure 3.8 (assuming $V_{P,i} < V_{N,i}$). This switching will cause charge redistribution and energy consumption as shown in Figure 3.9, where C_{MH} and C_{ML} are the total capacitance connected to V_{REF} and GND in the MSB part at P side respectively. At N side, the total capacitance connected to V_{REF} and GND in the MSB part are C_{ML} and C_{MH} respectively, so contrariwise due to the differential reset and switching. C_{LX} is the total capacitance connected to V_{REF} and GND in the LSB part at both P and N side; these capacitances are equal (all C_{LX}) as the LSB part has not been switched yet. There are 3 different types of charge flow. Q_1 is the charge required by one C_{K-i} to switch it from GND to V_{REF}, expressed as:

$$Q_1 = C_{K-i} \cdot (V_{REF} - \Delta V_{K-i}) \tag{3-9}$$

Q_2, Q_3, and Q_4 are the charges repelled from the capacitors connected to V_{REF} at the P side due to the increased DAC output $V_{P,i}$. The total of these repelled charges is expressed as:

$$Q_2 + Q_3 + Q_4 = (C_{MH} + C_{K-i} + C_{LX}) \cdot \Delta V_{K-i} \tag{3-10}$$

Q_5 and Q_6 are the charge absorbed by the capacitors connected to V_{REF} at N side due to the reduced DAC output $V_{N,i}$. The total of these absorbed charges is expressed as:

$$Q_5 + Q_6 = (C_{ML} + C_{LX}) \cdot \Delta V_{K-i} \tag{3-11}$$

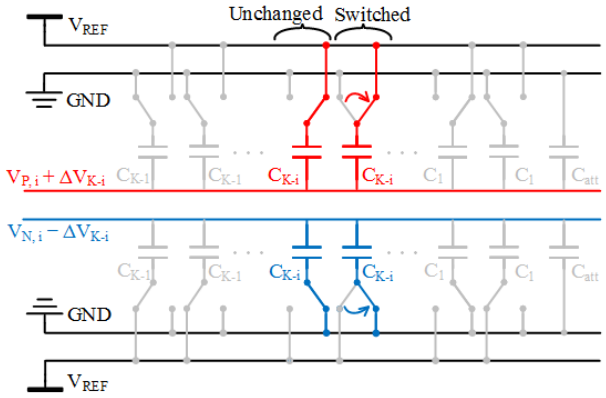


Figure 3.8: DAC switching after the i-th comparison during the conversion phase of a split monotonic DAC assuming $V_{P,i}<V_{N,i}$.

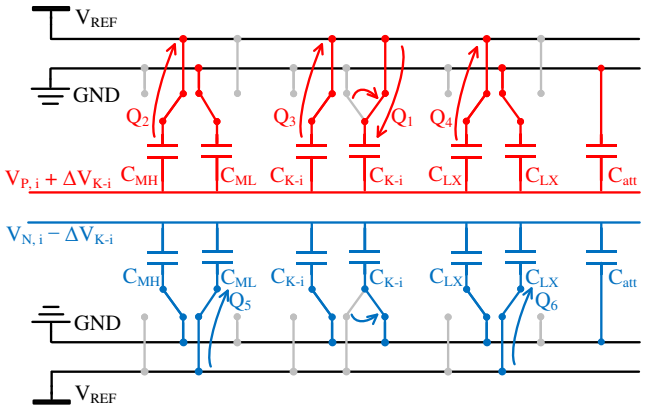


Figure 3.9: Charge flow after the i-th comparison during the conversion phase of a split monotonic DAC (assuming $V_{P,i}<V_{N,i}$) with equivalent combined MSB and LSB capacitors respectively.

The total energy consumption of this i-th DAC switching ($V_{P,i} < V_{N,i}$) is:

$$E_{Conversion,K-i}(V_{P,i}<V_{N,i})=[C_{K-i}\cdot(V_{REF}-2\Delta V_{K-i})+(C_{ML}-C_{MH})\cdot\Delta V_{K-i}]\cdot V_{REF} \quad (3\text{-}12)$$

If $V_{P,i} > V_{N,i}$, we can derive the energy consumption in a similar way as:

$$E_{Conversion,K-i}(V_{P,i}>V_{N,i})=[C_{K-i}\cdot(V_{REF}-2\Delta V_{K-i})+(C_{MH}-C_{ML})\cdot\Delta V_{K-i}]\cdot V_{REF} \quad (3\text{-}13)$$

Assuming every bit decision has the same probability of '1' and '0', the average energy consumption of the i-th DAC switching is the average of (3-12) and (3-13):

$$E_{Conversion,K-i}=C_{K-i}\cdot(V_{REF}-2\Delta V_{K-i})\cdot V_{REF}=C_{K-i}\cdot(1-2\Delta C_{K-i}/C_T)\cdot V_{REF}^2 \quad (3\text{-}14)$$

The average conversion energy for a split monotonic DAC during one conversion can be

expressed as:

$$E_{Conversion} = \sum_{i=1}^{K-1} C_{K-i} \cdot (1 - 2C_{K-i} / C_T) \cdot V_{REF}^2 \approx 0.33 C_T V_{REF}^2 \quad (3\text{-}15)$$

3.4.2 Reset energy

After the entire SAR conversion is done, the DAC outputs will converge to a range of [V_{CM} – 1LSB, V_{CM} + 1LSB] ($V_{CM} = ½V_{REF}$) because of the successive approximation algorithm. For a SAR ADC with a resolution higher than 8 bits, 1LSB is less than 0.8% of V_{CM} hence the DAC outputs can be seen as V_{CM}. The next step is to reset the DAC to the initial configuration as a preparation for the next tracking phase. The conventional method to reset the DAC is to instantaneously switch the entire DAC conversely with the conversion phase as shown in Figure 3.10. The DAC outputs will change by ΔV_{Reset} and recover to the last sampled V_{INP} and V_{INN}. For the capacitor pairs C_{K-i}, similar to the previous calculation, Q_7 and Q_8 can be expressed as:

$$Q_7 = C_{K-i} \cdot \Delta V_{Reset} \quad (3\text{-}16)$$

$$Q_8 = C_{K-i} \cdot (V_{REF} - \Delta V_{Reset}) \quad (3\text{-}17)$$

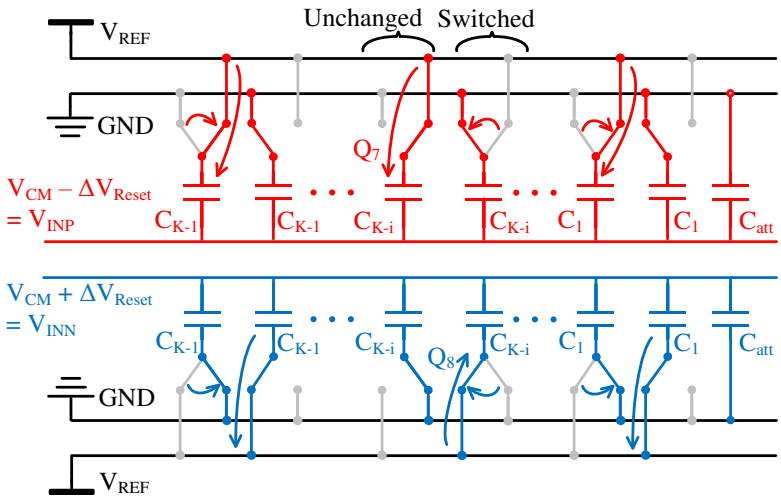


Figure 3.10: Charge flow during the conventional reset of a split monotonic DAC.

The total reset energy consumed by bit i of the DAC is:

$$E_{\mathrm{Re}\,set,K-i} = (\mathrm{Q}_7 + \mathrm{Q}_8) \cdot \mathrm{V}_{REF} = C_{K-i} V_{REF}^2 \tag{3-18}$$

which is proportional to $C_{K\text{-}i}$, independent of $\Delta V_{\mathrm{Reset}}$. The total reset energy of the entire DAC is:

$$E_{\mathrm{Re}\,set} = \sum_{i=1}^{K-1} C_{K-i}\, \mathrm{V}_{REF}^2 \approx 0.5 C_T\, \mathrm{V}_{REF}^2 = 1.5\mathrm{E}_{\mathrm{Conversion}} \tag{3-19}$$

3.4.3 Discussion

For a split monotonic DAC, the switching during conversion and reset are opposite operations while the reset consumes 50% more energy than the conversion. This is caused by the inherent switching properties of these two operations. As shown in Figure 3.9 and (3-14), during conversion, when one $C_{K\text{-}i}$ (P side) is switched from GND to V_{REF}, the other $C_{K\text{-}i}$ at the same side (P side) is already connected to V_{REF} and will contribute charge ($Q_3 = C_{K\text{-}i} \cdot \Delta V_{K\text{-}i}$) to be reused by the switched $C_{K\text{-}i}$ ($Q_1 = C_{K\text{-}i} \cdot (V_{REF} - \Delta V_{K\text{-}i})$), reflected as $C_{K\text{-}i} \cdot ((V_{REF} - \Delta V_{K\text{-}i}) - \Delta V_{K\text{-}i})$ in (3-14). For the conventional reset as shown in Figure 3.10 and (3-18), when one $C_{K\text{-}i}$ (N side) is switched from GND to V_{REF}, the other $C_{K\text{-}i}$ connected to V_{REF} is at the opposite side (P side) and on average all the charge ($Q_7 = C_{K\text{-}i} \cdot \Delta V_{\mathrm{Reset}}$ and $Q_8 = C_{K\text{-}i} \cdot (V_{REF} - \Delta V_{\mathrm{Reset}})$) is provided by V_{REF}, reflected as $C_{K\text{-}i} \cdot ((V_{REF} - \Delta V_{\mathrm{Reset}}) + \Delta V_{\mathrm{Reset}}) = C_{K\text{-}i} \cdot V_{REF}$ in (3-18).

3.5 Conclusions

The DAC consumes significant energy in a CR SAR ADC especially for high-resolution SAR ADCs. Smarter switching schemes can save DAC conversion energy. However, some schemes [30, 31, 32] introduce disadvantages like DAC output common mode shift or a 3rd reference voltage. On the other hand, some schemes [24, 25, 26] save conversion energy while their reset consumes similar or even 2x the energy compared to the conversion phase due to the inherent switching properties of these two operation phases: the conversion phase can reuse some charge from the DAC while the conventional reset absorbs all the charge from the reference voltage source. Schemes like [24, 25, 26] will be more attractive if the large reset energy can be mitigated to achieve a low overall energy consumption without the disadvantages of common mode shift or additional references.

Chapter 4 Reset-energy-free 'swap-to-reset'

This chapter introduces a reset-energy-free reset scheme, 'swap-to-reset' [33, 27]*, that deals with the large reset energy consumption for some switching schemes like,* [24, 25, 26]*.The split monotonic scheme* [25] *is chosen as an example to describe the 'swap-to-reset' operation. Part of this chapter was published in* [27].

4.1 Observations

In Chapter 3, the operation and energy consumption of the split monotonic scheme was described, from which two properties of this scheme have been observed:

- **Differential switching and reset**

  For the split monotonic scheme, the DAC is reset and switched differentially (Figure 3.7, Figure 3.8, and Figure 3.10). In other words, the number of capacitors and the total capacitance value connected to V_{REF} always remains the same. Each time a capacitor is disconnected from V_{REF}, its opposite element will be connected to V_{REF}.

- **DAC output convergence**

  Thanks to the fully differential operation, the DAC outputs ($V_{P,i}$ and $V_{N,i}$) start at the sampled input voltage (V_{INP}, V_{INN}) prior to conversion, and closely approximate V_{CM} by the end of the conversion.

Based on the above observations, the energy-free 'swap-to-reset' is introduced. The applicability of 'swap-to-reset' to other switching schemes is also discussed.

4.2 Reset-energy-free 'swap-to-reset'

As shown in Figure 4.1, 'swap-to-reset' is applied to a 1b DAC as an example. C_{PH}, C_{PL}, C_{NH}, and C_{NL} denote the capacitors connected to V_{REF} and GND at P and N side respectively and they are all equal to C_{K-i}. After the conversion is finished, the 2 capacitors at each side

are both connected either to V_{REF} or GND and the aim of reset is to have 1 capacitor connected to V_{REF} and 1 capacitor connected to GND at each side. The conventional method to reset the DAC is to switch the pair of capacitors opposite to the conversion phase (Figure 3.10), consuming large energy as described by (3-18). Alternatively, the DAC can be simply reset by swapping the positions of one pair of capacitors between P and N side as shown in Figure 4.1. The first step is to disconnect C_{PL} and C_{NH} from P and N sides (Figure 4.1 (a)). Subsequently, the N and P connections of C_{PL} and C_{NH} are swapped by connecting them to the opposite side (Figure 4.1 (b)). Since both DAC output voltages are the same (V_{CM}), the swap operation consumes no energy and the DAC is reset successfully (Figure 4.1 (c)). In the very next tracking and conversion phases, the previous C_{PL} will act as the new C_{NH} and the previous C_{NH} will act as the new C_{PL} (Figure 4.1 (c)). The energy consumption of 'swap-to-reset' for this DAC bit can be expressed as:

$$E_{S-to-R,K-i} = (Q_9 + Q_{10}) \cdot V_{REF} = 0 \tag{4-1}$$

If 'swap-to-reset' is applied to the entire DAC, the total reset energy is:

$$E_{S-to-R} = \sum_{i=1}^{K-1} E_{S-to-R,K-i} = 0 \tag{4-2}$$

Instead of energy-inefficient switch-to-reset, which releases some charge to GND and draws new charge from V_{REF}, 'swap-to-reset' reuses the charge and resets the DAC by swapping without charge dissipation, hence being energy-free.

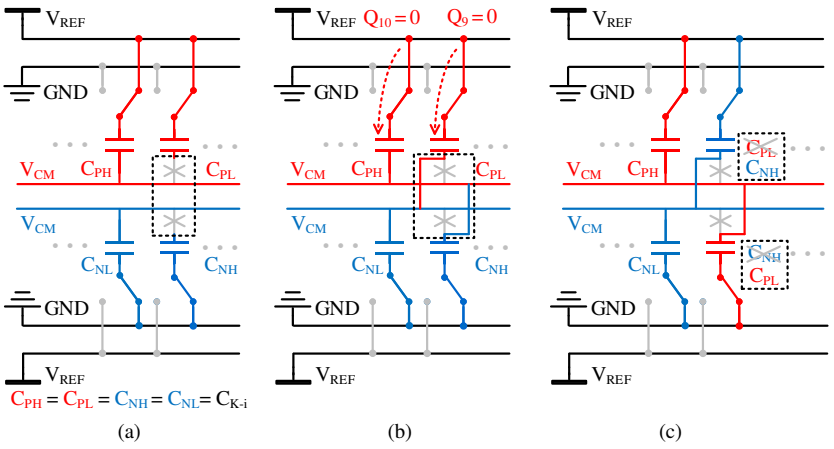


Figure 4.1: Operation and charge flow of the 'Swap-to-reset' scheme. (a) Step 1: disconnect from P and N sides; (b) Step 2: swap N and P connections without energy dissipation; (c) Successful reset, function of capacitors swapped.

4.3 Properties of ‘swap-to-reset’

Some important properties of ‘swap-to-reset’ are introduced in the following paragraphs. The general applicability and implementation tradeoffs are discussed, guiding the utilization of ‘swap-to-reset’ in practice.

4.3.1 General applicability

Previous discussions indicate the preconditions to apply ‘swap-to-reset’: the DAC must be reset and switched differentially and the DAC outputs must converge to [V_{CM}-1LSB, V_{CM}+1LSB] at the end of each conversion. The latter is inherently true if the former is satisfied. For instance, the schemes [24, 25, 26] that were mentioned before, reset and switch the DAC differentially and thus ‘swap-to-reset’ can be applied. The normalized theoretical energy reduction after applying ‘swap-to-reset’ is shown in Figure 4.2.

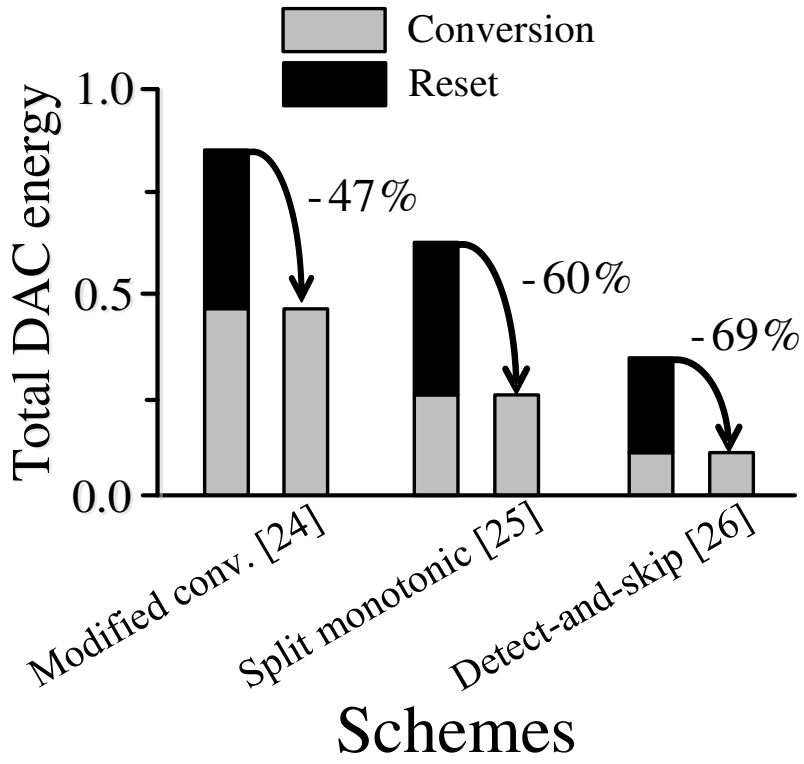


Figure 4.2: Normalized theoretical energy reduction after applying ‘swap-to-reset’ to [24, 25, 26].

4.3.2 Implementation tradeoff

From (4-1) and (4-2), it can be concluded that the energy consumption of the conventional reset for split monotonic is proportional to the capacitance while it is energy-free for 'swap-to-reset'. Since the DAC is binary scaled, the MSB part consumes the most significant reset energy. In order to conduct 'swap-to-reset', extra auxiliary circuits are required (switches and control logic). These extra circuits consume energy and increase the implementation complexity of the ADC. For that reason, 'swap-to-reset' can be limited to the MSBs of the DAC to eliminate the majority of the reset energy while the LSB part can use a conventional reset for circuit simplicity. In order to achieve the above energy saving, the sequence of these two reset operations is critical. 'Swap-to-reset' must be performed first because both DAC outputs have to be close to V_{CM} for the energy-free swapping.

Based on the above principle, the normalized total reset energy of a 12b split monotonic SAR ADC with 'swap-to-reset' applied to a different number of bits is illustrated in Figure 4.3. The majority (75%) of the reset energy can already be saved with 'swap-to-reset' utilized for the 2 MSBs only.

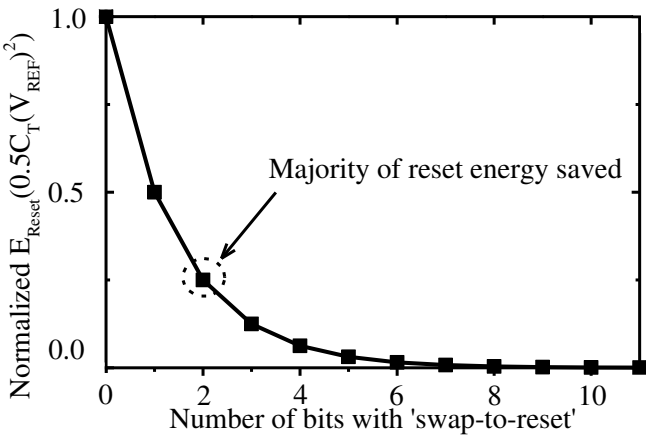


Figure 4.3: Normalized E_{Reset} of a 12b split monotonic SAR ADC with 'swap-to-reset' applied to a different number of bits.

Figure 4.4 shows the theoretical energy reduction after applying 2-MSB 'swap-to-reset' to [24, 25, 26]. Compared to Figure 4.2, the energy saving is less, but the circuit complexity and auxiliary circuit power overhead are reduced. Overall, limiting 'swap-to-reset' to several MSBs might be a favorable compromise.

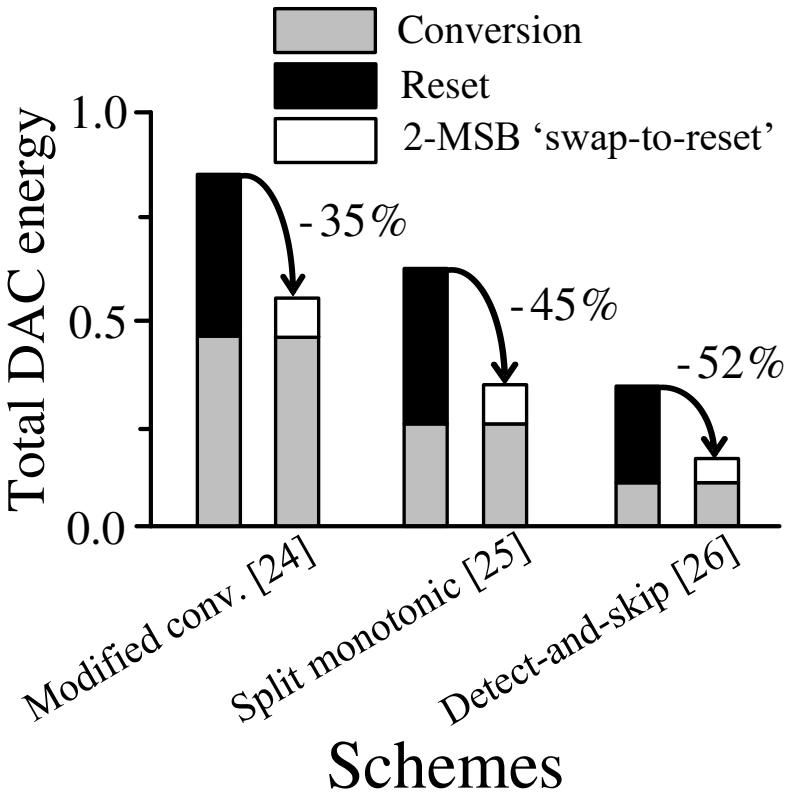


Figure 4.4: Normalized theoretical energy reduction after applying 2-MSB 'swap-to-reset' to [24, 25, 26].

4.3.3 Impact on input driver

As discussed before, the conventional reset will reset the DAC to the previous input voltage as shown in Figure 4.5 (a). For different input signal frequencies, the required voltage step during tracking is different: as shown in Figure 4.5 (a), for the conventional reset, this voltage change is small ($|\Delta V_1| \downarrow 0$) for a low-frequency input (V_{IN1}) while it can be large ($|\Delta V_2| \leq V_{REF}$) for a high-frequency input (V_{IN2}), which imposes a burden on the input driver in terms of driving strength, especially for higher input frequencies (Figure 4.5 (c)). For 'swap-to-reset' as shown in Figure 4.5 (b) this voltage change is restricted within $\frac{1}{2}V_{REF}$ ($|\Delta V_3|$) and frequency-independent, which relaxes the required driving strength of the input driver. This is why some SAR ADCs will set the DAC outputs to V_{CM} after conversion intentionally [34] while 'swap-to-reset' brings this benefit inherently. As a quantitative example: when V_{REF} = 0.8V, C_T = 9.0pF, f_{sample} = 40kS/s and further assuming that the

tracking time is 50% of the sampling period, the driver driving the conventional ADC requires at least 0.6μA of output current to charge C_T in time up to V_{REF}. With swap-to-reset, the driver's output current is reduced by 2x to 0.3μA (Figure 4.5 (c)). These values and the factor 2 reduction are significant when compared to the ADC's power consumption which is shown to be 0.4μW (later in TABLE 4-2).

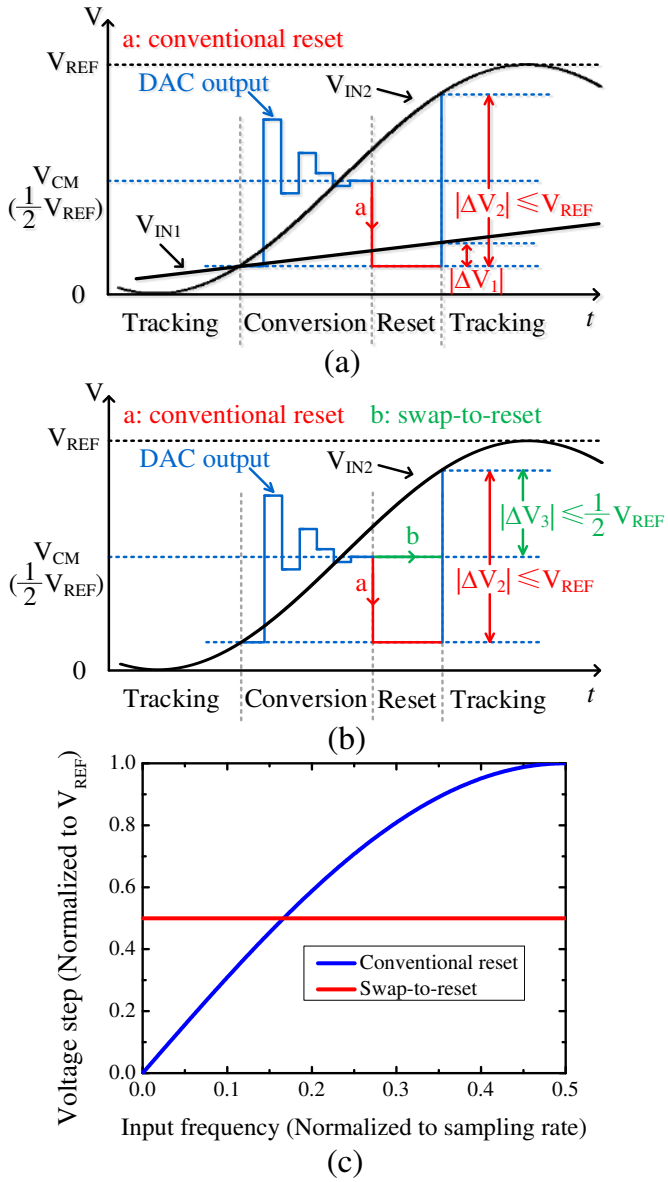


Figure 4.5: Impact of conventional reset (a) and 'swap-to-reset' (b) on SAR ADC input driver illustrated in time, and as a function of the input signal frequency (c).

4.4 Impact of non-idealities

Above discussions are based on the assumption that the DAC is ideally binary scaled without parasitics and mismatch. In practice, non-idealities are inevitable, hence the sensitivity of 'swap-to-reset' to the non-idealities needs to be discussed.

4.4.1 Impact on energy savings and distortion

In practice, due to the interconnections and transistors, parasitic capacitance is inevitable and has impact on the consumed energy and the performance of a SAR ADC. As shown in Figure 4.6, there are two important types of parasitic capacitance. The swap switches will introduce parasitic capacitance between the DAC outputs and GND ($C_{A,\,K\text{-}i}$, $C_{B,\,K\text{-}i}$), and the 'inverters' driving the DAC array lead to $C_{C,\,K\text{-}i}$ at the output of the drivers.

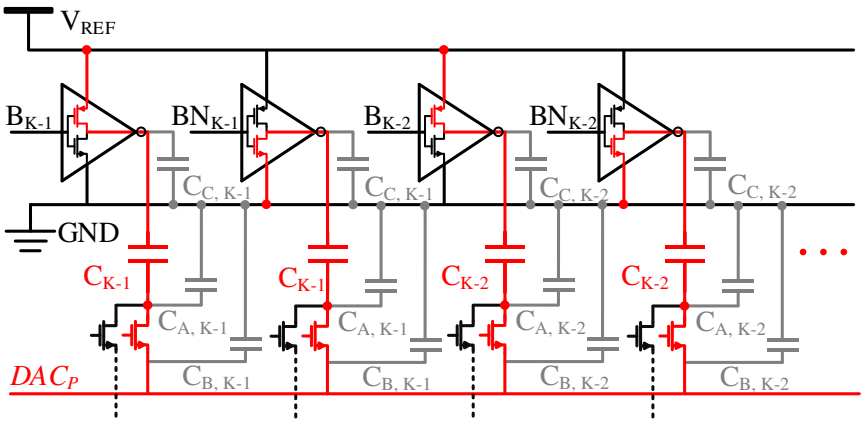


Figure 4.6: DAC array with parasitic capacitance (P side).

$C_{A,\,K\text{-}i}$ and $C_{B,\,K\text{-}i}$ will attenuate the full scale input range of the SAR ADC and increase the conversion energy slightly due to the increased total capacitance. Accordingly, (3-15) should be rewritten as:

$$E_{Conversion,\mathrm{pa}} = \sum_{i=1}^{K-1} C_{K-i} \cdot (1 - 2C_{K-i} / (C_T + C_{TP})) \cdot \mathrm{V}_{REF}^2 > 0.33 C_T \, \mathrm{V}_{REF}^2 \qquad (4\text{-}3)$$

where C_{TP} denotes the sum of $C_{A,\,K\text{-}i}$ and $C_{B,\,K\text{-}i}$ at one side. Since $C_{A,\,K\text{-}i}$ and $C_{B,\,K\text{-}i}$ are mainly the switch junction capacitance, they will change with the voltage at node DAC_P and might introduce signal-dependent charge injection, distorting the SAR conversion. Consequently,

the size of the switches has to be minimized sufficiently to make the signal-dependency of $C_{A,K-i}$ and $C_{B,K-i}$ negligible compared to the value of C_T.

$C_{C,K-i}$ will be switched and consume extra energy during both conversion and reset. However, with 'swap-to-reset', the DAC is reset by swapping rather than switching the capacitors, which also applies to the parasitic capacitance $C_{C,K-i}$. Consequently, the charge on $C_{C,K-i}$ is also preserved thanks to swapping and no reset energy is dissipated by $C_{C,K-i}$. The size scaling of $C_{C,K-i}$ may vary from the size of the inverters or the layout of the interconnection and it is usually not binary scaled. As an example, here it is assumed that $C_{C,K-i}$ is constant and equal to $0.01C_T$ for each capacitor. The energy saving of 'swap-to-reset' considering parasitic capacitance is shown in Figure 4.7. Compared to Figure 4.3, 2-bit 'swap-to-reset' saves less than 75% of the total reset energy now, since $C_{C,K-i}$ is not binary scaled. However, in absolute sense, the energy saving has increased thanks to energy-free swapping of a part of the parasitic $C_{C,K-i}$.

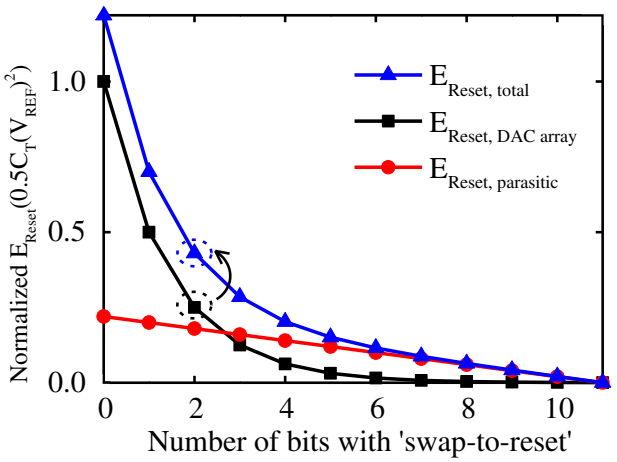


Figure 4.7: Normalized E_{Reset} considering parasitic capacitance of a 12b split monotonic SAR ADC with 'swap-to-reset' applied to a different number of bits.

4.4.2 Impact on ADC dynamic performance

'Swap-to-reset' swaps the positions of capacitors between N and P sides according to the previous conversion code to save energy, which implies that the DAC network is changing dependent on the input signal. This sub-section discusses the impact of 'swap-to-reset' on the dynamic performance from 3 aspects: systematic capacitor mismatch, random capacitor mismatch, and input signal dependency.

In order to perform a binary search in a SAR conversion, an accurate binary-scaled voltage shift after each comparison is required. However, even when the capacitors at both P and N side of the array are perfectly binary scaled, there can still be a systematic mismatch between P and N sides. This can be expressed as follows, where α indicates the systematic mismatch between P and N side:

$$\alpha = \frac{C_{N,K-i}}{C_{P,K-i}} - 1 = \frac{C_{TN}}{C_{TP}} - 1 \tag{4-4}$$

where C_{TP} and C_{TN} denote the total capacitance at P and N sides, respectively. According to Figure 3.1, the differential DAC voltage shift can be expressed as:

$$\Delta V_{DAC,i} = \left(\frac{C_{P,K-i}}{C_{RP,K-i} + C_{P,K-i}} + \frac{C_{N,K-i}}{C_{RN,K-i} + C_{N,K-i}}\right) \cdot V_{REF,ADC} \tag{4-5}$$

where $C_{RP,K-i}$ and $C_{RN,K-i}$ are the total capacitance at each side excluding $C_{P,K-i}$ and $C_{N,K-i}$ respectively. (4-5) can be simplified by replacing $C_{N,K-i}$ and $C_{RN,K-i}$ using (4-4):

$$\Delta V_{DAC,i} = \frac{2C_{P,K-i}}{C_{RP,K-i} + C_{P,K-i}} \cdot V_{REF,ADC} \tag{4-6}$$

For the conventional reset, the systematic mismatch has no impact because the binary voltage steps are maintained. If $C_{P,K-i}$ and $C_{N,K-i}$ are swapped and assuming the other capacitors remain at the original sides, (4-5) now equals to:

$$\Delta V_{DAC,i} = \left(\frac{(1+\alpha) \cdot C_{P,K-i}}{C_{RP,K-i} + (1+\alpha) \cdot C_{P,K-i}} + \frac{C_{P,K-i}}{(1+\alpha) \cdot C_{RP,K-i} + C_{P,K-i}}\right) \cdot V_{REF,ADC} \tag{4-7}$$

which is different from (4-6) and will cause non-binary steps, degrading the performance. The Matlab simulations in Figure 4.8 show the impact on ENOB and SFDR when changing the ratio of $C_{N,K-i}/C_{P,K-i}$ (simultaneously for all i=1, 2, 3, …, K-1). For conventional reset, the performance is not affected as the systematic mismatch does not induce non-binary scaling. If 'swap-to-reset' is utilized, the swap operation between $C_{P,K-i}$ and $C_{N,K-i}$ will cause non-linearity and degrade the SFDR. However, as a few percent of systematic mismatch can be tolerated before the performance is affected, this should not be a critical issue in practice.

With the presence of random mismatch, the voltage steps using conventional reset (4-5) and 'swap-to-reset' (4-7) are both non-binary. Considering the case i=1 where the nominal value of $C_{RP,K-1}$ and $C_{RN,K-1}$ is equal to $3 \cdot C_{P,K-1}$ and the nominal value of $C_{N,K-1}$ equal to $C_{P,K-1}$ (split

monotonic as shown in Figure 3.1), the nominal DAC voltage shift, $\Delta V_{DAC,1}$, equals to $0.5 \cdot V_{REF,ADC}$. For the simplicity of the simulation, $C_{RN,K-1}$ is fixed at $3 \cdot C_{P,K-1}$, $C_{N,K-1}$ is fixed at two extreme values, $0.95 \cdot C_{P,K-1}$ (α=-0.05) and $1.05 \cdot C_{P,K-1}$ (α=0.05) respectively, and $C_{RP,K-1}$ is swept between $2.9 \cdot C_{P,K-1}$ and $3.1 \cdot C_{P,K-1}$ as shown in TABLE 4-1.

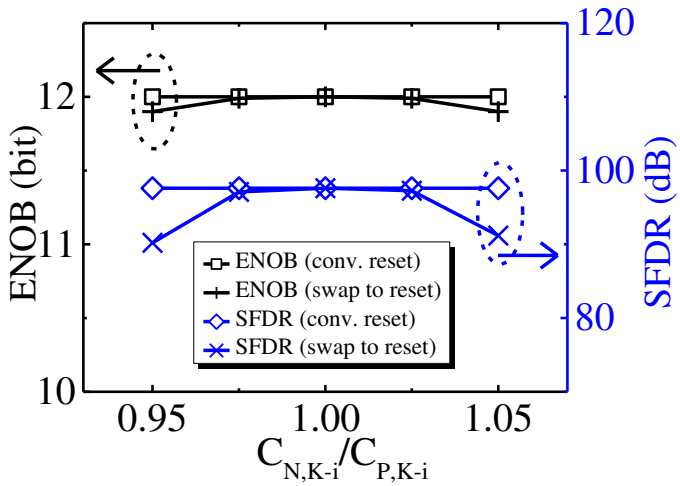


Figure 4.8: Dynamic performance of a SAR ADC with conventional reset and 'swap-to-reset' at different $C_{N,K-i}/C_{P,K-i}$ and near-Nyquist input.

TABLE 4-1: Capacitors value configuration for simulations.

Case	$C_{P,K-1}$	$C_{RP,K-1}$	$C_{N,K-1}$	$C_{RN,K-1}$
I	$C_{P,K-1}$	[$2.9 \cdot C_{P,K-1}$, $3.1 \cdot C_{P,K-1}$]	$0.95 \cdot C_{P,K-1}$	$3 \cdot C_{P,K-1}$
II	$C_{P,K-1}$	[$2.9 \cdot C_{P,K-1}$, $3.1 \cdot C_{P,K-1}$]	$1.05 \cdot C_{P,K-1}$	$3 \cdot C_{P,K-1}$

Now, the extra DAC voltage shift error introduced by 'swap-to-reset' compared to conventional reset can be evaluated:

$$ERR(\%) = \frac{V_{DAC,i}(s-to-r) - V_{DAC,i}(conv.-reset)}{V_{DAC,i}(conv.-reset) - 0.5 \cdot V_{REF,ADC}} \times 100\% \quad (4\text{-}8)$$

The simulated ERR versus $C_{RP,K-1}$ at Case I and II is shown in Figure 4.9. The extra error introduced by 'swap-to-reset' is at most 5% of the original error caused by the mismatch. Since mismatches are typically small, this additional 5% is even much smaller and can be ignored for practical situations. On top of that, the additional max 5% error can either add or subtract from the original error, giving equal probabilities to improving or degrading the final performance. Above discussion is further verified by the simulated SNDR and SFDR in Matlab (Figure 4.10) and also the measurement results to be shown later.

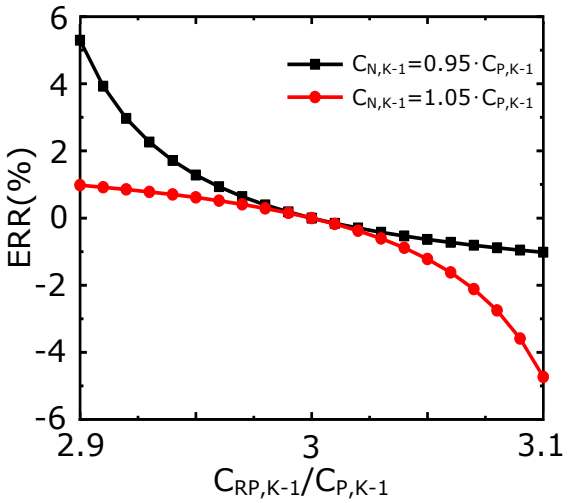


Figure 4.9: Simulated extra DAC voltage shift error (ERR) introduced by the 'swap-to-reset' operation with random mismatch.

Figure 4.10 shows the average ENOB and SFDR over 200 Monte Carlo runs with different amounts of random mismatch applied to all capacitors in the ADC (σ_{C_1}/C_1, where σ_{C_1} is the standard deviation of the unit capacitor. Subsequently, the standard deviation of each capacitor can be derived: $\sigma_{C_{K-i}}=\sigma_{C_1}\cdot\sqrt{(C_{K-i}/C_1)}$, i=1, 2, 3, …, K-1). As can be seen, conventional reset and 'swap-to-reset' have the same sensitivity to random mismatch, corresponding to previous discussion.

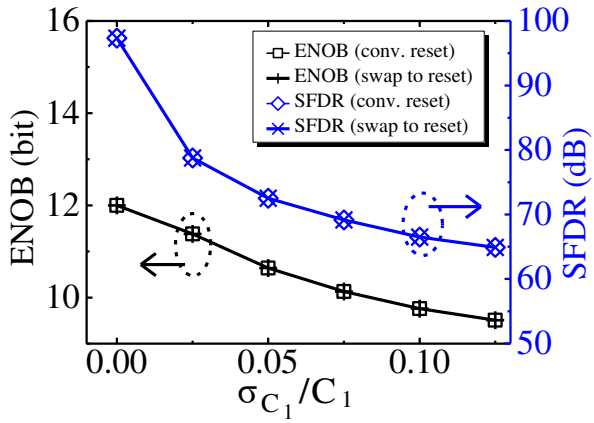


Figure 4.10: Average dynamic performance of a SAR ADC with conventional reset and 'swap-to-reset' at different σ_{C_1}/C_1 and near-Nyquist input (200 runs each).

Since the activity of 'swap-to-reset' depends on the last input signal, it principally causes

nonlinearity which can depend on the input frequency. In order to explore the significance of this impact, the above dynamic performance simulations are conducted at different input frequencies with $\sigma_{C_1}/C1 = 0.05$. As shown in Figure 4.11, the dynamic performances of a SAR ADC with conventional reset and 'swap-to-reset' still overlap each other.

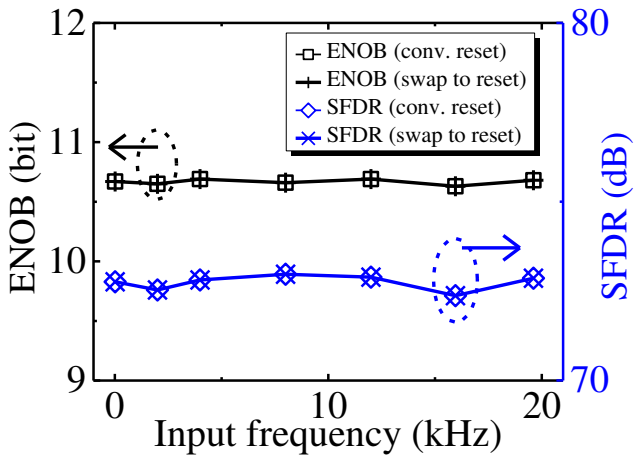


Figure 4.11: Average dynamic performance of a SAR ADC with conventional reset and 'swap-to-reset' at different input frequencies ($\sigma_{C_1}/C1 = 0.05$, 200 runs).

To summarize, the swap operation will not result in dynamic performance degradation in presence of random mismatch of the DAC array. This will be validated by measurements. However, systematic variations do have more impact and should be kept small enough.

4.5 A 12b 40kS/s SAR ADC with 'swap-to-reset'

In order to demonstrate the energy saving of the presented 'swap-to-reset' technique, it is utilized in a 12b asynchronous SAR ADC utilizing a split monotonic DAC, the architecture of which is illustrated in Figure 4.12. The clock for the logic is generated internally as in [35] hence only the sample clock is required externally. The SAR ADC uses bootstrapped switches to sample the inputs for the sake of good linearity. Moreover, a power-efficient bi-directional comparator [36] is adopted to reduce the energy consumption further.

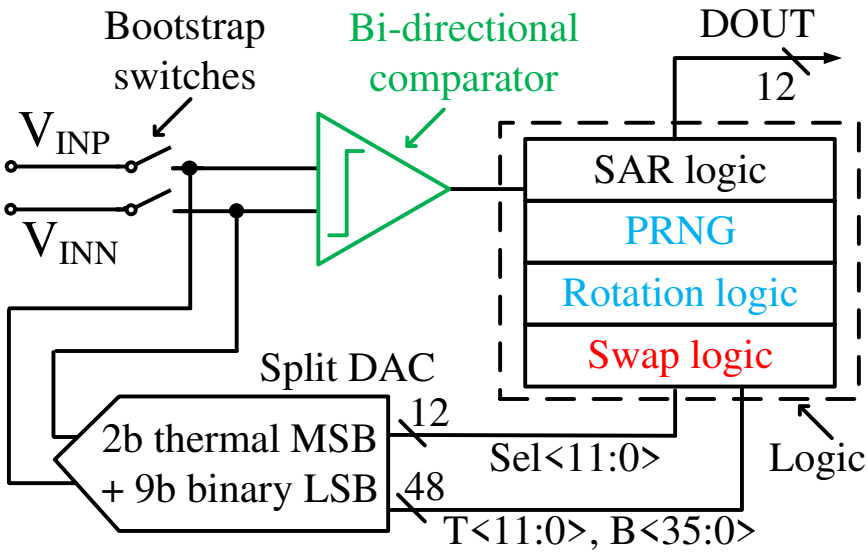


Figure 4.12: Architecture of the 12b SAR ADC with 'swap-to-reset'.

4.5.1 Split monotonic DAC

The DAC of the SAR ADC adopts the split monotonic scheme as shown in Figure 4.13. The 2 MSBs of the DAC use thermal encoding while the remaining 9b are binary scaled. Each capacitor is driven by an inverter to switch between V_{REF} and GND. Lateral metal-metal capacitors [37] are adopted to implement the DAC and the split unit capacitance for the LSB is 2.2fF, leading to a total capacitance of 9.0pF at each side. As shown in Figure 4.13, because of the differential structure and the split monotonic scheme, a total of 12 equally-sized (1.1pF) capacitors is needed for the 2 unary coded MSBs. The 2 MSBs utilize 'swap-to-reset' to save reset energy and a random rotation [38] to realize dynamic element matching to improve the linearity of the SAR ADC. These 2 operations are orthogonal and have no impact on the function of each other, which will be verified by the measurement results later.

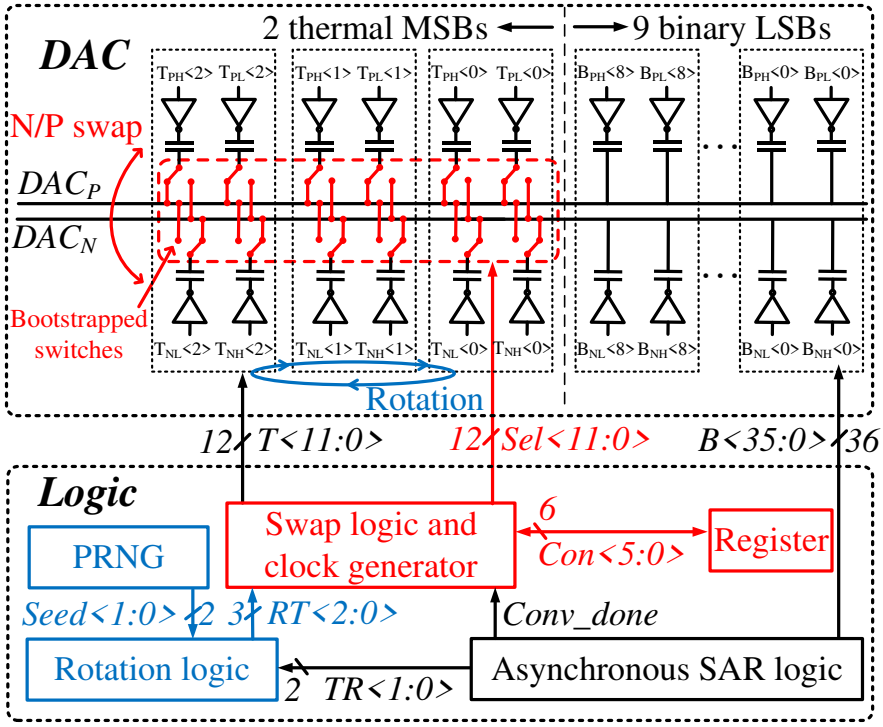


Figure 4.13: The DAC and the logic with 'swap-to-reset' and rotation.

4.5.2 Swap-to-reset

As shown in Figure 4.13, in order to swap the N/P connections of the 2 MSBs, 2 switches are required for each capacitor, resulting in a total of 24 switches while only 12 switches will be closed at the same time. Bootstrapped switches are utilized here as shown in Figure 4.14and the gate voltage of the NMOS switches ($M_{5,6}$) can be shifted to 1.8·VDD to improve the linearity. As discussed previously, the size of each switch is set to 1.5µm/60nm to minimize $C_{A,K\text{-}i}$ and $C_{B,K\text{-}i}$. The simulated $C_{A,K\text{-}i}$ and $C_{B,K\text{-}i}$ change from 620aF to 784aF when changing DAC_P from 0 to V_{REF}, which is negligible compared to C_T (9.0pF). Note that in case of a smaller C_T, the switches could be downscaled proportionally to maintain the same speed and linearity. For any differential capacitor pair, the N/P connections are complementary hence the 2 corresponding switches can share the same bootstrapped block as shown in Figure 4.14 and 12 bootstrapped clock signals (*Sel<11:0>*) are required. These signals are generated based on the N/P connections at the end of the last conversion (*Con<5:0>*) tracked by a register, since this determines which capacitors should be swapped during reset and the capacitor assignment in the very next conversion. Since the DAC is

complementary, it is sufficient to monitor the 6 capacitors at the P side (*Con<5:0>*).

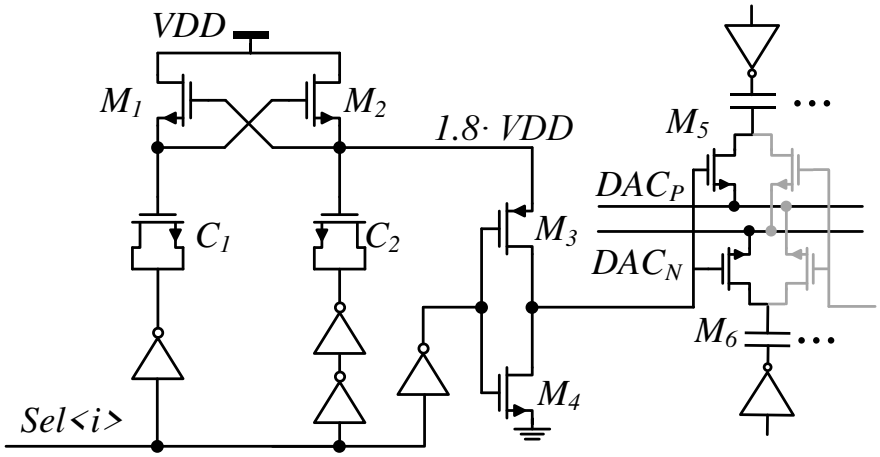


Figure 4.14: Bootstrapped switches for the 'swap-to-reset' operation.

The operation of 'swap-to-reset' is further demonstrated with key node waveforms in Figure 4.15, where the unary MSB capacitor DAC_TPH<2> and binary LSB capacitor DAC_B_{PH}<8> are chosen as an example; the remaining MSB and LSB capacitors operate similarly. *Clk_sample* is the sample clock of the SAR ADC and one conversion starts at the rising edge of *Clk_sample* ($t_{0,\,4,\,8}$). During conversion, the DAC is switched according to *Comp<i>*, the *i*-th comparison result in the conversion. For DAC_T_{PH}<2>, the current N/P connection also determines the DAC switching. For instance, during both $t_0 \sim t_1$ and $t_8 \sim t_9$, *Comp<1>* equals 0, but DAC_T_{PH}<2> is switched oppositely since it is connected to P (*Con<5>*=1 during $t_0 \sim t_1$) and N (*Con<5>* = 0 during $t_8 \sim t_9$) side respectively. As discussed previously, 'swap-to-reset' should be conducted prior to the conventional reset applied to the LSBs. In the SAR ADC of this work, the end of a conversion is indicated by *Conv_done*, which is adopted to trigger 'swap-to-reset' ($t_{1,\,5,\,9}$). At this moment, the N/P connection is stored in the register (*Con<5>*) and all the swap switches are opened (*Sel<11:10>=0*) as preparations for the swap operation. A rising edge (*Clk_BS*) is then generated from *Conv_done* by a delay chain shown in Figure 4.16. *Con<5>* decides whether *Sel<11>* or *Sel<10>* will copy this rising edge to bootstrap the corresponding switches and perform a swap operation ($t_{2,\,10}$) or keep the previous N/P connection (t_6). After the MSBs are swapped and reset, the LSBs are reset conventionally and the tracking phase starts ($t_{3,\,7,\,11}$).

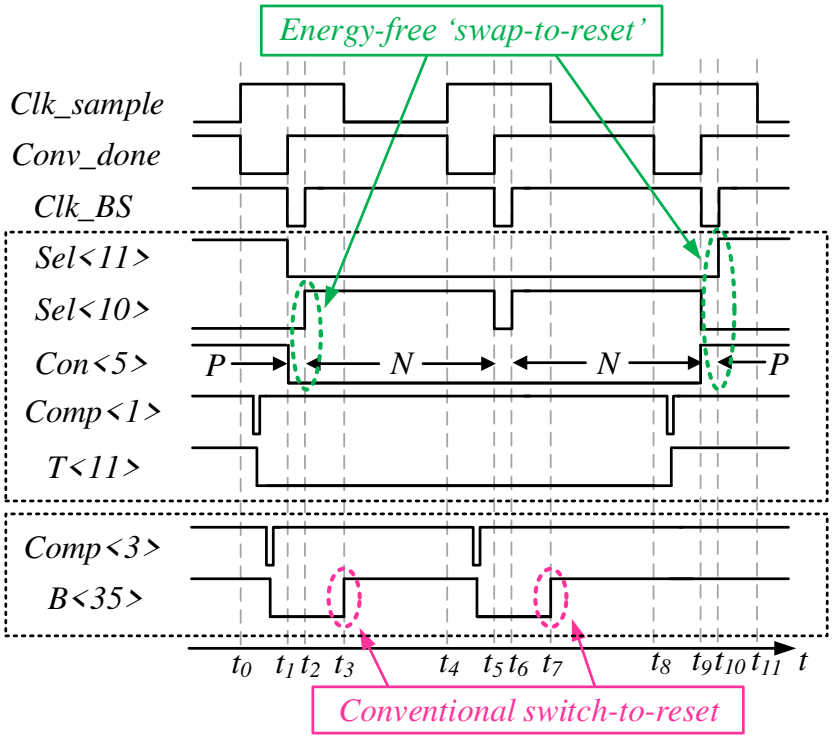


Figure 4.15: Key node waveforms of the 'swap-to-reset' operation.

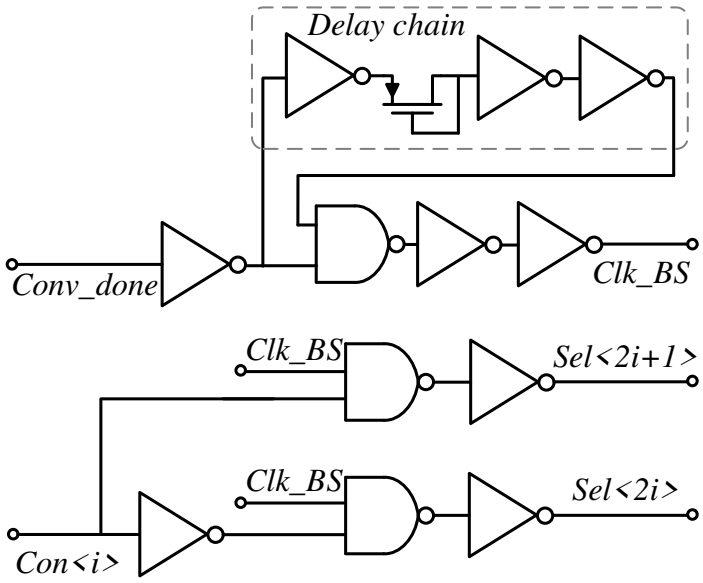


Figure 4.16: Clock generation for the swap switches.

Although the 'swap-to-reset' operation does not consume energy from V_{REF}, the

bootstrapped swap switches will consume extra energy as does the additional logic. In schematic simulations, the 'swap-to-reset' saves 45% of the total DAC energy as expected, while the swap switches and logic consume 5.4% more energy, resulting in a total energy saving of 39.6%.

4.5.3 Rotation

Rotation of the MSB capacitors [38] changes the position of the capacitors in each conversion and enhances the linearity. In this work, rotation is applied to the 3 unary elements encoding the 2 MSBs so that a random sequence ranging from 0 to 2 is required to indicate the random rotation. For this purpose, a pseudo random number generator (PRNG) is integrated, based on the maximum length sequence (MLS) [39] as shown in Figure 4.17. It is a 3-level 6-th order MLS generator, resulting in a pseudo random sequence with a periodic length of 728 (= $3^6 - 1$). 12 D flip-flops are utilized here for the 2b *Seed<1:0>* and the clock signal is equal to the sampling clock of the ADC, leading to a new random number for each conversion. The current and next *Seed<1:0>*'s are fed back through a sum and modulo-3 operation to the first D flip-flops. For this architecture, a sequence of 0's is also stable hence an *Rst* signal is presented to initialize the PRNG and avoid a sequence of 0's. This scheme is very low cost in hardware and the power consumption of this PRNG is less than 1% of that of the SAR ADC.

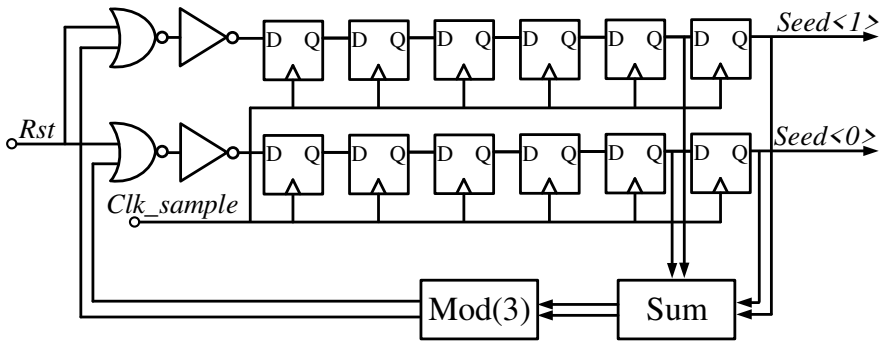


Figure 4.17: The PRNG based on MLS.

As shown in Figure 4.13, the 2 MSBs *TR<1:0>* are first decoded to a 3b rotated *RT<2:0>* guided by *Seed<1:0>*. Subsequently, *RT<2:0>* is transferred to *T<11:0>* based on the current N/P connections (*Con<5:0>*).

4.5.4 Floorplan of the DAC layout

Different from most DAC designs where the top plates of the capacitors are fixed to either P or N side of the DAC, the 'swap-to-reset' needs the flexibility to swap the top plates between P and N sides, leading to a different layout floor plan as shown in Figure 4.18. The DAC adopts lateral metal-metal capacitors [41] that are categorized into the 12 unary MSB cells and the 9b binary LSB cells. The DAC output nodes, DACP and DACN, are routed horizontally while the capacitor cells are placed vertically in order to swap between DACP and DACN. Two switches for the swapping operations are inserted for each 1.1pF unary cell and the bootstrap circuits are placed close to the switches to reduce the parasitic capacitance of the routing. To improve matching, the DAC is symmetric and dummy switches are inserted for the LSB array to ensure matching between the 9b LSB cells and the 12 MSB unary cells.

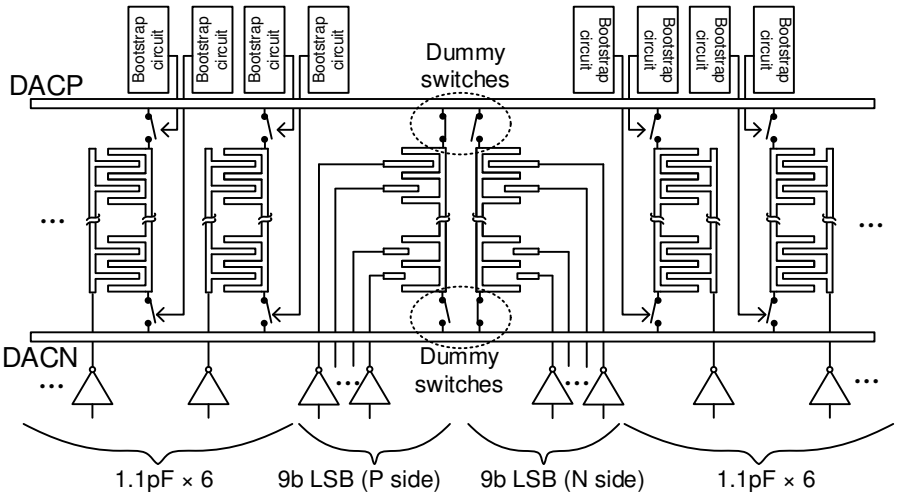


Figure 4.18: Floor plan of the DAC layout.

4.5.5 2D-exchangeable MSB capacitors

After applying 'swap-to-reset' and rotation, the capacitors of the 2 MSBs become exchangeable in two dimensions: each capacitor can be exchanged between P and N sides by 'swap-to-reset' and within P or N side by rotation. The DAC with exchangeable MSB capacitors improves the energy-efficiency and the linearity of the SAR ADC at the same time.

4.5.6 Experimental results

Die photo

The 12b SAR ADC is fabricated in 65nm CMOS technology occupying a chip area of 0.105mm^2 (Figure 4.19). The extra control logic and bootstrapped switches for 'swap-to-reset' occupy a chip area of 0.0024mm^2, which is about 2.3% of the total ADC chip area.

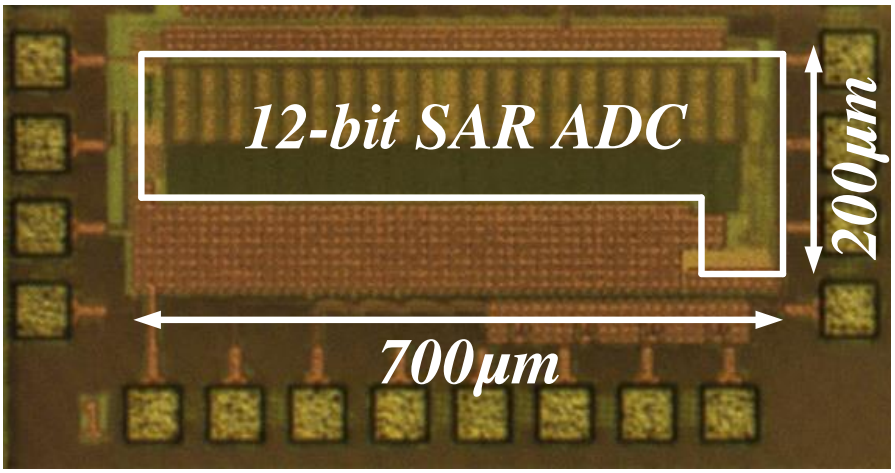


Figure 4.19: Die photo in 65 nm.

Power saving of 'swap-to-reset'

The SAR ADC operates at 0.8V VDD and 40kHz sampling frequency and the power consumption is shown in Figure 4.20. With both rotation and 'swap-to-reset' off, the SAR ADC consumes 450nW of which the DAC consumes 286nW (63.6%) (Column 1). By enabling 'swap-to-reset', 33% of the DAC power is saved while the remainder of the SAR ADC consumes 7% more power due to the auxiliary circuits of 'swap-to-reset', resulting in a total power saving of 18% for the entire SAR ADC, while the DAC now consumes 51% of the total SAR ADC power (Column 2). The 33% DAC power saving is less than the expected 45% (based on theory and schematic simulations), which is due to the parasitic capacitances $C_{C,\,K\text{-}i}$ (Figure 4.6 and Figure 4.7). Since rotation has no influence on the power saving of 'swap-to-reset', almost the same power saving is achieved when above measurements are repeated with rotation on despite the slight additional power introduced by the rotation logic (Column 3 and 4).

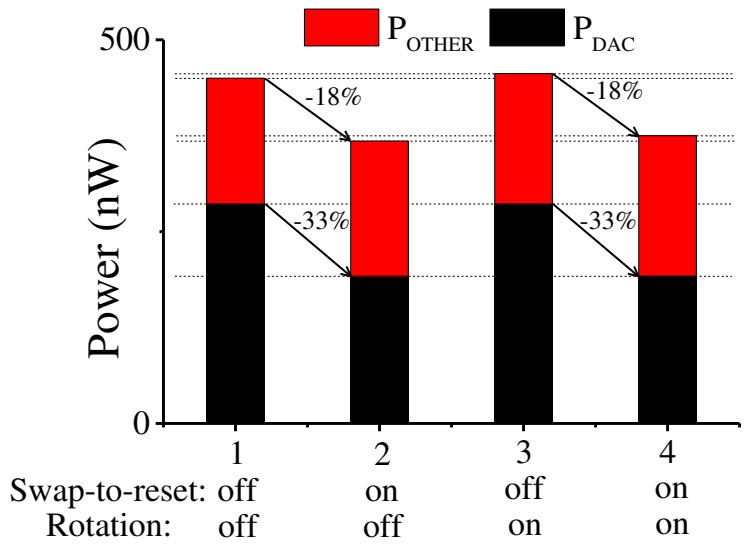


Figure 4.20: Measured ADC power with conventional reset and 'swap-to-reset'.

Dynamic and static performance

A near-Nyquist tone spectrum of the SAR ADC is measured with 4 combinations of enabling and disabling 'swap-to-reset' and rotation as shown in Figure 4.21. Regardless of 'swap-to-reset', rotation maintains the same SNDR (~64.2dB) and improves the SFDR by around 15.5dB as shown by Figure 4.21 (a) vs. (b) and Figure 4.21 (c) vs. (d). Regardless of rotation, enabling 'swap-to-reset' will maintain the same SNDR and SFDR shown by Figure 4.21 (a) vs. (c) and Figure 4.21 (b) vs. (d), which matches well with the previous discussion. The linearity improvement of rotation can be further observed in the INL/DNL plots as shown in Figure 4.22 with enabled 'swap-to-reset'. Without rotation, the INL error is relatively large for the 2MSBs, most likely caused by non-symmetrical layout of the MSB capacitors. With rotation enabled, this is resolved and INL remains within 1LSB. The SNDR and SFDR are also measured at different input frequencies with enabled 'swap-to-reset' and rotation (Figure 4.23). The performance is consistent throughout the Nyquist bandwidth. Above measurements reveal that 'swap-to-reset' and rotation are orthogonal and they have no impact on each other's function, which makes it suitable to combine these two techniques in the same design. By enabling 'swap-to-reset' and rotation, the SAR ADC achieves better energy-efficiency and better linearity at the same time.

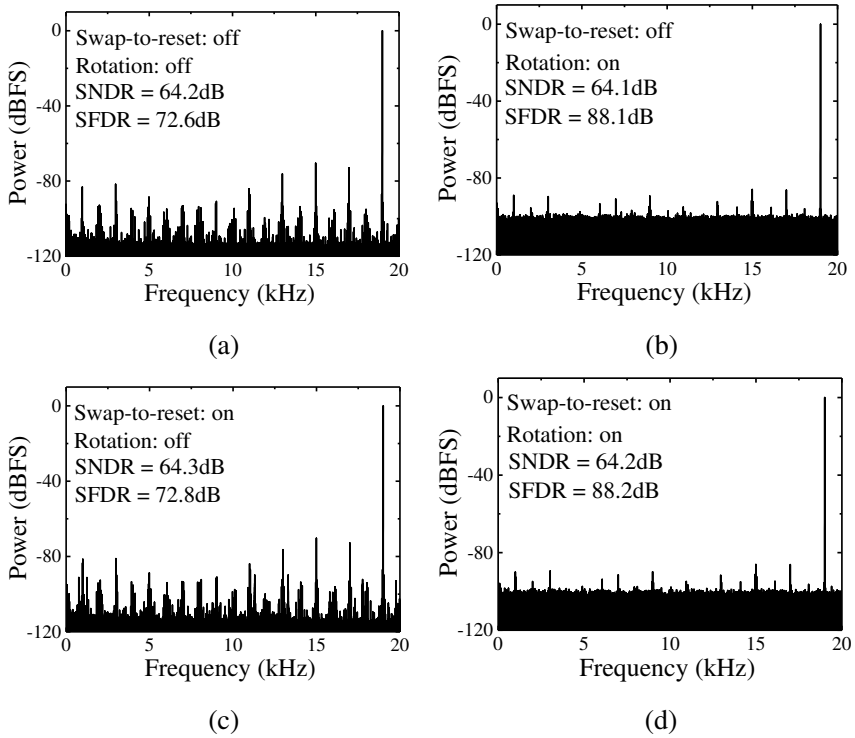


Figure 4.21: Measured spectrums with 4 combinations of enabling and disabling 'swap-to-reset' and rotation.

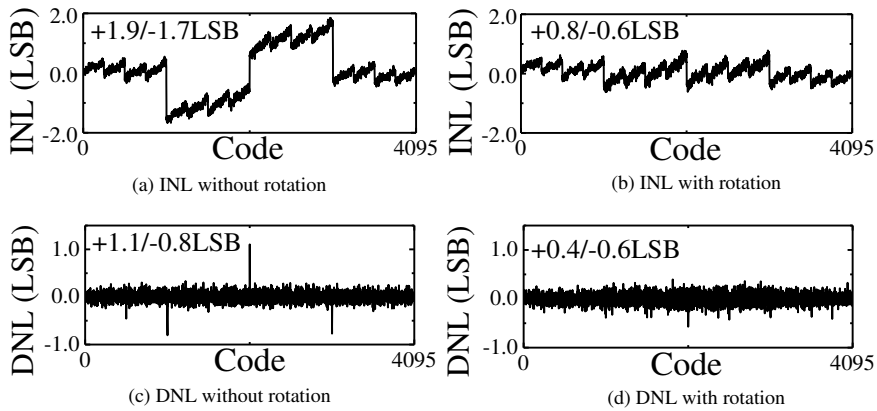


Figure 4.22: Measured INL/DNL before and after enabling rotation (with enabled 'swap-to-reset').

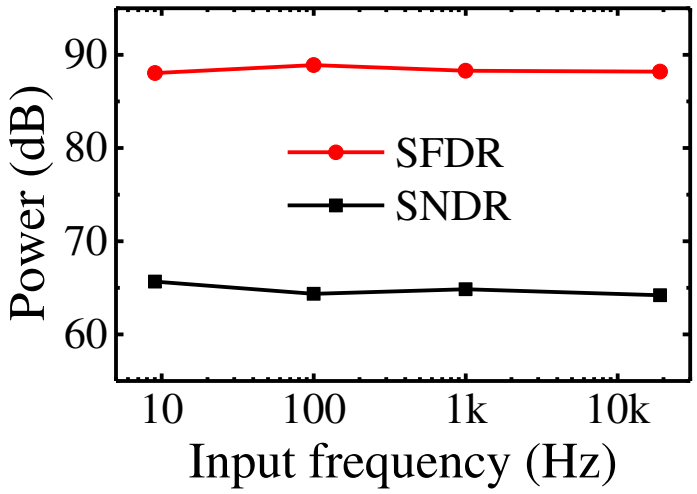


Figure 4.23: Measured SNDR and SFDR at different input frequencies with enabled 'swap-to-reset' and rotation.

Performance summary and comparison

The performance summary is shown in TABLE 4-2, together with a comparison to other low-power non-oversampled SAR ADCs. With 'swap-to-reset' and rotation, a FoM of 7.1fJ/conversion-step is achieved with high SFDR (88.2dB) in this work. [26], [40], [41], and [42] achieve a better FoM while at the cost of SFDR. [43] has slightly better SFDR but has a worse FoM. The FoM of this work is not outstanding compared to some work listed in the table. One of the reasons is the relatively large DAC capacitance (9pF) utilized. The good SFDR is attributed to the rotation operation among 2 MSBs, and the LSB part benefits from the relatively large DAC capacitance. The main goal of this prototype is to prove the validity of 'swap-to-reset' and the FoM is not specifically optimized. For [40] and [26], 'swap-to-reset' can also be utilized to reduce the DAC power and improve the power-efficiency further. As shown in Figure 4.24, Region II can be shifted towards the conversion energy axis thanks to the elimination of the reset energy.

TABLE 4-2: SAR ADC PERFORMANCE SUMMARY AND COMPARISON.

	This work		[40]	[26]	[41]	[42]	[43]
Year	**2016**		2014	2014	2017	2016	2016
Technology (nm)	**65**		65	40	65	40	65
Area (mm^2)	**0.105**		0.18	0.0065	0.03	0.01	0.28
VDD (V)	**0.8**		0.8	0.45	0.7	0.7	0.8
Sample rate (kS/s)	**40**		32	200	100	200	10
Resolution (bit)	**12**		12	10	11	12	14
Swap-to-reset	**Off**	**On**	-	-	-		-
Rotation	**Off**	**On**	-	-	-		-
Power (µW)	**0.45**	**0.38**	0.31	0.08	0.60	0.95	1.98
INL (LSB)	**1.9**	**0.8**	0.82	0.45	-	1.2*	2.26
DNL (LSB)	**1.1**	**0.6**	0.58	0.44	-	0.6*	2.28
SFDR (dB)	**72.8**	**88.2**	78.4	76.3	77.0*	80.1	88.8
SNDR (dB)	**64.3**	**64.2**	67.8	55.6	64.5	69.2	77.0
FoM (fJ/conv.-step)	**8.4**	**7.1**	4.8	0.85	4.5	2	34.2
P_{DAC}/P_{SAR}	**64%**	**51%**	51%	34%	16%	29%	20%
Switching scheme	**Split monotonic**		Modified conventional	Detect-and-skip	BBS [44]	ECR	Conven-tional
Applicability of 'swap-to-reset'	**Yes**		Yes	Yes	No	No	No

* Estimations from the plots

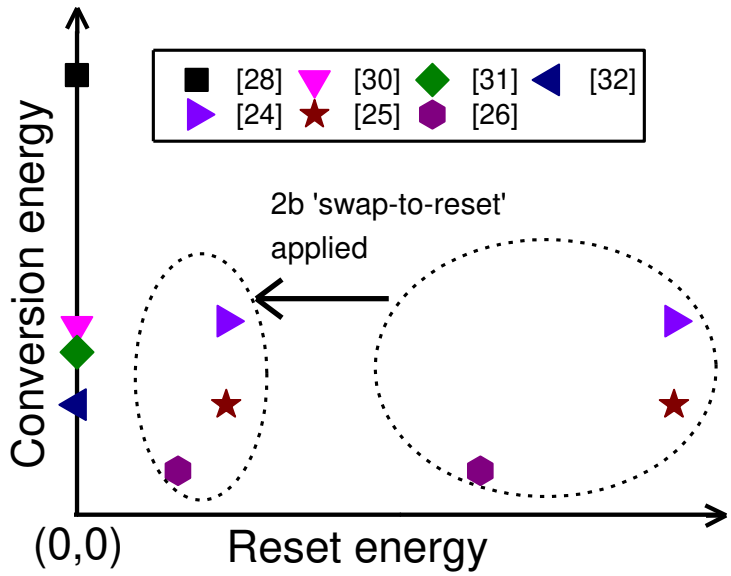


Figure 4.24: Change in reset energy for various switching schemes if 'swap-to-reset' is applied for the 2 MSBs.

4.6 Conclusions

In this chapter, an energy-free 'swap-to-reset' scheme is presented to deal with the large reset energy that is present for several recent low-power DAC switching schemes, by reusing the charge during reset. E.g., the schemes described in [24, 25, 26] consume a reset energy close to or higher than the conversion energy. As an example, for the split-monotonic scheme it was shown in Chapter 3 that the reset energy is about 1.5x the conversion energy. The 'swap-to-reset' can be utilized in all the differentially reset and switched DACs to make them reset energy free. Moreover, 'swap-to-reset' can be limited to only the MSB part of the DAC to save the majority of power while the rest of the DAC can use conventional reset for circuit simplicity. Essentially, this technique can shift the designs in Region II of Figure 3.6 towards Region I (Figure 4.24). The swap operation has no impact on the dynamic performance of the SAR ADC with the presence of DAC array mismatch. Along with rotation, a DAC is realized where each capacitor of the 2 MSBs can change positions between P and N sides ('swap-to-reset') and along P or N side (rotation). This improves the linearity (+15.4dB) and the energy efficiency (18%) of the SAR ADC at the same time.

Chapter 5 Low-power low-VDD voltage references

This chapter briefly reviews voltage references (VRs), from the conventional and modified bandgap references (also shortly called bandgaps or BGRs), to CMOS threshold-based VRs that are popular in low-power applications. Important specifications of VRs are explained and the advantages and disadvantages of BJT and MOSFET based bandgaps and four classes of threshold-based CMOS VRs are compared and discussed.

5.1 The role of the reference voltage

Reference voltages are essential in most SoCs (systems-on-chip), providing a stable voltage against power supply and process variations for sub-blocks, especially for ADCs and DACs as shown in Figure 5.1. In terms of temperature dependency, they should be designed according to the specific context. In many cases, a temperature-independent V_{REF} is required. However, the reference voltage sometimes needs to be designed with certain temperature coefficient (TC) to maintain a temperature-independence for a different parameter, e.g., G_m [18].

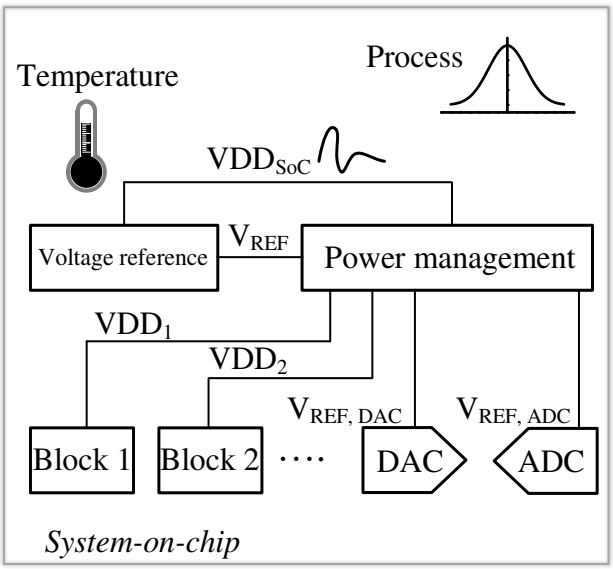


Figure 5.1: Reference-voltage generation in a SoC.

In this thesis, the voltage reference (VR) for SAR ADC conversion is the main concern. As shown in Figure 5.1, the reference voltage of a SAR ADC is usually generated by power management based on the output V_{REF} of the VR. Hence, the analog to digital conversion of an N-bit SAR ADC can be expressed as:

$$D_{OUT} = round(2^N \cdot \frac{V_{IN}}{V_{REF,\mathrm{ADC}}}) = round(2^N \cdot \frac{V_{IN}}{V_{REF}} \cdot \frac{1}{\beta}) \tag{5-1}$$

where D_{OUT} denotes the digital output code, V_{IN} is the analog input voltage, the full scale of V_{IN} is equal to $V_{REF,ADC}$, and β is an optional DC-DC coefficient in the power management block. It can be found that any disturbance or fluctuation on V_{REF} will be directly reflected on the digital output code D_{OUT}. Besides, the DC-DC coefficient should also be constant to realize an accurate conversion.

5.2 Important specifications

Process variation

During fabrication, process variation will occur inevitably to critical parameters such as gate oxide thickness, geometry, dopant depth, and so on, which will cause threshold voltage variations, mobility variations, etc. In order to maintain sufficient robustness of integrated circuits especially for mass production, process variations need to be modeled by the foundry for designers to keep adequate design margins.

In general, process variations are modeled from two aspects: corner variation and random mismatch. Corners represent the extremes of important parameter variations during fabrication from wafer to wafer and corner simulations indicate the variation range of certain specifications if fabricated in the specific technology. Random mismatch represents the parameter mismatch between nominally identical components and it is especially critical for analog circuits.

These two aspects are both important for VRs and relevant simulations are performed with a main focus on the variations of the output reference voltage. Since all the samples come from the same wafer in most VR publications, the measured variations among multiple samples mainly reflect the random mismatch.

For the corner simulations, the variation range divided by the mean value is used to evaluate the variations:

$$Variation(\%) = \frac{V_{REF,MAX} - V_{REF,MIN}}{E(V_{REF})} \times 100\% \quad (5\text{-}2)$$

where $V_{REF, MAX}$ and $V_{REF, MIN}$ are the maximum and minimum reference voltage in different process corners and $E(V_{REF})$ is the mean value. For random mismatch evaluation, the standard deviation is normally adopted.

VDD sensitivity

In low-power sensor systems, the power source can be a battery, an energy-harvesting supply, or the combination of the above two, while none of them might provide a stable supply voltage. Hence, VRs must provide sufficient immunity against power supply fluctuations. VDD sensitivity can be evaluated from two metrics: DC and AC behavior. Line sensitivity represents how much the DC output reference voltage changes with power supply on average:

$$LS(\%/\mathrm{V}) = \frac{V_{REF,MAX} - V_{REF,MIN}}{E(V_{REF}) \cdot (V_{DD,MAX} - V_{DD,MIN})} \times 100\% \quad (5\text{-}3)$$

where $V_{REF, MAX}$ and $V_{REF, MIN}$ are the maximum and minimum reference voltage when changing power supply from $V_{DD, MIN}$ to $V_{DD, MAX}$ respectively and $E(V_{REF})$ is the mean value.

PSRR describes the immunity against power supply variations, defined as the reciprocal of the AC gain from power supply to output V_{REF}:

$$PSRR(\mathrm{dB}) = 20\log(\frac{V_{dd}}{V_{ref}}) \quad (5\text{-}4)$$

where V_{ref} and V_{dd} are the small signal component of the power supply and the reference voltage.

Temperature dependency

Many parameters in integrated circuits are temperature-dependent, while a temperature-independent reference voltage is required in many cases. For an ADC, the reference voltage determines the full-scale input range and a variable reference voltage will deteriorate the conversion as seen from (5-1). Temperature dependency is usually evaluated by the temperature coefficient:

$$TC(\text{ppm/}^\circ\text{C}) = \frac{V_{REF,MAX} - V_{REF,MIN}}{E(V_{REF}) \cdot (\mathrm{T}_{MAX} - \mathrm{T}_{MIN})} \times 10^6 \quad (5\text{-}5)$$

where $V_{REF, MAX}$ and $V_{REF, MIN}$ are the maximum and minimum reference voltage when changing the temperature from T_{MIN} to T_{MAX} and $E(V_{REF})$ is the mean value. In this thesis, all the VR designs are optimized to achieve a low temperature coefficient.

Power consumption

For low-power sensor applications, the power consumption of the VR should also be low. In some occasions, the system can only tolerate sub-nW power consumption for the VR [45].

Minimum VDD

For low-power sensor applications, the VDD is usually low to achieve low-power consumption. Hence, the VR must be able to operate at low VDD (e.g., sub-1V).

Technology compatibility and scalability

The VR should be compatible with the selected technology for the sensor system to avoid extra cost during fabrication. Moreover, the VR design should also be friendly with respect to technology scaling.

Chip area

As discussed in Chapter 2, large chip area will reduce the density of integration and increase the cost so that small chip area is important especially for low-cost low-power applications.

5.3 Bandgap references

Bandgap voltage references are references where the output voltage is derived from the bandgap of the semiconductor material used. In this sub-chapter, bandgap references based on both BJTs and MOSFETs are reviewed and compared.

5.3.1 BJT-based bandgap references

Speaking of VRs, BJT-based bandgaps are the most popular architecture. One example of a conventional BJT-based bandgap is shown in Figure 5.2 [18]. Q_1 and Q_2 are both PNP BJTs

and Q_2 is n times larger than Q_1. For a PNP device, the collector current can be expressed as:

$$I_C = I_S \cdot \exp(\frac{V_{EB}}{V_T}) \tag{5-6}$$

where I_S is the saturation current, V_{EB} is the emitter-base voltage, and V_T is the thermal voltage. The negative feedback composed of the OPAMP and resistors forces V_X equal to V_Y so that the current flowing through R_1 (I_1) and R_2 (I_2) is the same (R_1 equal to R_2). Then we can express the emitter-base voltage difference of PNP Q_1 and Q_2 as:

$$V_{EB1} - V_{EB2} = V_T \ln\frac{I_1}{I_{S1}} - V_T \ln\frac{I_2}{nI_{S1}} = V_T \ln(n) \tag{5-7}$$

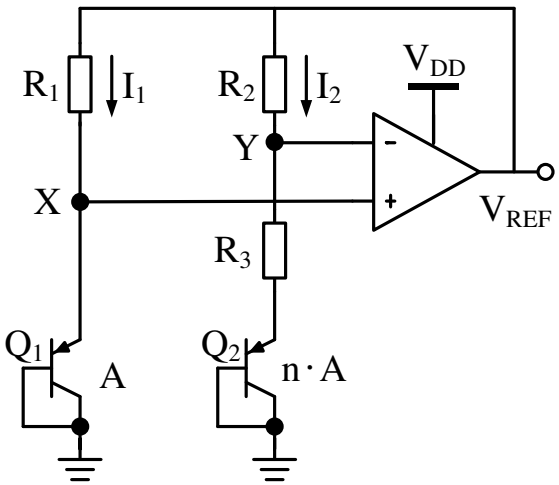


Figure 5.2: Example of a BJT-based conventional bandgap.

Subsequently, V_{REF} can be expressed as:

$$V_{REF} = V_{EB2} + \ln(n) \cdot (1 + \frac{R_2}{R_3}) V_T \tag{5-8}$$

In order to achieve a temperature-independent V_{REF}, ratio n and R_2/R_3 should be chosen carefully to realize $\partial V_{REF}/\partial T \approx 0$. At this point, V_{REF} can be expressed as [18]:

$$V_{REF} = \frac{E_g}{q} + (4 + m) V_T \tag{5-9}$$

where E_g is the bandgap energy of silicon (1.18eV) and m is temperature index of mobility equal to -1.5 approximately. When T approaches 0, V_{REF} is equal to E_g/q which is the reason

for the name ‘bandgap reference’ of this type of VR. Normally, V_{REF} is around 1.2V.

CMOS technology compatibility and scalability

In standard CMOS technology, PNPs can be realized vertically with the help of an N-well as shown in Figure 5.3. However, the area of BJTs cannot be easily scaled down with CMOS technology [46]. Moreover, the emitter current is controlled now instead of the collector current, which causes the base current to have some influence on the base-emitter voltage, which influences the accuracy of the reference.

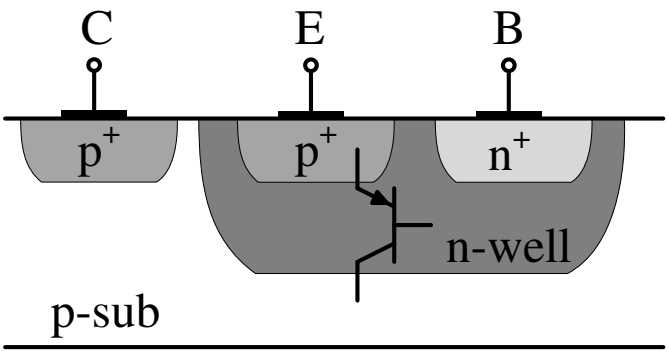


Figure 5.3: PNP realized in standard CMOS technology.

Process variations

Since the output reference voltage of bandgap references is based on the bandgap energy of silicon, which is a characteristic of the material, V_{REF} reveals very small process variations (e.g., a corner variation of ±0.5% is achievable [47]).

Temperature coefficient

The I-V characteristic of BJTs offers decent temperature coefficient compensation and the temperature coefficient is usually outstanding throughout a wide operational temperature range (e.g., 10ppm/ºC from -40 to 125ºC [47]).

Power consumption

It is difficult to apply conventional bandgap references in low-power sensor applications because the power consumption is usually in the order of µW, which is far beyond the power budget. Some modified bandgaps can achieve lower power consumption (e.g., 32-200nW

for [48, 49, 50]) while they are still far from the sub-nW specification [45].

Minimum VDD

According to (5-9), V_{REF} is around 1.2V [18], requiring a minimum VDD larger than 1.2V, which makes it incompatible with sub-1V systems. Although some revised bandgap designs can operate at sub-1V, usually the minimum VDD is still higher than 0.7V [50, 49]. Boost circuits can be utilized to increase the power supply at the expense of complexity and power consumption [48].

5.3.2 MOSFET-based bandgap references

Similar to the above BJT-based ones, bandgaps can also be implemented with MOSFETs as e.g. shown in Figure 5.1. The two BJTs are replaced with diode-connected NMOSTs with different sizes. For a MOSFET operating in the subthreshold region, the I-V characteristic reveals similar behavior with BJTs, which can be utilized for temperature compensation as well (assuming $V_{DS} >> V_T$):

$$I_D = \mu C_{OX} \frac{W}{L}(\eta - 1)V_T^2 \exp(\frac{V_{GS} - V_t}{\eta V_T}) \tag{5-10}$$

where μ is the carrier mobility, C_{OX} is the gate-oxide capacitance, W and L are the width and length of the transistor respectively, η is the sub-threshold slope factor, V_T is the thermal voltage, V_{GS} is the gate-source voltage and V_t is the threshold voltage [51].

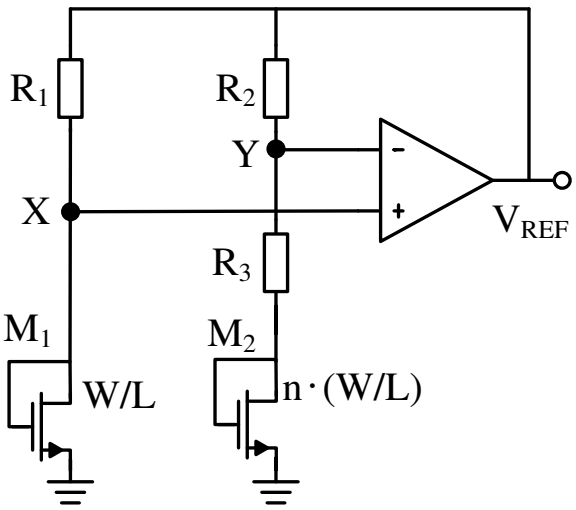


Figure 5.4: MOSFET-based bandgap reference.

Similarly, the voltage drop over resistor R_3 can be expressed as:

$$V_{GS1} - V_{GS2} = V_T \ln(n) \tag{5-11}$$

Subsequently, V_{REF} can be expressed as follows based on (5-10) and (5-11):

$$V_{REF} = V_{GS2} + \ln(n) \cdot (1 + \frac{R_2}{R_3}) V_T \tag{5-12}$$

where V_{GS2} can be expressed as:

$$V_{GS2} = V_t + \eta V_T \cdot \ln(\frac{V_T \cdot \ln(n) / R_3}{\mu_2 C_{OX2} (\frac{W}{L})_2 (\eta - 1) V_T^2}) \tag{5-13}$$

Since V_t normally reveals negative TC and the second term is negative for the sub-threshold region, showing negative TC as well, V_{GS2} also shows negative TC. By tuning the ratio of R_2/R_3, the TC of V_{REF} can be minimized.

Compared to BJT-based bandgaps, MOSFET-based bandgaps reveal larger process variations since the effective voltage over the junction source-channel is indirectly controlled by the gate-source voltage. Consequently, the output is also dependent on the V_t of the MOSFET which is hard to control precisely in CMOS technology, and on the capacitive voltage division from gate to channel (factor η), which also shows variations. As a result, most bandgap references utilize BJTs as the fundamental devices.

5.4 Threshold-based references

Recently, CMOS threshold-based VRs have been drawing more and more attention. Based on (5-10), many threshold-based CMOS VR designs have been proposed [19, 20, 52, 53], which can be categorized into 4 groups based on the fundamental topology: single V_t, V_t difference between different types of NMOS transistors, V_t difference between different PMOS transistors with different bulk control, and V_t difference between NMOS and PMOS. These categories will be discussed next.

5.4.1 CMOS VRs based on single V_t

The topology of a single-V_t based CMOS VR [53] is shown in Figure 5.4 where a diode-connected NMOS operates as a load transistor to generate V_{REF} from the gate.

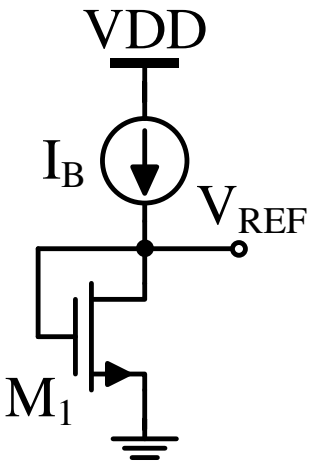


Figure 5.5: An example of a single-V_t CMOS VR [53].

From (5-10), V_{REF} in Figure 5.5 can be expressed as:

$$V_{REF} = V_{GS} = V_t + \ln\left(\frac{I_B}{\mu C_{OX}\frac{W}{L}(\eta-1)V_T^2}\right)\eta V_T \qquad (5\text{-}14)$$

In (5-14), the first term, threshold voltage V_t, is CTAT (complementary to absolute temperature) while the second term contains V_T (=kT/q) which is PTAT (proportional to absolute temperature). With a careful design of I_B, the temperature coefficient of V_{REF} can

be minimized. Compared with BJT-based bandgaps, CMOS VRs have evident advantages and suffer from some limitations as well.

CMOS technology compatibility and scalability

Single-V_t based CMOS VRs have no issue regarding the CMOS technology compatibility since only regular MOSFETs are sufficient for the designs. They can also scale easily with technology.

Process variations

The single-V_t based CMOS VRs highly rely on the absolute threshold voltage, which is very sensitive to the spread of the technology. The threshold voltage of an NMOS can be expressed as:

$$V_{t,nvt} = V_{FB} - \frac{Q_{SS}}{C_{OX}} + 2|\Phi_P| + \frac{|Q_d|}{C_{OX}} \tag{5-15}$$

where $V_{t,\,nvt}$ is the threshold voltage of a normal-V_t NMOS, V_{FB} is the flat-band voltage, Q_{SS} is the surface charge per unit area, C_{OX} is the gate-oxide capacitance, $2|\Phi_P|$ is the voltage required for strong inversion, and Q_d is the charge per unit area in the inversion layer [54]. In (5-15), every term is process-dependent, leading to a V_{REF} that is sensitive to process spread as well. At different process corners, V_t may have a variation of 15% [55] which will be directly reflected in V_{REF} as shown in (5-14), resulting in a much larger V_{REF} variation than bandgap references (e.g., 0.5% [47]). However, the absolute accuracy requirement strongly depends on the application. For instance, static variation in the reference voltage of a SAR ADC will only lead to a gain error, which may be critical or non-critical, dependent on the ADC's application.

Temperature coefficient

By careful optimization, single-V_t based CMOS VRs can achieve low TC (e.g., ~10ppm/ºC in [52]) while usually the operational temperature range is smaller than bandgap references (0~125ºC in [53]).

Power consumption

Since most MOSFETs in a CMOS VR operate in the subthreshold region, the corresponding power consumption is usually very low. For instance, the design [53] consumes only 2.6nW.

Minimum VDD

For CMOS VRs utilizing subthreshold MOSFETs, the V_{GS} of the MOSFETs can be lower than the threshold voltage. The threshold voltage of MOSFETs scales with technology and can be much lower than the forward biased voltage of a BJT (0.7V). For instance, the threshold voltage of an NMOS is around 0.4V in a 65nm technology. As shown in Figure 5.5, the minimum VDD only needs to be higher than V_{REF} plus the drain-source voltage of current source I_B, resulting in a minimum VDD of 0.45V [53]. Consequently, CMOS VRs can achieve sub-1V VDD more easily than bandgap references.

5.4.2 CMOS VRs based on V_t (low/high) difference

Most CMOS VRs are based on the threshold voltage difference between two transistors. One type of such a CMOS VR is based on the threshold voltage difference between nominal-V_t transistors and high/low-V_t transistors with an extra step of ion implantation or a different oxide thickness. In [19], a low-power 2-transistor VR is presented based on the V_t difference between a native NMOS and an I/O NMOS (thick oxide, for I/O purposes) as shown in Figure 5.6.

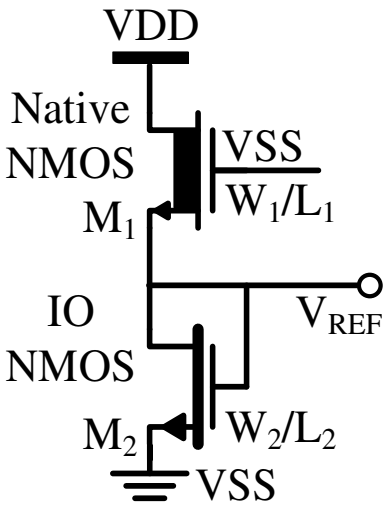


Figure 5.6: The voltage reference in [19].

The two transistors operate in sub-threshold region hence (5-10) applies here. The V_{REF} can then be derived as:

$$V_{REF} = \frac{\eta_1 \cdot \eta_2}{\eta_1 + \eta_2}\left(V_{t2} - V_{t1}\right) + \frac{\eta_1 \cdot \eta_2}{\eta_1 + \eta_2} V_T \ln\left(\frac{\mu_1 C_{ox1} W_1 L_2}{\mu_2 C_{ox2} W_2 L_1}\right) \quad (5\text{-}16)$$

where η_1 and η_2 are the sub-threshold factor for the two transistors respectively. By tuning the size of the two transistors, a temperature-insensitive V_{REF} can be achieved.

CMOS technology compatibility and scalability

Above CMOS VR is very simple in architecture, but it requires native NMOS, which is not supported by all the technologies. Consequently, the implementation of this VR is limited to certain technologies. In terms of scalability, new technology nodes may introduce problems for some extremely low-power CMOS VRs. In [19], the design is fabricated in 0.18µm, 0.13µm and 65nm respectively to verify the technology portability and both the temperature coefficient (TC) and power consumption are worse in 65nm. In fact, despite technology scaling down, most published low-power CMOS voltage references are fabricated in old technology nodes (0.18µm or 0.35µm). Leakage in advanced technologies can be an issue for extremely low-power high-accuracy circuits like a voltage reference. For instance, for the PMOS M_P shown in Figure 5.7 with zero-V_{GS} as in [20], I_P will be larger than I_{DS} if there is leakage current through the gate or the bulk. At typical corner and room temperature, the simulated I_{DS}/I_P is 99.9% in 180nm technology while only 67.7% in 65nm technology. The relatively large leakage in 65nm technology may lead to poor TC or even invalidate the TC cancellation topology of extremely low-power voltage references.

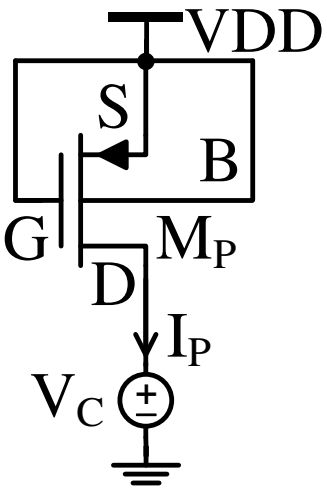


Figure 5.7: MOSFET leakage simulation setup.

Another possible problem in advanced technology nodes is the driving capability of such low-power VRs. A voltage reference normally does not need to drive a resistive load but a capacitive load (usually the gate of a transistor). However, if the following stage suffers from gate leakage, it may draw a DC current from the VR, it will impede with the bias point of the reference. Therefore, especially in advanced technology nodes where the gate leakage increases, the technology compatibility and scalability of this architecture is questionable.

Process variations

From (5-16), it can be noted that the process variation of the presented VR is highly dependent on the threshold voltage difference between the native NMOS and the I/O NMOS. These two types of transistors have different oxide thickness and different ion implantation, which makes it challenging to track the process corners of one another between these transistors. Consequently, the impact of process variations on the performance of this VR might be large.

Temperature coefficient

The temperature coefficient of this type of VR [19] is around 100ppm/ºC from -20 to 80ºC, revealing a relatively larger TC and a smaller temperature range than BJT-based bandgaps.

Power consumption

The presented VR [19] consumes extremely low power at room temperature (0.24nW with a VDD of 0.5V) thanks to the simple architecture and sub-threshold operation. However, due to the sub-threshold operation, the bias current and thus the power consumption change exponentially with temperature, resulting in about 6nW at 80ºC.

Minimum VDD

The VR in [19] operates at a minimum VDD of 0.5V at room temperature thanks to the sub-threshold operation.

5.4.3 CMOS VRs based on V_t (bulk) difference

The threshold voltage difference can also be realized between two identical transistors with different bulk control [20, 56]. The voltage reference proposed in [20] is shown in Figure 5.8.

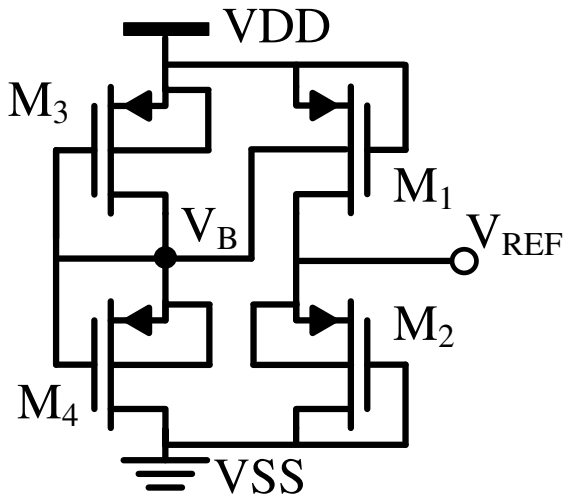


Figure 5.8: The voltage reference in [20].

$M_{1\text{-}4}$ are PMOSFETs and they all operate in sub-threshold region. The bulks of $M_{2\text{-}4}$ are connected to their source respectively. $M_{3\text{-}4}$ generate the bulk control voltage, V_B, to control M_1. It can be derived that:

$$V_{REF} = V_{t1} - V_{t2} + \eta V_T \ln\left(\frac{W_1 L_2}{W_2 L_1}\right) \tag{5-17}$$

where the threshold voltage difference due to bulk control can be expressed as:

$$\Delta V_{t,\text{bulk}} = V_{t1} - V_{t2} = \gamma\left(\sqrt{2\phi_b - \eta V_T \ln\frac{W_4 L_3}{W_3 L_4}} - \sqrt{2\phi_b}\right) \tag{5-18}$$

where γ is the bulk effect factor, and ϕ_b is the bulk potential. It can be noted that ΔV_t (bulk) is CTAT, hence can be cancelled out by the last term in (5-17), achieving a temperature-insensitive V_{REF}.

CMOS technology compatibility and scalability

Above voltage reference requires only regular transistors and the bulk control of the PMOS can be realized via the intrinsic Nwell, making the design compatible with standard CMOS technology.

In terms of technology scaling down, it should be mentioned that in advanced technology

nodes where the oxide thickness is thin, the channel is mainly controlled via the gate and the bulk effect will be reduced. Consequently, the ΔV_t (bulk) will be small and cause difficulty in the VR design.

Similarly, for such low-power designs, the driving capability might be a problem in advanced technology nodes due to the gate leakage as discussed in the previous sub-chapter.

Process variations

Since the presented VR only adopts PMOS and the bulk control can compensate the process variations, the reported process variations for the VR are about 3.8x smaller than for the VRs based on absolute threshold voltage.

Temperature coefficient

The temperature range of the presented VR [20] is from -40 to 85ºC with a TC between 48 to 104 ppm/ºC. Similar to the VR based on V_t (low/high) difference, both the temperature range and the TC are worse than BJT-based bandgaps.

Power consumption

The power consumption of this VR [20] is only 114pW thanks to the sub-threshold operation. However, since the voltage reference is self-biased, the power consumption increases exponentially with temperature due to the subthreshold operation, consuming more than 1nW at 80ºC.

Minimum VDD

The minimum VDD of the presented VR [20] is 1.2V while it is not the focus of optimization. Since the architecture does not enforce any restriction on the minimum VDD, it is expected to be able to achieve sub-1V operation [20].

5.4.4 CMOS VRs based on V_t (P/N) difference

Another type of threshold voltage difference comes from the difference between PMOS and NMOS [57]. The schematic of the VR is shown in Figure 5.9. The two transistors operate in sub-threshold region, hence V_{REF} can be derived as:

$$V_{REF} = \frac{\eta_1 \cdot V_{t2} - \eta_2 \cdot V_{t1}}{\eta_1} + \eta_2 V_T \ln\left(\frac{\mu_1 C_{ox1}(\eta_1 - 1)W_1 L_2}{\mu_2 C_{ox2}(\eta_2 - 1)W_2 L_1}\right) \quad (5\text{-}19)$$

where η_1 and η_2 are the sub-threshold factor of M_1 and M_2 respectively, and V_{t2} is the absolute value of the threshold voltage of M_2.

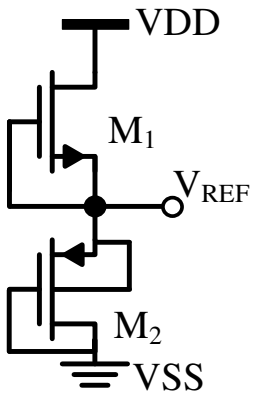


Figure 5.9: The voltage reference in [57].

CMOS technology compatibility and scalability

This design reveals no restriction on the utilization of the CMOS technology since it only requires regular PMOS and NMOS.

Similar as in previous sub-chapters, the driving capability is limited, which may pose a problem in advanced technology nodes due to gate leakage of subsequent stages.

Process variations

From (5-19), it can be noted that the process dependency of the VR is mainly determined by the process corner tracking between NMOS and PMOS, which is difficult to guarantee due to the different fabrication steps.

Temperature coefficient

The TC of the 12 samples in [57] varies from 37 to 551ppm/ºC in a range from -40 to 85 ºC. Both TC and temperature range are worse than BJT-based bandgaps.

Power consumption

The reported power in [57] is extremely low, 420fW at room temperature. Similar to [20], the power consumption also increases exponentially with temperature.

Minimum VDD

The minimum VDD of the presented VR in [57] can be as low as 0.4V at room temperature, which should be attributed to the subthreshold operation of the transistors.

5.5 Conclusions

A voltage reference is a key block in many SoCs. For a SAR ADC, the accuracy of the reference voltage has direct impact on the SAR conversion accuracy. Two mainstream types of VRs are bandgaps and non-bandgap CMOS VRs, both of which can be split into sub classes. The pros and cons of all these classes are summarized in TABLE 5-1.

TABLE 5-1: SUMMARY AND COMPARISON OF BANDGAPS AND CMOS VRS.

	Bandgaps		**Non-bandgap CMOS VRs**			
Topology	BJT	MOSFET	V_t	ΔV_t (low/high)	ΔV_t (bulk)	ΔV_t (P/N)
Process spread	Small	Large	Large	Medium	Medium	Large
CMOS technology compatibility and scalability	Poor	Good	Good	Medium	Medium	Good
Temperature range	Large	Medium	Medium	Medium	Medium	Medium
Temperature coefficient	Good	Medium	Medium	Medium	Medium	Medium
Power consumption	Large	Small	Small	Small	Small	Small
Minimum VDD	Large	Small	Small	Small	Small	Small

BJT-based bandgap references usually have smaller process spread, wider operational temperature range and a better temperature coefficient. On the other hand, CMOS bandgaps and other CMOS non-bandgap VRs reveal better scalability with technology, lower power consumption and lower minimum VDD. However, it is worth mentioning that CMOS VRs can also face some limitations in terms of CMOS technology scaling (due to leakage) or require special CMOS technology options (particular V_t requirements). In general, the above

comparison reveals that CMOS VRs are a better choice for low-power low-VDD applications such as low-power sensor systems while some problems have to be addressed to improve the performance of CMOS VRs.

Chapter 6 Low-power area-efficient CMOS voltage reference designs

This chapter introduces several sub-1V low-power CMOS VR designs based on threshold voltage differences. First, a VR design based on the threshold voltage difference between a nominal-V_t and a high-V_t transistor is presented, revealing low sensitivity to process variations. Subsequently, a high-efficiency duty-cycling scheme is introduced for VRs to lower the power consumption while still continuously providing a reference voltage. Furthermore, two improved VR designs based on threshold voltage difference between a nominal-V_t and a high-V_t transistor are presented. Finally, another design is based on the threshold voltage difference between two transistors of the same type but with different dimensions, compatible with low-cost CMOS technologies. Part of this chapter was published in [55, 58].

6.1 A 0.62V-VDD 25nW CMOS VR

As discussed previously, process and temperature dependency are critical for the voltage unit based on which a reference-voltage generator is designed. In this sub-chapter, the process and temperature characteristics of the threshold voltage difference between different types of MOSFETs will be discussed first and a 0.62V-VDD 25nW CMOS VR design [55] will be introduced subsequently.

6.1.1 Process dependency of the threshold voltage

A perfect VR provides a reference voltage that is independent of process, power supply and temperature variations. Process-independence is the most challenging property, as process variations are usually inevitable and there is not much that can be done to counteract their influence from the aspect of circuit design. As discussed in Chapter 5, bandgap references are based on a voltage unit from a well-defined physical mechanism while CMOS VRs

based on a threshold voltage reveal larger process variations.

As shown in Figure 6.1(a), for a nominal-V_t transistor with $V_{BS} = 0$, the simulated $V_{t,\,nvt}$ varies about 15% in this particular 65nm CMOS technology as shown in Figure 6.2. For most published CMOS VRs based on the absolute threshold voltage, measurements of multiple samples reveal smaller variation as those samples usually come from the same wafer and have the same process corner. But for a robust design, a VR should provide a stable reference voltage over different process corners. Here, the simulated process variation at three corners (typical, slow, fast) divided by the average value is calculated to evaluate the effect of process variations for various transistor sizes.

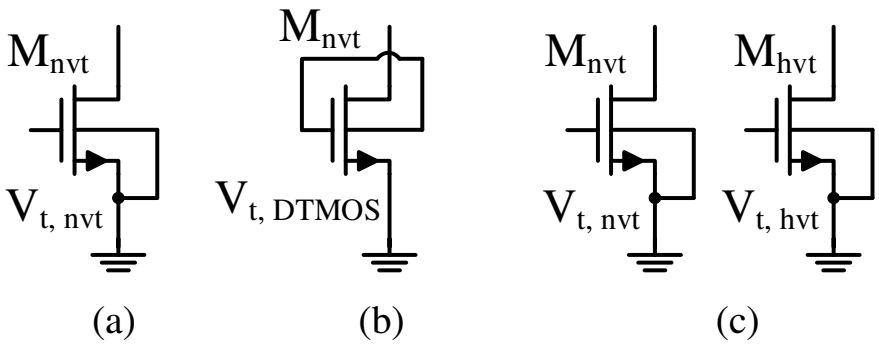


Figure 6.1: (a) nominal-V_t NMOS with $V_{BS} = 0$; (b) nominal-V_t NMOS with $V_{BS} = V_{GS}$; (c) nominal- and high-V_t NMOS with $V_{BS} = 0$.

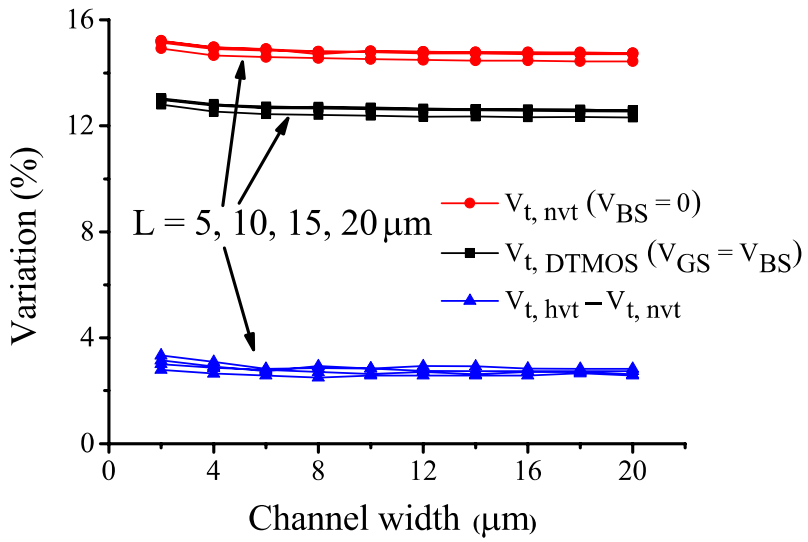


Figure 6.2: Simulated variation of $V_{t,\,nvt}$, $V_{t,\,DTMOS}$ and ($V_{t,\,hvt} - V_{t,\,nvt}$) in 3 process corners.

In [56], the authors claim that DTMOS, a dynamic threshold MOS with the back-gate connected to the gate shown in Figure 6.1 (b), could improve the threshold voltage stability over process corners. Now the threshold voltage should be rewritten as:

$$V_{t,nvt} = V_{FB} - \frac{Q_{SS}}{C_{OX}} + 2|\Phi_P| + \frac{|Q_d|}{C_{OX}} + \gamma(\sqrt{|2\Phi_P - V_{GS}|} - \sqrt{|2\Phi_P|}) \quad (6\text{-}1)$$

where γ is the body-effect coefficient. When $V_{t,nvt}$ diverges from the nominal value, V_{GS} will track this change and tune $V_{t,nvt}$ back towards the nominal value by back-gate control as in(6-1). It is claimed that DTMOS can reduce the process variation by a factor of 2 while in the simulations based on the utilized 65nm technology, the improvement is only about 20% (Figure 6.2, $V_{t,\,DTMOS}$).

In many modern CMOS technologies, the foundry provides, besides the normal transistors, transistors with a higher threshold voltage by applying an extra ion implantation step, while the oxide thickness remains the same. The threshold voltage shift due to this ion implantation can be expressed as:

$$\Delta V_{t,ion} = V_{t,hvt} - V_{t,nvt} = 2|\Delta\Phi_P| + \frac{\Delta|Q_d|}{C_{OX}} \quad (6\text{-}2)$$

where $V_{t,\,hvt}$ is the threshold voltage of the high-V_t NMOS. For a given implantation energy and a large t_{ox}, when t_{ox} decreases, there will be more ions implanted into the substrate, leading to a larger $\Delta V_{t,ion}$. However, when t_{ox} becomes sufficiently small and all the ions have penetrated into the substrate, a further decrease in t_{ox} will result in a smaller $\Delta V_{t,ion}$. Thus, in the vicinity of a certain t_{ox} with certain implantation energy, the threshold voltage shift $\Delta V_{t,ion}$ should be independent on t_{ox} [54], and thus becomes less sensitive to process variations as shown in Figure 6.3. This is confirmed in the simulations based on the utilized 65nm technology (Figure 6.2, $V_{t,\,hvt} - V_{t,\,nvt}$). The $\Delta V_{t,ion}$ varies only by 3%, which is a 5x process stability improvement compared to $V_{t,\,nvt}$. The above improvements are seen independent of sizing (W, L). To summarize, $\Delta V_{t,ion}$ is a more suitable voltage unit for CMOS VRs as it is much more stable over process corners compared to $V_{t,\,nvt}$ or $V_{t,\,DTMOS}$.

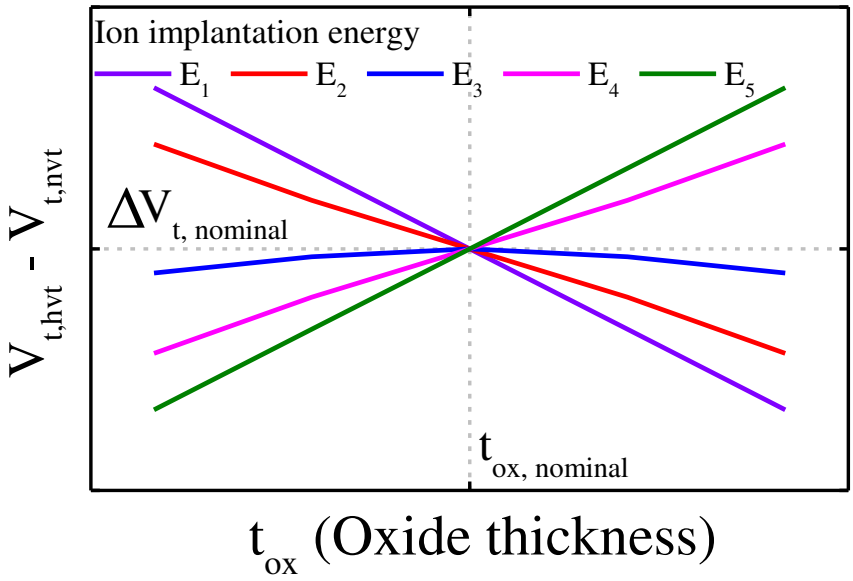


Figure 6.3: $\Delta V_{t,ion}$ changing with t_{OX} at different implantation energies.

6.1.2 Temperature characteristics of $\Delta V_{t,ion}$

In [59], the temperature dependency of $\Delta V_{t,ion}$ is derived by calculating $\partial \Delta V_{t,ion}/\partial T$. For a shallower implanted depth than the depletion edge, $\Delta V_{t,ion}$ is CTAT. This CTAT effect was confirmed by measurements. The measurement setup is shown in Figure 6.4. $M_{T1,\ T2}$ are normal-V_t and high-V_t transistors respectively, fabricated in 65nm technology. They are diode-connected and biased in the sub-threshold region. Large transistor sizes (W/L = 5µm/12µm) are chosen for both transistors as this is advantageous for matching and avoids short-channel and narrow-channel effects which will introduce a more complex temperature dependency.

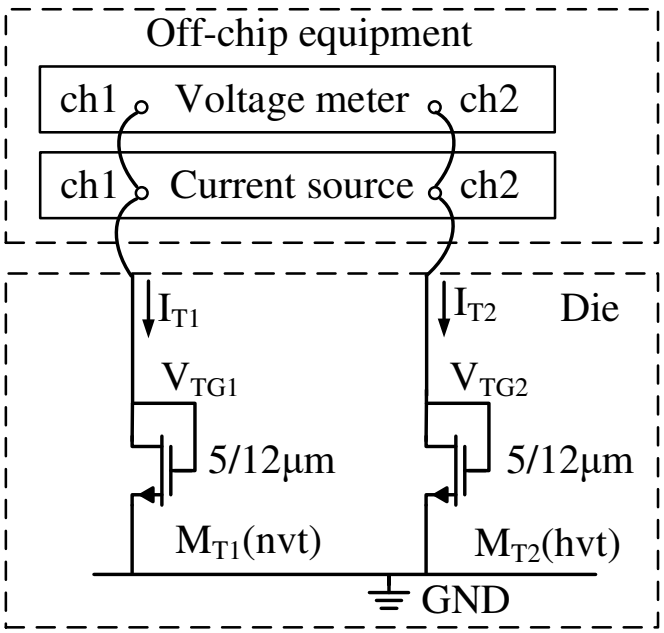


Figure 6.4: Measurement setup for a test pair, measuring the temperature sensitivity of ΔV_{TG} and for defining the current ratio for creating a temperature-insensitive ΔV_{TG}.

When $V_{TG1, TG2} >> V_T$ (V_T is the thermal voltage), the current flowing in $M_{T1, T2}$ could simply be expressed as (5-10). Hence, the gate voltage difference of MT1 and MT2 could be expressed as:

$$\Delta V_{\mathrm{TG}} = (V_{t,hvt} - V_{t,nvt}) + \ln\left(\frac{I_{T2}}{I_{T1}} \cdot \frac{\mu_{n1}}{\mu_{n2}} \cdot \frac{C_{OX1}}{C_{OX2}} \cdot \frac{(W/\mathrm{L})_1}{(W/\mathrm{L})_2}\right) \cdot \eta \mathrm{V}_T \qquad (6\text{-}3)$$

where the first term is CTAT and the second term is PTAT. By properly setting the current ratio k (I_{T2}/I_{T1}) of $M_{T1, T2}$, the TCs (Temperature Coefficient) of these two terms can cancel out each other, which makes ΔV_{TG} insensitive to temperature. In Figure 6.5, two branches of current (I_{T1} = 8nA, $I_{T2} = k \cdot I_{T1}$) are pushed into the drains of $M_{T1, T2}$ and the gate voltages $V_{TG1, TG2}$ are measured for different current ratio k from -25°C to 110°C (Figure 6.5 (a)). The measured results fit well with the simulations in Cadence (Figure 6.5 (b)). Corresponding to (6-3), with an increasing current ratio, the TC of ΔV_{TG} varies from negative to positive. By optimizing this ratio (e.g. 1.4 in this case), a temperature-insensitive ΔV_{TG} can be achieved.

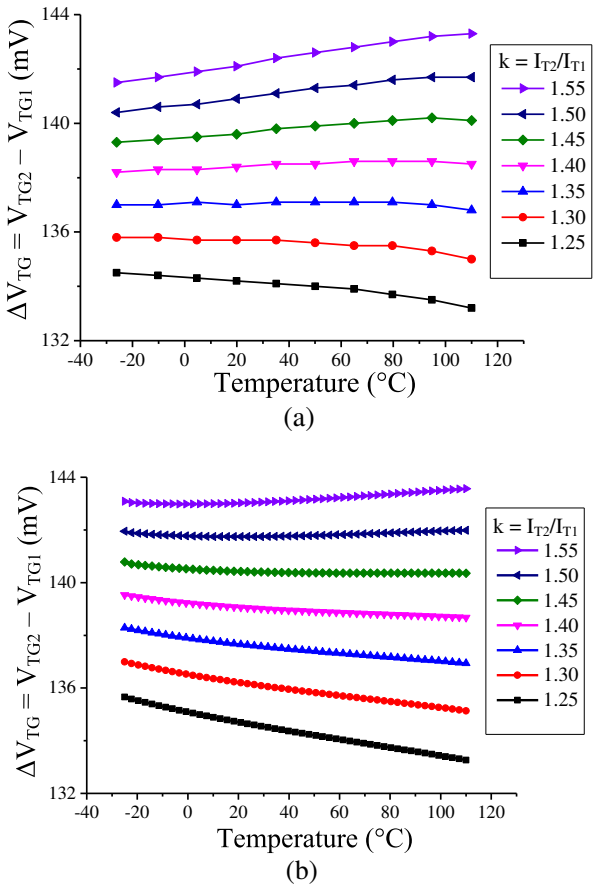


Figure 6.5: Measured (a) and simulated (b) ΔV_{TG} of the test pair with different current ratios.

6.1.3 Architecture of the CMOS VR

Now that a temperature- and process-insensitive ΔV_G can be achieved according to the previous discussion, the next step is to generate a reference voltage relative to ground. The VR core is shown in Figure 6.6 (right-hand side). $M_{1,2}$ are normal-V_t and high-V_t transistors respectively. They are diode-connected and operate in sub-threshold, as the test pair. Since the dimensions (11.2µm/12µm) of $M_{1,2}$ are different from those of the test pair, the optimized k (1.5) for a temperature-insensitive ΔV_G ($V_{G2} - V_{G1}$) is also slightly different. A negative feedback loop using an OPAMP forces V_P to equal V_{G2}, so that the voltage drop over resistor R_1 equals ΔV_G. By copying current I_1, a temperature-insensitive V_{REF}, which only depends on temperature-insensitive current and resistor ratios as well as the temperature-insensitive ΔV_G is achieved as follows:

$$V_{REF} = I_0 \cdot R_0 = \frac{I_0}{I_1} \cdot \frac{R_0}{R_1} \cdot \Delta V_G \tag{6-4}$$

where R_0 equals the sum of R_{0a} and R_{0b}. Since V_{REF} is temperature-insensitive while V_P is CTAT as V_P tracks the CTAT threshold voltage, the accuracy of a single-transistor current copy will be affected by the drain-source voltage, introducing a complex TC to V_{REF}. Hence, as shown in Figure 6.6, a cascode structure is chosen here to achieve an accurately copied current. The transistors composing the cascode structure operate in the sub-threshold region and the drain-source voltage is designed to be larger than 100mV to diminish channel length modulation effects. V_G is generated by the feedback loop and V_{RB} is a fraction of V_{REF} so the cascode structure does not consume too much voltage headroom, making it compatible with low-VDD operation.

The OPAMP composing the negative feedback is shown in Figure 6.6, left-hand side. It consists of two stages whose gain is large enough to guarantee V_P to be close enough to V_{G2}. RC-Miller compensation is adopted to ensure the stability of the negative feedback loop. The bias for the OPAMP is generated by a copy of current I_1, which is approximately expressed as $\Delta V_G/R_1$.

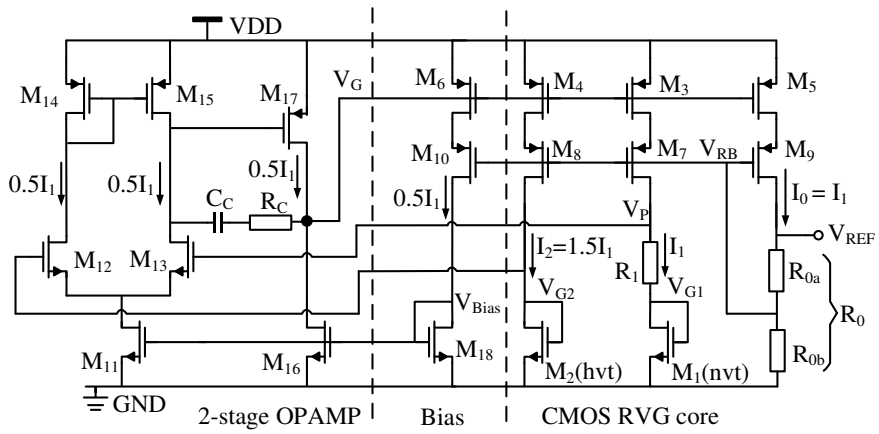


Figure 6.6: CMOS VR architecture.

6.1.4 Key features of the CMOS VR

This sub-chapter introduces the key features of the presented CMOS VR.

Minimum VDD

From Figure 6.6, it is easy to observe that the minimum operational VDD for the VR core is:

$$VDD_{\min,core} = V_{G2} + V_{DS4} + V_{DS8} \tag{6-5}$$

where V_{G2} is the gate voltage of M_2 and $V_{DS4,\,8}$ are the drain-source voltage drop of $M_{4,\,8}$ respectively. Similarly, the minimum operational VDD for the OPAMP is:

$$VDD_{\min,OPAMP} = V_{SG14} + V_{DS12} + V_{DS11} \tag{6-6}$$

where V_{SG14} is the source-gate voltage of M_{14}, and $V_{DS11,\,12}$ are the drain-source voltage drop of $M_{11,\,12}$ respectively. The minimum power supply of the VR is determined by the larger one of (6-5) and (6-6). Due to the sub-threshold operation of $M_{2,\,14}$, voltages V_{G2} and V_{SG14} are smaller than the absolute threshold voltage value of $M_{2,\,14}$. $V_{DS4,\,8,\,11,\,12}$ need to be at least about 100mV. The simulated minimum VDD is about 720mV among 5 process corners from -25°C to 110°C, which means this VR is suitable for sensor networks and other sub-1V systems.

Power consumption

From Figure 6.6, it is found that the power consumption of this VR is proportional to I_1. In order to suppress the power consumption, a large R_1 is required at the expense of chip area. On the other hand, current I_1 must force $M_{1,\,2}$ to operate in the sub-threshold region and it must be large enough to make (5-10) valid. As a tradeoff between chip area, temperature performance and power consumption, R_1 is set to 17MΩ and R_0 is set to 48.5MΩ, leading to I_1 of 8.25nA. The simulated power consumption of the VR at 0.8V VDD is about 40nW. Since ΔV_G changes little with process, power supply and temperature, the current consumption of the VR is also stable over PVT corners.

Process-dependency of voltage stability

The complete VR is also simulated at different corners (Figure 6.7). The simulated V_{REF} varies about only ±1.5% (3% variation range) over five corners, well corresponding to the threshold voltage simulations in Chapter 6.1. This implies that the presented threshold voltage difference based VR reveals much better process stability than absolute threshold voltage based VRs.

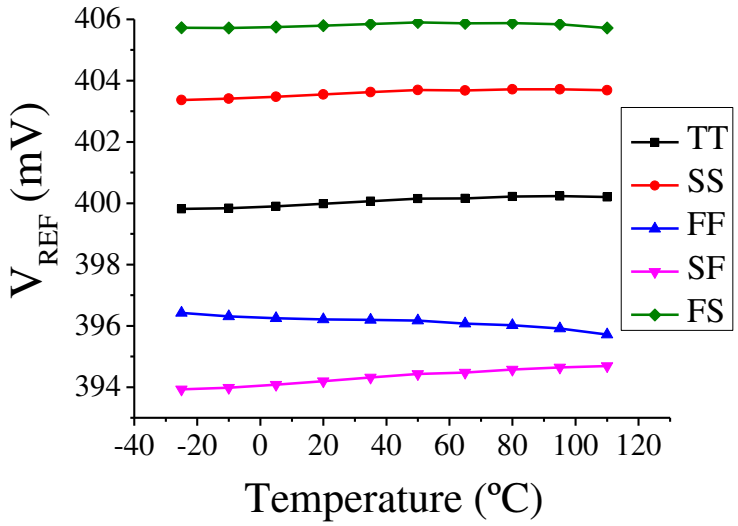


Figure 6.7: Simulated V_{REF} in 5 process corners.

6.1.5 Experimental results

This sub-chapter shows experimental results of the presented CMOS VR.

Die photo

The prototype is fabricated in 65nm CMOS and occupies a chip area of 0.0748mm^2 as shown in Figure 6.8.

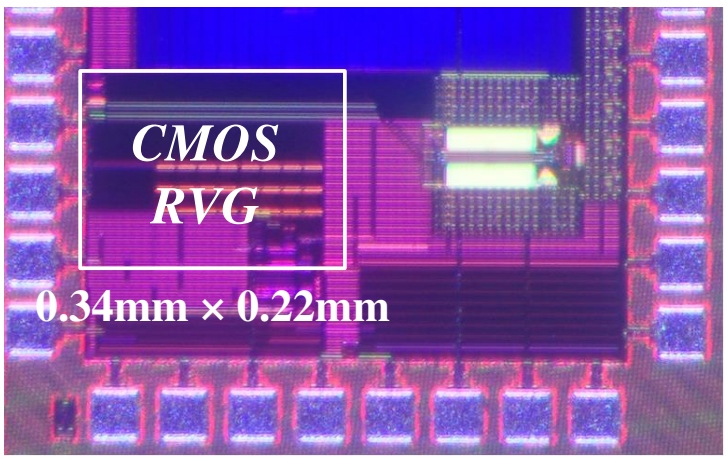


Figure 6.8: Die photo of the CMOS VR in 65nm CMOS.

Minimum VDD and line sensitivity

A total of 15 VR samples was measured. They all begin to operate from a minimum VDD between 0.60 ~ 0.62V. A sample with 0.62V minimum VDD is selected for the measurements shown here. Figure 6.9 displays the V_{REF} as a function of VDD. From 0.62V to 2.0V, the line sensitivity is 0.07%/V.

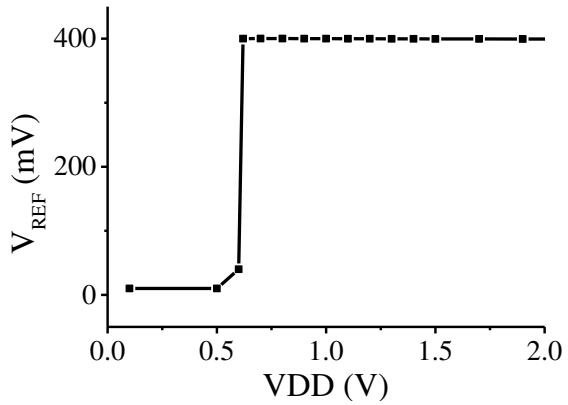


Figure 6.9: Measured output reference voltage of the VR versus power supply.

Power consumption

The current consumption as a function of VDD is shown in Figure 6.10. At 0.8V VDD, the measured power consumption is 38nW. At the minimum supply of 0.62V, the measured power consumption is 25nW.

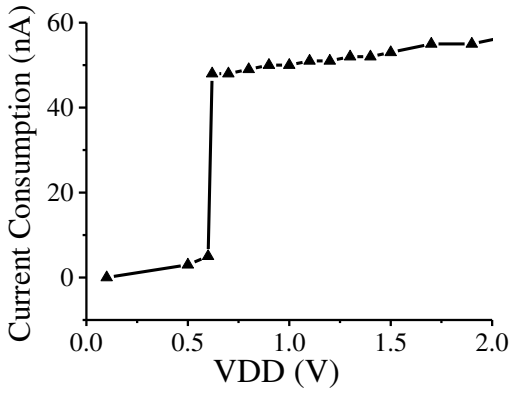


Figure 6.10: Measured current consumption of the VR versus power supply.

PSRR

The PSRR is measured by measuring the transfer from a tone superimposed on VDD to the output of the VR. The measured PSRR of the VR is better than 49dB up to near Nyquist frequency as shown in Figure 6.11.

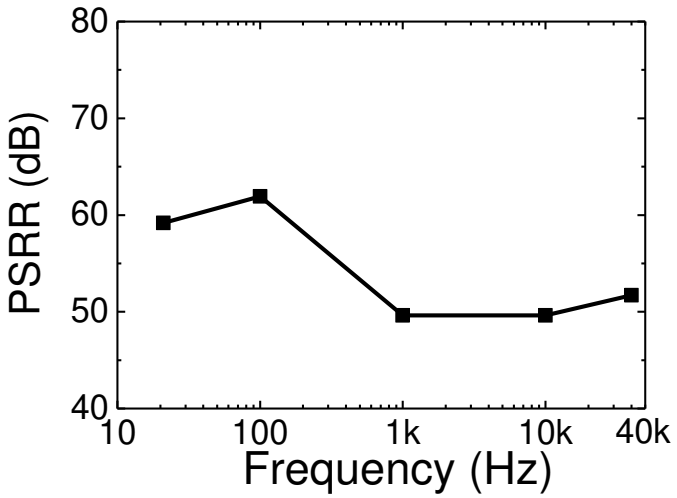


Figure 6.11: Measured PSRR of the VR.

Temperature coefficient

The temperature dependency of the 15 samples is shown in Figure 6.12. From -25°C to 110°C, the TCs vary from 44 to 248 ppm/°C with an average TC of 108ppm/°C. At 25°C, the average output reference voltage is 389.9mV with a 4.0mV standard deviation. According to Monte-Carlo simulations, the dominant reason for part-to-part variation is mismatch in the OPAMP input stage and the current mirror $M_{3\text{-}5,\ 7\text{-}9}$.

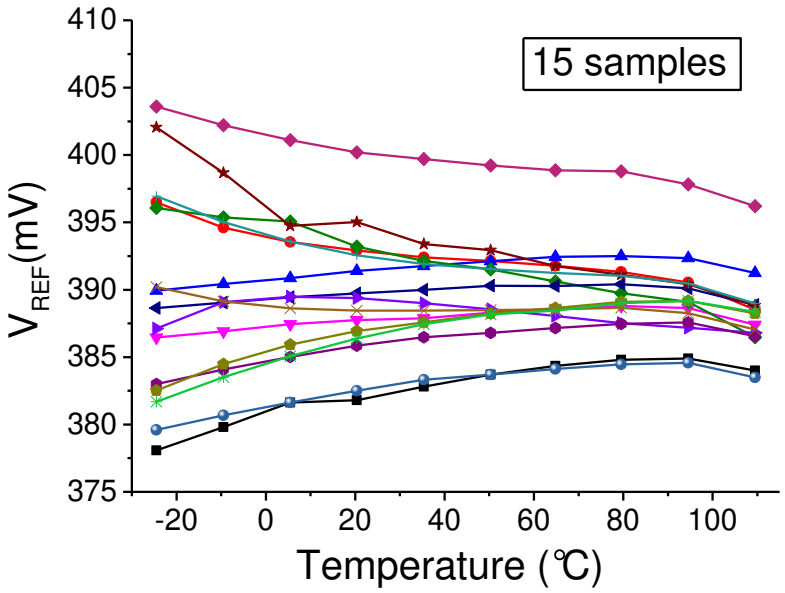


Figure 6.12: Measured temperature dependency of 15 samples.

Summary and comparison

TABLE 6-1 compares this VR with other low power CMOS and BJT VRs. Compared with [48, 49, 50, 52], the presented VR consumes lower power and will be lower than [53] after applying the duty-cycling scheme to be presented in Chapter 6.2. The designs [19, 20, 57] consume much lower power while it should be noted that the capability of these designs to drive the following circuitry needs to be addressed due to the gate leakage, especially considering the adopted relatively more advanced technologies. Besides, the sample-to-sample variation is comparable to BJT VRs and substantially better than V_t-based CMOS VRs. Further, thanks to the feedback loop with OPAMP in the presented design, it reveals better line sensitivity and PSRR than other V_t-based VRs.

TABLE 6-1: VR PERFORMANCE SUMMARY AND COMPARISON.

	[50]	[49]	[48]	[19]	[20]	[57]	[52]	[53]	This work
Type	BJT	BJT	BJT	ΔV_t (low/high)	ΔV_t (bulk)	ΔV_t (P/N)	V_t	V_t	ΔV_t (low/high)
Technology (nm)	130	180	130	65	180	65	350	180	65
VDD_{min} (V)	0.75	0.7	0.5	0.5	1.2	0.4	0.9	0.45	0.62
Area (mm^2)	0.070	0.02	0.026	0.0009	0.005	0.0001	0.045	0.043	0.077
TC (ppm/°C)	40	114	75	89~118	48~124	252	10	165	108
Power (nW)	170	52.5	32	0.24	0.114	0.00042	36	2.6	25
Sample-to-sample V_{REF} variation: σ/μ	1.0	1.05	0.67	-	1.9	-	3.1	3.9	1.0
Line sensitivity (%/V)	0.005	-	-	0.33	0.38	0.47	0.27	0.44	0.07
PSRR @100Hz (dB)	-	62	-	40	42	-	47	45	62

6.2 A high-efficiency duty-cycling VR

For the presented VR in Chapter 6.1, the power consumption can be reduced further with a duty-cycling technique. This sub-chapter presents a high-efficiency duty-cycling VR [55], enabling a low active rate of the VR and providing a constant reference voltage.

6.2.1 Duty-cycling and start-up of the VR

In order to disable the VR while VDD remains on, switch transistors are inserted in each branch between PMOS and NMOS as shown in Figure 6.13. While not shown in the figure, the current paths in the OPAMP are disabled in a similar way. To boost duty-cycling speed, voltages V_G and V_{Bias} should be restored quickly. To do so, two switched capacitors C_{S1}, C_{S2} are placed at these nodes to save and restore their levels when the VR is duty-cycled.

Besides this duty-cycling technique, the VR also needs a start-up circuit to guarantee correct start-up of the circuit when VDD is switched on for the very first time. The start-up circuit

is also shown in Figure 6.13. Assuming the duty-cycling switches are on, the moment VDD is switched on, V_S will jump to a high voltage level due to C_S being discharged prior to this moment, and thus open transistor M_{S2}. V_G is then discharged and $M_{3\text{-}6}$ are switched on gradually, enabling current flow and functionality of the circuit. As soon as V_{Bias} rises sufficiently, M_{S1} will pull V_S to ground to switch off M_{S2} and disable the start-up circuit. The VR core takes over and will settle to the proper operation state. The start-up time is approximately 1.5ms. In case the duty-cycling switches are not on (or already duty-cycled) during the moment VDD is switched on, correct start-up is still ensured, but the initial start-up will take longer due to the duty-cycled operation.

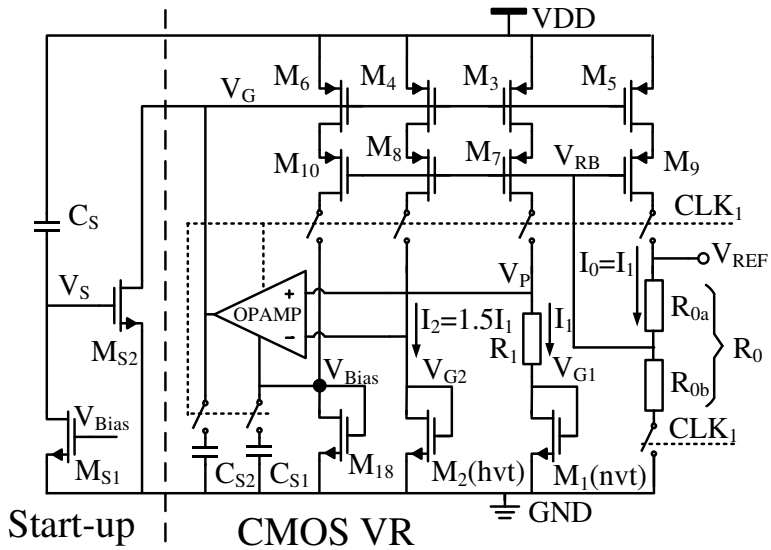


Figure 6.13: VR with start-up circuit and duty-cycling switches.

6.2.2 One-stage sample-and-hold

Even though the VR is duty-cycled, a continuously stable reference voltage is preferred. A one-stage S&H could be adopted to sample and hold the reference voltage of the VR as shown in Figure 6.14. The VR and the switched capacitor network (S_A, C_A) are controlled by the same clock CLK_1 and voltage V_A is used as a continuous output reference voltage fed to the follow-up block. This scheme suffers from two problems: first, at the moment CLK_1 switches the VR and S_A on, V_A would experience a large start-up ripple of V_{REF}, the output of the VR. Second, when VR and S_A are switched off and C_A holds the sampled voltage, due to the voltage drop over NMOS switch S_A, there will be leakage through S_A causing droop of V_A. As a result, voltage V_A is neither stable nor accurate for most of the time, which will

cause performance loss of the SAR ADC compared to operation with a non-duty-cycled VR.

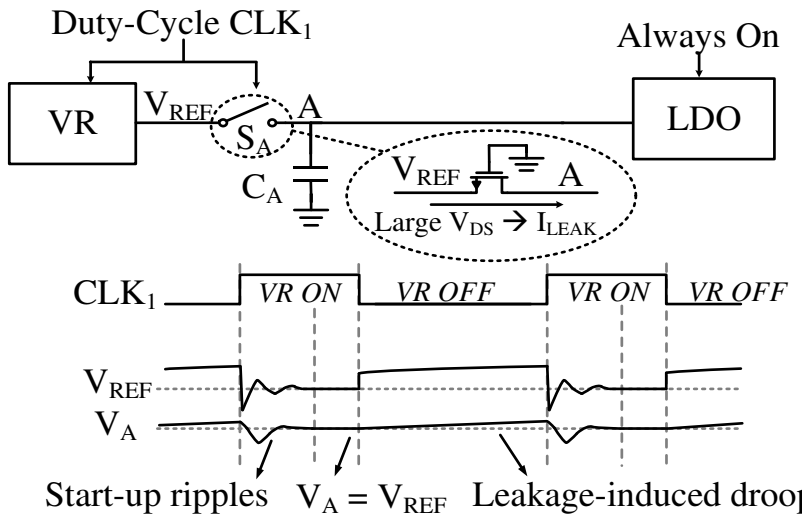


Figure 6.14: Architecture and waveforms of a one-stage S&H.

6.2.3 Three-stage dual-clock sample-and-hold

To solve the above problems, a three-stage dual-clock S&H is presented as shown in Figure 6.15. Compared to Figure 6.14, two more switched capacitors controlled by CLK_2 are inserted between node A and the follow-up block. CLK_1 and CLK_2 have the same frequency but different pulse widths. CLK_1 switches the VR and S_A on simultaneously as before, thus V_A will be stable after some start-up time. At that time, CLK_2 switches S_B and S_C on, so that voltage V_B and V_C are refreshed from the stable V_A. In this way, V_C is isolated from the start-up behavior of the VR. Subsequently, CLK_1 and CLK_2 switch the VR and $S_{A, B, C}$ off simultaneously and the hold phase starts. As before, the leakage through S_A causes an unstable V_A. However, the voltage drop over S_B is smaller than that of S_A leading to smaller leakage from node B because the leakage of a MOS switch is proportional to the voltage drop between drain and source. Furthermore, the voltage drop over S_C is again smaller than that of S_B so that the leakage from node C becomes very small. As a result, a very stable V_C is achieved during the entire clock period, and the simulated maximum ripple is merely 0.1mV. Above discussion indicates that a too high or too low V_{REF} will either make the leakage in the S&H switches too high, or will increase the RC time, which would slow down the settling time and thus degrade the duty-cycling speed. As a result, a V_{REF} of 400mV is chosen here.

The performance requirements for node A, B and C are different as it is more important to start-up fast at node A and B than to leak slightly, while small leakage is more important to enable longer hold time and better stability at node C. However, a small C_B will lead to a large leakage at node B and increase the leakage on C_C subsequently. Consequently, the value of $C_{A,B,C}$ is set to 12.5pF, 25pF and 50pF respectively. S_A is set to about 5 times the size of S_B and S_C, while S_B and S_C have the same size.

In this work, the duty-cycle clocks CLK_1 and CLK_2 are generated externally from an FPGA. The frequency is 20Hz and the pulse widths are 5ms and 2.5ms respectively. This frequency is determined by the maximum hold time the duty-cycling could achieve plus the start-up time and refresh time needed. Because of the low frequency of operation and the insensitivity to the exact timing, they could be generated on chip with little power consumption. According to simulations, this logic would consume only 2nW and occupy only 50µm x 12µm. Measurement results of this design will not be shown at this point, but they will be shown later in Chapter 8, where this design is integrated in a system with VR, LDO, and SAR ADC.

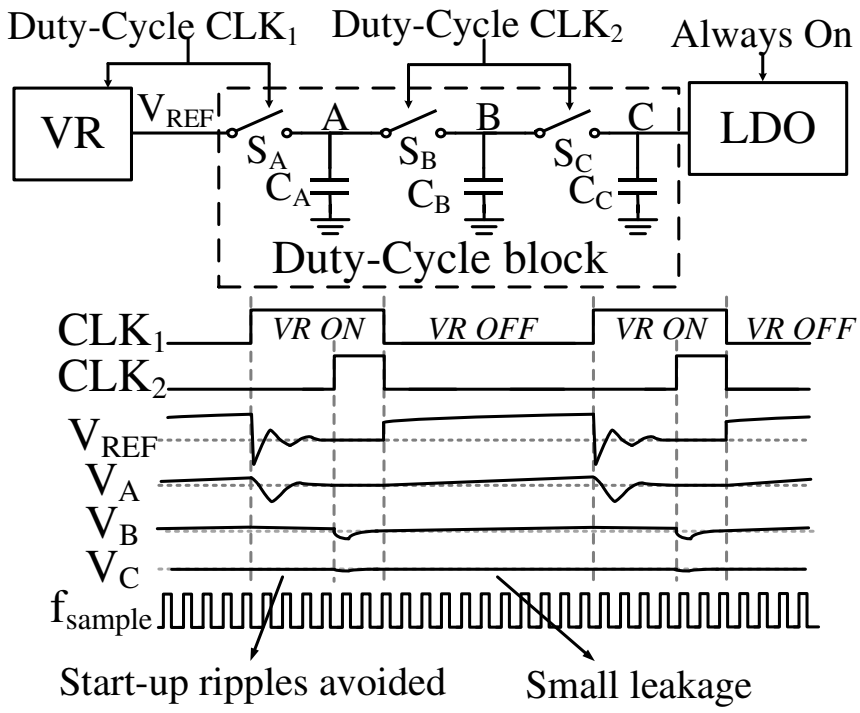


Figure 6.15: Architecture and waveforms of a three-stage S&H.

6.3 A resistor-less CMOS VR

In this sub-chapter, a resistor-less CMOS VR is introduced, achieving small chip area thanks to the adopted MOS-resistors.

6.3.1 Chip area occupation of resistors

For the VR in Chapter 6.1, the low power consumption is realized at the expense of large poly resistors (~65MΩ), occupying large chip area (140µm x 230µm). According to Ohm's law, in order to achieve a constant output reference voltage and lower current consumption, the resistor will be inversely proportional with the total current consumption of the VR in Chapter 6.1. As shown in Figure 6.16, about 54% of the voltage reference area is occupied by the resistors of the VR in Chapter 6.1 and this percentage will increase rapidly when scaling down the power consumption. Therefore, an alternative implementation for the resistor is needed.

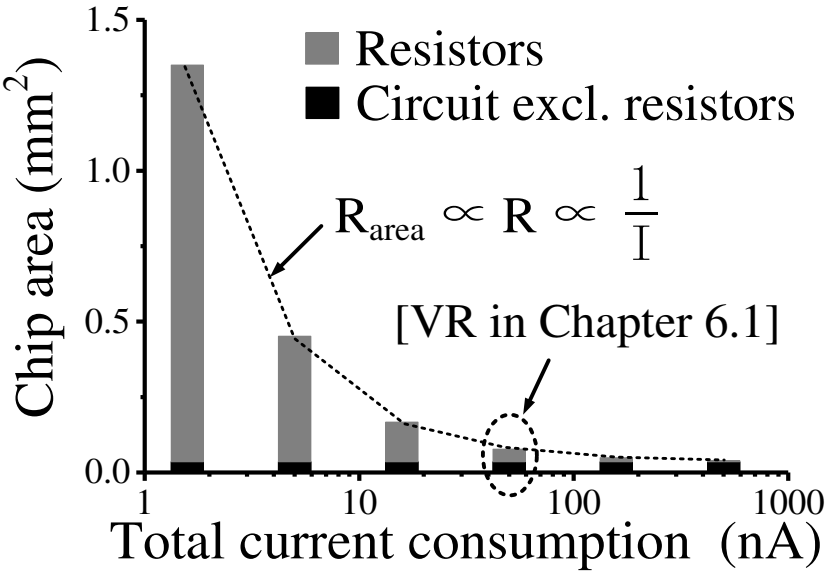


Figure 6.16: Chip area of resistors and the rest of the VR in Chapter 6.1, when scaling down the total current consumption.

6.3.2 MOS resistors

In CMOS technology, MOSFETs in linear region can also operate as a resistor and reveal higher resistance per chip area compared to poly resistors. As shown in (6-7), the drain-source current of an NMOS in linear region can be simplified (V_{GS}-V_t >> V_{DS}/2):

$$I_D = \mu C_{OX} \frac{W}{L}\left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2 \right] \approx \mu C_{OX} \frac{W}{L}(V_{GS} - V_t)V_{DS} \tag{6-7}$$

where V_{DS} is the drain-source voltage. The equivalent resistance is:

$$R_{DS} \approx \frac{1}{\mu C_{OX} \frac{W}{L}(V_{GS} - V_t)} \tag{6-8}$$

It can be noted that R_{DS} is sensitive to process parameters and it takes some effort to achieve a constant ($V_{GS} - V_t$). For the VR in Chapter 6.1, the accuracy of the absolute resistance is not that important but the ratio between R_0 and R_1 is critical as shown in (6-4). MOSFETs in linear region cannot be used since the biasing will be a problem in this scenario.

As alternative, diode-connected MOSFETs are considered. Now, the drain-source current is not linear with the drain-source-voltage, that is to say, the resistance between the drain and the source is not constant. However, the MOSFET is self-biased and has a predictable relation between the drain-source current and drain-source voltage. This can be used advantageously to realize a voltage multiplier with stacked identical diode-connected MOSFETs as shown in Figure 6.18. PMOS devices are adopted to eliminate the body effect, achieving the same V_t for all stacked devices. The function of the voltage multiplier can be expressed as (6-9), which can replace $R_{1,0}$ in Figure 6.6 to save chip area.

$$V_{SD23} = V_{SD2} + V_{SD3} = 2V_{SD1} \tag{6-9}$$

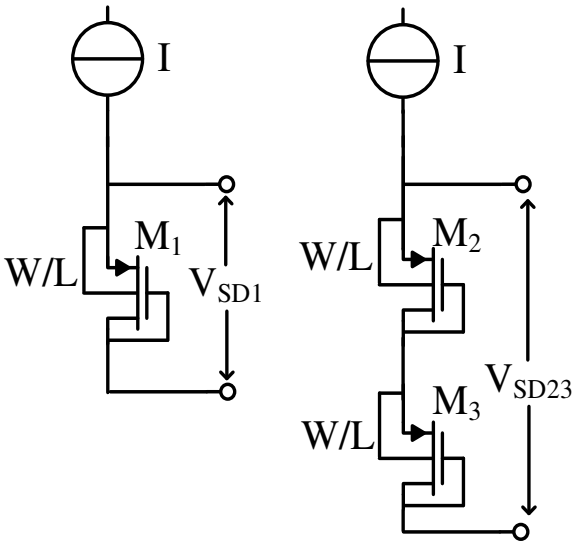


Figure 6.17: Voltage multiplier with stacked diode-connected PMOS.

6.3.3 The resistor-less CMOS VR

The resistor-less CMOS VR is shown in Figure 6.18. Compared to Figure 6.6, resistor $R_{1,0}$ are replaced with identical diode-connected PMOSs (M_{R1}, M_{R01}, M_{R02}, …, M_{R0N}) and I_0 is made equal to I_1. As a result, the reference voltage can be expressed as:

$$V_{REF} = 3 \cdot (V_P - V_{G1}) = 3\Delta V_G \tag{6-10}$$

where ΔV_G can be expressed similarly as (6-3).

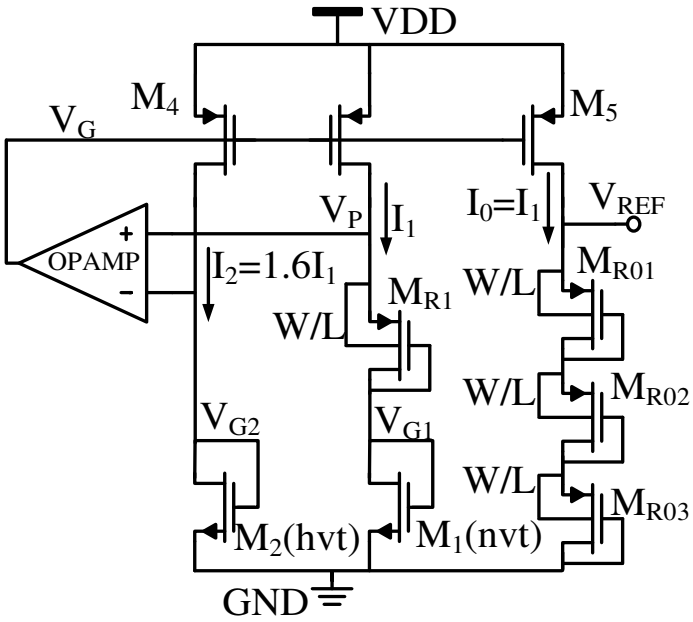


Figure 6.18: The resistor-less CMOS VR.

It should be noted that R_1 in Figure 6.6 not only carries the reference voltage ΔV_G (which is copied and multiplied to the output), but also generates the reference current ($\Delta V_G/R_1$) for the biasing of $M_{1,2}$ and the OPAMP. Since ΔV_G is stable over PVT variations, the generated reference current is also stable, guaranteeing the correct biasing for the entire VR. However, in the presented resistor-less VR, the reference current should be expressed as:

$$I_D = \mu C_{OX} \frac{W}{L}(\eta - 1)V_T^2 \exp\left(\frac{\Delta V_G - \left|V_{t,M_{R1}}\right|}{\eta V_T}\right) \tag{6-11}$$

which is very sensitive to process and temperature variations. As shown in Figure 6.5, ΔV_G is around 140mV, which means (6-11) can be really small, especially at slow corner and low temperature, invalidating the initial pre-condition ($V_G >> V_T$) of the VR. In terms of temperature dependency, $|V_{t,MR1}|$ is CTAT, leading to an exponentially increasing I_D with temperature. Since all the branches of the VR are biased from this reference current, the current consumption of the VR is also proportional to I_D and exponentially increasing with temperature, leading to a quite high current consumption at high temperature. What is worse, a high biasing current at high temperature will bias $M_{1,2}$ in saturation region, making the topology of the VR invalid. In order to maintain an appropriate biasing at all process corners and throughout the entire temperature range, the sizing of M_{R1} needs to be chosen carefully. Even so, the operational temperature range of the resistor-less VR cannot cover the same

temperature range as the VR in Chapter 6.1. According to (6-3), ΔV_G is independent of the absolute biasing current but only the current ratio. However, the biasing current changes so significantly with temperature that this introduces undesirable temperature dependency. As a result, the current ratio between I_2 and I_1 needs to be tuned to achieve a V_{REF} with small temperature coefficient. The current ratio is set to 1.6:1 in the presented design.

6.3.4 Simulation results

The presented resistor-less VR is simulated in 65nm CMOS technology. In order to make a better comparison, the resistor-less VR is designed to consume the same power at room temperature with the VR in Chapter 6.1. The only modifications are the replacement of the large resistors and the tuned current ratio.

The layout of the VR is shown in Figure 6.19 (350x135µm), where most chip area is occupied by the capacitors at the output node. The OPAMP in the negative feedback loop also occupies large chip area. The 4 MOS-resistors occupy only 40x12µm which reveals 67x area reduction compared to poly resistors. Note that each MOS-resistor requires a stand-alone Nwell, increasing the chip area compared to PMOS transistors in the same Nwell. However, the MOS-resistor still reveals superiority in terms of area. The chip area of the VR core (excluding the decoupling capacitors) is reduced by 59% compared to the VR in Chapter 6.1 thanks to the adopted MOS resistors.

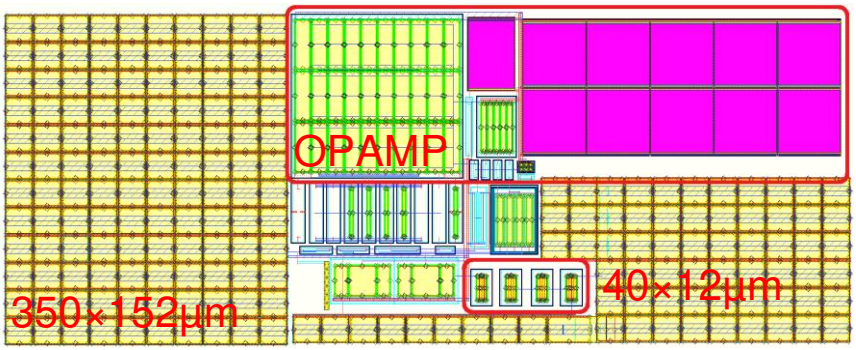


Figure 6.19: Layout of the resistor-less VR in 65nm CMOS.

Similar to the VR with poly resistors, the presented VR can also operate at low VDD. The VDD dependency of the V_{REF} and the current consumption at typical corner and room temperature are illustrated in Figure 6.22 and Figure 6.21 respectively. The VR operates from a minimum VDD of 0.5V and the line sensitivity is 0.2%/V. The VR consumes around

48nA at 0.8V VDD, which is nearly the same as for the VR in Chapter 6.1.

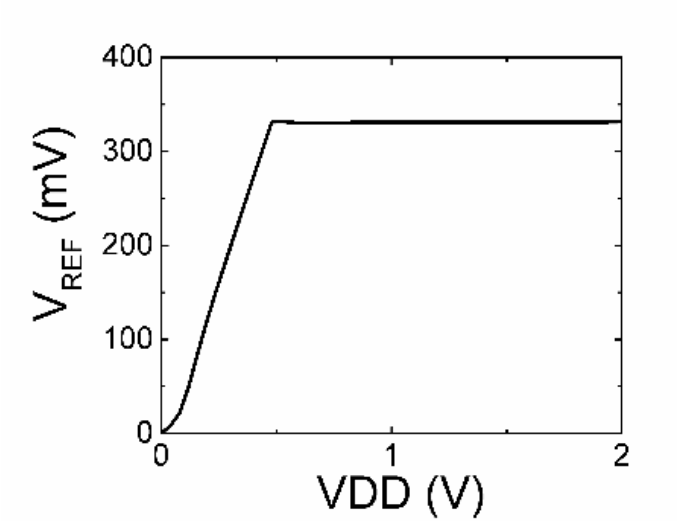


Figure 6.20: VDD dependency of V_{REF} at typical corner and room temperature.

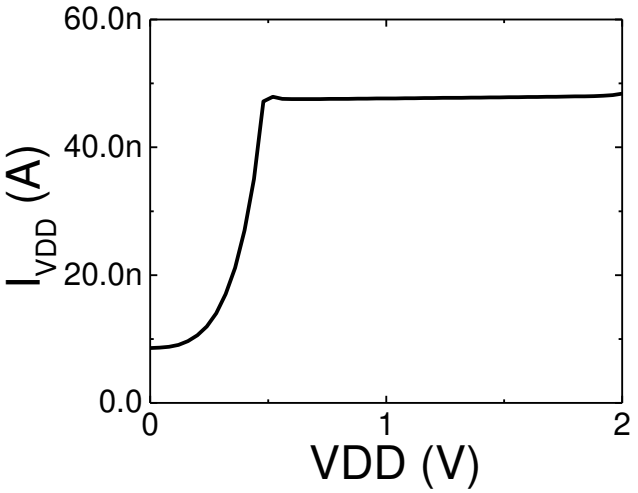


Figure 6.21: VDD dependency of current consumption at typical corner and room temperature.

The generated reference voltage is simulated at 5 process corners with a VDD of 0.8V throughout the temperature range from 0ºC to 100ºC (Figure 6.22). At the typical corner, the temperature coefficient is optimized to be 15.2ppm/ºC. At the other corners, the temperature coefficients are 53.5, 57.5, 103.4, and 114.8ppm/ºC respectively, due to the large biasing current variations as discussed in the above sub-chapter. The current consumption of the VR at 5 corners is shown in Figure 6.22. It increases exponentially with temperature. At 100ºC and fast corner, the VR consumes more than 1µW.

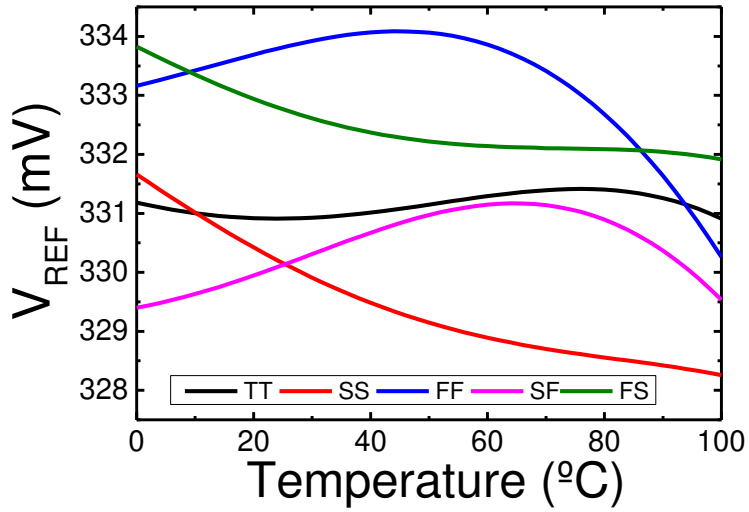


Figure 6.22: Simulated V_{REF} at 5 process corners from 0ºC to 100ºC.

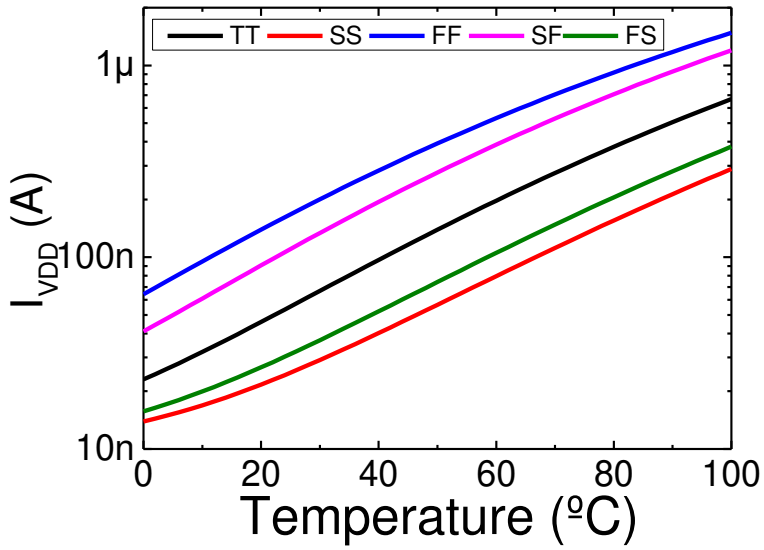


Figure 6.23: Current consumption of the resistor-less VR.

The PSRR of the VR is shown in Figure 6.24. The negative feedback loop results in a high PSRR of 70dB at DC and the 85dB PSRR at high frequency mainly attributes to the capacitors (~100pF) at the output node.

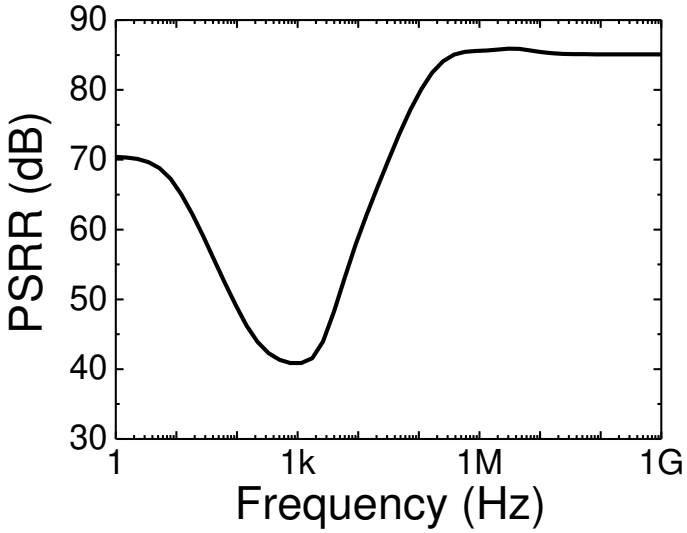


Figure 6.24: PSRR of the resistor-less VR.

Summary and comparison

The performance of the presented resistor-less CMOS VR is summarized in TABLE 6-2 and compared with the VR in Chapter 6.1. This design is tuned to have the same power consumption at room temperature with the VR in Chapter 6.1. At high temperature, this design consumes much higher power due to the adopted MOS-resistors. Average power variation is defined to evaluate how the power changes with temperature. The VR in Chapter 6.1, with the help of low-TC poly resistors, reveals 36x smaller power variation over temperature than the presented design. As discussed in the previous chapter, the large variation of the biasing current limits the operational temperature range to [0,100°C]. The adoption of the MOS-resistors reduces the poly resistor area by 67x and the VR chip area by 39% while the decoupling capacitors at the output node occupy a lot of area. Excluding the decoupling capacitors, the area reduction is 59%. In terms of corner variations, the resistor-less design reveals smaller variation since the large biasing current variation introduces temperature dependency to the V_{REF} and happens to balance out the variation of ΔV_t.

TABLE 6-2: Performance summary and comparison with the VR in Chapter 6.1.

		Resistor-less VR	VR in Chapter 6.1
Type		ΔV_t	ΔV_t
Results type		Simulations	Measurements
VDD_{min} @TT&25°C (V)		0.5	0.62
Using poly resistor?		No	Yes
Area (mm^2)	Excluding decoupling capacitors	0.021	0.051
	Including decoupling capacitors	0.047	0.077
Temperature range (°C)		[0,100]	[-25,110]
TC (ppm/°C)		15@TT	108
Power @0.8V & @TT&25°C (nW)		38	38
Power @0.8V & @TT&T_{max} (nW)		534	39
Average power variation (1/ºC)[a]		0.29	0.008
V_{REF} corner variations (%)		±0.5	±1.5
Line sensitivity (%/V)		0.2	0.07
PSRR @100Hz (dB)		59	62

[a] Defined as P_{Tmax} / P_{Tmin} / (T_{max} - T_{min}).

6.4 A sub-nW resistor-less CMOS VR

The previous three sub-chapters introduce some techniques for a low-power small-area CMOS VR. However, the proposed designs still suffer from large chip area (with poly resistors) or large power variations over temperature and reduced operational temperature range. This sub-chapter presents a low-power and small-area CMOS VR with a large temperature range from -40ºC to 125ºC and a stable sub-nW power consumption over the entire temperature range [58].

6.4.1 Fundamental principle

In Chapter 6.2, a 3-stage sample-and-hold is presented to duty-cycle the voltage reference in Chapter 6.1 to reduce the power consumption. One step further, the techniques used in these designs can be combined in a more straightforward way so that the entire voltage reference operates dynamically to achieve low power.

6.4.2 Dynamic operation

In the VR in Chapter 6.1, the gate voltage difference, ΔV_G, is already a reference voltage that is insensitive to PVT while the resistors and the negative feedback loop generate the biasing current and a reference voltage relative to ground. The gate voltage difference can be sampled and held on a capacitor as shown in Figure 6.25. The dynamic operation is divided into two phases: sample phase (φ_1) and hold phase (φ_2). During the sample phase, a storage capacitor C_S is connected between V_{hg} and V_{ng} and the charge stored on C_S is $\Delta V_g \cdot C_S$. During the hold phase, the bottom plate of C_S is shorted to ground and the top plate is floating as in Figure 6.25 (b). The charge on C_S will remain the same so that the voltage of the top plate will be ΔV_g, which is the desired reference voltage relative to ground. It is noted that there is just a voltage shift from sample to hold so that there is no charge redistribution or power consumption. During the hold phase, the reference voltage is provided from the storage capacitor C_S so that the two branches of M_{nvt} and M_{hvt} can be switched off and the voltage reference does not consume power.

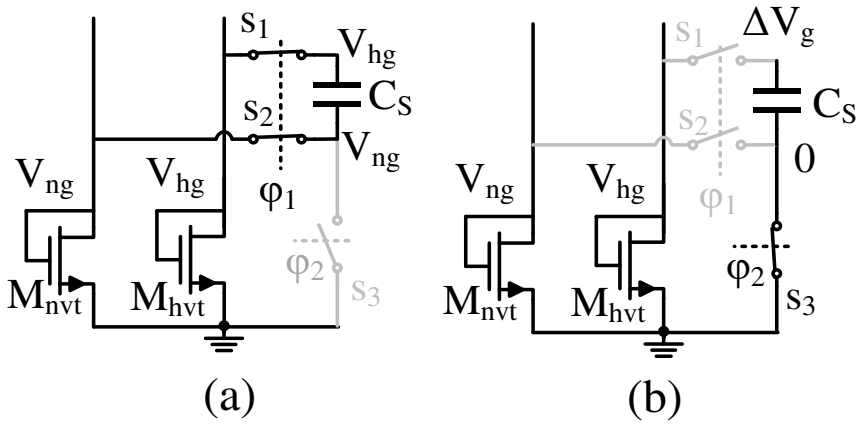


Figure 6.25: (a) Sample phase of the dynamic voltage reference; (b) hold phase.

The value of C_S and the leakage through s_1 in the hold phase determine how stable C_S can hold the reference voltage ΔV_g. A multi-stage switched capacitor circuit can be used to reduce the leakage and hence prolong the hold time as in Chapter 6.2 (Figure 6.26). During the sample phase, C_{S1} and C_{S2} sample the gate voltage difference in parallel. During the hold phase the bottom plates of C_{S1} and C_{S2} are shorted to ground simultaneously so that both the top plate voltages equal to ΔV_g. Now that the V_{DS} of MOS switch s_4 is much smaller than that of s_1, the leakage through s_4 is smaller than s_1, leading to a more stable ΔV_{g2} than ΔV_{g1} as described in Chapter 6.2.

Instead of a negative feedback loop utilizing an OPAMP, this design adopts an open loop with switched capacitors, which reduces the circuit complexity and improves the startup time.

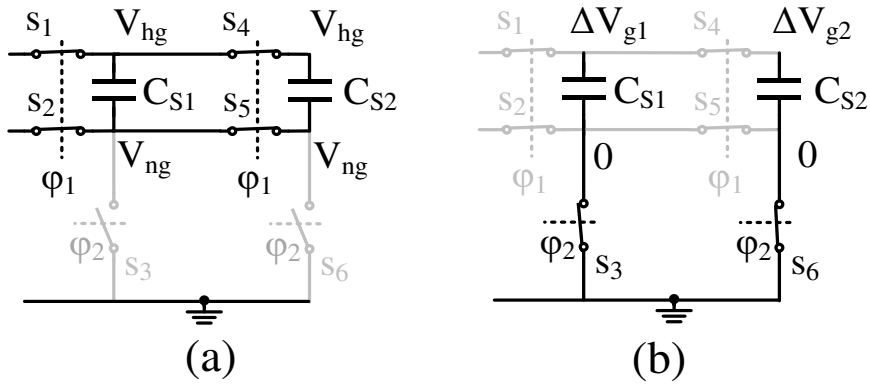


Figure 6.26: Multi-stage capacitors to prolong the hold time; (a) sample phase, (b) hold phase.

6.4.3 Bias current generation

During the sample phase, two current branches with a certain ratio are required. ΔV_g is mostly determined by this current ratio while it has a weak relation with the absolute current. However, if the absolute I_1 and I_2 fluctuate too much, ΔV_g will be affected and the temperature range would be compromised like the VR in Chapter 6.3.

In order to achieve a wide temperature operation range and a low-power voltage reference throughout this range, a temperature-insensitive bias current is required. The conventional current reference [18] requires a resistor. In a sub-nA design, this resistor might be in the order of 100MΩ, causing large chip area. Alternatively, the resistor can be replaced by a switched capacitor [18] as shown in Figure 6.27. The equivalent resistance can be expressed as:

$$R=\frac{1}{f_{Clk}\cdot C_2} \tag{6-12}$$

where f_{clk} is the clock frequency. In many SoCs, a real-time clock (RTC) is running in the background and it is assumed here that a 32.768kHz clock is continuously available. The capacitance value of C_2 is 400fF, resulting in a reference current of 140pA. In order to filter the high frequency components introduced by the switches, C_1 (200fF) is placed between the gate of M_2 and VDD.

As discussed previously, in advanced technology nodes where the gate leakage is large, the accuracy of a low-power voltage reference will be greatly impacted. In this design, thanks to the dynamic operation, a large biasing current of about 3nA can be tolerated during the short active time of the two core transistors while achieving low average power. Thanks to the large bias current, the impact of leakage becomes relatively smaller, such that a better accuracy can be achieved.

Since the RTC frequency and C_2 reveal very small temperature dependency, the bias current varies only a factor 2 from -40 to 125 ºC, which helps to bias the voltage reference core in the proper region and to achieve a low power consumption variation over temperature.

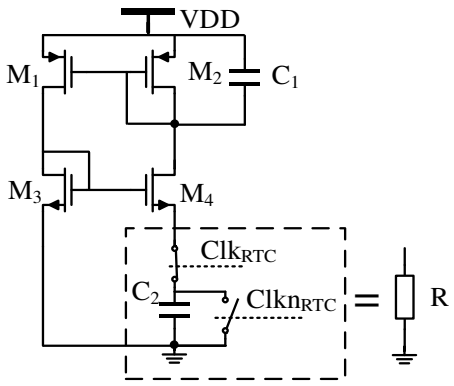


Figure 6.27: Bias current generation with switched capacitor equivalent resistor.

6.4.3 Simulation results

The complete voltage reference is shown in Figure 6.28 comprising of voltage reference core, current bias, sample-and-hold network and the load capacitor C_L. Switch M_9 and M_{10} are inserted to duty cycle the two branches of M_{nvt} and M_{hvt}. A two-stage sample and hold is adopted to reduce the leakage and hence increase the hold time. Two clock signals are required: Clk_{RTC} is the background RTC clock (32.768kHz) of the system and Clk_{DC} (32Hz = 32.768kHz/1024) is the duty-cycle clock of the voltage reference with 2.34% (3/128) active time, which can be derived easily from the RTC. C_{S1} and C_{S2} are set to 1pF and 2pF respectively and a capacitor load C_L equal to 5pF is driven in the following simulations. The following simulation results are obtained with 0.9V VDD at typical corner and room temperature unless stated otherwise.

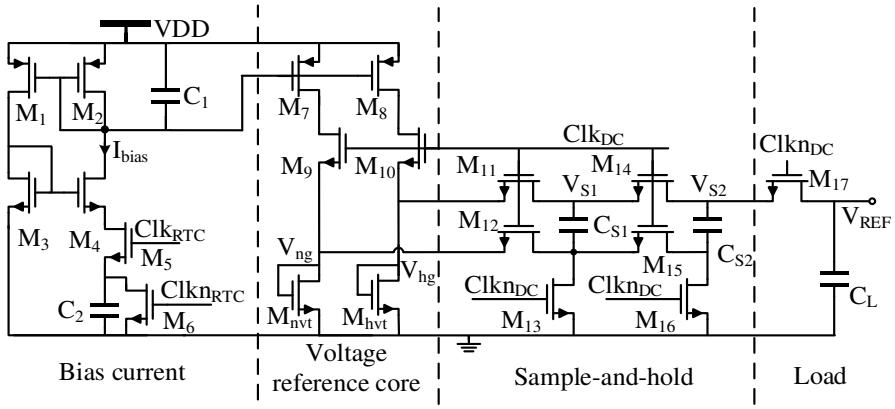


Figure 6.28: The complete dynamic voltage reference with capacitor load.

Timing Diagram

The operation timing of the voltage reference is shown in Figure 6.29. The bias current is always on in the background while the voltage reference is duty-cycled. Since the output voltage is stored on capacitors, it takes several clock cycles to charge the load capacitor during the initial period. During the sample phase (φ_1), C_L is disconnected from C_{S2} since now V_{S2} is connected to V_{hg} which causes an undesirable ripple $\Delta V_{\varphi 1}$ equal to 0.4mV (0.09% of V_{REF}) at typical corner and room temperature. During the hold phase (φ_2), C_L is connected back to C_{S2} and V_{REF} is refreshed. Thanks to the multi-stage sample and hold, the voltage change $\Delta V_{\varphi 2}$ of V_{REF} during φ_2 is only 0.021mV (0.016% of V_{REF}). At the worst corner and temperature, $\Delta V_{\varphi 1}$ is 0.56mV and $\Delta V_{\varphi 2}$ is 0.123mV.

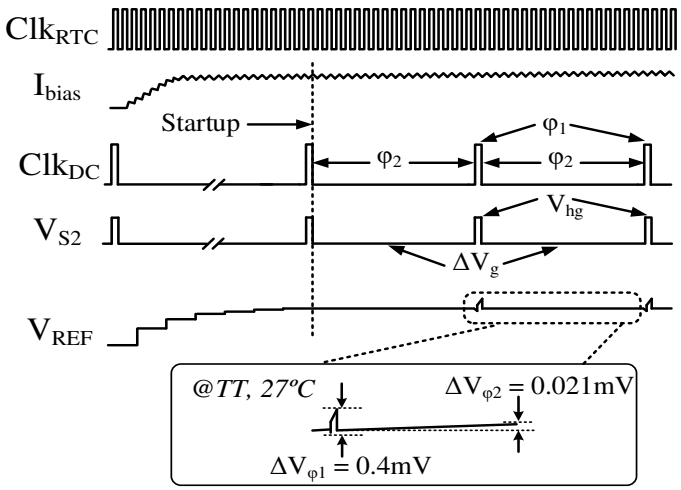


Figure 6.29: The timing of the voltage reference with capacitor load.

Temperature Coefficient

The temperature dependency of V_{REF} is shown in Figure 6.30 at 5 corners from -40 to 125ºC. The V_{REF} at the beginning of φ_2 is shown here. Over these corners, a best TC of 5.3ppm/ºC and an average TC of 18.1ppm/ºC are achieved.

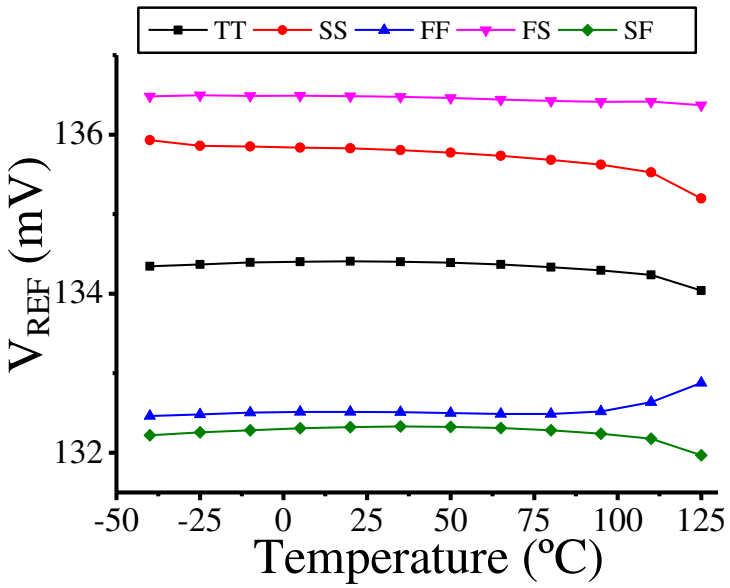


Figure 6.30: Temperature dependency of VREF at 5 corners.

Power Consumption

The total power consumption and its breakdown versus temperature are shown in Figure 6.31. Thanks to the temperature-insensitive bias current, the voltage reference has only 2x power variation throughout the large temperature range from -40 to 125ºC. The voltage reference core consumes less than 0.2nW due to the short 2.34% active time. The always-on bias current generation consumes most of the power. Duty cycling this block could further reduce the total power consumption. At different corners, the power consumption at room temperature varies from 0.304 to 0.361nW and the maximum power is 0.639nW at FF corner and 125ºC.

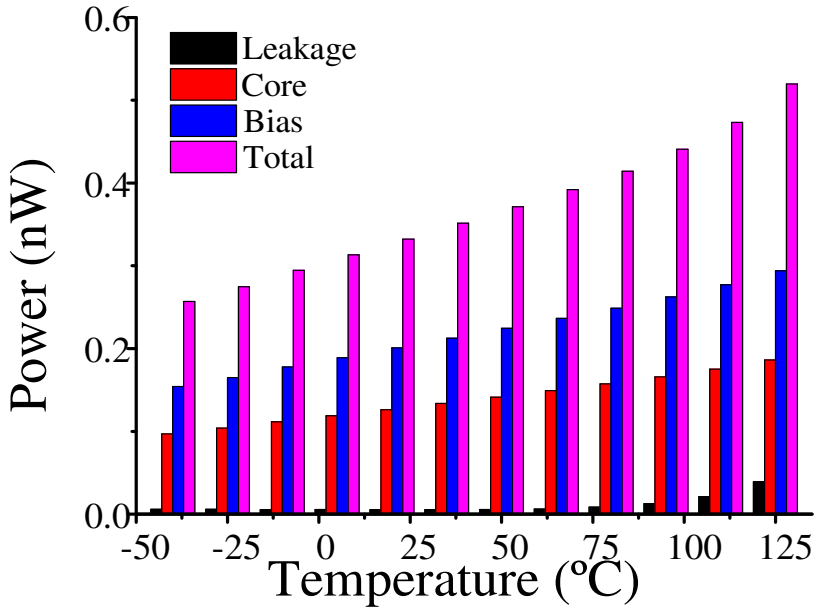


Figure 6.31: Power breakdown of the dynamic voltage reference.

Process Variations

From Figure 6.30, it is found that V_{REF} fluctuates 3% at 5 corners at room temperature, which corresponds well to the voltage reference in Chapter 6.1 (Figure 6.7).

Line Sensitivity

The minimum VDD at all the corners throughout the temperature range is 0.9V. At typical corner, the voltage reference reveals a line sensitivity (LS) of 1.29%/V (Figure 6.32).

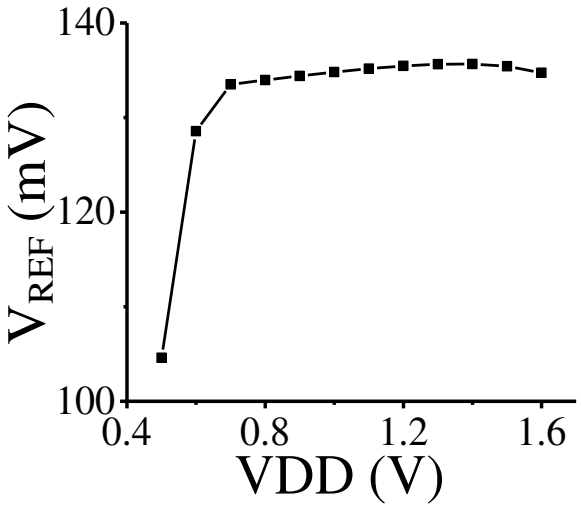


Figure 6. 32: VDD dependency of the V_{REF}.

Chip Area

The layout of the voltage reference (excluding the load C_L) is shown in Figure 6.33. Instead of large resistors, switched capacitors are utilized. As a result, the voltage reference occupies a chip area of only 4600µm^2.

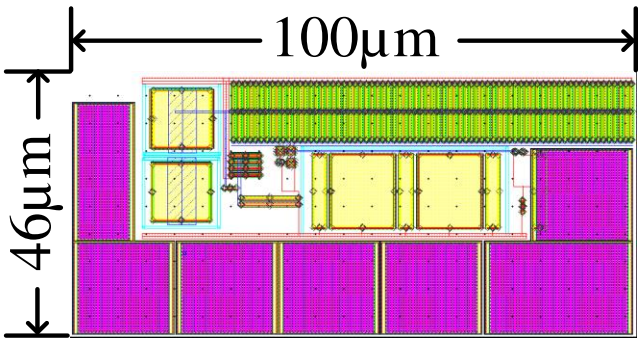


Figure 6.33: Layout of the dynamic VR in 65nm CMOS.

Summary and comparison

The performance summary and comparison of the dynamic VR are shown in TABLE 6-3. This design and the VRs in Chapter 6.1 and 6.3, are all based on the threshold voltage difference between nominal-V_t and high-V_t transistors. The difference is the way how the preliminary generated reference voltage (the gate voltage difference) is converted to a

voltage relative to ground. By utilizing a dynamic operation to sample and hold the gate voltage difference directly, the design is simplified and no resistors are required, achieving low power and small chip area. The power consumption is reduced by 8x and the chip area is reduced by 5x and 11x compared to the VRs in Chapter 6.3 and 6.1 respectively. The low-power current generator maintains a small temperature dependency of the V_{REF} and the power consumption. Compared with [19], which is based on the threshold voltage difference between native and I/O NMOS, this design reveals smaller corner variations. Compared to [19] and [60], the presented design has better TC and lower power consumption variation throughout a wider temperature range.

TABLE 6-3: Performance summary and comparison of the dynamic VR.

	This work	Chapter 6.3	Chapter 6.1	*[19]*	*[60]*
Results type	Simulated		Measured		
Technology(nm)	65	65	65	65	180
Topology	$\Delta V_{t,ion}$	$\Delta V_{t,ion}$	$\Delta V_{t,ion}$	$\Delta V_{t,type}$	BJT
VDD_{min} (V)	0.9	0.5	0.62	0.5	>1.2
V_{REF} (V)	0.134	0.331	0.390	0.327	1.190
Duty-cycle rate (active time)	2.34%	10%[b]	10%	-	0.003%
Temperature range (ºC)	-40~125	0~100	-25~110	-40~80	-20~100
Power(nW)@25ºC	0.33	2.5	2.5	0.240	2.98
Power(nW) @T_{max}	0.52 @125ºC	531 @100ºC	2.6 @110ºC	2.2 @80ºC	200 @100ºC
Average power variation (1/ºC)[a]	0.012	0.29	0.008	0.8	4.2
TC (ppm/ ºC)	5.3~31.3	15~115	44~248	89~118	24.7
LS (%/V)	1.29	0.2	0.07	0.33	0.062
Corner variation (%)	3	1	3	10[b]	-
Area (μm^2)	4600	21490[c]	51240[c]	9300	980000

[a.] Defined as P_{Tmax} / P_{Tmin} / (Tmax - Tmin).

[b.] Assuming the 3-stage duty-cycling technique is applied.

[c.] Excluding decoupling capacitors.

6.5 CMOS VR based on single-type of transistor

The three voltage references introduced in the previous sub-chapters are based on the

threshold voltage difference between nominal-V_t and high-V_t transistors. However, high-V_t transistors are not supported by all CMOS technologies due to cost. In this chapter, a low-power resistor-less voltage reference using only nominal-V_t transistors is presented. It is based on the threshold voltage difference between nominal-V_t transistors with different sizes.

6.5.1 Threshold voltage and the sizing

The threshold voltage of nominal-V_t transistors changes with its size, e.g., due to short channel and narrow channel effects. In the adopted 65nm CMOS technology, the threshold voltage is simulated with difference sizes as shown in Figure 6.34. It can be found that the V_t decreases with an increasing length of the NMOS and approaches a stable value with large length, while the width has less impact on the V_t and the V_t remains constant with a width larger than certain value. Now that a threshold voltage difference can be achieved with the same type of NMOS with different sizes, the temperature and process dependency of this voltage difference has to be investigated before being adopted in a voltage reference design.

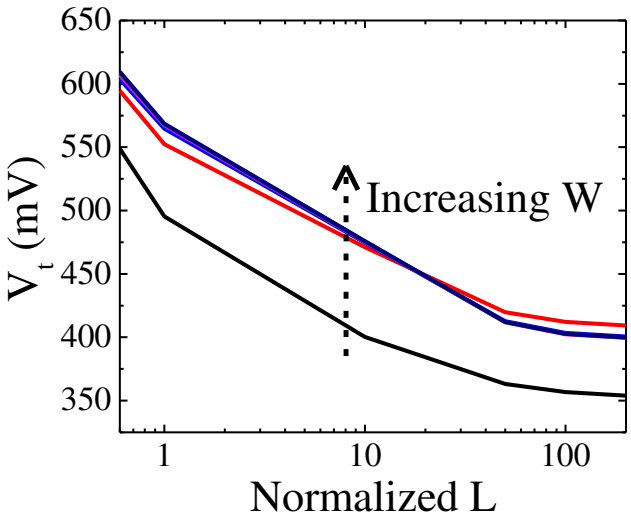


Figure 6.34: Threshold voltage of the nominal-V_t NMOS with different size in 65nm CMOS.

The threshold voltage difference between two transistors with the same width but with different length is investigated. W is set to a large value, such that the sensitivity of V_t to W is negligible and V_t only depends on the length. Then, the length of one transistor is fixed at 10µm, while the other length L is swept. The achieved $\Delta V_{t,sizing}$ is shown in Figure 6.35 for 3 process corners. For a larger length difference, the threshold voltage difference also

becomes larger. However, it also suffers from increased process variations.

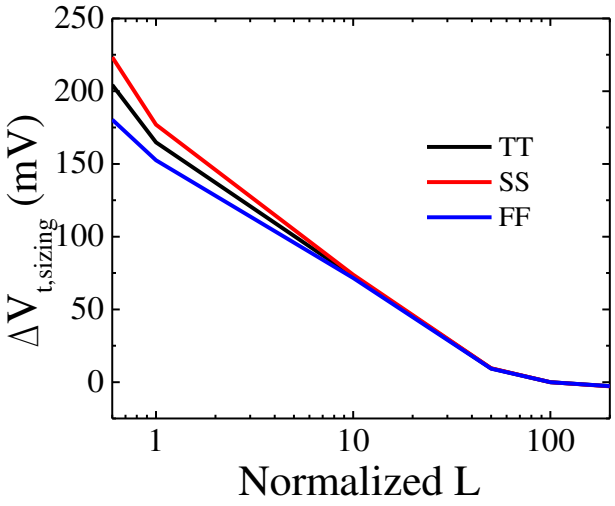


Figure 6.35: Threshold voltage difference $\Delta V_{t,sizing}$ between two transistors with identical width W, but different length (10µm vs L).

The temperature coefficient of the threshold voltage is shown in Figure 6.36. As before, one transistor has a length of 10µm, while the other length L is swept. A larger threshold voltage difference reveals a larger TC. Moreover, the TC is proportional to absolute temperature.

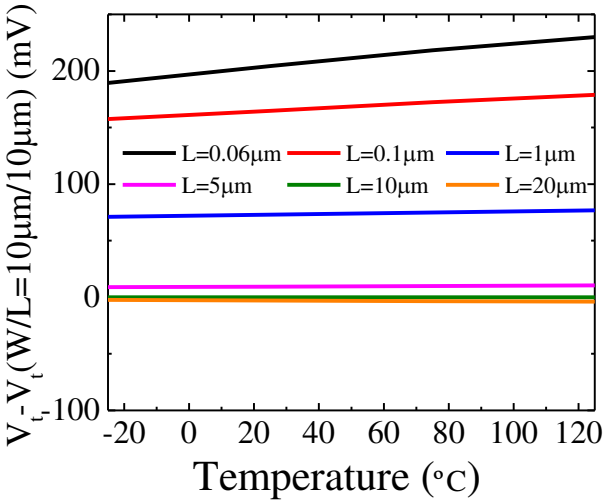


Figure 6.36: Temperature coefficient of the threshold voltage difference between two transistors with identical width W, but different length (10µm vs L).

6.5.2 A resistor-less VR with single-type of NMOS

If the topology from Chapter 6.3 is used, but the two different types of transistors are replaced with the same type of transistors with different size, a resistor-less voltage reference that is more compatible to cheap CMOS technology can be realized. The feasibility of this should be evaluated from 3 aspects as follows.

Temperature coefficient and the value of ΔV_G

As shown in Figure 6.36, $\Delta V_{t,sizing}$ reveals a positive TC, opposite to $\Delta V_{t,ion}$. This is not a big problem as it can be seen from (6-3) that by certain design ratio, the coefficient of the second term can be negative and the TCs can still cancel out each other. The drawback is that the resulting ΔV_G will be smaller than $\Delta V_{t,sizing}$. A small ΔV_G will be sensitive to noise and offset of the OPAMP in the negative feedback loop.

The biasing of MOS resistors

Another problem introduced by a smaller ΔV_G is the biasing of the MOS resistors. During normal operation, the MOS resistor is biased with a V_{SG} equal to ΔV_G. If ΔV_G is not large enough, the MOS resistor will be biased in deep sub-threshold region and it requires a large MOS resistor size to generate large enough biasing current for the two core transistors.

Process variation

The previous discussion indicates that a large ΔV_G is preferred while a larger ΔV_G will suffer more from process variations (Figure 6.35). As a result, the sizing of the two core transistors is a tradeoff between above points.

A resistor-less voltage reference using only nominal-V_t transistors was designed and is shown in Figure 6.37. The size of the two core transistors are chosen to be 10µm/2µm and 2×10µm/10µm, which results in a $\Delta V_{t,sizing}$ of 35mV. The current ratio is 2.3:1, leading to a ΔV_G of about 19mV. As a result, the MOS resistors have to be very large to generate enough biasing current at all corners throughout the temperature range. They are set to be 400µm/0.06µm, made up with 20 transistors (20µm/0.06µm) in parallel. ΔV_G is multiplied by 12 times and a V_{REF} around 230mV is generated.

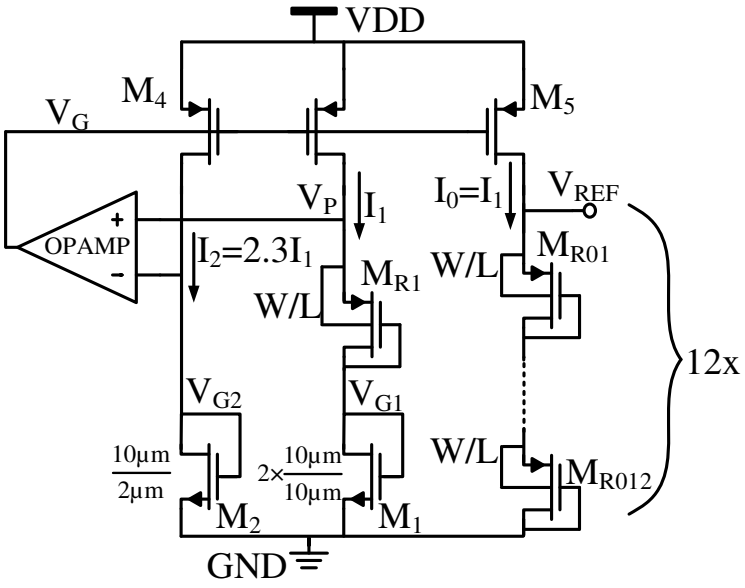


Figure 6.37: The resistor-less voltage reference using only nominal-V_t transistors

6.5.3 Simulation results

The resistor-less voltage reference using only a single-type of transistors is simulated in 65nm CMOS technology. At typical corner and room temperature, the VDD dependency of the V_{REF} is shown in Figure 6.38. It operates from a minimum VDD of around 0.6V and the line sensitively is 0.5% from 0.6V to 2.0V.

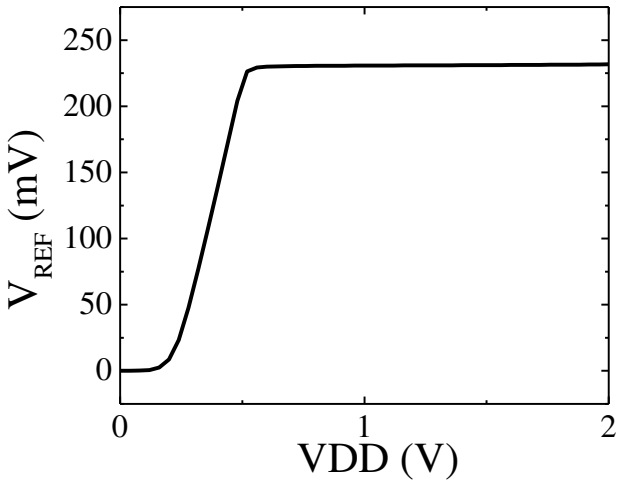


Figure 6.38: VDD dependency of V_{REF} at typical corner and room temperature.

The temperature dependency of V_{REF} at different corners is shown in Figure 6.39. At the typical corner, the TC is optimized to be 25.8 ppm/ºC from 0 to 100ºC. The TC of V_{REF} is 48.5ppm/ºC, 129.3 ppm/ºC, 63.8 ppm/ºC, and 95.2 ppm/ºC at SS, FF, SF, and FS corner respectively. Similar with the VR in Chapter 6.3, due to the adoption of the MOS resistors, the temperature range is limited and the TC has a large variation between corners. At room temperature, the variation of V_{REF} is 6%, which is worse than for the $\Delta V_{t,ion}$-based VRs while still better than for the absolute V_t-based VRs (~15%). Similar as the VR in Chapter 6.3, the power consumption also reveals an exponential relation with temperature. At the typical corner and room temperature, the current consumption is around 19nA.

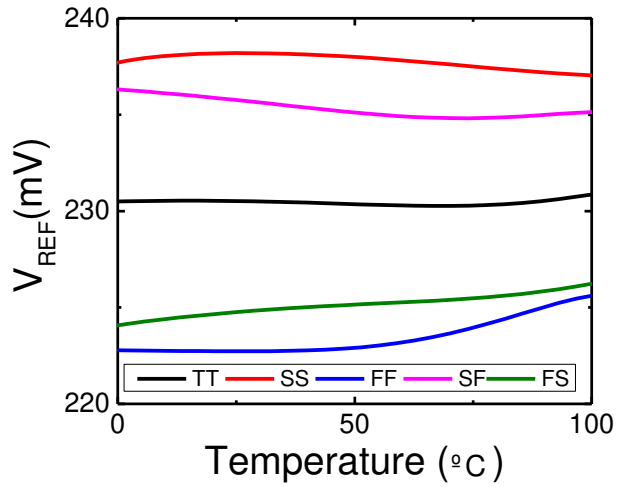


Figure 6.39: Temperature dependency of V_{REF} at 5 corners.

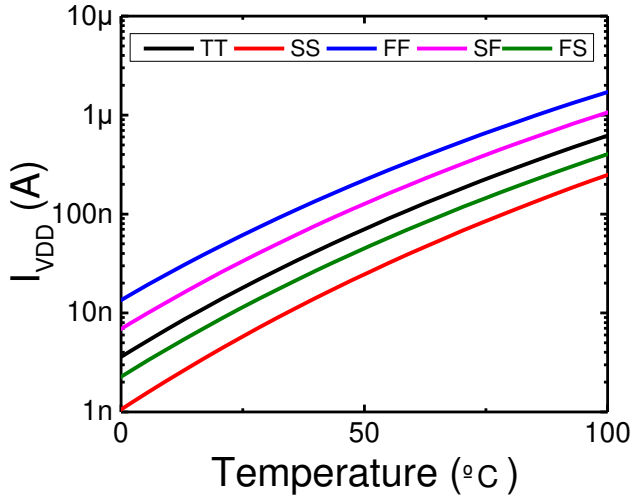


Figure 6.40: Temperature dependency of current consumption.

The PSRR of the voltage reference is shown in Figure 6.41(with 50pF decoupling capacitor at the output V_{REF} node), revealing a similar curve as the VR in Chapter 6.3.

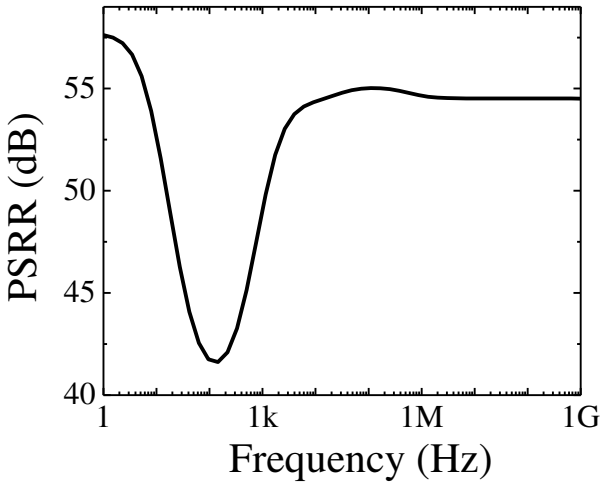


Figure 6.41: PSRR of the voltage reference.

The layout of the voltage reference in shown in Figure 6.42, which occupies a chip area of 0.026mm^2, while 0.018mm^2 is occupied by the decoupling capacitors. The MOS-resistors also occupy large chip area due to the large size (20×20µm/0.06µm) and large ratio (12x). The required stand-alone Nwell for each single MOS resistor doubles the chip area further. The OPAMP occupies small chip area.

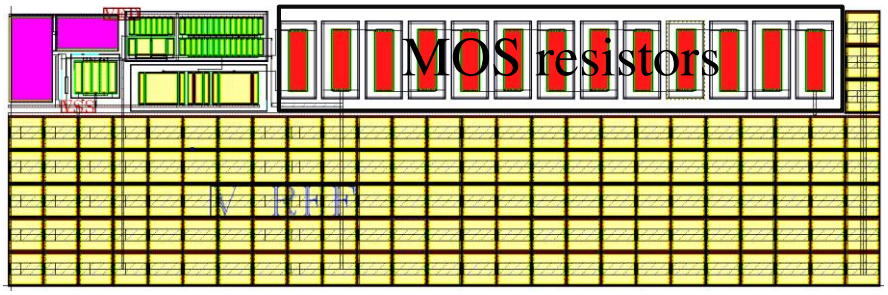


Figure 6.42: Layout of the VR in 65nm CMOS.

The performance summary and comparison with the VRs from previous sub-chapters is listed in TABLE 6-4. The presented resistor-less VR, based on the threshold voltage difference between nominal-V_t transistors with different sizing, is more compatible to low-cost technology. It reveals similar power consumption as previous designs. Due to the adoption of MOS resistors, the temperature coefficient is affected and the temperature range is limited. The power consumption is changing exponentially with temperature like the VR in Chapter 6.3. The process variation is 2x worse than the $\Delta V_{t,ion}$-based VRs while still more than 2x better than the absolute V_t-based VRs. The chip area is only 8000µm^2 thanks to the

MOS resistors and optimized OPAMP.

TABLE 6-4: Performance summary (simulations) and comparison of the presented VR.

	This section	Chapter 6.4	Chapter 6.3	Chapter 6.1
Results type	Simulated			Measured
Technology(nm)	**65**	65	65	65
High-V_t transistor required?	**No**	Yes	Yes	Yes
Topology	**ΔV_t (size)**	ΔV_t (low/high)		
VDD_{min} (V)	**0. 6**	0.9	0.5	0.62
V_{REF} (V)	**0.230**	0.134	0.331	0.390
Duty-cycle rate (active time)	**10%**[b]	2.34%	10%[b]	10%
Temperature range (ºC)	**0~100**	-40~125	0~100	-25~110
Power (nW)@25ºC	**1.1**	0.33	2.5	2.5
Power (nW) @T_{max}	**360 @100º C**	0.52 @125ºC	531 @100ºC	2.6 @110ºC
Average power variation (1/ºC)[a]	**0.16**	0.012	0.29	0.008
TC (ppm/ ºC)	**25.8~129.3**	5.3~31.3	15~115	44~248
LS (%/V)	**0.5**	1.29	0.2	0.07
Corner variation (%)	**6**	3	1	3
Area (μm^2)	**8000**	4600	21490[c]	51240[c]

[a.] Defined as P_{Tmax} / P_{Tmin} / (Tmax - Tmin).

[b.] Assuming the 3-stage duty-cycling technique is applied.

[c.] Excluding decoupling capacitors.

6.6 Comparisons

This chapter introduces two fundamental principles for a voltage reference core: $\Delta V_{t,ion}$ and $\Delta V_{t,sizing}$, which are compared in TABLE 6-5. $\Delta V_{t,ion}$-based VRs have smaller process variations and the resulting ΔV_G is large, reducing the design complexity, while the $\Delta V_{t,sizing}$-based VRs are more compatible to low-cost CMOS technology.

TABLE 6-5: Comparison of $\Delta V_{t,ion}$ and $\Delta V_{t,sizing}$ topologies.

Topology	$\Delta V_{t,ion}$	$\Delta V_{t,sizing}$
Process variation	Good	Medium
Value of the achieved ΔV_G	Large	Small
Technology compatibility	Medium	Good

Subsequently, the preliminarily generated reference voltage, ΔV_G, needs to be converted to a reference voltage relative to ground. Three methods are presented in this chapter: poly resistor, MOS resistor, and dynamic operation, which are compared in TABLE 6-6. Using poly resistors results in good temperature performance while the chip area is large. On the contrary, using MOS resistors reduces chip area but results in worse temperature performances. The dynamic operation can achieve small chip area and good temperature performance simultaneously.

TABLE 6-6: Comparison of methods to copy ΔV_G.

Method to copy ΔV_G	Poly resistor	MOS resistor	Dynamic operation
Chip area	Large	Small	Small
Temperature range and TC	Good	Poor	Good
Temperature dependency of power	Small	Large	Small

6.7 Conclusions

CMOS non-bandgap voltage references are popular thanks to the low-VDD and low-power properties. Some problems of prior-art CMOS VRs like the large process variations and the compatibility with technology have been addressed in this chapter. Several techniques and designs for low-power voltage references have been introduced and compared: two fundamental principles for a voltage reference core ($\Delta V_{t,ion}$ and $\Delta V_{t,sizing}$); three methods to copy the preliminarily generated reference voltage, ΔV_G, and output a reference voltage relative to ground (poly resistors, MOS resistors, and dynamic operation); a multi-stage sample-and-hold block to duty-cycle a static VR to reduce the average power. These techniques reveal tradeoffs regarding chip area, temperature performance, power consumption, technology compatibility, etc. By combining above techniques, a CMOS voltage reference with low power (nW-range or sub-nW), low VDD (sub-1V), small area ($<5000\mu m^2$) can be realized.

Chapter 7 CR-DAC reference drivers for SAR ADCs

The CR DAC in a SAR ADC generates binary voltage steps to realize a binary search algorithm as shown previously in (3-2). Besides the requirement of a highly linear binary DAC, a constant voltage reference is also very critical to generate the binary voltage steps. In most SAR ADC publications, the generation of a voltage reference is ignored, and an external instrument is usually used to provide the reference voltage externally during the experiments. However, in an integrated system, the reference generation must be present on-chip and its implementation needs to be investigated and addressed. In the previous chapter we discussed the voltage-reference generation itself. The combination of such an on-chip reference voltage generator and the DAC can lead to undesired interactions: the reference driving problem.

This chapter discusses and compares several existing voltage-reference driver solutions for a CR DAC where each of them has some shortcomings to overcome. Part of this chapter was published in [61].

7.1 CR-DAC reference drivers

From literature, there are generally three categories of solutions to the reference driving problem of the CR DAC in a SAR ADC: fully active drivers, hybrid drivers that comprise an active driver and a passive driver (a decoupling capacitor), and fully passive drivers, as shown in Figure 7.1. Among the first category, two solutions will be introduced: driving a binary DAC with a fully active driver, and driving a redundant DAC with a fully active driver. Among the second category, driving a binary DAC with an active driver combined with a large passive decoupling capacitor is introduced. Among the fully-passive driver category, a V_{REF} voltage drop compensation and a signal-independent V_{REF} drop scheme are discussed.

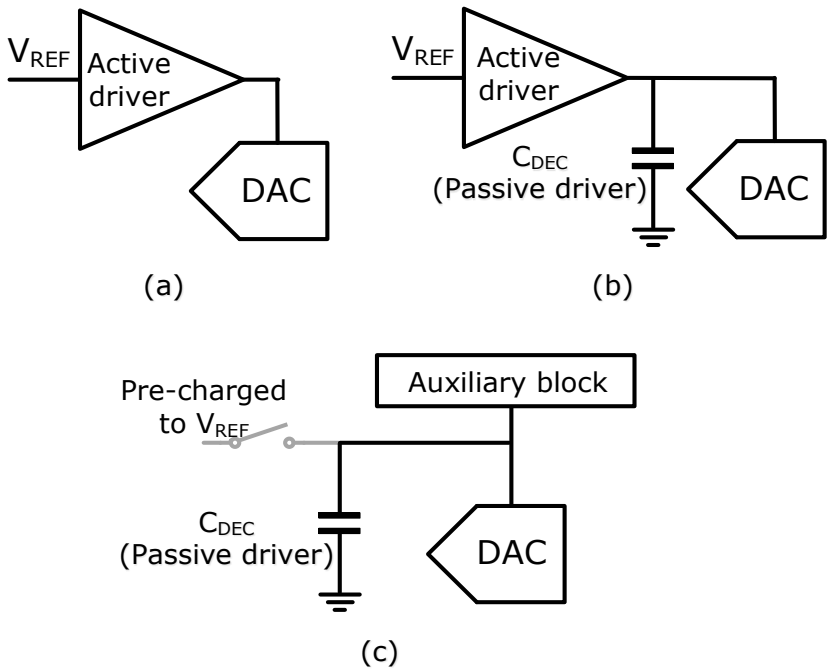


Figure 7.1: Three categories of solutions to the reference driving: (a) a fully active driver; (b) a hybrid driver comprising an active driver and a passive driver; (c) a fully passive driver.

7.1.1 Driving a binary DAC with a fully active driver

The most conventional and straightforward solution to the driving problem in a DAC is to use an active driver [62, 63, 64, 21, 22]. In general, a K-bit SAR ADC requires at least (K-1) DAC switching steps and a constant reference voltage is required after each switching step (Figure 7.2). As a result, the driver needs a bandwidth much larger than the sampling rate of the SAR ADC, consuming high power. In [62, 63, 64, 22, 21], the active driver consumes 9x, 25x, 0.8x, 0.7x, and 4.5x the power of the SAR ADC respectively.

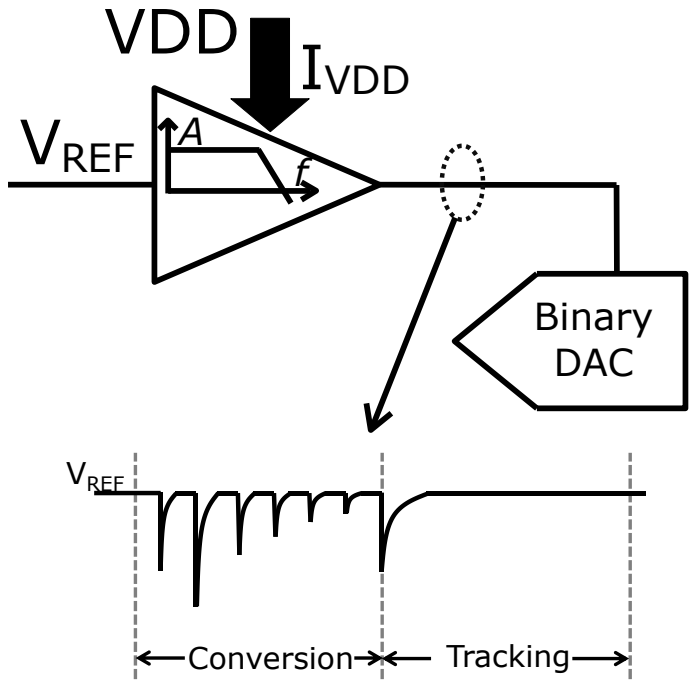


Figure 7.2: Driving a binary DAC with an active driver.

7.1.2 Driving a redundant DAC with a fully active driver

In order to relax the harsh requirements for the active driver driving a binary DAC, redundancy can be inserted in the DAC. Redundancy helps to tolerate the errors that happened in previous conversion steps due to settling errors in the reference voltage or comparator noise, as long as the error is still within the redundancy range and the later comparisons are correct. Consequently, the reference driver does not need to recover the reference voltage up to the accuracy normally required for each bit that precedes the redundancy, but to a significantly lower accuracy, depending on the amount of redundancy applied, which reduces the speed and the power requirements for the driver (Figure 7.3). However, a redundant DAC means more steps of comparison, resulting in longer conversion time and possibly lower sampling rate of the SAR ADC. Moreover, the achieved preliminary raw non-binary data has more bits than the resolution of the SAR ADC, hence requiring digital post processing at the expense of circuit complexity and power consumption.

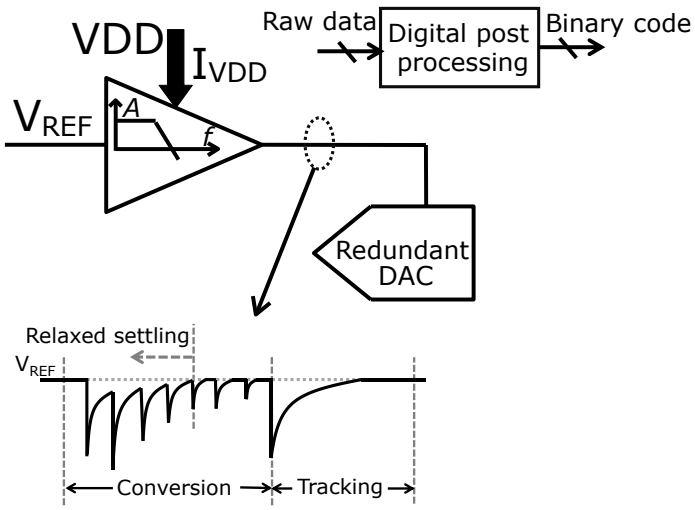


Figure 7.3: Driving a redundant DAC with a relaxed active driver.

7.1.3 Driving a binary DAC with a hybrid driver

Apart from a high-bandwidth driver, a large capacitor can also be utilized to provide a nearly constant reference voltage during the conversion of a binary DAC. In order to achieve a negligible reference voltage drop on the capacitor, the decoupling capacitance has to be large enough, at the expense of chip area. For example, in [65] it is 200x the total capacitance of the DAC in the SAR ADC. In the meantime, a low-speed active driver is recovering the reference voltage on the capacitor slowly as shown in Figure 7.4, consuming low power. Compared with driving a binary DAC with an active driver (sub-chapter 7.1.1), driving with a large decoupling capacitor sacrifices chip area for low power consumption.

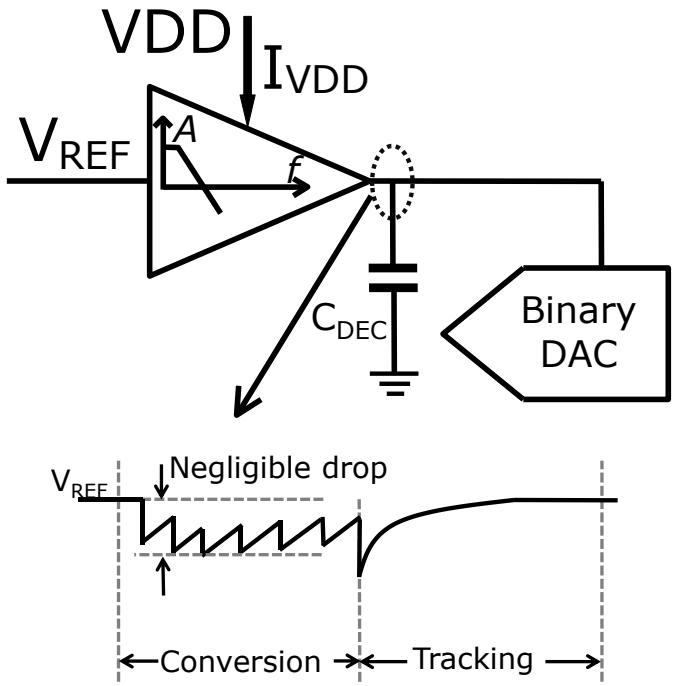


Figure 7.4: Driving a binary DAC with an active driver and a large decoupling capacitor.

7.1.4 Passive driving with reference voltage drop compensation

In order to get rid of both a power-hungry driver and a large decoupling capacitor, some solutions have been presented using a small decoupling capacitor driving a binary DAC passively and eliminating the signal-dependency of the reference voltage drop. As shown in Figure 7.5, in [66], one capacitor (C_{DEC}) is pre-charged to V_{REF} and besides, an extra capacitor array is pre-charged to V_{REFC}, a voltage higher than V_{REF}. During conversion, according to the specific code and charge consumption, a part of the extra capacitor array (C_{C1}, C_{C2},...) is connected to C_{DEC} to drive the DAC together to maintain a constant reference voltage (Figure 7.5). Equivalently, the charge consumed by the DAC is provided by part of the extra capacitor array. This scheme requires an extra reference voltage (V_{REFC}) higher than V_{REF} (usually V_{REF} = VDD), making it difficult to produce.

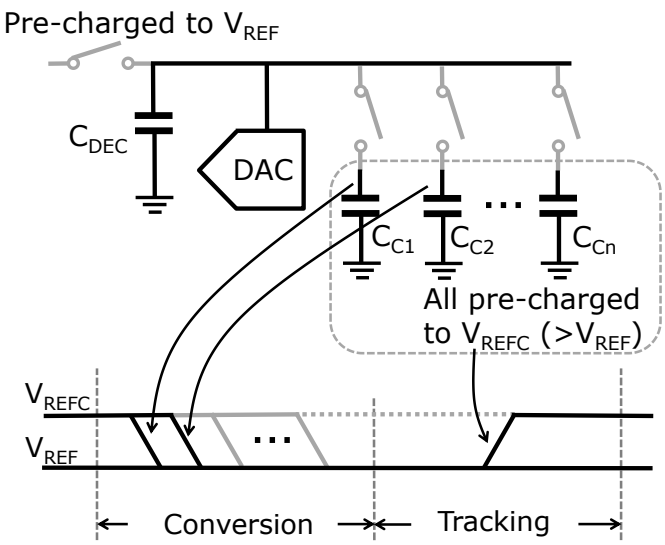


Figure 7.5: Passive driving with constant reference voltage [66].

7.1.5 Passive driving with signal-independent reference voltage drop

Alternatively to constant reference voltage compensation, a reference voltage drop can be tolerated and calibrated later. In [67, 68, 69], the reference voltage drop is not eliminated but made signal-independent. In [67], similar with [66], one capacitor, C_{DEC}, is pre-charged to V_{REF} and an extra capacitor array is discharged to ground during tracking (Figure 7.6). During conversion, a part of the extra capacitor array is connected to C_{DEC} for each switching step to draw the same amount of charge from C_{DEC} irrespective of the signal. In [68] and [69], the DAC, driven by a pre-charged reservoir capacitor [68] or multiple reservoir capacitors (one for each bit) [69], is designed in a way that the charge consumption is signal-independent. In [67, 68, 69], calibration and digital post processing are required to correctly reconstruct the output, increasing the implementation complexity and power consumption.

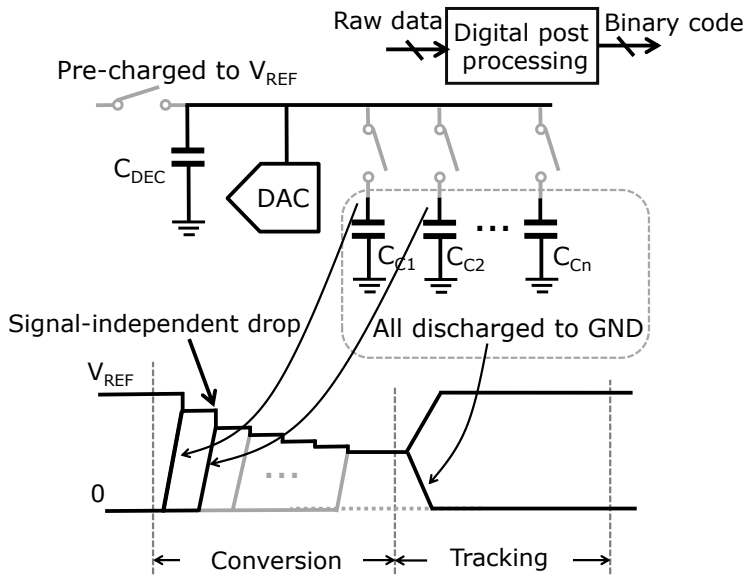


Figure 7.6: Passive DAC driving with signal-independent reference voltage drop [67].

7.1.6 Comparison of driver solutions

A comparison between the above driver solutions is summarized in TABLE 7-1. Using an active driver and an active decoupling capacitor simply trades off between power consumption and chip-area. In order to get rid of these tradeoffs, redundancy and passive decoupling capacitor drivers are developed so that the power requirements for the driver and area requirements for the capacitor are relaxed. However, digital post-processing or a higher reference voltage generator is required which in total degrades both the power and area improvements.

TABLE 7-1: Comparison between different driving solutions for a CR DAC.

	Driver power	Driver area	Digital post-processing
Active driver	High	Low	No
Active driver with redundant DAC	Medium	Medium	Yes
Hybrid driver	Low	Large	No
Passive driver with constant reference voltage	Medium	Medium	No
Passive driver with signal-independent V_{REF} drop	Medium	Medium	Yes

7.2 Conclusions

In this chapter, the design challenges of the reference driver for our preferred CR DAC are discussed. For the existing reference driver solutions, both active drivers and hybrid drivers result in high power and/or large chip area. On the other hand, a power-hungry and/or large driver is not needed when applying redundancy or a fully passive driver. While these techniques show a better power/area tradeoff, they come with some disadvantages like digital post-processing or a higher reference voltage. As a result, the challenge is to find solutions that are both low power and small area, without such disadvantages.

Chapter 8 Low-power and area-efficient SAR ADCs with reference driver

This chapter introduces two SAR ADC designs with different integrated reference driver. The first design utilizes a large off-chip capacitor, resulting in a low-power driver at the expense of area [55]. *In the second design, a low-power and area-efficient discrete-time reference driver is presented* [61]*, which avoids all the disadvantages of the current reference drivers for SAR ADCs discussed in Chapter 7.1.*

8.1 A SAR ADC with duty-cycled reference generation

This sub-chapter presents a 10b 80kS/s SAR ADC with low-power duty-cycled reference generation. It integrates the voltage reference presented in Chapter 6.1 with the high-efficiency duty-cycling technique discussed in Chapter 6.2, a low-power LDO with an off-chip capacitor, and a low power SAR ADC. In the SAR ADC, a bi-directional dynamic comparator is adopted, which consumes about half the power compared to a regular dynamic structure and maintains noise and gain performance. By combining above techniques, the reference-included SAR ADC achieves a competitive 2.4fJ/conversion-step FoM. The design of the voltage reference and the duty-cycling technique have been introduced in Chapter 6 and will not be repeated in this chapter.

8.1.1 Architecture of the SAR ADC with reference generation

The architecture of the SAR ADC with reference generation is shown in Figure 8.1. The system operates at one single external 0.8V VDD. The voltage reference (Chapter 6.1) generates a 0.4V reference voltage and is duty-cycled by CLK_1 to save power. With a 3-stage sample-and-hold block (Chapter 6.2), a continuously stable reference voltage is

provided to the LDO. The LDO then multiplies the reference voltage to 0.6V and powers the SAR ADC. An off-chip capacitor is used to stabilize the LDO (similar as the solution discussed in Chapter 7.1.3). The LDO is always-on to provide a stable supply and reference to the ADC during both tracking and conversion phases of the ADC.

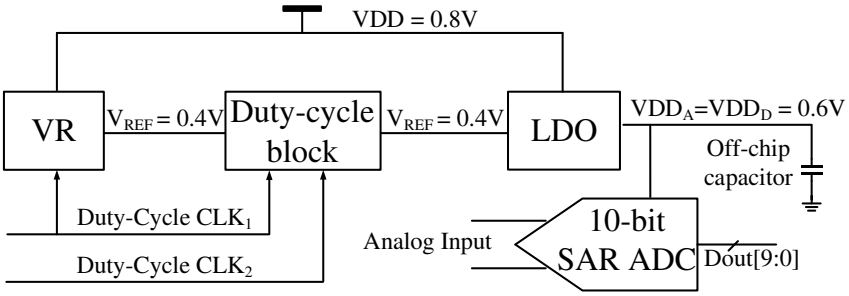


Figure 8.1: Architecture of the SAR ADC with reference generation.

8.1.2 LDO design

In this work, an off-chip capacitor (10μF) is adopted in the LDO driving the SAR ADC, which enables a low-power LDO at the expense of area. The SAR ADC in this work is primarily using dynamic circuits, which consume little static power but require large current peaks once in a while. Since the feedback loop of the LDO is too slow to respond to this load change, the off-chip capacitor will provide those current peaks with slight voltage drop. As a result, the LDO only needs to provide a nearly constant current equal to the average current consumption of the SAR ADC.

The schematic of the LDO is shown in Figure 8.2. A 2-stage OPAMP is utilized to achieve high loop gain. Since the impedance at the output of the LDO is very high, the resulting main pole locates at a very low frequency, so no extra compensation is needed here to guarantee the loop stability. As discussed previously, the LDO is always-on, which requires an always-on bias voltage for M_{19} and M_{25}. Looking back at Figure 6.13, V_{Bias} is duty-cycled and C_{S1} stores the voltage of V_{Bias} to make the rebuilding faster. Similar to the duty-cycling block, another S&H (C_{SB}) controlled by CLK_2 is inserted to generate continuous biasing voltage for M_{19} and M_{25}. Since the desirable output voltage of the LDO (0.6V) is 1.5x the input reference voltage (0.4V), divider resistors are inevitable, as long as the induced static current consumption. Hence, the divider resistors are set to 40MΩ and 80 MΩ, occupying large chip area. The current consumption of the LDO is $1.35I_1$, where I_1 is defined by ΔV_G and R_1 as shown in Figure 6.6.

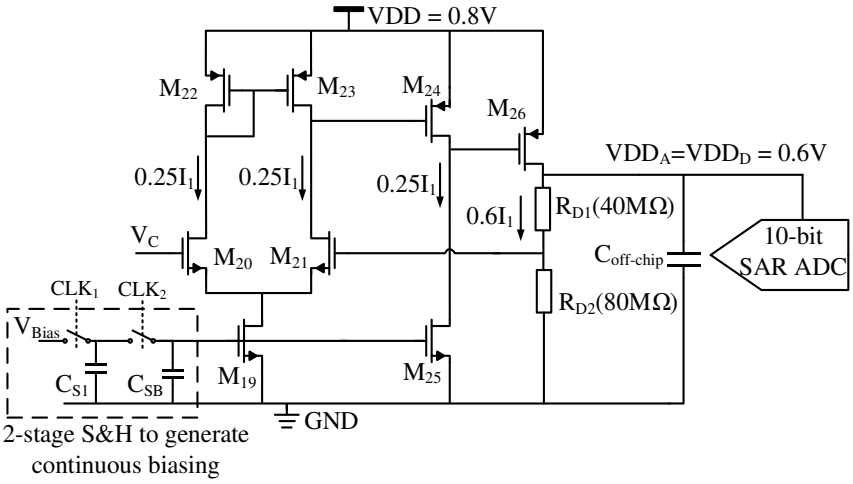


Figure 8.2: Schematic of the LDO with continuous biasing generation.

8.1.3 SAR ADC design

The 10b asynchronous SAR ADC is shown in Figure 8.3. The clock for the SAR logic is generated internally as in [35], hence only the sample clock is required externally. The DAC is segmented into 3 thermal encoded MSBs and 7 binary encoded LSBs, reducing power consumption and avoiding large MSB DNL errors. Lateral metal-metal capacitors [37] are adopted to implement the DAC and the total capacitance is 256fF for high power-efficiency. The power-efficiency of the SAR ADC is further improved by a low-power bi-directional dynamic comparator.

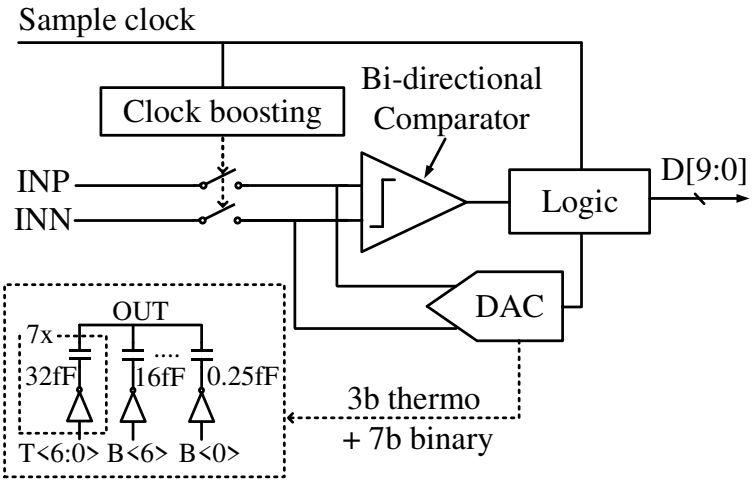


Figure 8.3: Architecture of the 10b SAR ADC.

8.1.4 Bi-directional comparator

The schematic and operation of a typical dynamic comparator [16] is shown in Figure 8.4. The comparator comprises an integration-based preamplifier and a latch. During the reset phase, the parasitic capacitors C_{PP} and C_{PN} (C_{PP} equals C_{PN}) are charged to VDD by M_4 and M_3 respectively. The comparison starts when CLK goes high. C_{PP} and C_{PN} are discharged through input pair M_2/M_1 and V_{AP} and V_{AN} will drop according to the input voltages V_{INP} and V_{INN}. In time, the common mode of V_{AP} and V_{AN} is gradually decreasing while the differential input signal is gradually amplified. When the common mode of V_{AP} and V_{AN} reaches the threshold of the latch, the latch will take over and output the comparison result. Next, CLK will go low and the pre-amplifier and latch are reset to their initial conditions. Thanks to the amplification of the preamplifier, the noise and power efficiency of the overall comparator are dominated by the preamplifier. The equivalent input noise of this preamplifier equals [16]:

$$\sigma_V \approx kT\sqrt{\frac{8}{q}}\cdot\frac{1}{\sqrt{C_{PP}\cdot(V_{DD}-V_{thlatch})}}\propto\frac{1}{\sqrt{Q_C}} \tag{8-1}$$

where $V_{thlatch}$ is the threshold voltage of the latch and Q_C represents the absolute value of average transferred charge on parasitic capacitor C_{PP} and C_{PN} before the latch takes over. The preamplifier energy dissipation of one comparison equals:

$$E_C = 2C_{PP}\cdot V_{DD}^2 \tag{8-2}$$

From (8-1) and (8-2), the trade-off between noise and energy consumption can be observed. For fixed V_{DD} and $V_{thlatch}$, the equivalent input noise of the preamplifier is proportional to $(C_{PP})^{-0.5}$, while the energy consumption is proportional to C_{PP}. If one wishes to reduce the noise voltage by a factor of 2, the consumed energy has to be quadrupled.

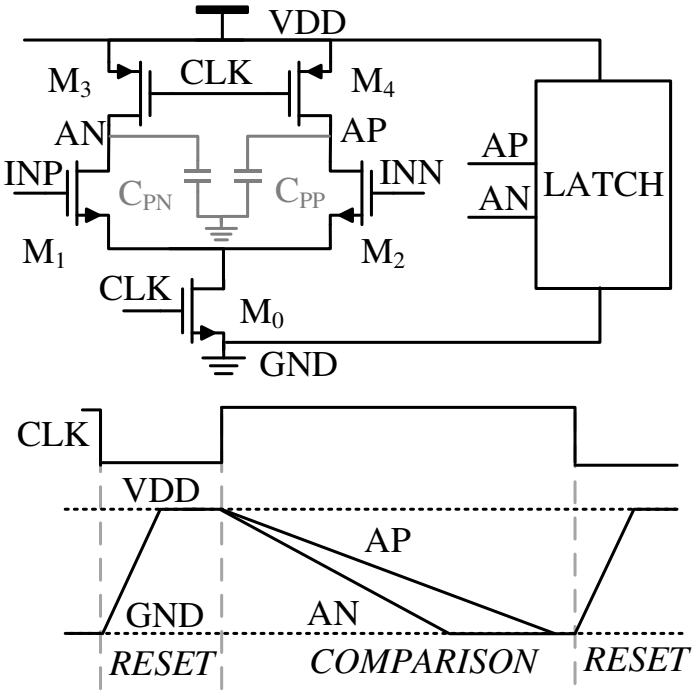


Figure 8.4: Prior-art dynamic comparator [16] and waveforms of key nodes.

When reflecting on the operation of the dynamic comparator (Figure 8.4), one can note that the discharging slope of C_{PP} and C_{PN} is used to perform dynamic amplification. On the other hand, the charging slope of C_{PP} and C_{PN} is not used for amplification, but only to reset the comparator. The bi-directional preamplifier takes advantage of both slopes to perform amplification and reduces the required charge consumption by charge reusing, thus improving the power-efficiency by a factor of two.

As shown in Figure 8.5 and Figure 8.6, a PMOS input stage, M_3/M_4, is inserted in parallel with NMOS pair M_1/M_2. Before the comparison starts, V_{AP} and V_{AN} are pushed to ground by M_6 and M_7. Then, the PMOS input pair M_3/M_4 is enabled first by switching on tail transistor M_5. C_{PP} and C_{PN} are charged and V_{AP} and V_{AN} increase according to the input signal. An OR gate is utilized to detect when V_{AP} or V_{AN} reaches half VDD. At that point, the PMOS pair M_3/M_4 is disabled by switching off M_5 while M_0 is switched on to enable NMOS pair M_1/M_2 together with the latch. From this moment onwards, this bi-directional comparator operates as the typical structure and achieves the same gain (see Figure 8.6). A further advantage of this comparator is that V_{AP} and V_{AN} return inherently to their initial condition (GND) at the end of the comparison, which avoids a reset cycle. An RST signal is still present to avoid floating V_{AP} and V_{AN} between cycles. For this bi-directional preamplifier, the sum of absolute value of average transferred charge on C_{PP} and C_{PN} during

charging and discharging is

$$Q_{CB} = C_{pp} \cdot \left(\frac{V_{DD}}{2} - 0 \right) + C_{pp} \cdot \left(\frac{V_{DD}}{2} - V_{thlatch} \right) = C_{pp} \cdot \left(V_{DD} - V_{thlatch} \right) = Q_C \tag{8-3}$$

which means that with the same C_{PP} and C_{PN}, the bi-directional preamplifier has the same noise performance as the typical structure. However, as C_{PP} and C_{PN} are only charged to half VDD rather than VDD, the energy consumption of the bi-directional preamplifier is

$$E_B = 2C_{PP} \cdot \frac{V_{DD}}{2} \cdot V_{DD} = C_{PP} \cdot V_{DD}^2 \tag{8-4}$$

which is only half of (8-3).

Note that the threshold of the OR gate does not have to be very precise as it only changes the noise performance and consumption slightly. For the whole dynamic comparator, the power consumption ratio of preamplifier and latch is about 3:1, which suggests this bi-directional comparator saves about 37.5% of the power of the typical comparator. In practice, the additional logic causes 4.5% overhead, which is mostly due to short-circuit current in the OR gate, thus saving 33% overall.

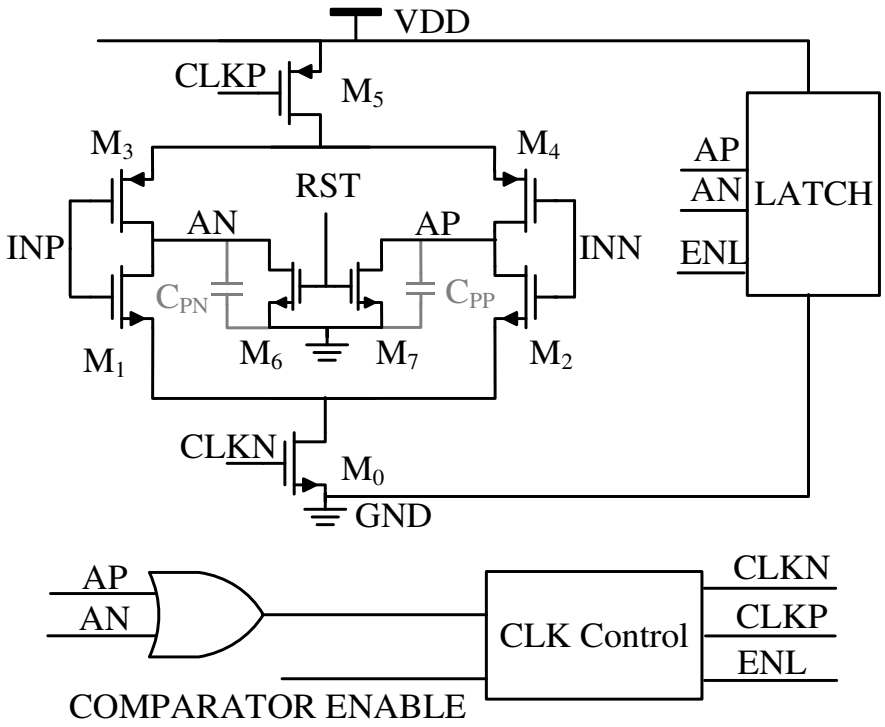


Figure 8.5: Bi-directional dynamic comparator.

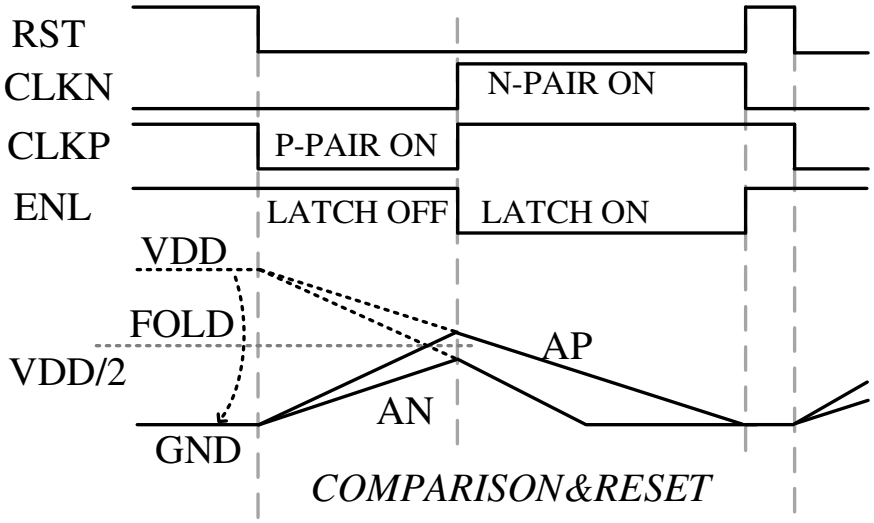


Figure 8.6: Key nodes waveforms of the bi-directional dynamic comparator.

8.1.5 Measurement results

The SAR ADC with duty-cycled reference generation was implemented in a 65nm CMOS technology and occupies 0.266mm^2, dominated by the large resistors used in the voltage reference and LDO (Figure 8.7). It further requires an external capacitor, as discussed previously.

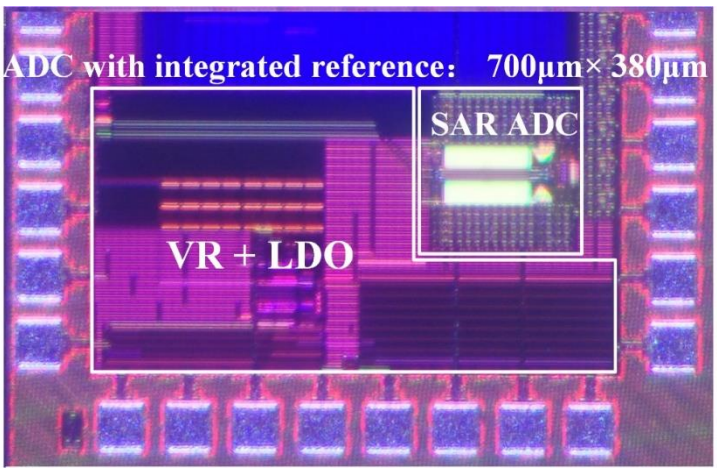


Figure 8.7: Die photo of the SAR ADC with integrated reference generation.

The power breakdown and ENOB of the reference-included ADC (operating at 80kS/s with

near-Nyquist input) with different duty-cycling rates of the VR are shown in Figure 8.8 and Figure 8.9. The VR is duty-cycled with a clock running at 20Hz. At 10% duty-cycle of the VR, the power consumption of the VR is 3.7nW from 0.8V supply, which is far less than that of the ADC core. Meanwhile, the ENOB remains 9.1bit regardless of the duty-cycling, resulting in a FoM of 2.4fJ/conversion-step. Note that since the LDO is always-on, the power consumption and the inevitable dropout loss due to the voltage drop between power supply and output of the LDO takes about 1/3 of the total power consumption.

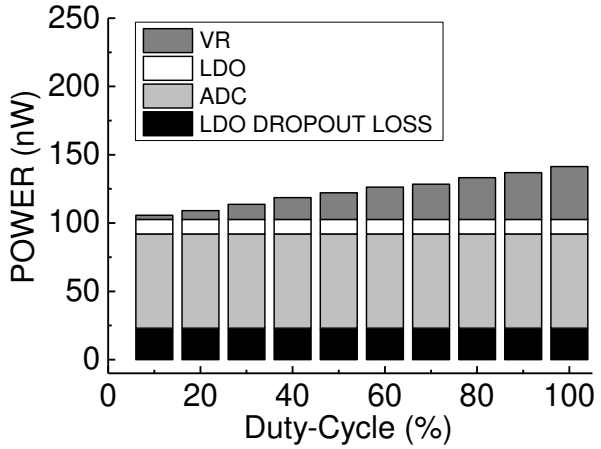


Figure 8.8: Measured power breakdown of the reference-included ADC at 80kS/s and near-Nyquist input versus different duty-cycling rates.

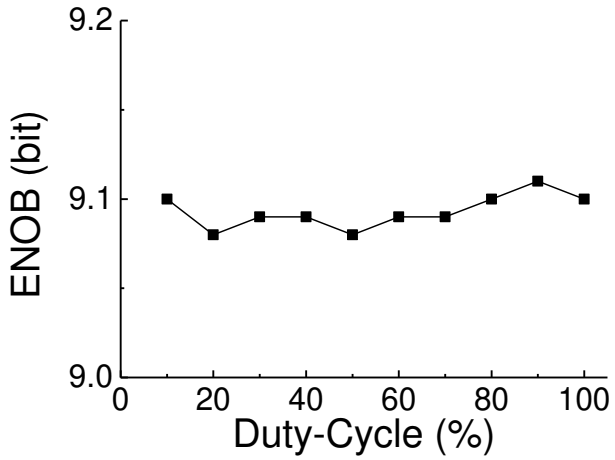


Figure 8.9: Measured near-Nyquist ENOB of the reference-included 10b ADC at 80kS/s versus different duty-cycling rates.

The PSRR of the whole system is also demonstrated by imposing an intentional interference on the external power supply. As a reference in the comparison, the ADC without VR or LDO or any external decoupling capacitors powered by an external power supply (0.6V) imposed with 1kHz 150mV$_{PP}$ interference is first measured. The input signal is modulated by the interference and two large spurs at $F_{sig}\pm F_{VDD}$ are observed (Figure 8.10). Along with other noise from the external power supply, the ADC achieves a poor SNDR (30.2dB) and SFDR (34.2dB).

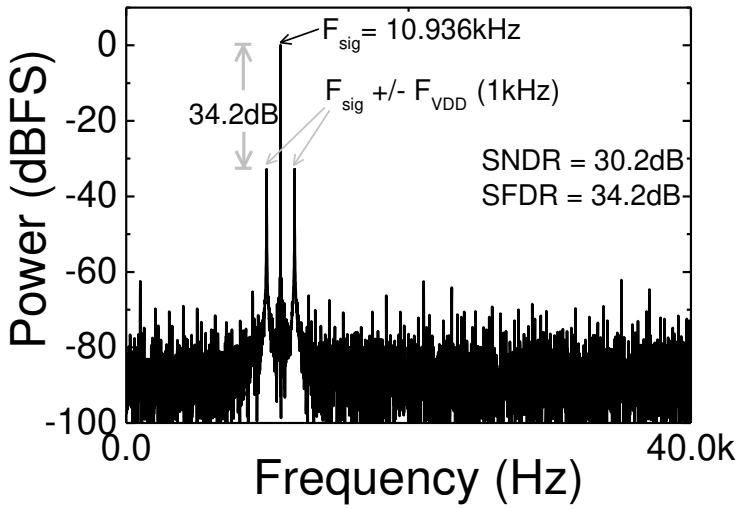


Figure 8.10: Measured spectrum of the ADC powered by external power supply (0.6V) imposed with 1kHz 150mV$_{PP}$ interference.

Subsequently, the ADC powered by a 10% duty-cycled VR and LDO with the same interference imposed on the external power supply (0.8V) is measured while all external decoupling capacitors are removed except for the LDO output capacitor. Figure 8.11 displays the spectrum, which reveals 64.4dB suppression on the intermodulation spurs at $F_{sig}\pm F_{VDD}$ and better noise suppression. The achieved SNDR and SFDR are the same as the case with an ideal clean supply powering the ADC directly.

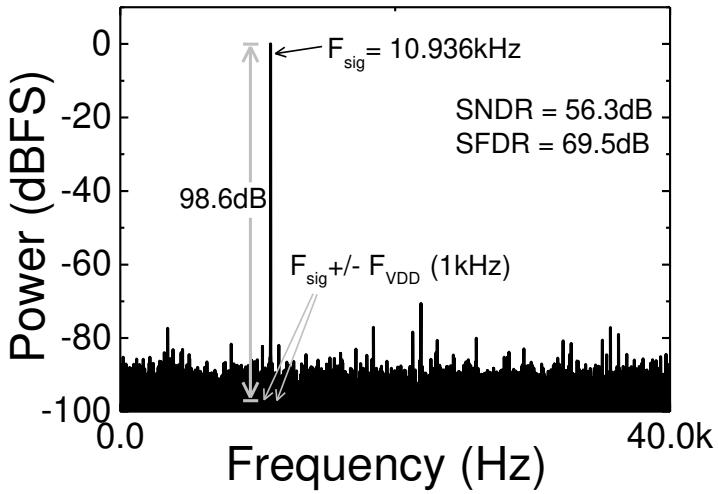


Figure 8.11: Measured spectrum of the ADC powered by a 10% duty-cycled VR and LDO with 1kHz 150mVPP interference imposed on the external power supply (0.8V).

With 10% duty-cycling, other performances of the SAR ADC are also measured. The maximum DNL is 0.94LSB and the maximum INL is 0.60LSB (Figure 8.12).

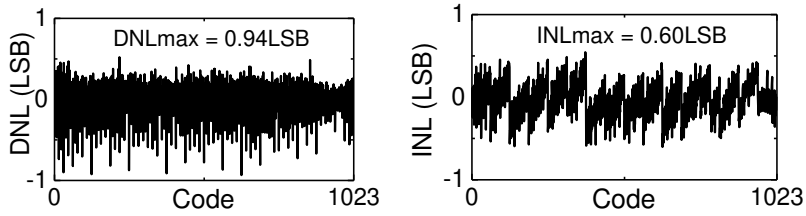


Figure 8.12: Measured DNL and INL of the ADC with 10% duty-cycled VR.

At near Nyquist input, the SNDR is 56.6dB and the SFDR is 65.0 dB (Figure 8.13).

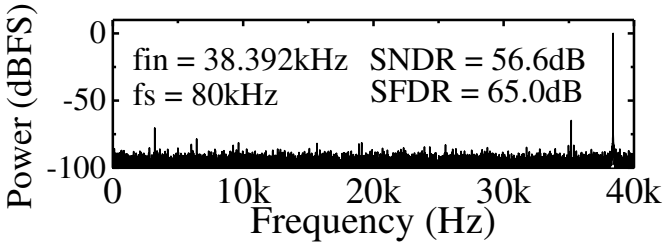


Figure 8.13: Measured spectrum of the ADC with 10% duty-cycled VR.

The SFDR and SNDR versus input frequency are shown in Figure 8.14. While the SFDR slowly degrades due to the T&H, the SNDR is maintained at a constant level.

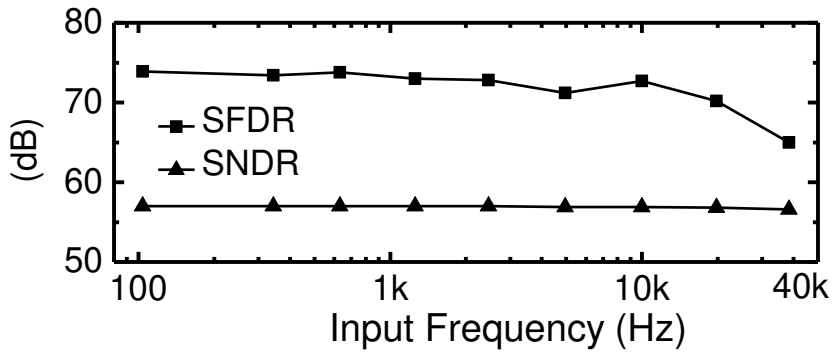


Figure 8.14: Measured SFDR and SNDR of the ADC with 10% duty-cycled VR versus input frequency.

The summary of the presented reference-included SAR ADC and the comparison with other works are shown in TABLE 8-1 Compared with other low-power SAR ADCs, this work is the only one to integrate a voltage reference and an LDO with an ADC. Meanwhile, it has a comparable ENOB and FoM.

TABLE 8-1: SAR ADC performance summary and comparison.

	[70]	[26]	[71]	[35]	This work
Technology (nm)	90	40	90	65	65
Area (mm²)	0.04	0.0065	0.042	0.076	0.26
Supply voltage (V)	0.4	0.45	0.4	0.6	0.8
Sample rate (S/s)	250k	200k	500k	40k	80k
Resolution (bit)	10	10	10	10	10
INL (LSB)	0.67	0.45	0.62	0.48	0.60
DNL (LSB)	0.43	0.44	0.34	0.32	0.94
ENOB (bit)	8.6	8.95	8.72	9.4	9.1
Including reference	No	No	No	No	Yes
Power (μW)	0.2	0.084	0.5	0.072	0.106
FoM (fJ/conv.step)	2.02	0.85	2.47	2.7	2.4

8.1.6 Conclusions

In this sub-chapter, a fully-integrated low-power 10b SAR ADC with duty-cycled reference generation is described. As discussed in Chapter 6.1, the low-power low-VDD voltage reference generates an accurate reference voltage over PVT corners. With a high-efficiency duty-cycling block (Chapter 6.2), which enables a 10% duty-cycling, the power consumption of the voltage reference is greatly reduced and becomes negligible compared to that of the SAR ADC. In the SAR ADC, a low-power bi-directional dynamic comparator is adopted, which makes use of both charging and discharging phases (which means reuse of charge) to perform pre-amplification, resulting in higher power-efficiency. Compared to a typical comparator [16], this bi-directional comparator reduces the power by 33% including the power of extra logic circuits while maintaining the same noise performance. With the above techniques, the reference-included SAR ADC achieves a FoM of 2.4fJ/conversion-step.

8.2 A DAC-compensated discrete-time driver for a CR DAC

This sub-chapter presents a charge-redistribution SAR ADC with an integrated low-power and area-efficient discrete-time reference driver [61]. An on-chip capacitor is pre-charged to the reference voltage during tracking phase and drives the DAC of the SAR ADC passively during conversion phase. The charge sharing between the driving capacitor and the DAC will cause reference voltage drop and code-dependent non-binary DAC switching steps. This is compensated by switching an auxiliary DAC array together with the regular binary DAC array according to each specific code. The compensation relaxes the required decoupling capacitor and introduces little overhead in power or chip area. The above driving scheme is applied to a 10b 20MS/s SAR ADC fabricated in 65nm CMOS where the first 3 DAC switching steps are compensated. With a near-Nyquist input tone, the SNDR and SFDR of the SAR ADC with the uncompensated reference driver are 54.4dB and 58.9dB. After enabling the compensation, the SNDR and SFDR are increased to 56.8dB and 72.4dB, achieving 2.4dB and 13.5dB improvement respectively. The SAR ADC consumes a total power of 133.1μW while the discrete-time reference driver with and without compensation add 17.2μW and 14.0μW respectively. The SAR ADC with integrated reference driver occupies a chip area of 0.081mm2 where 8.6% is occupied by the reference driver.

8.2.1 Concept of the DAC-compensated discrete-time driver

The CR DAC in a SAR ADC samples the input signal and performs a binary search. Taking the split monotonic DAC [25] as an example, where each DAC bit is split into 2 half pairs, the differential DAC output voltage shift of the *i*-th switching step can be expressed as:

$$\Delta V_{DAC}(i) = 2 \cdot \frac{C_i}{C_T} \cdot V_{REF} \tag{8-5}$$

where C_i is the switched binary-scaled capacitance at each side of the DAC, C_T is the total capacitance at each side of the DAC, and V_{REF} is the reference voltage. In order to achieve binary steps of $\Delta V_{DAC}(i)$, V_{REF} should be constant, which may cost a lot of effort as discussed in Chapter 3. One example of an ideal binary search in a split monotonic DAC is shown in TABLE 8-2.

TABLE 8-2: First 3 DAC switching steps with ideal reference driver.

V_{REF} [V]	C_i	ΔV_{DAC} [V]
1	8C	0.5
1	4C	0.25
1	2C	0.125

As discussed in Chapter 7, one category of reference drivers makes use of a pre-charged decoupling capacitor to drive the DAC. Considering a single SAR conversion with such a passive driver, in order to perform an accurate binary search, the decoupling capacitor (C_{DEC}) has to be large enough to minimize the reference drop. If C_{DEC} is not large enough, the voltage on C_{DEC} will change according to the specific code, causing signal-dependent non-linearity. The DAC output voltage shift can be expressed as:

$$\Delta V_{DAC}^{'}(i) = 2 \cdot \frac{C_i}{C_T} \cdot V_{REF}(D_i) \neq \frac{1}{2} \Delta V_{DAC}^{'}(i-1) \tag{8-6}$$

where D_i is the current code, varying from 0 to 2^i-1, and $V_{REF}(D_i)$ is the reference voltage after switching to code D_i. One example of above case is illustrated in TABLE 8-3. The first column denotes the reference voltage change when switching C_i, which is code-dependent. Only one case is shown in the table. Due to the charge sharing, the reference voltage is

dropping and causes code-dependent non-binary search steps, leading to ADC non-linearity.

TABLE 8-3: First 3 uncompensated DAC switching steps with passive driver.

V_{REF} [V]	C_i	ΔV_{DAC} [V]
1→ 0.95	8C	0.48
0.95→ 0.88	4C	0.22
0.88→ 0.85	2C	0.10

Looking back at (8-6), it can be noted that the non-binary search is caused by the non-constant $V_{REF}(D_i)$, which is inevitable with a small C_{DEC}. If an adjusted 'C_i' can be chosen according to $V_{REF}(D_i)$, the non-binary search can be corrected. As shown in TABLE 8-4, for the second and third switching steps, a specific auxiliary capacitor (C_{a2} and C_{a3}) can be switched in addition to the capacitors from the binary DAC array. Although the reference voltage still suffers from code-dependent drop, V_{DAC} can now be made binary scaled again. Since the charge consumption of each switching is code-dependent, the resulting reference voltage drop and the required auxiliary capacitors (C_{a2} and C_{a3}) also vary from code to code. TABLE 8-4 only illustrates the case for one code. Compared with TABLE 8-3, the reference voltage drop (first column) is slightly different due to the extra auxiliary capacitors being switched. Note that V_{REF} on C_{DEC} is always decreasing, thus the correction can never recover the original full-scale range, but it can achieve binary scaled output steps. This results in a slightly smaller ADC full-scale range, while it recovers the ADC linearity. Also note that the first voltage step effectively determines the scale, and thus only step 2 and further need to be compensated (by means of C_{a2} and C_{a3}).

TABLE 8-4: First 3 compensated DAC switching steps with passive driver.

V_{REF} [V]	C_i	ΔV_{DAC} [V]
1→ 0.95	8C	0.48
0.95→ 0.87	$4C+C_{a2}$	0.24
0.87→ 0.83	$2C+C_{a3}$	0.12

8.2.2 Calculation of the auxiliary capacitance

While the auxiliary DAC could be implemented in various ways, it is assumed here that it

is also a differential DAC array for the sake of simplicity and good matching to the main DAC.

In order to achieve correct compensation, the capacitance of the auxiliary DAC has to be determined carefully. The calculation of the compensation capacitance is derived subsequently. For the i-th switching step, the output voltage shift at each side of the DAC can be expressed as follows:

$$\begin{aligned}\Delta V_{DAC+,i} &= \frac{C_{S,i}}{C_T}\cdot(V_{REF,i}-0)+\frac{C_{R+,i}}{C_T}\cdot(V_{REF,i}-V_{REF,i-1}) \\ &= \alpha_{S,i}\cdot V_{REF,i-1}+(\alpha_{R+,i}+\alpha_{S,i})\cdot\Delta V_{REF,i}\end{aligned} \tag{8-7}$$

$$\begin{aligned}\Delta V_{DAC-,i} &= \frac{C_{s,i}}{C_T}\cdot(0-V_{REF,i-1})+\frac{C_{R-,i}}{C_T}\cdot(V_{REF,i}-V_{REF,i-1}) \\ &= -\alpha_{S,i}\cdot V_{REF,i-1}+\alpha_{R-,i}\cdot\Delta V_{REF,i}\end{aligned} \tag{8-8}$$

where two variables are defined:

$$\Delta V_{REF,i} = V_{REF,i}-V_{REF,i-1} \tag{8-9}$$

$$\alpha_x = C_x / C_T \tag{8-10}$$

In above equations, $\Delta V_{DAC+,i}$ and $\Delta V_{DAC-,i}$ are the positive and negative voltage shifts of the two DAC outputs respectively; $C_{S,i}$ is the total switched capacitance and differential switching is maintained as well for the compensation; $V_{REF,i}$ is the reference voltage on C_{DEC} after the i-th switching step ($V_{REF,0}$ denotes the original reference voltage); $\Delta V_{REF,i}$ is the reference voltage drop due to the charge sharing by the i-th switching; $C_{R+,i}$ and $C_{R-,i}$ are the total capacitance connected to the reference voltage both before and after the i-th switching step at each side; and α_x denotes the ratio between C_x and C_T. Since the DAC adopts the split monotonic scheme, the total capacitance connected to V_{REF} in the DAC remains constant as C_T, which can be expressed as:

$$C_{S,i}+C_{R+,i}+C_{R-,i} = C_T \tag{8-11}$$

$$\alpha_{S,i}+\alpha_{R+,i}+\alpha_{R-,i} = 1 \tag{8-12}$$

In (8-7) and(8-8), one parameter, $\Delta V_{REF,i}$ is still unknown. It can be found using to the law of charge conservation. The charge absorbed by each side of the DAC can be expressed as:

$$Q_{+,i} = C_{S,i}\cdot(V_{REF,i}-\Delta V_{DAC+,i})+C_{R+,i}\cdot(\Delta V_{REF,i}-\Delta V_{DAC+,i})$$

$$= C_{S,i} \cdot V_{REF,i-1} + \left(C_{S,i} + C_{R+,i}\right) \cdot (\Delta V_{REF,i} - \Delta V_{DAC+,i}) \tag{8-13}$$

$$Q_{-,i} = C_{R-,i} \cdot (\Delta V_{REF,i} - \Delta V_{DAC-,i}) \tag{8-14}$$

The total charge absorbed by the DAC equals the charge loss of C_{DEC}. Assuming C_{DEC} equals γ times C_T, we achieve:

$$Q_{+,i} + Q_{-,i} + \gamma C_T \cdot \Delta V_{REF,i} = 0 \tag{8-15}$$

Subsequently, $\Delta V_{REF,i}$ can be expressed as follows by solving (8-15):

$$\Delta V_{REF,i} = -\frac{2\alpha_{S,i}\alpha_{R-,i}}{\gamma + 2\alpha_{R-,i} - 2\alpha_{R-,i}^2} \cdot V_{REF,i-1} \tag{8-16}$$

(8-16) indicates three conditions where the reference voltage drop equals 0. As expected, when an infinitely large C_{DEC} is used (γ is infinite), the consumed charge can be provided by C_{DEC} without voltage drop. If $\alpha_{S,i}$ or $\alpha_{R-,i}$ is 0, the resulted reference voltage drop is also 0. The former corresponds to no switched capacitance and the latter indicates a special condition where no charge is consumed from the reference voltage when all the capacitance connected to GND is switched to V_{REF} ($\alpha_{S,i} + \alpha_{R+,i} = 1$) at one side of the DAC. However, above 3 conditions are not feasible in a practical design and thus reference voltage drop is inevitable.

The resulting differential DAC voltage shift can be expressed as:

$$\Delta V_{DAC,i} = \Delta V_{DAC+,i} - \Delta V_{DAC-,i} = 2\alpha_{S,i} V_{REF,i-1} \frac{\gamma + \alpha_{R-,i}}{\gamma + 2\alpha_{R-,i} - 2\alpha_{R-,i}^2} \tag{8-17}$$

In (8-17), $2\alpha_{S,i}V_{REF,i-1}$ is the desired DAC voltage shift and the coefficient with the ratio between two polynomials indicates the impact of the reference voltage drop due to charge sharing. Similar as in (8-17), an infinite γ results in a coefficient equal to 1 and the desirable DAC voltage shift. In general, $\alpha_{S,i}$ is binary-scaled and $V_{REF,i-1}$ and $\alpha_{R-,i}$ are code-dependent, causing code-dependent DAC voltage shifts. The normalized DAC voltage shift driven by a $20C_T$ C_{DEC} without compensation is shown in TABLE 8-5. As expected, the DAC voltage steps are non-binary and symmetric.

TABLE 8-5: Normalized DAC voltage steps driven by a $20C_T$ C_{DEC} passively without compensation.

No compensation			
Code	Switching steps		
	1st	2nd	3rd
000X	512.0	254.8	127.5
001X	512.0	254.8	131.0
010X	512.0	258.0	126.3
011X	512.0	258.0	127.5
100X	512.0	258.0	127.5
101X	512.0	258.0	126.3
110X	512.0	254.8	131.0
111X	512.0	254.8	127.5

One freedom that can be tuned in (8-17) is $\alpha_{S,i}$ ($\alpha_{R-,i}$ is determined by $\alpha_{S,i}$ according to (8-12) since $\alpha_{R+,i}$ is known before each switching). Although the reference drop cannot be avoided, $\Delta V_{DAC,i}$ can still be binary scaled by choosing an appropriate $\alpha_{S,i}$. Moreover, for a symmetric DAC, $\alpha_{S,1}$, $\alpha_{R+,1}$, and $\alpha_{R-,1}$ are the same regardless of the MSB decision, leading to a code-independent $\Delta V_{DAC,1}$ that can be used as the reference for $\Delta V_{DAC,i}$ tuning during the following switching steps.

For the first DAC switching where no compensation is applied ($\alpha_{S,1} = 0.25$, $\alpha_{R-,1} = 0.25$, and assuming $V_{REF,0} = 1$), when a C_{DEC} equal to $20C_T$ is adopted, $\Delta V_{REF,1}$ equals to -1/163 and $\Delta V_{DAC,1}$ equals to 81/163 according to (8-16) and (8-17). For simplicity, the calculation of the second switching step below is under the assumption that the first comparison result is 0 (the case of 1 is totally symmetric). If the second comparison result is also 0, by forcing $\Delta V_{DAC,2} = 0.5\Delta V_{DAC,1}$ according to (8-17), $\alpha_{S,2}$ can be solved (note that in this case $\alpha_{R+,2}$ is 0.75 so that $\alpha_{R-,2}$ equals to $0.25-\alpha_{S,2}$). Two roots are achieved from above calculation: $\alpha_{S,2}$= 0.1256 and $\alpha_{S,2}$= 27.0411. The precondition indicates that $\alpha_{S,2}$ must be smaller than 1, hence the second root is not valid and left out. The first root is a valid solution: in addition to the nominal switched binary DAC ($0.125C_T$), a compensation capacitance $C_{A,i}$ ($=\alpha_{A,i}C_T$) equal to $0.0006C_T$ leads to a binary differential DAC output voltage shift.

Similarly, if the second comparison result is 1, above calculation can be repeated and it should be noted that $\alpha_{R+,2}$ is 0.25. Two roots are solved: $\alpha_{S,2}$= 0.1240 and $\alpha_{S,2}$= 27.3740 (left

out). In this case, the calculated $\alpha_{S,2}$ is smaller than the nominal binary DAC (0.125). In order to achieve decent matching, it is favorable to keep the binary DAC and switch an additional auxiliary DAC, which thus needs to make a -0.001 compensation. As a result, the solution 0.1240 in this case cannot be used either. However, the previous derivation assumed that the auxiliary DAC is switched in the same way as the binary DAC at each side, while a solution smaller than the nominal switched binary DAC indicates that the auxiliary capacitance $C_{A,i}$ should be switched oppositely with $C_{S,i}$ in order to keep $C_{S,i}$ as ($C_T/2^{i+1}$). Modifying above equations and repeating the derivation, $\Delta V_{REF,i}$ and $\Delta V_{DAC,i}$ can be expressed:

$$\Delta V_{REF,i} = -\frac{2(\alpha_{S,i} - \alpha_{A,i})(\alpha_{R-,i} + \alpha_{A,i}) + 2\alpha_{A,i}}{\gamma + 2(\alpha_{R-,i} + \alpha_{A,i}) - 2(\alpha_{R-,i} + \alpha_{A,i})^2} \cdot V_{REF,i-1} \tag{8-18}$$

$$\Delta V_{DAC,i} = 2(\alpha_{S,i} - \alpha_{A,i}) V_{REF,i-1} \frac{\gamma + \alpha_{R-,i} + \alpha_{A,i} + \beta}{\gamma + 2(\alpha_{R-,i} + \alpha_{A,i}) - 2(\alpha_{R-,i} + \alpha_{A,i})^2} \tag{8-19}$$

where β is expressed as:

$$\beta = \frac{2(\alpha_{R-,i} + \alpha_{A,i}) - 1}{\alpha_{S,i} - \alpha_{A,i}} \cdot \alpha_{A,i} \tag{8-20}$$

(8-18) and (8-19) are similar to (8-16) and (8-17) and by replacing $\alpha_{A,i}$ with 0, (8-18) and (8-19) will be simplified to (8-16) and (8-17). Note that in the current case, with compensation DAC, $\alpha_{S,i}$ is fixed and (8-12) should be rewritten:

$$\alpha_{S,i} = 1/2^{(i+1)} \tag{8-21}$$

$$\alpha_{S,i} + \alpha_{A,i} + \alpha_{R+,i} + \alpha_{R-,i} = 1 \tag{8-22}$$

Using (8-19), the case of a second comparison result equal to 1 can be re-calculated and the solved valid solution is $\alpha_{A,2}$=0.00097, which should be switched oppositely with the binary DAC ($C_{S,2}$). For the following switching steps, above calculation can be repeated: first using (8-17) to solve $\alpha_{S,i}$. If $\alpha_{S,i}$ is larger than $1/2^{(i+1)}$, the compensation for this case is to switch an auxiliary capacitor equal to $(\alpha_{S,i}-1/2^{(i+1)})C_T$ in the same way as the binary capacitor $(1/2^{(i+1)})C_T$. If $\alpha_{S,i}$ is smaller than $1/2^{(i+1)}$, (8-19) should be used for the calculation and the compensation is to switch an auxiliary capacitor equal to $\alpha_{A,i}$ oppositely with the binary capacitor.

During the previous calculation, only the differential DAC output voltage shift is considered while the common mode shift of the DAC output voltage should be negligible to avoid causing signal dependent comparator offset. Taking the sum of (8-7) and (8-8), the DAC common mode shift is:

$$\Delta V_{DACCM,i} = (\Delta V_{DAC+,i} + \Delta V_{DAC-,i}) / 2 = \Delta V_{REF,i} / 2 \tag{8-23}$$

From the previous calculation, with a C_{DEC} equal to $20C_T$, $\Delta V_{REF,1}$ is 1/163 and results in a $\Delta V_{DACCM,1}$ of merely 0.6% of the initial reference voltage. As a result, the impact on the comparator offset caused by the compensation scheme is negligible.

While the above calculations show the ideal case, in practice the parasitic capacitances must be taken into consideration as well, since they also change the energy consumption of the DAC. Two types of parasitic capacitance are most critical (Figure 8.15): the parasitic capacitance at the DAC output nodes (C_{PT}) and those at the other plates of the binary DAC array (C_{PB}). C_{PT} should be included in C_T and C_{PB} increases the charge consumption of the DAC when switched from ground to V_{REF}. Consequently, the final values of the capacitors in the auxiliary DAC should be determined after layout extraction. Also note that the capacitance of the auxiliary DAC contributes to $C_{R+,i}$, $C_{R-,i,}$, and C_T. Since its exact value is not known before the calculation, the calculation gives a first estimate, and iteration is advised taking into account the auxiliary DAC capacitance as well as the layout extracted parasitics.

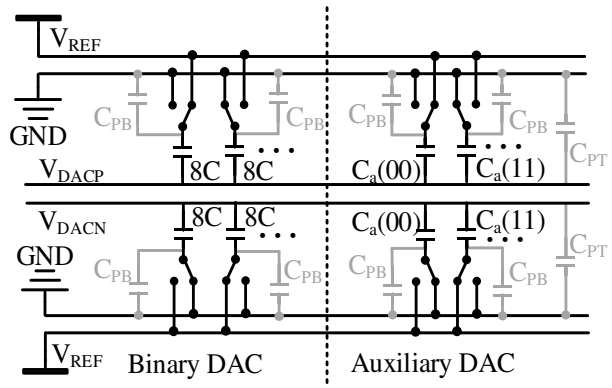


Figure 8.15: Two types of critical parasitic capacitances for the compensation.

TABLE 8-6 shows the numerical values of the auxiliary capacitors based on above calculations for the compensation of the first 3 switching steps in a split monotonic DAC

with a decoupling capacitance of $20 \cdot C_T$, where parasitic capacitance is also taken into account after layout extraction. The capacitors for the binary DAC and the auxiliary DAC are shown. The 1st switching step requires no compensation as explained earlier. Note that a negative sign in the table means that the switching of this auxiliary capacitance is opposite with the related binary capacitor. TABLE 8-6 shows that the total capacitance of the auxiliary DAC is only 1.4% of the binary DAC for the compensation of the first 3 switching steps, which introduces little power and chip area overhead. In order to compensate n switching steps, a total of (2^n-2) different possibilities are needed.

TABLE 8-6: First 3 compensated DAC switching steps and the auxiliary capacitance.

3b compensation						
Code	Switching steps/auxiliary capacitance					
	1st	Auxiliary cap	2nd	Auxiliary cap	3rd	Auxiliary cap
000X	512.0	0	256.0	$0.0018C_T$	128.0	$0.00135C_T$
001X	512.0	0	256.0	$0.0018C_T$	128.0	$-0.0014C_T$
010X	512.0	0	256.0	$-0.0011C_T$	128.0	$0.0012C_T$
011X	512.0	0	256.0	$-0.0011C_T$	128.0	$0.00025C_T$
100X	512.0	0	256.0	$-0.0011C_T$	128.0	$0.00025C_T$
101X	512.0	0	256.0	$-0.0011C_T$	128.0	$0.0012C_T$
110X	512.0	0	256.0	$0.0018C_T$	128.0	$-0.0014C_T$
111X	512.0	0	256.0	$0.0018C_T$	128.0	$0.00135C_T$

From TABLE 8-5 and TABLE 8-6, the presented compensation scheme can be sketched: the non-binary steps in TABLE 8-5 are made binary by making the switched capacitance non-binary as in TABLE 8-6. Different from [70, 71, 72], the V_{REF} drop is still signal-dependent after compensation while the DAC output steps are binary now by tuning the switched capacitance. In this way, no calibration or digital post-correction is needed to generate the final output code.

Above discussion is under the assumption that the voltage on the decoupling capacitance is recovered to V_{REF} at the start of each conversion, and that C_{DEC} is not recharged by the driver during conversion. This enables the use of a discrete-time driver which is only active during the tracking phase. As shown in Figure 8.16 (a), during the conversion phase, $V_{REF,DEC}$ drops gradually due to charge sharing with the DAC. During the tracking phase, C_{DEC} is pre-charged via the PMOS pass gate while a comparator is detecting when $V_{REF,DEC}$ has reached

V_{REF} (Figure 8.16 (b)). At that moment, the pass gate is switched off and C_{DEC} is disconnected from the power supply. For a symmetric DAC like a split monotonic DAC, the tracking phase consumes no energy from the reference so that the voltage of C_{DEC} will remain at V_{REF} until the next conversion starts. The discrete-time driver significantly saves power compared to an always-on driver.

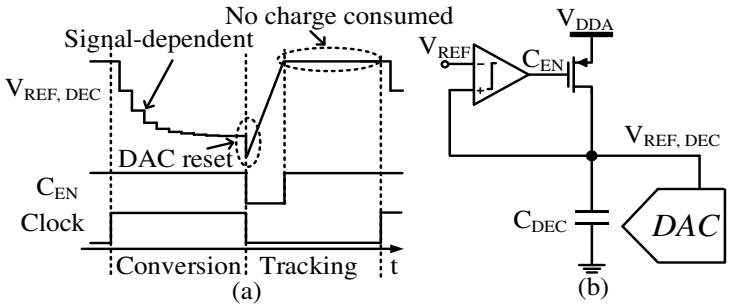


Figure 8.16: (a) $V_{REF, DEC}$ during conversion; (b) pre-charger with cross-detector.

Taking the noise, offset and delay of the comparator into account, the final pre-charged voltage on C_{DEC} can be expressed as:

$$V_{DEC,pre} = V_{REF} + V_{OS} + V_{noise} + I_{ch} \cdot \tau / C_{DEC} \tag{8-24}$$

where V_{OS} is the offset of the comparator, V_{noise} is the input-referred noise in voltage, I_{ch} is the pre-charging current, and τ is the delay of the comparator. V_{OS}, I_{ch}, and τ, as long as they are constant, only introduce a gain error for the SAR ADC. As for V_{noise}, it will contribute to ADC output noise and should preferably be set well below 1LSB.

8.2.3 Behavioral simulations

The presented method was verified with Matlab simulations where a 10b SAR ADC with a split monotonic DAC is driven by different C_{DEC}'s and a different number of compensated steps. It is assumed that the reference voltage on C_{DEC} is recovered at the start of each conversion. It can be found from Figure 8.17 that it requires a C_{DEC} equal to $2^9 \cdot C_T$ to achieve an ideal SNDR of 62dB and an SFDR above 80dB if the reference voltage drop is not compensated. For smaller C_{DEC}, the SNDR and SFDR will drop, but this can be mitigated by compensating more and more switching steps, at the cost of more complexity in the auxiliary DAC. In practice, a tradeoff must be made between the performance improvement and the complexity of the hardware.

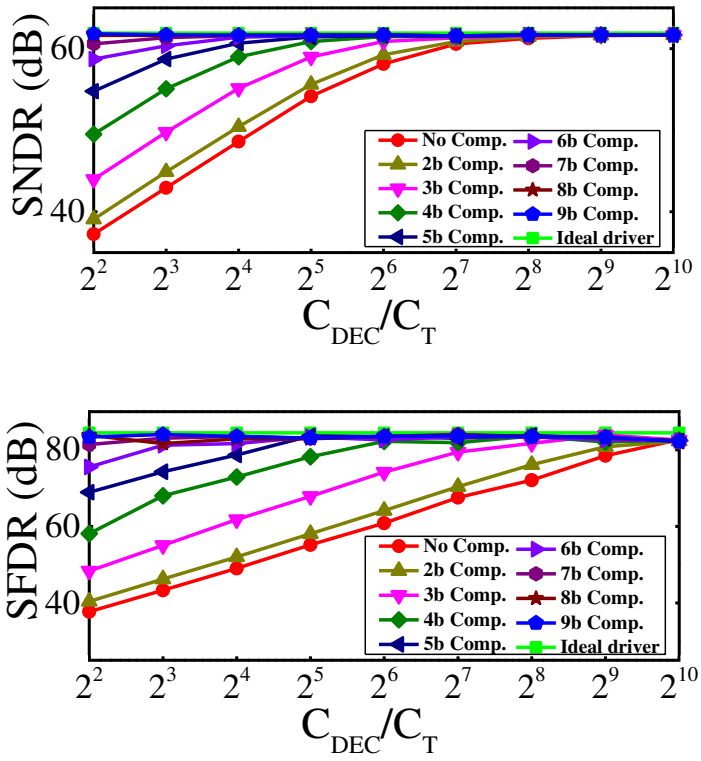


Figure 8.17: Behavioral simulation of SNDR/SFDR of a 10b SAR ADC driven by the discrete-time reference driver with a different number of compensated switching steps at different ratio of C_{DEC}/C_T.

The first switching steps consume the most charge and cause the largest V_{REF} drop, hence being the most urgent to be compensated. Moreover, the amount of compensation hardware increases exponentially with the amount of compensated switching steps as discussed in Chapter 8.2.2. As shown in Figure 8.18, compensating more than 4 switching steps can barely gain any improvement while the hardware complexity keeps growing. As shown in Figure 8.17, to achieve the same SNDR, 3b compensation can save about 3x in C_{DEC} when compared to the uncompensated case.

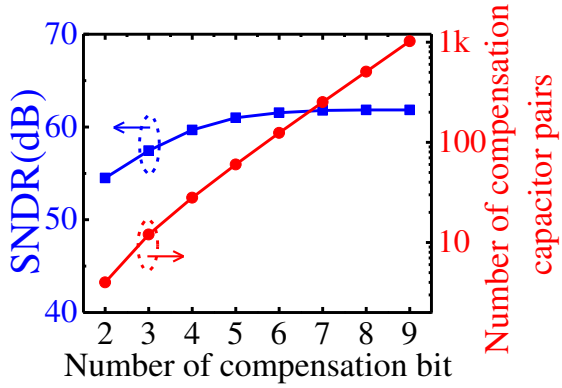


Figure 8.18: SNDR and hardware complexity versus number of compensated steps.

The impact of the compensation scheme on SAR ADC linearity is further investigated via INL/DNL plots as shown in Figure 8.19, where the INL/DNL without and with 3b/4b/5b compensation are depicted. Without compensation, an INL error pattern is observed that gives rise to 3rd order harmonic distortion. The pattern is caused by signal-dependent reference voltage drop which modulates with the signal and thus creates distortion. With compensation, the INL curve is segmented into 2^{NoC} (NoC is the number of compensation bits) groups and shifted towards 0. The INL and DNL are globally reduced (especially around 1/4 and 3/4 full-scale input range, where originally the largest errors occurred), but locally (at the segment transitions) new errors can occur. However, when compensating more bits, the INL and DNL are gradually improving (Figure 8.19).

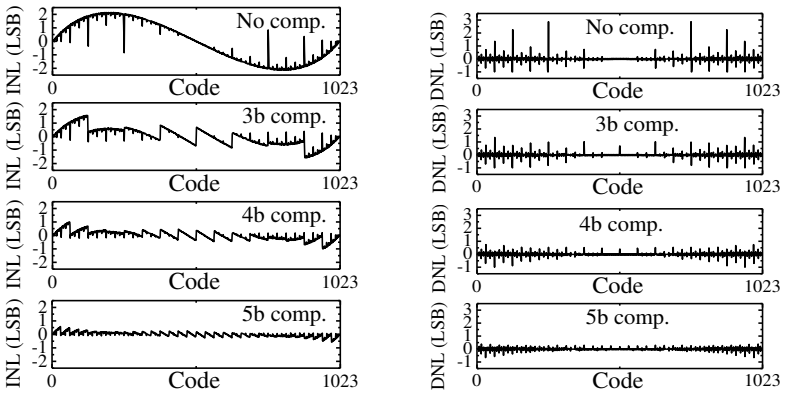


Figure 8.19: Behavioral simulations of INL and DNL with a different number of compensation steps.

The above discussion is also seen in the dependency of SNDR/SFDR on input amplitude (Figure 8.20). With a small input, the SNDR/SFDR with compensation are worse than those

without compensation due to the worse INL at the middle of the input range. When the input amplitude is large, the SNDR/SFDR with compensation improves the performance.

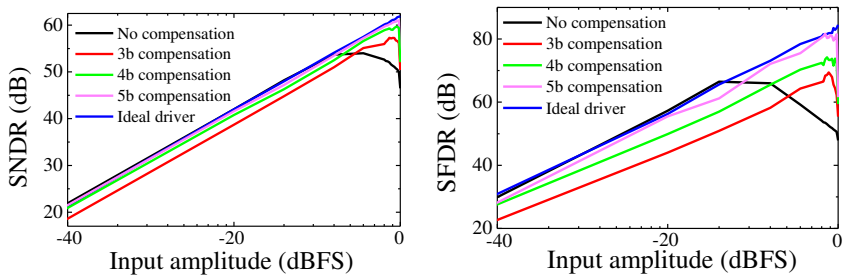


Figure 8.20: Behavioral simulations of SNDR/SFDR versus input amplitude.

The calculation in Chapter 8.2.2 indicates that with a C_{DEC} equal to $20C_T$, the first switching step generates a constant $\Delta V_{DAC,1}$ (=81/163) that corresponds to a 0.6% full-scale range reduction, while, as shown in Figure 8.20, the maximum SNDR/SFDR are achieved with an input amplitude of -1dBFS for the 3b compensation case, which is caused by the large INL error at small and large input (Figure 8.19). With more compensation bits, the range is approaching full scale (Figure 8.20).

Due to the charge sharing, the reference voltage keeps dropping. For a C_{DEC} equal to $20C_T$ driving a 10b SAR ADC, the simulated reference voltage drop ranges from 1.2% to 2.0% during each conversion.

As shown previously in TABLE 8-6, the required auxiliary capacitors are very small and their capacitances are non-integer multiples of the unit capacitor so that the impact of matching is worth mentioning. Figure 8.21 shows the SNDR/SFDR of the SAR ADC driven by an ideal driver as well as the presented discrete-time driver with 3b compensation and without compensation. Different capacitor standard deviations (normalized to the unit capacitance) are used to model mismatch and the average and the standard deviation of SNDR/SFDR among a total of 200 runs are monitored. When a small mismatch is only applied to the binary DAC, the performance is limited by the V_{REF} drop and the compensation can still achieve considerable improvement. When the mismatch is large, the improvement is reduced since now the performance is limited by the mismatch. If the mismatch is only applied to the compensation DAC, the performance gain is relatively constant until an extremely large mismatch is applied (30%). Even though the relative mismatch of the compensation DAC is large, the absolute mismatch of the compensation DAC is still very small, so that it has little impact on the performance of the SAR ADC. Thus, the compensation scheme is relatively robust against mismatch.

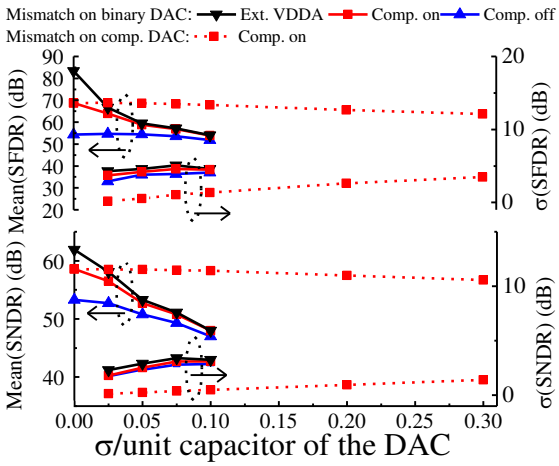


Figure 8.21: Impact of mismatch on SFDR/SNDR (mean and sigma) for different driving schemes.

Another problem is mismatch between C_{DEC} and C_T, as the compensation capacitance is calculated based on a certain ratio between those two. Figure 8.22 shows the impact of C_{DEC} and C_T mismatch where the compensation capacitance is calculated for a C_{DEC} equal to $20C_T$ and C_{DEC} has a variation from -90% to 100%. As can be seen, the compensation is not very sensitive to the actual value of C_{DEC} and gives an almost constant improvement when C_{DEC} varies from -20% to 50%. When C_{DEC} is larger than 1.5x the nominal value, the compensation starts to worsen the performance since now the compensation DAC is too far away from the desired value. When C_{DEC} is less than 0.8x the nominal value, apart from the deviation of the compensation, the smaller C_{DEC} accelerates the performance degradation.

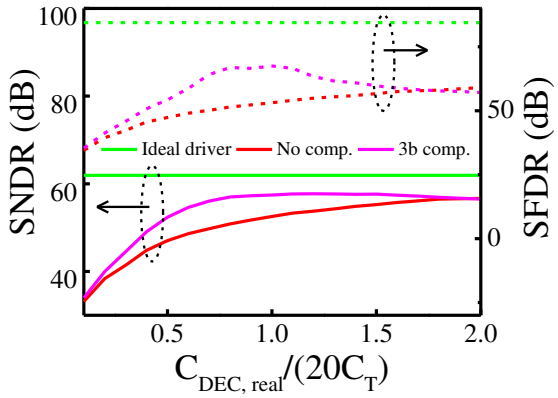


Figure 8.22: SNDR/SFDR versus the actual $C_{DEC,\,real}$ (normalized to $20C_T$).

8.2.4 Circuit implementation

In order to demonstrate the presented DAC-compensated driving scheme, it is adopted to drive a 10b SAR ADC, which is shown in Figure 8.23, where the first 3 DAC switching steps are compensated. The main DAC is segmented into 3b unary split-monotonic MSBs and 6b binary monotonic LSBs. In order to avoid missing codes caused by an unsettled DAC as in [72], 8LSB redundancy is inserted in the main DAC similar to [37] (so that the weights of the DAC array are 512, …, 32, 16, 8, 8, 4, 2,1) and digital reconstruction logic is included to obtain regular 10b binary output codes. Since 8 LSB is very small (8% of full-scale), the redundancy will cause little reference voltage drop or signal range loss. The unit capacitance is about 2fF, leading to a C_T of 1pF. The main DAC is implemented with lateral metal-metal capacitors as in [37]. The auxiliary DAC is connected in parallel with the main DAC and controlled by the MSB-code D_{OUT}<10:8>, with a total capacitance of 14.2fF (1.4% of C_T). A C_{DEC} equal to about 20·C_T is adopted to drive the DAC passively. The pre-charger operates at 1.0V VDD and charges the C_{DEC} to a V_{REF} of 0.8V. The rest of the SAR ADC (S&H, comparator, and logic) also operates at 0.8V VDD.

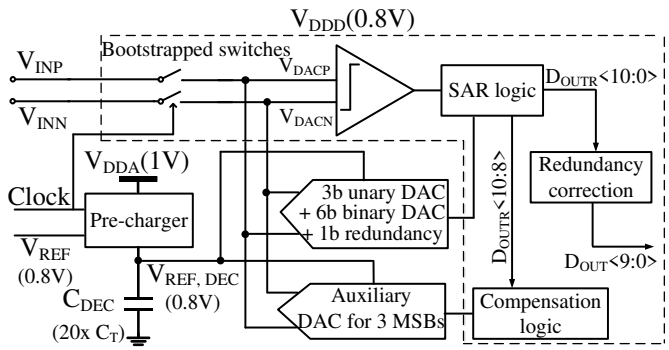
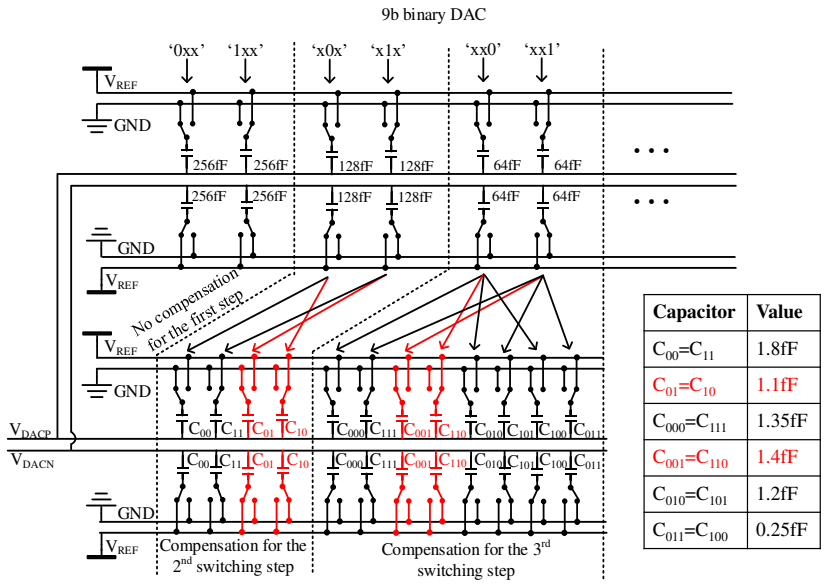


Figure 8.23: 10b SAR ADC with 3 compensated DAC switching steps.

As discussed in Chapter 8.2.3, as a tradeoff between performance and circuit complexity, the first 3 switching steps are compensated in this work. The auxiliary DAC as well as the 9b binary DAC (only 3b is shown) is illustrated in Figure 8.24 for the reset phase. After each comparison, one corresponding pair of capacitors in the binary DAC will be switched according to the comparison result as shown in the top part of Figure 8.24. For instance, when the comparison result is '0', one capacitor is switched from GND to V_{REF} at P side and the other way around at N side. As discussed in Chapter 8.2.3, the first switching step is signal-independent due to the symmetry of the DAC, hence no compensation is needed and the induced DAC voltage step is used as a reference for the compensation of further steps. There are 4 capacitor pairs for the compensation of the 2nd switching step, corresponding to

the 4 possible codes after the first 2 bit decisions. Similarly, there are 8 capacitor pairs for the compensation of the 3rd switching step as there are 8 possible codes by then. Due to symmetry, each code and its complement require the same compensation capacitance but switch oppositely. For instance, C_{10} and C_{01} are the compensation capacitors for code '10' and '01'; they have the same value but are switched oppositely. The red capacitors in Figure 8.24 correspond to the cases when no valid positive solution can be solved from (8-17) and the auxiliary capacitor should be switched oppositely to the corresponding capacitor in the binary DAC. For instance, when the first two comparisons equal to "11", C_{11} should be switched in the same way (from V_{REF} to GND at P side) as the 2nd switching step of the binary DAC. When the first two comparisons equal to "01", C_{01} should be switched oppositely to the 2nd switching step of the binary DAC. Consequently, the auxiliary DAC should be reset to the proper states accordingly as shown in Figure 8.24. The values of these capacitors are calculated after layout extraction since the parasitic capacitance will change the charge consumption and the compensation capacitance. The capacitor values are also shown in the right-hand side table and are the same as previously described in TABLE 8-6. The total compensation capacitance at each side of the DAC is about 14.2fF, only 1.4% of the total capacitance of the DAC array. In order to get a good matching with the main DAC, the auxiliary DAC is implemented using the same type of capacitors as the main DAC and they are placed close to each other in the layout.



Capacitor	Value
$C_{00}=C_{11}$	1.8fF
$C_{01}=C_{10}$	1.1fF
$C_{000}=C_{111}$	1.35fF
$C_{001}=C_{110}$	1.4fF
$C_{010}=C_{101}$	1.2fF
$C_{011}=C_{100}$	0.25fF

Figure 8.24: Reset phase of the binary DAC and the auxiliary DAC.

In order to reduce the chip area of C_{DEC}, it is implemented with MOS capacitors. This implies it will not match accurately with the DAC due to different types of capacitance. However, the compensation is not sensitive to the ratio between C_{DEC} and C_T as discussed earlier (Figure 8.22).

The schematic of the pre-charger is shown in Figure 8.25. Different from the conceptual diagram in Figure 8.16, in order to improve the PSRR, C_{DEC} is charged by a current source instead of a pass transistor. The current source is realized with a beta-multiplier with cascade current mirrors, which also generates the bias for the OPAMP in the crossing detector. The crossing detector is comprised of an OPAMP and several logic gates. The output of the detector controls M_7 to enable and disable the charging of C_{DEC}. Since the pre-charging only happens during tracking phase, the sampling clock is used to force M_7 to switch off during conversion. The noise of the comparator is mainly determined by the first stage ($M_{0\sim4}$), whose input-referred noise is simulated to be 0.2mV (0.13LSB). At different VDD and temperature, V_{OS}, I_{ch}, and τ in (8-24) will deviate and lead to different $V_{REF,pre}$. At 1V VDD and room temperature, $V_{REF,pre}$ is 806mV, which causes a gain error as long as this is constant for all samples. When VDD is changing from 1V to 1.5V, $V_{REF,pre}$ changes from 806mV to 813.2mV and the VDD dependency of $V_{REF,pre}$ is 14.4mV/V. From -40 to 85ºC, $V_{REF,pre}$ changes from 804.8mV to 807.8mV and the temperature dependency is 0.024mV/ºC. At different process corners, $V_{REF,pre}$ ranges from 805.6mV to 809.0mV.

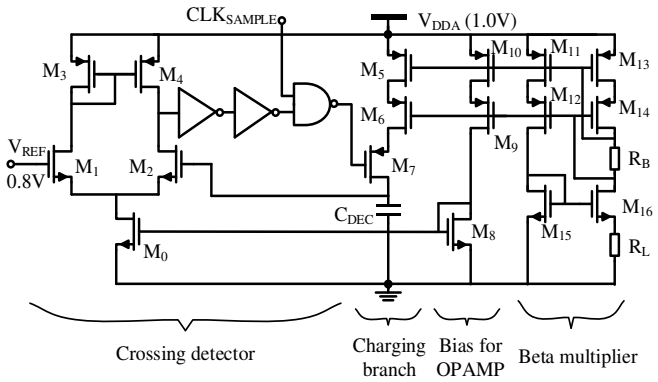


Figure 8.25: Schematic of the pre-charger.

8.2.5 Simulation results

The SAR ADC with extracted information is simulated at circuit level to verify the presented compensation scheme. No thermal noise or mismatch is included in the simulation. Due to the long simulation time, only a 128-point FFT is performed and the comparison with the behavioral model (including parasitic capacitance) with the same input amplitude (0.35·full-scale) is listed in TABLE 8-7. The absolute performance of the post-layout simulation deviates from the behavioral model, as the circuit simulation also includes other non-idealities such as T&H distortion, hence showing slightly different results as the behavioral model (Figure 8.20). In general, the post-layout simulations show the same trend as the behavioral model.

TABLE 8-7: Simulation results of layout-extracted view and behavioral model.

	Behavioral simulations		Post-layout simulations	
	With parasitic capacitance			
	Input amplitude = 0.35·full-scale			
	10000-point FFT		128-point FFT	
	SNDR	SFDR	SNDR	SFDR
No compensation	54.5dB	58.7dB	54.2dB	58.0dB
3b compensation	57.6dB	67.1dB	57.5dB	63.8dB
Ideal driver	60.5dB	81.6dB	60.4dB	69.3dB

8.2.6 Measurement results

The prototype is fabricated in 65nm CMOS technology and occupies a chip area of 0.081mm^2 (Figure 8.26). The SAR ADC core occupies a chip area of 0.074mm^2 and the pre-charger, C_{DEC}, compensation DAC, and the control logic add only 9.5% more chip area to the SAR ADC, where C_{DEC} is dominant.

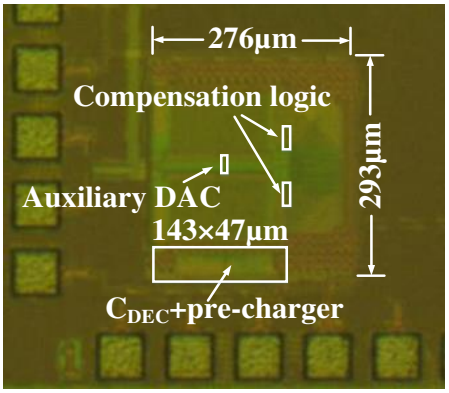


Figure 8.26: Die photo in 65nm CMOS.

At 20MS/s and with a near-Nyquist input tone, the compensation reduces the 3rd order harmonic by 13.5dB and the SNDR is improved by 2.4dB, achieving 56.8dB SNDR and 72.4dB SFDR (Figure 8.27, both cases with redundancy). The THD is improved from 56.9dB to 64.1dB which can be explained from Figure 8.19 and Figure 8.27. The compensation scheme worsens the INL at the middle of the full-scale input range but greatly improves the INL at 1/4 and 3/4 of the full-scale input range. As a result, the 3rd order distortion is greatly reduced (SFDR) with increased high order distortion (Figure 8.27). However, the introduced high order distortion increment is smaller than the 3rd order reduction and the THD is still improved. Despite the large THD improvement, the SNDR improvement is only 2.4dB, limited by the SNR (Figure 8.27).

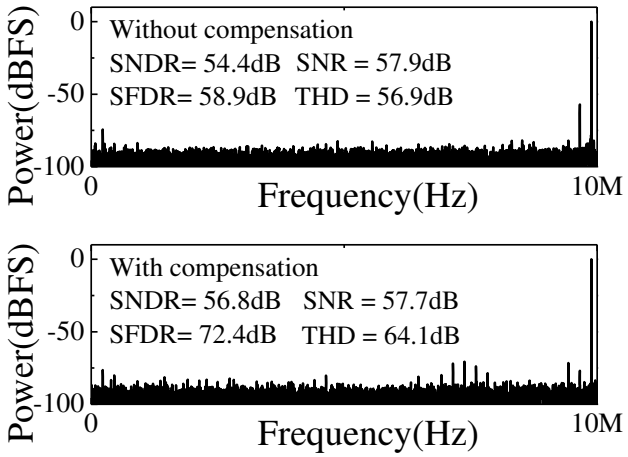


Figure 8.27: Measured spectrum without and with compensation.

The linearity improvement can be further observed in INL/DNL plots (Figure 8.28). The initial 3rd-order distortion shape in the INL plot is caused by the V_{REF} drop and improved by the compensation. Since only 3 switching steps are compensated, transitions in the INL curve become visible for the lower uncompensated bits, which is in line with the previous discussion (Figure 8.19). Compared with our previous work [72], the INL_{max} is greatly improved thanks to the redundancy.

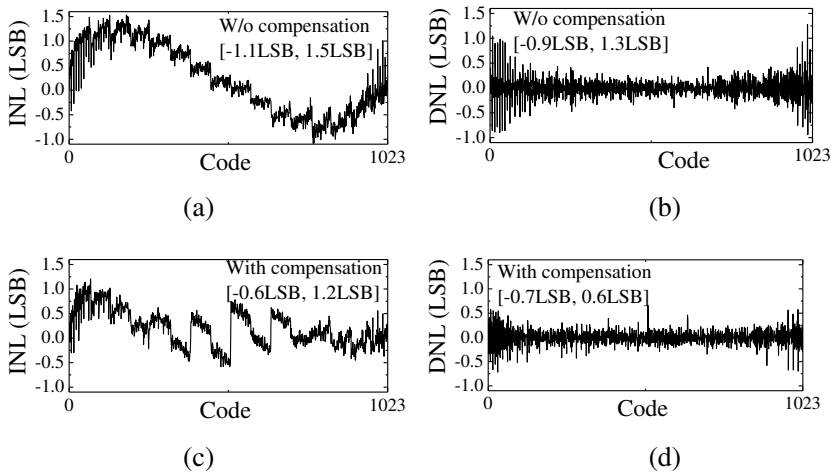


Figure 8.28: (a) INL without compensation; (b) DNL without compensation; (c) INL with compensation; (d) DNL with compensation.

The SNDR and SFDR at different input frequencies are also measured with different driving schemes: external power supply, and on-chip discrete-time driver without and with compensation as shown in Figure 8.29. The compensation improves the performance throughout the entire bandwidth. Since only the first 3 switching steps are compensated and the other steps still suffer from V_{REF} drop, the SNDR/SFDR of the SAR ADC with compensation at a near-Nyquist input remains 1.3dB/4.7dB lower than the case with external power supply.

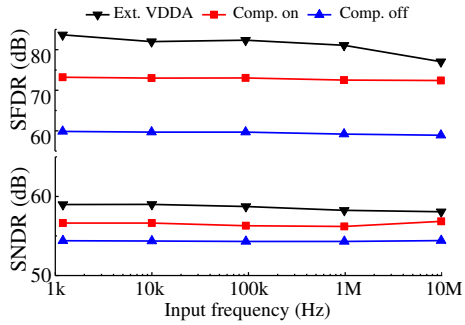


Figure 8.29: Measured SNDR and SFDR at different input frequencies with DAC driven by external power supply, and C_{DEC} without and with 3 compensation steps.

The power consumption and breakdown are shown in Figure 8.30. The stand-alone SAR ADC consumes 0.133mW and the discrete-time reference driver adds 0.014mW/0.017mW without/with compensation respectively, where the added power is dominated by the driver and the drop-out loss. The power introduced by the auxiliary DAC and extra compensation logic is only about 2% of the SAR ADC power consumption.

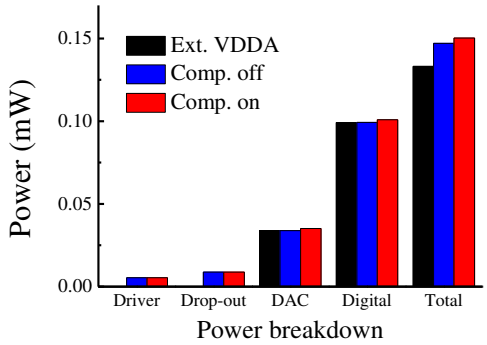


Figure 8.30: SAR ADC power breakdown at near-Nyquist input with DAC driven by external power supply, and C_{DEC} without and with 3 compensation steps.

The PSRR of the discrete-time driver is also demonstrated by removing all the external decoupling capacitance and forcing a sinewave interference at the power supply to measure the dynamic performance. Figure 8.31 shows the SNDR and SFDR of the SAR ADC at a near-Nyquist input tone with different amplitudes of interference (at 4.9MHz) on the power supply for the 3 driving scenarios as discussed above. When driven by an external VDD, the SAR ADC reveals no power regulation ability and the performances degrades rapidly with an increasing interference amplitude. With a realistic interference amplitude of 20mVpp, the

discrete-time reference maintains an SNDR/SFDR drop of less than 1.8dB/1.9dB.

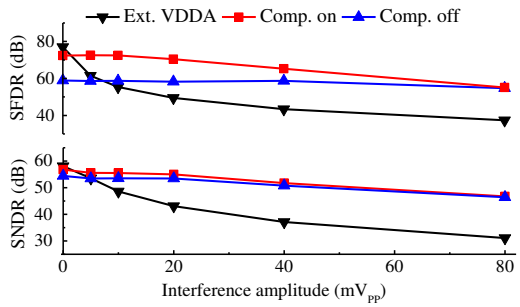


Figure 8.31: Measured SNDR and SFDR for different interference amplitudes at 4.9MHz on the power supply when using an external supply directly, or when using the on-chip driver and C_{DEC} without and with compensation.

TABLE 8-8 summarizes this work and compares it with other SAR ADCs with reference driver. The work in TABLE 8-8 can be categorized into two types: this work, our previous work [72], [67] and [69] utilize C_{DEC} as the driver, while [62, 63, 64] use an active driver. Compared with an active driver, driving with C_{DEC} reveals advantages both in power consumption (P_{driver}/P_{ADC} ranges from 5~12.9%) and chip area ($Area_{driver}/Area_{ADC}$ ranges from 8.1~16%). Compared with our previous work [72], redundancy introduces a little bit more chip area while improving the SFDR /SNDR of the SAR ADC by 4.6dB/1.4dB. Compared to [67] and [69] which require calibration and digital post-processing, the presented discrete-time reference realizes the compensation in the analog domain, eliminating the cost for calibration and reducing the complexity. After enabling the compensation, the presented reference driver improves the SNDR/SFDR with little power overhead, enhancing the Walden FoM from 17.2fJ/conv.-step to 13.3fJ/conv.-step and the Schreier FoM from 162.7dB to 165.0dB.

TABLE 8-8: Performance summary and comparison.

	This work		[72]	[67]	[69]	[62]	[63]	[64]
Technology (nm)	**CMOS 65**		CMOS 65	FinFET 16	CMOS 65	CMOS 28	CMOS 28	CMOS 28
VDD (V)	**1.0/0.8**		1.0/0.8	0.8	1.2	1.2/1.1	1.8/1.0	0.9
Sample rate (MS/s)	**20**		20	303	80	104	100	100
Resolution (bit)	**10**		10	12	14	12	15	12
C_T (pF)	**1**		1	1	4.1	3.6	1.25	0.9
V_{REF} driver	**C_{DEC}**	**C_{DEC}**	**C_{DEC}**	**C_{DEC}**	**C_{DEC}**	Driver	Driver	Driver
Compensation	**No**	**Yes**	Yes	-	-	-	-	-
Calibration and digital processing required?	**No**	**No**	No	Yes	Yes	-	-	-
ADC area (mm^2)	**0.074**		0.069	0.27	0.55	0.003	0.077	0.0046
V_{REF} driver area (mm^2)	**0.006**	**0.007**	0.007	0.043*	N/A	0.004	0.023	0.0028
C_{DEC} included in area?	**Yes**	**Yes**	Yes	Yes	Yes	N/A	N/A	No
C_{DEC} (pF)	**20**	**20**	20	50	160	-	-	-
$Area_{driver}$ /$Area_{ADC}$ (%)	**8.1**	**9.5**	10.8	16	N/A	133.3	29.9	60.9
ADC power (mW)	**0.133**		0.136	3.6	31.1	0.88	4.8	0.35
V_{REF} driver power (mW)	**0.014**	**0.017**	0.015	0.18*	4.0	0.72	3.2	1.56
P_{driver}/P_{ADC} (%)	**10.5**	**12.8**	10.1	5	12.9	81.8	66.7	445.7
SFDR (dB)	**58.9**	**72.4**	67.8	73.6	88.6	-	-	75.4
SNDR (dB)	**54.4**	**56.8**	55.4	63.9	71.3	63	67.1	64.4
FoM (fJ/conv.-step)	**17.2**	**13.3**	15.7	9.2	146.3	13.2	43.2	12.5
$FoM_{Schreier}$ (dB)**	**162.7**	**165.0**	163.6	169.9	161.9	168.1	165.1	168.6

* The power and chip area do not include the driver used during tracking phase.

** $FoM_{Schreier}$ (dB) = SNDR+10*$\log_{10}(f_{snyq}/2/P)$.

8.2.7 Conclusions

In this sub-chapter, a low-power and area-efficient discrete-time reference is presented. The discrete-time passive driver replaces the continuous-time driver to save power. Moreover, the reference drop is compensated to reduce C_{DEC} hence saving substantial chip area. The compensation for the first 3 DAC switching steps in this work reduces C_{DEC} by a factor of 3. The presented compensation is realized in the analog domain, requiring no calibration or digital processing. A similar compensation technique with tweaked capacitor weights can

also be adopted in [68] and [69] to get rid of the calibration and digital processing. The presented passive driving scheme combines the advantages of a charge-redistribution DAC (simple and insensitive to parasitic capacitance) and a charge-sharing DAC (only using the reference during tracking). The 10b 20MS/s prototype ADC proves that the reference driver can be made with low power (12.8% of the ADC core) and small area (0.07mm^2).

8.3 Conclusions

In this chapter, two SAR ADCs with integrated reference driver are presented. The first design also integrates a low-power voltage reference which is made with little power with the help of a 3-stage sample-and-hold stage. Regarding the reference driver, it is realized with an active driver and a large decoupling capacitor as discussed in Chapter 7.1.3, achieving low power at the expense of area. The second design utilizes a passive decoupling capacitor combined with reference-drop compensation, to avoid a power-hungry driver or chip area. Compared with other passive drivers [66, 67, 68, 69], the presented scheme aims at binary DAC voltage steps directly by analog domain compensation, hence avoiding calibration or digital post processing. Consequently, the DAC-compensated driving scheme reveals low power (passive driver), small area (C_{DEC} equal to $20C_T$), and low circuit complexity (no calibration or digital processing) simultaneously.

Chapter 9 Conclusions and suggestions for future research

Low-power and area-efficient techniques for SAR ADCs with on-chip reference generation have been presented in this thesis for low-power applications like IoT sensors and flexible biomedical sensors. In this chapter, conclusions of the thesis are explicated and some suggestions for future research are given.

9.1 Conclusions

In order to achieve better overall performance of an integrated system, co-design is a very effective approach, which means two or more blocks are designed synergistically instead of separately. Apart from co-design, the optimization of each sub block is also very important for an integrated system. Consequently, this thesis studies the integration of SAR ADCs with reference generation, aiming for low power consumption and area efficiency at system level (co-design) and block level.

The presented DAC-compensated reference driver in Chapter 8.2 is an example of co-design, where the DAC is modified according to the passive driver. The compensation is realized in analog domain, requiring no calibration, trimming, or digital post processing. The reference driver achieves low power (12.8% of the ADC core) and occupies small area (10.5% of the ADC core) simultaneously by means of co-design.

In a SAR ADC, the DAC and the comparator usually dominate the total power consumption, hence being urgent to optimize. Since the mainstream implementations of the DAC and comparator are normally dynamic circuits, power can be reduced by reusing the charge. For the energy-free 'swap-to-reset' in Chapter 4, 1/3 of the DAC energy can be saved by reusing the charge during the reset phase. For the bi-directional dynamic comparator in Chapter 8.1.4, 1/3 of the power can be saved by reusing the charge for both the first and the second comparison phase.

Low-VDD and low-power voltage references need to be addressed with the development of low-power applications, where CMOS VRs reveal several advantages, e.g., lower power consumption, better CMOS technology compatibility and scalability, and smaller minimum

operational VDD, compared to the popular BJT-based bandgaps. Subthreshold operation of MOSFETs is a key to achieve low-VDD and low-power operation (Chapter 6). The threshold voltage difference induced by extra ion implantation between nominal-V_t and high-V_t MOSFETs has very small process variations (5x smaller than absolute V_t in the adopted technology), hence being a suitable candidate for the CMOS voltage reference designs. By combining above techniques, the presented voltage reference operates from a minimum VDD of 0.62V and consumes 25nW, revealing a small corner variation of ±1.5%.

Switched capacitors can be widely used in low-power and area-efficient voltage references. Multi-stage switched capacitors can sample the reference voltage and hold it with small leakage, providing constant voltage, while the voltage reference can be duty-cycled to save power. The presented 3-stage switched capacitor can realize a 10% duty-cycling of the voltage reference while providing a reference voltage with an inaccuracy within ±0.013%. Moreover, switched capacitors can be used to replace large resistors in low-power designs, reducing the chip area and power consumption significantly. The voltage reference presented in Chapter 6.4 saves more than 7x power consumption and 11x chip area compared with the one in Chapter 6.1.

9.2 Suggestions for future research

Due to the limited time, some primary thoughts have not been further investigated and will be introduced briefly in this sub-chapter as suggestions for future research.

For the SAR ADC with integrated reference generation, the co-design of the reference driver and the SAR ADC has been proved to be an effective approach in this thesis. On the other hand, the voltage reference in Chapter 8.1 is duty-cycled to operate in discrete time to save power, which resembles the discrete time operation of a SAR ADC and the reference driver in Chapter 8.2. One step further, the voltage reference can also be involved in the co-design to achieve better overall performance in a larger scope.

The scope of this thesis is restricted to the integration and the co-design of a SAR ADC and the reference generation. Furthermore, the integration and co-design of a SAR ADC with more auxiliary blocks should be investigated. For instance, if the input driver of a SAR ADC can guarantee a very accurate common mode of the inputs, this common mode information can be extracted and used as a reference voltage for the CS SAR ADCs and the reference driver can be eliminated, achieving simpler circuitry complexity and better power efficiency.

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M. Liu, A. van Roermund, and P. Harpe, "A 10b 20MS/s SAR ADC with DAC- Compensated Discrete-Time Reference Driver," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 2, pp. 417-427, Feb. 2019.

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Summary

Low-Power Area-Efficient SAR ADCs with On-chip Voltage Reference

This thesis focuses on low-power and area-efficient techniques for SAR ADCs with on-chip reference generation for the CR DAC. In order to achieve better performance of an integrated system, both system level and block level optimization are investigated. This thesis can be expanded from three aspects: SAR ADC power optimization, low-power low-VDD voltage reference, and the reference driver for the CR DAC in a SAR ADC.

In a SAR ADC, the power consumption of the DAC and the comparator dominate the total power consumption. In Chapter 3, different DAC topologies (CS and CR) and CR DAC switching schemes are summarized and compared, where the reasons to adopt CR DACs in our designs are given. Some CR DAC schemes save power consumption while introducing new problems like DAC common mode shift or a required 3rd reference voltage. Some other schemes save power during conversion without previous problems while introducing large reset power consumption. An energy-free 'swap-to-reset' scheme is proposed in Chapter 4 to deal with the large DAC reset energy by charge reusing which can be widely applied to many existing switching schemes and make them more energy-efficient. As for the comparator, a bi-directional comparator is proposed in Chapter 8 to reuse the charge for both comparison phases, hence reducing half the power of the typical dynamic preamplifier.

With low-power low-VDD applications getting more and more popular, low-power and low-VDD voltage references draw a lot of attention as an essential block in most SoCs. An overview of BJT-based and CMOS-based voltage references is given in Chapter 5, where the motivations to investigate on CMOS voltage reference for low-power applications are explicated. In Chapter 6, several low-power and low-VDD voltage references have been proposed. A 0.62V-VDD 25nW CMOS voltage reference makes use of the threshold voltage difference between high-V_t and nominal-V_t transistors and achieves small variations over process corners (Chapter 6.1). In order to reduce the power consumption further, a 3-stage sample-and-hold is proposed to provide a constant reference voltage while the voltage reference is being duty-cycled (Chapter 6.2). Above design makes use of large poly resistors to suppress the power consumption, occupying large chip area. In the design of Chapter 6.3, the poly resistors are replaced with MOSFETs to reduce the chip area while the temperature characteristic of the threshold voltage of a MOSFET gives large power consumption deviation over temperature. Subsequently, the sample-and-hold can be directly applied to the voltage reference core to make the voltage reference fully dynamic to reduce the power

and achieve stable power over temperature (Chapter 6.4). Previous designs need to make use of two types of transistors, which increases the fabrication cost. The design in Chapter 6.5 makes use of single-type of transistors and they are set in different sizes to generate a threshold voltage difference as the primary voltage unit for the voltage reference.

In Chapter 7, the design challenges of the reference driver brought by our preference of CR DACs over CS DACs are discussed by studying the literature. In Chapter 8, two SAR ADC designs with reference driver are implemented. The first design makes use of an off-chip capacitor to stabilize the reference voltage for the DAC in the SAR ADC, achieving low-power at the expense of area. The second design uses a pre-charged on-chip capacitor to drive the DAC passively. The non-binary voltage steps caused by the reference voltage drop due to the DAC charge consumption is pre-calculated and compensated by tuning the switched capacitance. As a result, the DAC voltage steps can be binary again. The solution achieves low power and occupies small area at the same time without the need of calibration, trimming, or digital processing.

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Biography

Maoqiang Liu was born on November 10, 1987, in Liaoning, China. In 2010, he received the B.S. degree from the department of Electronics Engineering and Computer Sciences, Peking University, Beijing, China. In 2013, he received the M.S. degree from the school of Microelectronics, Peking University, Beijing, China.

Since 2013, he started to pursuing his PhD's degree in the Integrated Circuits group (named Mixed-Signal Microelectronics group at that time) at Eindhoven University of Technology, Eindhoven, The Netherlands. His research is on low-power mixed-signal circuits with a main focus on the low-power reference voltage generator, low-power SAR ADCs, and the integration of these two aspects in a system, which are presented in this dissertation.

Since 2017, he has been with the AMSIP group of NXP in Eindhoven, The Netherlands.