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Low-Power Delta-Sigma Modulators for Medical Applications

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Cover image:
The cover image, by Ali Fazli and Amin Ojani, shows the digitization of an ECG signal. The piece of circuit illustrates a switched-capacitor integrator using correlated double sampling technique.

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To Sonya
whose beauty, sweetness, and wisdom empower me to be the man that I am

To my family
whose boundless love and belief in me form the core of my being.

Abstract

Biomedical electronics has gained significant attention in healthcare. A general biomedical device comprises energy source, analog-to-digital conversion (ADC), digital signal processing, and communication subsystem, each of which must be designed for minimum energy consumption to adhere to the stringent energy constraint.

The ADC is a key building block in the sensing stage of the implantable biomedical devices. To lower the overall power consumption and allow full integration of a complete biomedical sensor interface, it is desirable to integrate the entire analog front-end, back-end ADC and digital processor in a single chip. While digital circuits benefit substantially from the technology scaling, it is becoming more and more difficult to meet the stringent requirements on linearity, dynamic range, and power-efficiency at lower supply voltages in traditional ADC architectures. This has recently initiated extensive investigations to develop low-voltage, low-power, high-resolution ADCs in nanometer CMOS technologies. Among different ADCs, the ΔΣ converter has shown to be most suitable for high-resolution and low-speed applications due to its high linearity feature.

This thesis investigates the design of high-resolution and power-efficient ΔΣ modulators at very low frequencies. In total, eight discrete-time (DT) modulators have been designed in a 65nm CMOS technology: two active modulators, two hybrid active-passive modulators, two ultra-low-voltage modulators operated at 270mV and 0.5V supply voltages, one fully passive modulator, and a dual-mode ΔΣ modulator using variable-bandwidth amplifiers.

The two active modulators utilize traditional feedback architecture. The first design presents a simple and robust low-power second-order ΔΣ modulator for accurate data conversion in implantable rhythm management devices such as cardiac pacemakers. Significant power reduction is achieved by utilizing a two-stage load-compensated OTA

as well as the low-V_{th} devices in analog circuits and switches. An 80dB SNR (13-bit) was achieved at the cost of 2.1μW power in 0.033mm^2 chip core area. The second design introduces a third-order modulator adopting the switched-opamp and partially body-driven gain-enhanced techniques in the OTAs for low-voltage and low-power consumption. The modulator achieves 87dB SNDR over 500Hz signal bandwidth, consuming 0.6μW at 0.7V supply.

The two hybrid modulators were designed using combined SC active and passive integrators to partially eliminate the analog power associated with the active blocks. The first design employs an active integrator in the 1st stage and a passive integrator in the less critical 2nd stage. A 73.5dB SNR (12-bit) was achieved at the cost of 1.27μW power in a 0.059mm^2 chip core area. The latter modulator utilizes a fourth-order active-passive loop filter with only one active stage. The input-feedforward architecture is used to improve the voltage swing prior to the comparator of the traditional passive modulators, which enables a simpler comparator design without requiring a preamplifier. It also allows the use of three successive passive filters to obtain a higher-order noise shaping. The modulator attains 84dB SNR while dissipating 0.4μW power at a 0.7V supply.

Two ultra-low-voltage DT modulators operating at 0.5V and the state-of-the-art 270mV power supplies were proposed. The former modulator employs a fully passive loop filter followed by a 0.5V preamplifier and dynamic comparator, whereas the latter one exploits the inverter-based integrators with clock boosting scheme for adequate switch overdrive voltage. The first design incorporates a gain-boost scheme using charge redistribution amplification in the passive filter as well as a body-driven gain-enhanced preamplifier prior to the comparator in order to compensate for the gain shortage. It attains 75dB SNR consuming 250nW power, which is a record amongst the state-of-the-art ultra-low-power ΔΣ modulators. The second design uses feedforward architecture that suggests low integrators swing, enabling ultra-low-voltage operation. The degraded gain, GBW and SR of the inverter amplifiers operating at such a low voltage are enhanced by a simple current-mirror output stage. The attained FOM is 0.36pJ/step.

A fully passive DT modulator was presented aiming for analog power reduction, the dominant part of power in the active modulators. A careful analysis of passive filter's non-idealities, including the noise, parasitic effect, and integrator's loss were essential to meet the performance requirement necessary for an implantable device. The chip was tested simultaneously with its active counterpart, showing significant power reduction at the cost of 4× core area and 12dB SNR loss.

The designed dual-mode modulator employs variable-bandwidth amplifiers in combination with oversampling ratio to provide tunable resolution. This work presents the design, implementation, and test results of a two-stage amplifier using the second stage replica that provides tunable GBW but consistent DC gain.

Preface

This Ph.D. thesis presents the results of my research during the period February 2009 to December 2013 at division of Electronic Devices, Department of Electrical Engineering, Linköping University, Sweden. The Doctoral degree comprises 4 years of full-time studies plus 1 year of full-time teaching duties.

This thesis investigates the design of low-power, low-voltage, high-performance ΔΣ modulators in nanometer CMOS technologies. In total, eight discrete-time (DT) modulators have been designed: two active modulators, two hybrid active-passive modulators, two ultra-low-voltage modulators operating at 270mV and 0.5V supply voltages, one fully passive modulator, and a dual-mode ΔΣ modulator using variable-bandwidth amplifiers and adjustable oversampling ratio. This research work has resulted in several papers published in international conferences and journals. The following papers are included in the thesis:

- **Paper 1 – Ali Fazli** and Atila Alvandpour, "A 2.1 μW 80 dB SNR DT ΔΣ Modulator for Medical Implant Devices in 65nm CMOS," *Journal of Analog Integrated Circuits and Signal Processing* (*Springer*), vol. 77, no. 1, pp. 69-78, 2013.

- **Paper 2– Ali Fazli,** Fahad Qazi, Jerzy J. Dabrowski, and Atila Alvandpour, "Design of OTAs for Ultra-Low-Power Sigma-Delta ADCs in Medical Applications," *IEEE International Conference on Signal and Electronic Systems* (*ICSES*), pp. 229-232, Gliwice, Poland, September 2010.

- **Paper 3 – Ali Fazli** and Atila Alvandpour, "A 0.7-V 600-nW 87-dB SNDR DT-ΔΣ Modulator with Partly Body-Driven and Switched Op-amps for

Biopotential Signal Acquisition," *IEEE Biomedical Circuits and Systems Conference* (*BioCAS*), pp. 336-339, Hsinchu, Taiwan, November 2012.

- **Paper 4 – Ali Fazli** and Atila Alvandpour, "A 0.5-V 250-nW 65-dB SNDR Passive ΔΣ Modulator for Medical Implant Devices," *IEEE International Symposium on Circuits and Systems* (*ISCAS*), pp. 2010-2013, Beijing, China, May 2013.

- **Paper 5 – Ali Fazli** and Atila Alvandpour, "A 270-mV ΔΣ Modulator Using Gain-Enhanced, Inverter-Based Amplifier," *Journal of Electronics Letters*, Submitted, 2013.

- **Paper 6 – Ali Fazli,** Fahad Qazi, and Atila Alvandpour, "Low-Power DT ΔΣ Modulators Using SC Passive Filters in 65 nm CMOS," *accepted for publication in IEEE Transactions on Circuits and Systems–I: Regular Papers*, pp.-, issue 99, 2013.

- **Paper 7 – Ali Fazli** and Atila Alvandpour, "A 0.7-V 400-nW Fourth-Order Active-Passive ΔΣ Modulator with One Active Stage," *IEEE International Conference on Very Large Scale Integration* (*VLSI-SoC*), pp. 1-6, Istanbul, Turkey, October 2013.

- **Paper 8 – Ali Fazli** and Atila Alvandpour, "A Programmable-Bandwidth Amplifier for Ultra-Low-Power Switched-Capacitor Application," *IEEE European Conference on Circuit Theory and Design* (*ECCTD*), pp. 761-764, Linköping, Sweden, August 2011.

- **Paper 9– Ali Fazli** and Atila Alvandpour, "A Variable Bandwidth Amplifier for a Dual-Mode Low-Power ΔΣ Modulator in Cardiac Pacemaker System," *IEEE International Symposium on Circuits and Systems* (*ISCAS*), pp. 1918-1921, Beijing, China, May 2013.

The following publications are not included in this thesis. These papers are either fragments of the journal papers included in the thesis or beyond the scope of the thesis:

- **Ali Fazli** and Atila Alvandpour, "A 2.1 μW 76 dB SNDR DT Delta-Sigma Modulator for Medical Implant Devices," *IEEE NORCHIP Conference,* pp. 1-4, Copenhagen, Denmark, November 2012.

- **Ali Fazli**, Martin Hansson, Behzad Mesgarzadeh and Atila Alvandpour, "A Low Voltage and Process Variation Tolerant SRAM Cell in 90-nm CMOS," *IEEE International Symposium on VLSI Design, Automation and Test* (VLSI-DAT), pp. 78-81, Hsinchu, Taiwan, April 2010.

- **Ali Fazli,** Fahad Qazi, Jerzy J. Dabrowski, and Atila Alvandpour, "Design of OTAs for Ultra-Low-Power Sigma-Delta ADCs in Medical Applications," *Swedish System-on-Chip Conference* (*SSoCC*), Kolmården, Sweden, May 2010.

- **Ali Fazli**, Martin Hansson, Behzad Mesgarzadeh and Atila Alvandpour, "A Low Voltage and Process Variation Tolerant 6T Asymmetric SRAM Cell," *Swedish System-on-Chip Conference* (*SSoCC*), Arild, Sweden, May 2009.

Contributions

The main contributions of this dissertation are as follows:

- Design, analysis, and implementation of a low-power second-order single-bit ΔΣ Modulator in a 65nm CMOS process using power-efficient two-stage load-compensated OTAs and an effective power-optimization scheme (Paper 1).
- Design, analysis, and implementation of two ultra-low-power second-order single-bit ΔΣ Modulators in a 65nm process in a single chip using an active-passive or fully passive loop filter (Paper 6).
- Comparative study of three implemented ΔΣ Modulator architectures mentioned above in terms of the system-level analysis, the circuit noise, and the non-idealities associated with the SC passive filters (Paper 6)
- Design and power analysis of several OTA topologies suitable for low-power low-voltage ΔΣ modulators (Paper 1 and 2).
- A novel fourth-order active-passive feedforward ΔΣ Modulator with one active stage attaining state-of-the-art 47fJ/step figure of merit (Paper 7).
- Development of a novel ultra-low-voltage (0.5V power supply) ultra-low-power (250nW) ΔΣ Modulator in 65nm technology using fully passive low-pass filter and state-of-the-art 0.5V building blocks (Paper 4)
- Development of an ultra-low-voltage (270mV) 0.85μW feedforward ΔΣ Modulator in 65nm technology using a novel gain-boosted inverter-based amplifier and charge pump clock boosters (Paper 5)
- Development of a new partially body-driven gain-enhanced two-stage amplifier suitable for low-voltage operation (Paper 3).

- Design, analysis, and implementation of a new low-power variable-bandwidth amplifier (VBA) suitable for SC applications (Paper 8).
- Development of a novel dual-mode low-power delta-sigma modulator using variable-bandwidth OTAs and adjustable oversampling ratio (Paper 9)

Abbreviations

ADC	Analog-to-Digital Converter
CDS	Correlated Double Sampling
CIFB	Cascade-of-Integrators Feedback
CIFF	Cascade-of-Integrators Feedforward
CMFB	Common Mode Feedback
CMOS	Complementary Metal-Oxide-Semiconductor
CMR	Common Mode Range
CMRR	Common Mode Rejection Ratio
CT	Continuous Time
DAC	Digital-to-Analog Converter
DC	Direct Current
DEM	Dynamic Element Matching
DR	Dynamic Range
DT	Discrete Time
ECG	Electrocardiogram
EEG	Electroencephalogram

ENOB	Effective Number of Bit
FOM	Figure-of-Merit
GBW	Gain Bandwidth Product
IC	Integrated Circuit
IEEE	The Institute of Electrical and Electronics Engineers
ITRS	International Technology Roadmap for Semiconductors
LSB	Least Significant Bit
MIM	Metal Insulate Metal
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
NMOS	N-channel Metal-Oxide-Semiconductor
NTF	Noise Transfer Function
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PMOS	P-channel Metal-Oxide-Semiconductor
PSD	Power Spectral Density
PSRR	Power Supply Rejection Ratio
PVT	Process-Voltage-Temperature
RMS	Root-Mean-Square
RTO	Return to Open
RZ	Return to Zero
SC	Switched Capacitor
SNDR	Signal-to-Noise and Distortion Ratio
SNR	Signal-to-Noise Ratio
SO	Switched Opamp
SR	Slew Rate
STF	Signal Transfer Function
VBA	variable bandwidth amplifier

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Without the help, support, and encouragement of a large number of people it would not be possible for me to write this thesis. I would like to thank the following people and organizations:

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Ali Fazli

Linköping, December, 2013

Contents

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Part I

Background

Chapter 1

Introduction

1.1 Motivation and Scope of This Thesis

Biomedical electronics has gained significant attention in healthcare industry, where biomedical devices are becoming widespread for use in the diagnosis of disease or other conditions, or in the cure, mitigation and prevention of disease. They are used in wide variety of conditions such as cardiac pacemakers for cardiac arrhythmia, cochlear implants for deafness or retinal implants for blindness. A large amount of activity is being researched in brain-machine interfaces for paralysis, stroke, and blindness [1]. A general biomedical device comprises energy source, analog preprocessing, analog-to-digital conversion (ADC), digital signal preprocessing, and communication subsystem, each of which must be designed for minimum energy consumption to adhere to the stringent energy constraint.

The ADC is one of the key building blocks in all biomedical electronic systems. As of particular interest in this thesis, the ADC is an important block in the sensing stage of the biomedical systems, such as implantable devices, for accurate detection of the physiological signals like electrocardiogram (ECG) and electroencephalogram (EEG). To minimize the overall power consumption and allow full integration of a complete biomedical sensor interface, it is desirable to integrate the entire analog front-end, back-end ADC and digital processor in a single chip. While digital circuits benefit substantially from the technology scaling-down, it is becoming more and more difficult to meet the stringent requirements on linearity, dynamic range, and power-efficiency at lower supply voltages in traditional ADC architectures. This has recently initiated

extensive investigations to develop low-voltage, low-power, high-resolution ADCs in nanometer CMOS technologies. Among different ADCs, the ΔΣ converter has shown to be most suitable for high-resolution and low-speed applications due to its high linearity property, which is obtained from the intrinsically linear single-bit quantizer and the oversampling technique.

This thesis addresses the possibility of designing high-performance and ultra-low-power ΔΣ modulators at very low frequencies. In total, eight discrete-time (DT) modulators have been designed in a 65nm CMOS technology, spanning from 10- to 14-bit of resolution. Both circuit-level and system-level approaches are used in the design of low-power low-voltage ΔΣ ADCs with power supply varying from 270mV to 0.9V and power consumption ranging from 250nW to 2.1μW. By applying these approaches to the ΔΣ ADC design, several test chips have proven the possibility of designing high-performance low-power low-voltage converters in nanometer CMOS technologies.

1.2 Importance of Ultra-Low-Power Designs

Ultra-low-power design is important in systems that need to be portable and therefore operate with a long lifetime battery or other source of reasonable size or small rechargeable battery with long time between recharges. The more compact the system, the smaller the energy source, and the more stringent is the power constraint. Ultra-low-power design is also important in the systems that need to minimize the heat dissipation. As an example, biomedical systems that are implanted within human body need to fulfill all the mentioned constraints. They need to be very small in size and lightweight with minimal heat dissipation in the tissue that encompasses them. In some systems like cardiac pacemakers, the implanted devices are often powered by a small non-rechargeable battery. In others, like cochlear implants, the units are traditionally powered by wireless energy source using a cell outside the body [1]. In either case, the power dissipation dictates the size of the receiving coil, or battery, and thereby sets a minimum size constraint on the systems. In the implanted systems operating with a battery with limited number of wireless recharges, there is a stringent need for ultra-low-power circuit design such that frequent surgery is not needed to change the battery in a patient. The system must operate ideally for 10-30 years without need for battery replacement.

Not restricted to biomedical implantable devices, many non-invasive biomedical systems such as cardiac tags that are attached to clothing for patient status monitoring rely either on battery or wireless RF energy. Also, bio-potential acquistion systems for portable medical applications need to adhere to strict requirement on low power consumption.

This thesis, to a large extent, uses biomedical systems in general and implantable devices in particular, as examples of low-power integrated circuit designs. Nevertheless, the principles, circuit techniques and topologies, and the ADC architectures are useful and applicable to several other systems such as in sensor networks, cell phones and audio applications.

Ultra-low-power analog-to-digital converter (ADC) in this thesis usually refers to an ADC that operate anywhere from tens of nanoWatt to tens of microWatt. Generally saying, an ADC that dissipates 1μW rather than, say, 20-30μW without compromising performance can be referred to as an ultra-low-power ADC. There are several performance measures or figure-of-merits (FOMs) that can be used to evaluate the power-efficiency of an ADC. These will be extensively discussed in the succeeding Chapters where the performance of the proposed ΔΣ modulators are compared with that of the previously reported modulators.

Ultra-low-voltage ADC in this thesis is referred to an ADC that operate with a power supply far below the nominal supply voltage of the used technology. For instance, the typical supply voltage in a 65nm CMOS technology is 1.1V, where the threshold voltage of the standard device is around 0.45V. As a convention throughout this thesis, when the operating supply is less than half of the nominal supply and/or near or less than the threshold voltage of a certain technology, the corresponding ADC is considered to be an ultra-low-voltage ADC. An ultra-low-voltage, 0.5V, continuous-time (CT) delta-sigma modulator is presented in 0.18μm CMOS technology with 0.5V threshold voltage by Pun in 2007 [2]. A 0.5V SC modulator is presented by Yang in 2012 [3] in 0.13μm CMOS technology where the threshold voltages of the PMOS and NMOS are -0.27V and 0.22V, respectively. In Chapter 4, the circuit design challenges in very low voltage operation and the existing low-voltage modulators are explained in details. Also, two ultra-low-voltage ΔΣ modulator operating at 0.5V and 0.27V supply voltages are introduced in 65nm CMOS technology [4], [5].

1.3 Discrete-Time versus Continuous-Time

Discrete-time (DT) or Continuous-Time (CT)? This is most probabely the first design choice that a designer has to do. Among several reported low-voltage low-power ΔΣ modulators, the DT loop filters [3]-[9] are the preferred choise compared to their CT counterparts. The DT modulator is more attractive for high-resolution applications due to its higher linearity and accuracy [10]. The CT modulator, however, has a distinct feature that can help to reduce the power consumption. It is the absence of switches in the active-RC integrator, which relaxes the settling requirements on the amplifires and eliminates the need for clock boosting circuits for switches, in low-voltage operation [11]. The relaxed settling requirements in the active-RC filters can be translated into the mitigated gain-bandwidth (GBW) of the amplifiers, and therefore reduced power consumption. As a rule of thumb, the amplifier's GBW in a CT modulator can be chosen to be one to three times of the sampling frequency, while that of the DT modulator has to be five to seven times of the sampling frequency for accurate settling [12]. On the other hand, amplifier in the active-RC integrator has to drive the integrating resistor of the succeeding integrator. This resistive loading will obviously reduce the amplifier's DC gain. To minimize the gain degradation, either very large integrating resistor compared to the amplifier output resistance must be used or a gain boosting scheme to be integrated in the amplifier topology, like the one in [11]. The

larger resistors in the integrators, particularly that of the second integrator, dictate a higher noise and larger parasitic capacitances. In low-voltage operation, boosting the gain is more difficult due to the absence of the transistor cascoding, and will cost more area and power consumption. Furthermore, in CT filters, the amplifires require power-hungry CT common-mode feedback (CMFB) circuitries for the robust biasing against process, voltage and temperature (PVT) variations, rather than power-efficient SC CMFBs. This is rather a drawback with the use of CT loop filters. Compared to that of the DT modulator, the performance of the CT modulator is more sensitive to clock-related nonidealities, such as clock jitter in the feedback digital-to-analog converter (DAC) and excess loop delay [11], [13]. Fortunately, these nonidealities are largely mitigated in low speed applications like biomedical applications. The RC time-constant variation is present in any CT modulator implementation, which can largely affect the performance or even create reliability issue (instability). The DT modulator is more robust against the capacitor ratio variations than the RC variations in its CT counterpart. As the simulation results show in the CT modulator presented in [2], the SNDR can vary up to 7dB with respect to ±20% RC variations. In this thesis, the focus of the research will be on the possibility of designing high-resolution low-power converters using DT implementation in nanometer CMOS technologies.

1.4 Power-Efficient Subthreshold Regime of Transistor Operation

Subthreshold, or weak inversion operation has become increasingly attractive in low-power systems design. In biomedical applications, subthreshold regime is highly beneficial since the bandwidth requirements are modest in such low speed applications, whereas energy efficiency is of great importance [14]. The g_m/I ratio is maximum in this regime such that the speed per watt is maximized. In other words, the least power is dissipated for a given bandwidth. For a certain current, the transconductance, g_m, of a transistor operating in weak inversion region is about five times of that in strong inversion region. On the other hand, the high g_m/I ratio and exponential dependency to voltage and temperature make this regime highly sensitive to transistor mismatch, power supply noise, and temperature variation. Therefore, careful sizing and appropriate biasing and feedback circuits are required for robust operation. Also, linearity of analog circuit is worse in this regime. The supply voltage has to be sufficiently high in digital circuits to ensure robust operation across all process corners. The modulator designs running under 1MHz clock frequency, presented in **Paper 1**–**7**, repeatedly use the advantage of subthreshold operation regime for power efficiency, either partially or thoroughly, both in digital and analog circuits. For examples, the input transistors in the partly body-driven amplifiers employed in **Papers 3** and **7** benefit from the high g_m/I ratio of the weak inversion operation to attain a few MHz GBW at only tens of nanowatt power consumption. The preamplifier circuit in fully passive modulators presented in **Papers 4** and **6** take advantage of subthreshold operation. Moreover, the

entire digital and analog circuits of the inverter-based modulator introduced in **Paper 5** operating at 270mV power supply enjoy from the weak inversion regime.

1.5 Organization of This Thesis

This thesis is organized into two parts:

- Part I - Background
- Part II - Publications

Part I provides the background, the previous circuit techniques and modulator architectures, and further clarifications and explanations for the concepts used in the papers. The nine papers included in this thesis fall in four categories: (i) low-power ΔΣ modulators using standard active approach (Chapter 2), (ii) low-power ΔΣ modulators using passive and hybrid active-passive approaches (Chapters 3), (iii) low-voltage low-power ΔΣ modulators which benefits from both mentioned approaches, and eventually (iv) low-power dual-mode modulator.

Chapter 1 discusses the motivations behind this research, the importance of low-power design, the thesis organization, the summary of the papers, and broad discussions related to the type of the ΔΣ ADC.

Chapter 2 describes the design of low-power ΔΣ modulators using traditional feedback architecture and active (OTA-based) integrators in nanometer CMOS technologies. An experimental second-order single-bit ΔΣ modulator (**Papers 1**) is presented where special measures are taken in the circuit design to reduce the power consumption.

Chapter 3 introduces new approaches for power reduction in the ΔΣ modulators. It describes the design and analysis of the passive filter and associated circuit nonidealities. Then three ultra-low-power modulator designs employing active-passive filter structure (**Papers 6, 7**) and a fully passive filter topology (**Papers 6**) are presented. A novel fourth-order feedforward active-passive modulator is presented with only one active stage (**Papers 6**), presenting an impressive figure of merit compared to the state-of-the-art low-power ADCs.

Chapter 4 discusses the major design challenges in very low-voltage operation. This Chapter uses both active and passive circuit approaches that are discussed in Chapters 2 and 3, and serves as a background for the ΔΣ modulator designs in **Paper 3 - Paper 5**. Two ultra-low-voltage delta-sigma converters operating at 0.5V and 270mV power supplies are introduced. The former design utilizes a fully passive filter structure and the state-of-the-art 0.5V circuit blocks. The latter design employs a novel gain-boosted inverter-based amplifier and a clock boosting scheme for the switching devices in a feedforward modulator topology.

Chapter 5 presents a new variable bandwidth amplifier (VBA) with tunable unity-gain frequency but consistent DC gain (**Papers 8**). Thereafter, a dual-mode delta-sigma modulator which combines the designed VBAs with adjustable oversampling ratio

(OSR) is introduced (**Papers 9**). The main advantage of this flexible ADC is that it optimizes both the integration area and the power consumption.

Chapter 6 concludes the thesis and suggests future investigations.

In Part II, the papers included in this thesis are presented in full.

1.6 Summary of Papers

This thesis addresses the possibility of designing high-resolution and power-efficient ΔΣ modulators at very low frequencies. In total, eight DT modulators have been designed in a 65nm CMOS technology - two traditional feedback active modulators (**Papers 1** and **3**), two hybrid active-passive modulators (**Papers 6** and **7**), two ultra-low-voltage modulators operated at 270mV and 0.5V supply voltages (**Papers 4** and **5**), one fully passive modulator (**Papers 6**), and a dual-mode ΔΣ modulator using variable-bandwidth amplifiers and adjustable OSR (**Papers 9**).

The two active modulators in **Papers 1** and **3** utilize traditional feedback architecture. The first design presents a simple and robust low-power second-order ΔΣ modulator for accurate data conversion in implantable rhythm management devices, such as cardiac pacemakers. The system-level and low-power design considerations are discussed in **Paper 1**. Significant power reduction is achieved by utilizing a two-stage load-compensated OTA as well as the low-V_{th} devices in the analog circuits and the switches, allowing the modulator to operate at 0.9V power supply. An 80dB peak SNR (13-bit) is achieved at the cost of 2.1μW power in only 0.033mm^2 chip core area. The second design presented in **Paper 3** introduces a 0.7V third-order modulator intended for measurement of biopotential signals in portable medical applications. Switched-opamp and new partially body-driven gain-enhanced techniques have been adopted in the amplifiers for low-voltage operation and low-power consumption. The modulator achieves 87dB peak SNDR over 500Hz signal bandwidth, while consuming 600nW at 0.7V supply voltage.

The two hybrid modulators, suited for implantable medical devices, are designed using combined active and passive SC integrators to partially eliminate the analog power consumption associated with the active blocks. The first design in **Paper 6** employs an active integrator in the 1st stage and a passive integrator in the less critical 2nd stage. A 73.5dB SNR (12-bit) is achieved at the cost of 1.27μW power in a 0.059mm^2 chip core area. The latter modulator presented in **Paper 7** utilizes a fourth-order active-passive loop filter with only one active stage. The input feedforward architecture is used to improve the voltage swing prior to the comparator of the traditional passive modulators, which enables a simpler comparator design requiring no preamplifier. The feedforward modulator architecture enables the higher-order noise shaping (4th-order) using cascade of three successive power-efficient passive filters. The active stage is to reduce the noise and offset of the comparator and to minimize the capacitive area caused by the passive stages. The total capacitor size decreases by 51% as compared to the fully passive modulator in **Paper 6**. The modulator attains 84dB

SNR while dissipating 0.4μW power at a 0.7V supply. An impressive figure of merit (of 47fJ/step) is achieved as compared to the state-of-the-art low-power ADCs.

Two ultra-low-voltage DT modulators operating at 0.5V (**Papers 4**) and the state-of-the-art 270mV (**Papers 5**) power supplies are proposed in which the former employs a fully passive, second-order, loop filter followed by 0.5V preamplifier and dynamic comparator, whereas the latter exploits inverter-based integrators and a clock boosting scheme that provides adequate overdrive voltage for the switches. The first design incorporates a SC gain-boost technique by using a charge redistribution amplification scheme in the passive filter. Also, a body-driven gain-enhanced preamplifier is used prior to the comparator to somewhat compensate for the lack of gain. It attains 75dB SNR at the cost of only 250nW power, which is a record amongst the state-of-the-art ultra-low-power ΔΣ modulators. The second design utilizes an input feedforward architecture that enables low integrators internal swing, supporting ultra-low-voltage operation. The switches are driven by a charge pump clock doubler. The reduced gain, GBW and SR of the inverter-based amplifiers operating at 270mV power supply are enhanced by a simple power-efficient current-mirror output stage. The modulator achieves 64.4dB and 61dB peak SNR and SNDR, respectively, over a 1kHz signal bandwidth. The power consumption is 0.85μW at 270mV supply voltage. The attained FOM is 0.31pJ/[conversion-step].

A second-order modulator using fully passive filter structure is presented in **Paper 6** which aims for analog power reduction, the dominant part of the power in the classical modulators. Careful analysis of the nonidealities in the passive filter including the thermal noise, the parasitic effect, and the integrator's leakage are essential to meet the performance requirements necessary for an implantable device. The chip was tested simultaneously with its active counterpart fabricated in the same chip, which demonstrates significant power reduction at the cost of 4× the core area and 12dB SNR loss. The proposed modulator presents a peak SNR of 68dB, and consumes 0.43μW power consumption at 0.7V operating power supply. The active core area is 0.125mm^2.

The **Paper 8** presents the design, implementation, and the test results of a variable bandwidth two-stage amplifier. Two replicas of the second stage in a load-compensated two-stage amplifier are used to provide tunable GBW (or 3dB cut-off frequency corner) with consistent DC gain. A dual-mode second-order single-bit ΔΣ modulator is introduced in **Paper 9**, which employs the proposed VBAs in combination with the adjustable OSR. The choice of the sampling frequencies to be a multiple of 32 makes it very easy to provide a 64kHz master clock input and then produce the other sampling frequency, i.e. 32kHz, by a division-by-2 using a D-FF. This can significantly reduce the complexity of the clock generation circuitry. Therefore, the shift from one mode to another is accomplished by merely dividing the input clock frequency by two, while at the same time the GBW is reduced by switching off the replica stages that can reduce the power consumption. As a result, the FOM is improved by 100%.

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Chapter 2

Low-Power ΔΣ Modulators: Active Approach

2.1 Introduction

This Chapter describes the design of low-power ΔΣ modulators using traditional distributed feedback architecture and active (OTA-based) integrators in nanometer CMOS technologies. It investigates the design and power analysis of several OTA topologies [1], [2], as the key analog component and the most power consuming block of the ΔΣ modulators (**Papers 1, 2**). The fundamentals of the traditional modulator topology are discussed, and then the concept of quantization noise shaping and oversampling techniques are described. The circuit noise-shaping phenomenon is also discussed. As a practical example, the circuit noise analysis of an implemented second-order ΔΣ modulator is included. Afterwards, the recent circuit techniques and innovations concerning the design of low-power ΔΣ converters are reviewed in brief. The system-level design and low-power modulator design considerations are explained in details. The experimental implementation of the second-order single-bit ΔΣ modulator presented in **Papers 1** has been integrated in a 65nm CMOS process with metal-insulator-metal (MIM) capacitors, and operates from a 0.9V supply voltage. The performance comparison of the proposed modulator with the state-of-the-art low-power modulators is provided in this Chapter.

2.2 Amplifier Design

OTAs are the most critical block of the ΔΣ ADCs and consume most of the power [3]-[5]. For example, about 90% of the power in modulators presented in [3] and [4] are

analog power dissipation, which the major part belongs to the amplifiers. It is therefore worthwhile to study the low power OTA topologies and the optimal analog performance parameters for power optimization.

2.2.1 OTA Requirements

The main requirements for the OTA are dc gain, gain-bandwidth product (GBW) and output swing. OTAs are the core analog circuits of the ΔΣ modulators. Particularly, the first OTA determines the overall modulator performance and thus consumes the major part of the power. To minimize the power, optimal analog performance parameters (gain and GBW) need to be determined. Figure 2.1 shows the simulated SNR with respect to the dc gain and GBW of the first OTA in a second-order single-bit modulator at behavioral level. The minimum gain and GBW to obtain more than 90dB SNR is about 35dB and 1.2MHz, respectively [2]. This minimum requirement is drawn only from the SNR point of view. While considering high power supply rejection ratio (PSRR), good distortion performance, and robust operation in the presence of process-voltage-temperature (PVT) variation, enough margin has to be placed for the minimum gain and GBW.

2.2.2 OTA Topology Selection

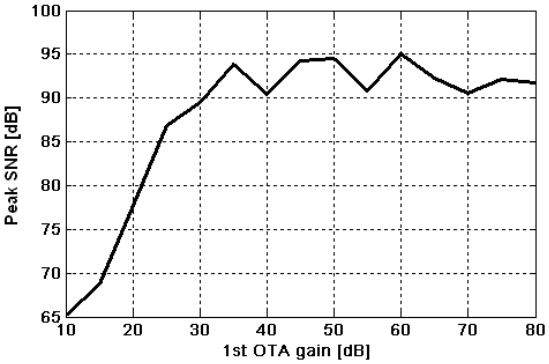
The determining factors for the amplifier to be used in the low-power modulator include power-efficiency, low-voltage operation, dc gain and GBW, voltage swing, etc.

In terms of power-efficiency it is always beneficial to have lower number of current branches. As a result, the single-stage topology like the telescopic cascode, folded cascode, or current-mirror OTA is preferred to the multi-stage topology. The multi-stage OTA, on the other hand, requires large capacitors for frequency compensation, which increases the total power consumption.

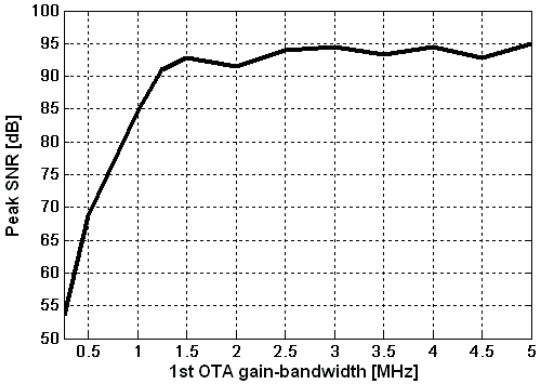
The voltage swing is of great importance for obtaining the required dynamic range (DR) in low-voltage modulator design in nanometer CMOS processes. The importance of the output swing can be clearly seen in the following equation:

$$DR = \frac{P_{in,\max}}{P_{kT/C}} = \frac{V_{in,\max}^2 . OSR . C_S}{8kT} \tag{2.1}$$

where $V_{in,max}$ is the maximum signal amplitude at the modulator input, C_S is the input sampling capacitor, OSR represents the oversampling ratio, k denotes the Boltzmann constant, and T is the absolute temperature. The DR is directly proportional to the output swing. The output swing can determine the modulator reference voltage, the size of the sampling capacitor, and finally the power consumption [3]. An OTA topology that can provide rail-to-rail output swing is absolutely required in low-voltage low-power designs. Due to the limited headroom, cascode topologies such as folded cascode [6]-[8] and telescopic cascode [9] amplifiers cannot be used in supply voltages below 0.6V. Therefore, to acquire the necessary gain a two-stage topology, either Miller [10] or load compensated [2], must be chosen. The latter one is preferred for medical applications because it avoids additional power consumption due to driving the Miller



(a)



(b)

Figure 2.1: SNR variation versus the first OTA's (a) dc gain and (b) GBW. The GBW simulations are done with the gain set to 50dB [2].

capacitor. The detailed power analysis of the commonly used amplifier topologies will be discussed in details in section 2.2.3.

2.2.3 OTA Power Analysis

The ΔΣ ADCs have been extensively investigated and developed with respect to the OTA's nonidealities such as finite DC gain, finite GBW, limited slew-rate (SR), and thermal noise [11]-[13]. In this subsection, however, we reconsider the power efficiency aspect of the mostly used OTA topologies in the low-power domain.

Consider the two-stage load-compensated OTA, shown in Fig. 2.2a. Assume that the non-dominant pole due to the parasitic capacitance at node *x* is placed beyond 3×GBW so that a sufficient phase margin and hence closed loop stability can be achieved. The DC gain and GBW of the OTA in strong inversion regime can be expressed as:

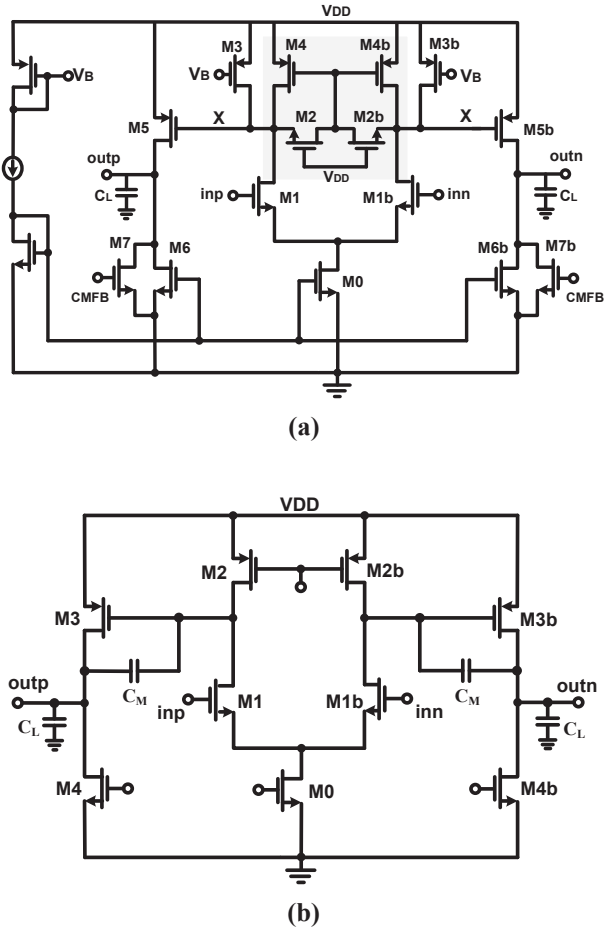


Figure 2.2: Two-stage amplifiers (a) load-compensated (b) Miller compensated [2].

$$A_0 = g_{m1}R_{out1} \times g_{m5}R_{out2} \tag{2.2}$$

$$GBW = \frac{g_{m1}g_{m5}R_{out1}}{2\pi C_L} \tag{2.3}$$

where g_{mi} is the transconductance of the ith transistor, R_{outi} is the output resistance in the ith OTA's stage, and C_L is the output load capacitance. It is assumed in the succeeding analysis that all transistors operate in moderate inversion region and that equal current draws in all amplifier's branches. Moreover, the g_{mi} can be expressed as given by (2.4):

$$g_{mi} = g_m = \frac{2I_{D1}}{(V_{GS} - V_{th})} \tag{2.4}$$

I_{D1} represents the current of each branch. Equal overdrive is assumed for all transistors. Substituting (2.4) into (2.3) and replacing $R_{out} = (\lambda.I_{D1})^{-1}$ we get

$$GBW = \frac{g_m^2 R_{out1}}{2\pi C_L} = \frac{g_m^2}{2\pi.C_L.(\lambda_n + |\lambda_p|).I_{D1}} \tag{2.5}$$

Combining (2.4) and (2.5), the total current drawn by a load-compensated two-stage OTA, $I_{2S\text{-}LC}$, can be expressed as:

$$I_{2S-LC} = 4 \times I_{D1} = GBW.\pi.(V_{GS} - V_{th})^2.(\lambda_n + |\lambda_p|).(2C_L) \tag{2.6}$$

The terms $(V_{GS}\text{-}V_{th})^2$ and $(\lambda_n + |\lambda_p|)$ in (2.6) clearly indicate that the overall current can be reduced significantly in moderate inversion region with $V_{GS}\text{-}V_{th} \approx 0.05\text{-}0.1$V and $\lambda_n + |\lambda_p| << 1$.

Similarly, for the Miller OTA shown in Fig. 2.2b, with the same GBW, overdrive voltage and load capacitor C_L, the total current can be derived as follows [3]:

$$GBW = \frac{g_{m1}}{2\pi C_M} \tag{2.7}$$

C_M is the Miller compensation capacitance. Combining (2.4) with (2.7) gives

$$I_{D1} = GBW.\pi.(V_{GS} - V_{th}).C_M \tag{2.8}$$

The non-dominant pole due to the load capacitance C_L has to be placed beyond 3×GBW to attain safe phase margin as given by (2.9)

$$\frac{g_{m4}}{2\pi(C_M + C_L)} = 3.GBW \tag{2.9}$$

This condition gives

$$I_{D4} = GBW.\pi.(V_{GS} - V_{th}).(3C_M + 3C_L) \tag{2.10}$$

Therefore, combining (2.8) with (2.10) will result in

$$I_{Miller} = 2 \times (I_{D1} + I_{D4}) = GBW.\pi.(V_{GS} - V_{th}).(8C_M + 8C_L). \tag{2.11}$$

The factor 2 accounts for the differential circuit realization. Several differences can be identified between (2.6) and (2.11). Equation (2.11) also demonstrates that an extra power can be dissipated for driving the two Miller capacitances in the Miller OTA shown in Fig. 2.2b.

Similarly, for the single-stage OTA shown in Fig. 2.3, with the same GBW, overdrive voltage and load capacitor C_L, the total current can be derived as follows [3]:

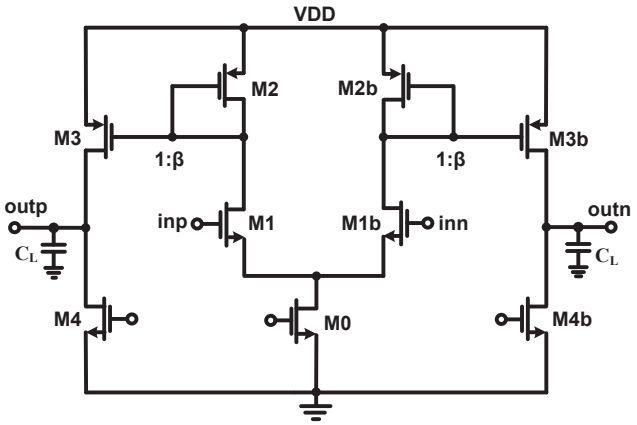


Figure 2.3: The single-stage current-mirror OTA.

$$GBW = \frac{\beta.g_{m1}}{2\pi C_L} \tag{2.12}$$

where β is the mirrored current ratio. Combining (2.4) with (2.12) gives

$$I_{D1} = GBW.\pi.(V_{GS} - V_{th}).\frac{C_L}{\beta} \tag{2.13}$$

The current at the output branch is

$$I_{D3} = \beta.I_{D1} \tag{2.14}$$

Therefore, the total current of the current mirror OTA is

$$I_{CM} = 2\times(I_{D1} + I_{D3}) = GBW.\pi.(V_{GS} - V_{th}).(2C_L + \frac{2C_L}{\beta}). \tag{2.15}$$

In a similar manner, the current expressions of the telescopic and folded cascode topologies can be derived, as given in Table 2-1.

TABLE 2-1: FUNDAMENTAL BOUND FOR CURRENT CONSUMPTION OF VARIOUS AMPLIFIER TOPOLOGIES.

Topology	Total Current
Two-Stage Load-Compensated (2.6)	$GBW.\pi.(V_{GS}-V_{th})^2.(\lambda_n+\lvert\lambda_p\rvert).(2C_L)$
Two-Stage Miller (2.11)	$GBW.\pi.(V_{GS}-V_{th}).(8C_M+8C_L)$
Single-Stage Current-Mirror (2.15)	$GBW.\pi.(V_{GS}-V_{th}).(2C_L+2C_L/\beta)$
Single-Stage Telescopic Cascode	$GBW.\pi.(V_{GS}-V_{th}).(2C_L)$
Single-Stage Folded Cascode	$GBW.\pi.(V_{GS}-V_{th}).(4C_L)$

As clearly seen from the Table 2-1, the two-stage load-compensated OTA can achieve the best power-efficiency compared to other OTA topologies, due to its advantage in low bias current and low speed of the target medical applications. Since the bias current is low (~200nA) in this OTA, the output resistance is inherently high and the dominant pole due to the C_L is then located at very low frequency with a minimal load capacitor value, 2pF for the first OTA in a second-order modulator in [2]. Therefore, the load compensation is preferred to the Miller compensation in this application as it prevents additional power for driving the Miller capacitor. It should be noted that although the current-mirror OTA (Fig. 2.3) is a single-stage topology, it consumes more power than the two-stage load-compensated topology. This can be explained in the following manner. The current ratio of the load-compensated OTA to the current mirror amplifier can be given as

$$\frac{I_{2S-LC}}{I_{CM}} = (V_{GS} - V_{th}).(\lambda_n + |\lambda_p|)\frac{2C_L}{2C_L + 2C_L/\beta}. \tag{2.16}$$

The last term is approximately one as β is relatively large, but the term $(V_{GS}\text{-}V_T)\times(\lambda_n + |\lambda_p|)$ is adequately smaller than one.

2.2.4 Comparison of OTA Topologies

The choice of amplifier topology plays a key role in low-voltage, low-power integrator design. The most important merits of the five amplifier topologies, attracted to the low-power modulator designs, are examined in this subsection: two-stage load-compensated, two-stage Miller (class-A), single-stage current-mirror, telescopic cascode, and folded cascode. The designs, analyses and simulation results can be found in details in **Paper 2** [1]. The power analysis and comparison were carried out in section 2.2.3, and summarized in Table 2-1. Here, the focus of the comparison is mainly on GBW, thermal noise, and output swing. The comparison results are summarized in Table 2-2.

The folded cascode OTA, shown in Fig. 2.4a, features a low output swing and is somewhat noisier than the others. The telescopic cascode amplifier, shown in Fig. 2.4b, provides the lowest output swing amongst different topologies, due to stacking five transistors. The two-stage load-compensated amplifier provides higher power-efficiency, rail-to-rail output swing, and minimal C_L for the balanced GBW and phase margin. The fundamental FOM of this OTA can be expressed as:

$$FOM_{2S-LC} = \frac{GBW \times C_L}{I_{2S-LC}} = \frac{1}{2\pi.(V_{GS} - V_{th})^2.(\lambda_n + |\lambda_p|)}. \tag{2.17}$$

2.3 Traditional ΔΣ Modulator Topology

The amplifier as a critical building block of the ΔΣ ADC was presented in section 2.2 in terms of performance requirements for various topologies. The power analysis and comparison among popular low-power topologies were explained in brief as well.

TABLE 2-2: COMPARISON OF THE KEY PERFORMANCE METRICS OF VARIOUS AMPLIFIER TOPOLOGIES.

Topology	GBW (ω_u)	Thermal Noise (differential)	Output Swing (single-ended)
Two-Stage Load-Compensated	$g_{m1}^2 R_{out1} / C_L$	$8kT\gamma/g_{m1}(1+g_{m3}/g_{m1})$	$V_{DD} - 2\times V_{DSAT,min}$
Two-Stage Miller Class-A	g_{m1}/C_M	$8kT\gamma/g_{m1}(1+g_{m2}/g_{m1})$	$V_{DD} - 2\times V_{DSAT,min}$
Single-Stage Current-Mirror	$\beta g_{m1}/C_L$	$8kT\gamma/g_{m1}(1+g_{m2}/g_{m1})$	$V_{DD} - 2\times V_{DSAT,min}$
Single-Stage Telescopic Cascode	g_{m1}/C_L	$8kT\gamma/g_{m1}(1+g_{m4}/g_{m1})$	$V_{DD} - 5\times V_{DSAT,min}$ [a]
Single-Stage Folded Cascode	g_{m1}/C_L	$8kT\gamma/g_{m1}(1+g_{m3}/g_{m1}+g_{m2}/g_{m1})$	$V_{DD} - 4\times V_{DSAT,min}$

(a) The output swing is one V_{DSAT} lower than that of folded cascode because of the tail current source.

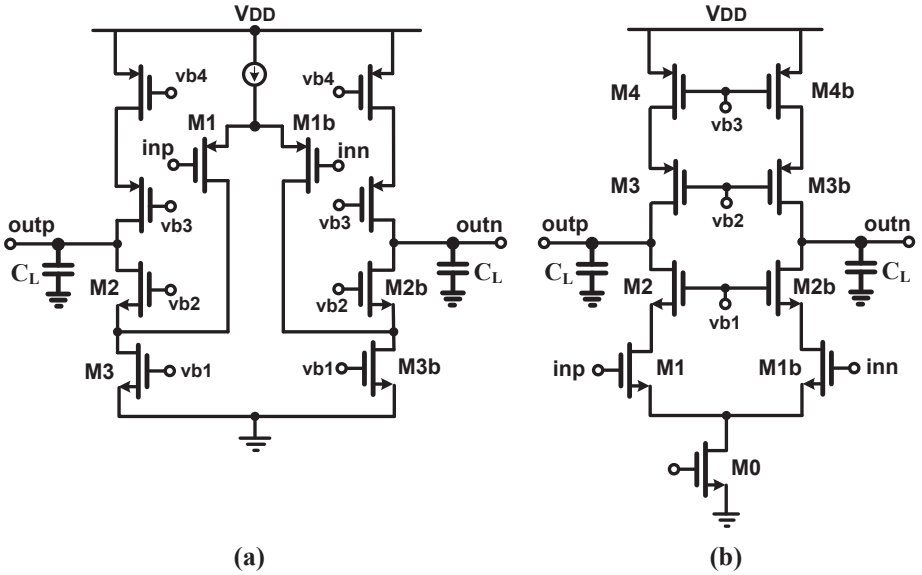


Figure 2.4: (a) Folded cascode OTA (b) Telescopic cascode OTA.

In this section, the single-loop single-bit traditional ΔΣ modulator topology is introduced. The term *traditional* is frequently used in this text in order to identify this

topology from the full feedforward topology, employed in the modulators presented in **Paper 5** and **7**. There are several degrees of freedom in the ΔΣ modulator design space, such as the oversampling ratio, number of quantization bits, and modulator order, which will be discussed in sections 2.3.2-2.3.4.

2.3.1 Single-Bit ΔΣ Modulator

First-order, second-order, and third-order modulator architectures are investigated with respect to the signal transfer function (STF) and noise shaping property.

The block diagram of a first-order single-loop modulator is shown in Fig. 2.5a. The single-bit quantizer can be replaced by a gain factor g and the added white quantization noise E. The factor g represents the equivalent gain of the quantizer [13]. The ability of noise shaping can be improved by increasing the order of loop filter, but higher-order filters are more prone to loop instability. Therefore, coefficients, a_i, are inserted inside the loop in order to stabilize the entire modulator. The signal and noise transfer functions (NTF) of the first-order modulator can be derived in z-domain as follows:

$$STF_1 = \frac{Y}{X}(z) = \frac{a_1 g.z^{-1}}{1+(a_1 g-1)z^{-1}} \tag{2.18}$$

$$NTF_1 = \frac{Y}{E}(z) = \frac{1-z^{-1}}{1+(a_1 g-1)z^{-1}}. \tag{2.19}$$

The denominator of both STF and NTF can be controlled by $a_1 g$-1 factor in order to eliminate the term $(a_1 g\text{-}1).z^{-1}$, resulting in STF = z^{-1} and NTF = 1- z^{-1}, respectively, for the ideal first-order noise shaping. The ideal STF is only one delay, i.e z^{-1}, while the ideal NTF is a first-order high-pass filter. The optimal loop coefficient obtained from the behavioral simulation is $a_1 = 0.7$ and the quantizer gain g is considered to be 0.9.

The block diagram of a second-order single-loop modulator is shown in Fig. 2.5b. The STF and NTF of the second-order modulator can be derived in z-domain as follows:

$$STF_2 = \frac{Y}{X}(z) = \frac{a_1 a_2 g.z^{-2}}{1+(a_2 g-2)z^{-1}+(1+a_1 a_2 g-a_2 g)z^{-2}} \tag{2.20}$$

$$NTF_2 = \frac{Y}{E}(z) = \frac{(1-z^{-1})^2}{1+(a_2 g-2)z^{-1}+(1+a_1 a_2 g-a_2 g)z^{-2}}. \tag{2.21}$$

The coefficients $a_1 = 0.23$ and $a_2 = 0.3$ are the optimal signal and feedback scaling factors obtained from the behavioral simulations. Basically, the loop coefficients are determined from the loop stability constraint, the maximum linear swing of the integrators, and the required SNR. It is worthwhile to recall that by setting $a_1 a_2 g = 1$ and $a_2 g = 2$, the transfer functions of STF = z^{-2} and NTF = $(1\text{-}z^{-1})^2$ can be achieved for an ideal second-order noise shaping. For a practical realization, however, further sacling of the loop coefficients is imposed by the robust and stable modulator operation and the

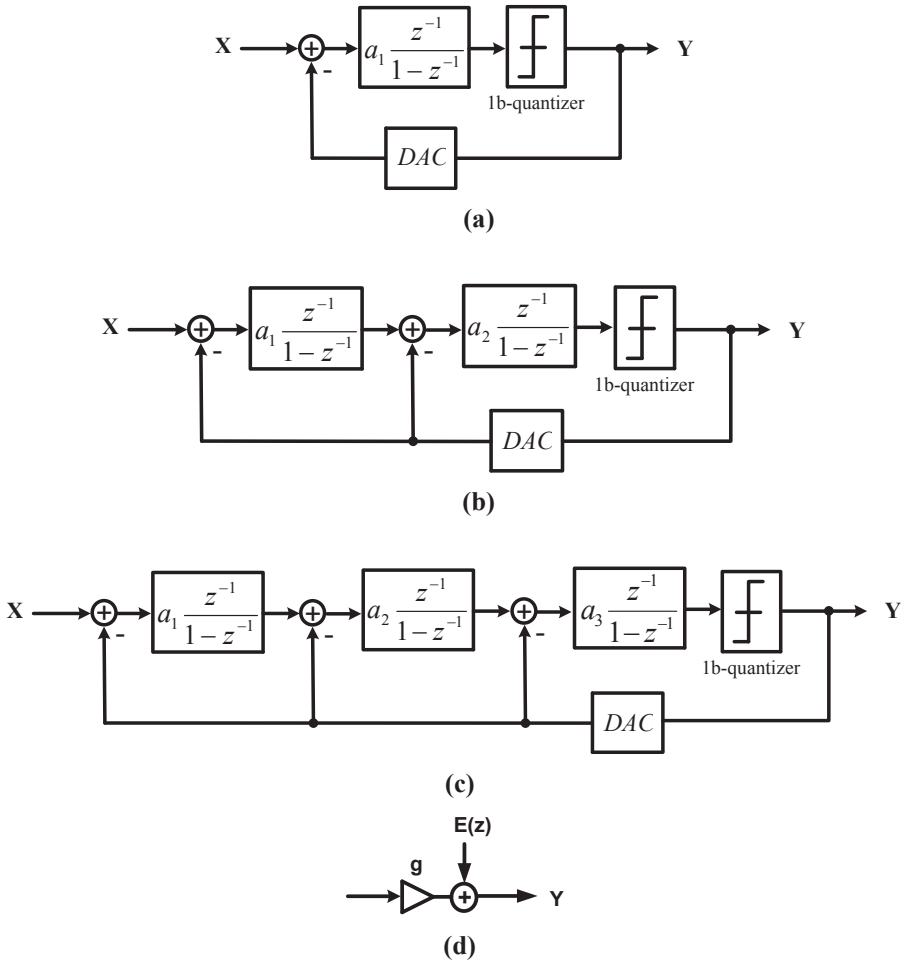


Figure 2.5: Traditional single-loop modulator topology (a) first-order (b) second-order (c) third-order, (d) the linearized model of a single-bit quantizer. Each integrator's transfer function represents the ideal active integrator and a loop coefficient a_i.

necessary linearity performance. Similarly, the STF and NTF of the third-order modulator shown in Fig. 2.5c can be expressed as given by (2.22) and (2.23). Optimal coefficients a_1 = 0.23, a_2 = 0.3, and a_3 = 0.4 are obtained from a large number of behavioral simulations.

$$STF_3 = \frac{Y}{X}(z) = \frac{a_1 a_2 a_3 g.z^{-3}}{1 + k_1 z^{-1} + k_2 z^{-2} + k_3 z^{-3}} \tag{2.22}$$

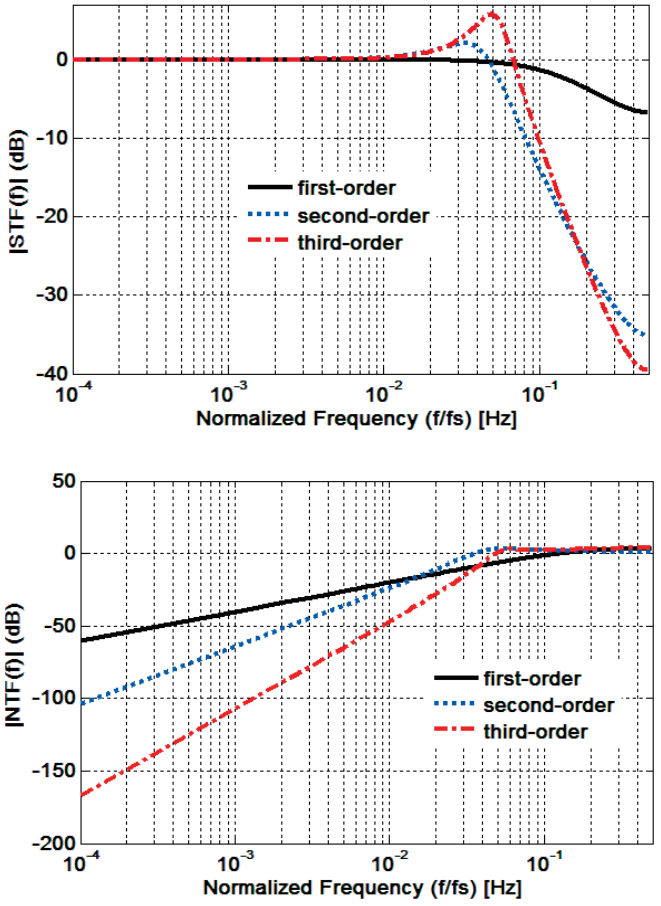


Figure 2.6: The magnitude of the STFs and NTFs of the first-order, second-order and third-order modulators.

$$NTF_3 = \frac{Y}{E}(z) = \frac{(1-z^{-1})^3}{1+k_1 z^{-1}+k_2 z^{-2}+k_3 z^{-3}}. \tag{2.23}$$

with $k_1 = a_3g - 3$, $k_2 = a_2a_3g - 2a_3g + 3$, and $k_3 = a_1a_2a_3g - a_2a_3g + a_3g - 1$.

It can be clearly seen from Fig. 2.6 that three modulators have a unity gain STF at lower frequencies, and the NTF of higher-order modulators become steeper in the signal band, meaning a higher ability of in-band quantization noise shaping. Obviously, in a first-order modulator the NTF has a slope of 20dB/dec in low frequencies, while the slope of the NTFs in the second-order and third-order modulators is 40 and 60dB/dec,

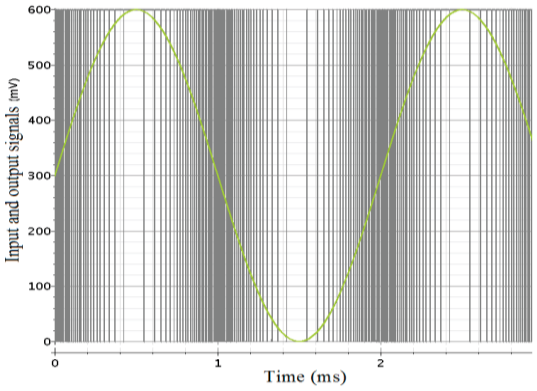


Figure 2.7: Input and output waveforms of a second-order single-loop modulator with single-bit quantization. A full-scale input signal (0dB) was applied. The supply voltage and reference voltage were set to 0.6V.

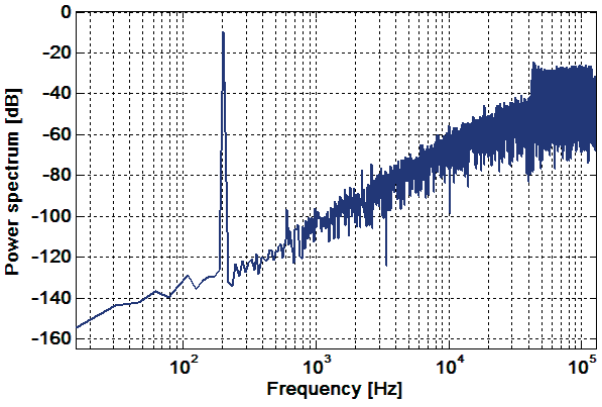


Figure 2.8: Output power spectrum of a second-order single-loop single-bit modulator oversampled by 256 with 203Hz input and -3.52dBFS amplitude.

respectively. As illustrated in Fig. 2.6 by the NTFs magnitude, first-, second-, and third-order high-pass filtering are achieved due to the noise shaping property of the delta-sigma modulator.

Behavioral simulations were carried out to find the optimal loop coefficients for acquiring both loop stability and the required SNR. In this model, the gain and GBW of the OTAs in a second-order modulator were set to 40dB and 1.8MHz, respectively. The gain and GBW requirements were drawn from Fig. 2.1. Figure 2.7 shows the

waveforms of a full scale input and related output for a single-bit modulator. With loop coefficients (a_1,a_2) = (0.23,0.3) and sampling frequency of 256kHz, the modulator can obtain over 90dB SNR. The output power spectrum is shown in Fig. 2.8 for a 203Hz and -3.52dBFS sinusoidal input.

2.3.2 Oversampling

As seen from (2.19), (2.21) and (2.23), the ideal NTF of an n-th order ΔΣ modulator can be expressed as $(1-z^{-1})^n$. Therefore, the total quantization noise power inside the signal band ($-f_B$ to f_B) is:

$$\begin{aligned} P_e &= \int_{-0.5fs}^{0.5fs} S_e(f).|H_e(f)|^2 df = \\ &= \int_{-fB}^{fB} \frac{\Delta^2}{12 f_s}.|1-z^{-1}|^{2n} df = \\ &= \int_{-fB}^{fB} \frac{\Delta^2}{12 f_s}.(\frac{2\pi f}{f_s})^{2n} df = \\ &= \frac{\Delta^2}{12}.\frac{1}{\pi(2n+1)}(\frac{\pi}{M})^{2n+1} \end{aligned} \tag{2.24}$$

In above calculation, it is assumed that $f/f_s << 1$, where f_s is the sampling frequency. Δ is the quantization step, and is equal to $V_{FS}/2^N$, where V_{FS} is the full scale signal. The power spectral density (PSD) of the quantization noise is white, and evenly distributed within $\pm f_s/2$. M is the oversampling ratio. The signal power is:

$$P_S = \frac{(\frac{V_{FS}}{2})^2}{2} = \frac{V_{FS}^2}{8} = \frac{2^{2N}.\Delta^2}{8} \tag{2.25}$$

Therefore, the theorethical peak SNR can be expressed as

$$SNR = \frac{P_S}{P_e} = \frac{3\pi}{2}.(2^B-1)^2.(2n+1).(\frac{M}{\pi})^{2n+1}. \tag{2.26}$$

B is the number of bits in the quantizer. It is evident from (2.26) that the modulator SNR can be ebhanced by (2n+1).3dB by each doubling the oversampling ratio M. However, M is restricted by the clock speed and power consumption. The higher the M is, the larger SNR can be achieved according to (2.26). On the other hand, the higher sampling clock frequency increases the power consumption in the digital circuits. Moreover, the higher sampling frequency also increases the bandwidth requirements in the amplifiers for sufficient settling purpose. As a consequence, the analog power consumption also increases. It is therefore desirable to maintain a lower M. Since in the target medical applications the signal bandwidth is quite low (less than 500Hz), the increase in M would not cause an unbearable increase in the clock frequency. For instance, with M = 250 the maximum sampling frequency f_s will be 250×2f_B = 250kHz.

2.3.3 Single-Bit versus Multi-bit Modulator

As seen from (2.26), increasing the number of bits in the quantizer enhances the SNR significantly. For each additional bit, the SNR increases by 6dB. The use of a multi-bit quantizer also improves the loop stability [11], hence the loop coefficients can be enlarged, resulting in more powerful noise shaping ability. The main drawback of using multi-bit quantizer is that the nonlinearity of multi-bit DAC directly affects the linearity of the converter. The multi-bit quantization is avoided in the presented modulator (section 2.5) because the internal DAC usually requires dynamic element matching (DEM) [11], [12] or other complementary linearization techniques that increase the hardware complexity and hence the power consumption.

2.3.4 Order of Loop Filter

The order of loop filter n can increase the modulator SNR according to (2.26). However, when higher-order loop filters are used, the loop stability problem becomes the primary concern. As a consequence, smaller loop coefficients are introduced to ensure the loop stability, which compromises the noise shaping ability. This will be discussed more in section 2.4. With the insertion of loop coefficients a_i the theoretical SNR obtained in (2.26) can be reduced to [12]

$$SNR = SNR_{Ideal}.(g.\prod_{i=1}^{n} a_i). \tag{2.27}$$

where g is the quantizer gain. Normally, the product of the coefficients is less than unity. On the other hand, increasing the order of filter also increases the hardware complexity. Clearly, there are trade-offs among the modulator order, oversampling ratio, and power consumption.

2.4 Shaping of Circuit Noise

In the previous section, the noise shaping property of the in-band quantization-noise in a ΔΣ ADC was discussed. This noise shaping property also attenuates the baseband circuit noise which is introduced in the forward path of modulator after the first stage. This part concentrates on the analysis of circuit noise. To do so, first a generalized linear model of a third-order single-loop modulator is demonstrated, as shown in Fig. 2.9, in which all noise sources are specified. The baseband output signal can be expressed as:

$$Y \approx X + Q_1 + \frac{Q_2}{H_1} + \frac{Q_3}{H_1 H_2} + \frac{Q_C}{H_1 H_2 H_3} + \frac{Q_n}{g H_1 H_2 H_3} \tag{2.28}$$

where H_1, H_2 and H_3 are the integrators transfer functions, Q_1, Q_2 and Q_3 are the input-referred circuit noise injected at the input to each stage, respectively, while Q_C and Q_n denote the comparator input-referred noise and the quantization noise. The g is the equivalent gain of the quantizer. As illustrated in Fig. 2.5, the ideal transfer function of

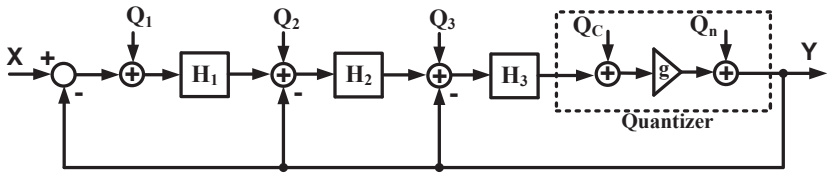


Figure 2.9: Linear model of the single-loop third-order ΔΣ modulator.

each integrator can be written as

$$H_i(z) = a_i \frac{z^{-1}}{1-z^{-1}}, i = 1,2,3 \tag{2.29}$$

where infinite DC gain and bandwidth are assumed for each amplifier in the integrator. By substituting (2.29) into (2.28), the equation (2.28) can be written as:

$$Y \approx X + Q_1 + \frac{1-z^{-1}}{a_1 z^{-1}} Q_2 + \frac{(1-z^{-1})^2}{a_1 a_2 z^{-2}} Q_3 + \frac{(1-z^{-1})^3}{a_1 a_2 a_3 z^{-3}} Q_C + \frac{(1-z^{-1})^3}{g a_1 a_2 a_3 z^{-3}} Q_n. \tag{2.30}$$

Figure 2.10 illustrates how each source of circuit noise specified in Fig. 2.9 obtains noise shaping inside the loop filter. Obviously, comparator noise Q_C and quantization noise Q_n get the highest attenuation by the preceding filters H_1 to H_3, while Q_2 is only shaped (low-pass filtered) by a first-order high-pass filter $(1-z^{-1})/a_1$ and the circuit noise related to the first stage (i.e., Q_1) does not gain any shaping, and directly appears at the modulator output associated with input signal X. Therefore, in a high-resolution ADC design, the noise produced from the input stage is a limiting factor and special care needs to be taken. It is also interesting to see the effect of oversampling over the circuit noise components in the following. When the circuit noise is white, the power of the baseband noise can be obtained by integrating the input-referred noise over the signal bandwidth

$$P_{N-in} = \int_{-f_B}^{f_B} S_{Q_1}(f).\left|H_{Q_1}(f)\right|^2 df + \int_{-f_B}^{f_B} S_{Q_2}(f).\left|H_{Q_2}(f)\right|^2 df + \ldots \tag{2.31}$$

From (2.30), $|H_{Q1}(f)|^2 = 1$, $|H_{Q2}(f)|^2 = 2/a_1^2 \sin(\pi f/f_s)$ and so on. Solving the integral of (2.31) will result in

$$P_{N-in} = \frac{1}{M} P_{N1} + \frac{1}{a_1^2} \cdot \frac{\pi^2}{3M^3} P_{N2} + \frac{1}{a_1^2 a_2^2} \cdot \frac{\pi^4}{5M^5} P_{N3} + \frac{1}{g^2 a_1^2 a_2^2} \cdot \frac{\pi^4}{5M^5} P_{Qn} \tag{2.32}$$

where P_{N1}, P_{N2} and P_{N3} are the noise powers at the input to first, second and third integrators, respectively [13], while $P_{Qn} = \Delta^2/12$ is the quantization noise power. M is

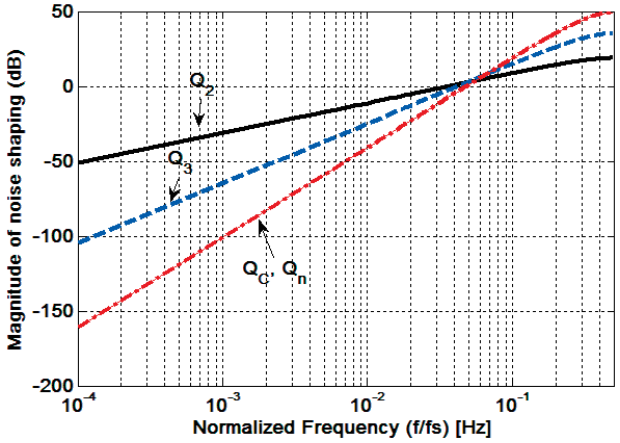


Figure 2.10: Circuit noise shaping of various noise sources injected at the input of the integrators in a third-order ΔΣ modulator.

the oversampling ratio (OSR) which is defined as $f_s/2f_B$ with f_s the sampling frequency and f_B the signal bandwidth. It is apparent from (2.32) that the circuit noise is attenuated by the oversampling. In particular, the noise contributions from the second and third stages are highly suppressed inside the loop with $1/M^3$ and $1/M^5$ factors. The (2.30) indicates the fact that the noise from the first integrator, i.e. Q_1, is not affected by the noise shaping phenomenon inside the loop filter, but it is affected by the oversampling, as can be seen from the first term in (2.32). For further clarification, the circuit noise of an experimental second-order ΔΣ modulator presented in [14] will be discussed in the subsequent section. The related circuit design and the experimental test results will be presented in section 2.5.

2.4.1 Circuit Noise Analysis

The two main sources of circuit noise are thermal noise and flicker noise (or 1/f noise) in MOS transistors. The equivalent input-referred power spectral density of a MOS transistor can be modeled as a voltage source between the gate and source terminals, and is given by

$$\frac{\overline{V_{n,in}^2}}{\Delta f} = \frac{4kT\gamma}{g_m} + \frac{K}{WLC_{ox}f}, \left[v^2 / Hz\right] \tag{2.33}$$

where k is the Boltzmann constant, T is the absolute temperature, K and γ are technology dependent factors, and g_m is the transconductance of the transistor.

For a second-order single-bit active modulator presented in [2] with $a_1 = 0.23$, $a_2 = 0.3$, $M = 250$, according to (2.32), the baseband noise at the input of the second integrator is attenuated by 10^{-3} relative to the noise introduced at the input of the first

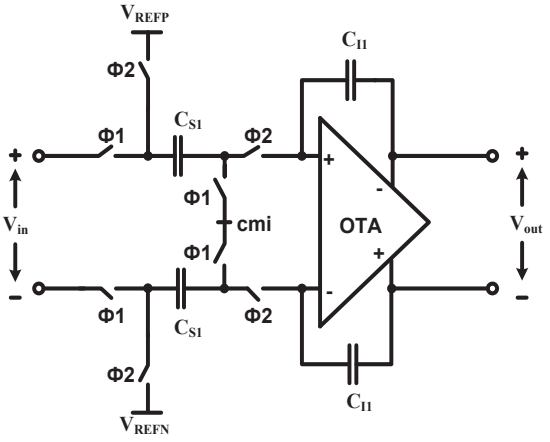


Figure 2.11: Fully differential input stage's switched-capacitor integrator.

integrator. Therefore, the total input-referred noise can be approximated by the first integrator noise. The main sources of noise at the input of the first integrator are thermal noise due to the sampling and DAC switches and the input-referred noise from the OTA circuit. For the time being, it is assumed that the OTA has infinite gain and GBW, and that there are no parasitic capacitances. Therefore, the only source of noise is due to thermal noise generated in sampling switches. There are four paths through which noise is sampled in C_{S1} during Φ_1 and Φ_2 clock phases, as shown in the integrator of Fig. 2.11. The total low frequency thermal noise power introduced at the input of the first stage is given by [15]

$$P_{kT/C} = \frac{4kT}{C_{S1}} \tag{2.34}$$

Another switching noise, uncorrelated to (2.34), is sampled into integrating capacitor C_{I1} in Φ_2 clock phase. When referring to input by dividing it to the integrator gain, a second (thermal) noise term appears

$$P_{kT/C} = \frac{2kT}{C_{I1}}\left(\frac{C_{I1}}{C_{S1}}\right)^2 \tag{2.35}$$

Another noise contribution is added by the OTA and can be derived at the output as follows. The open loop transfer function of the OTA approximated as a single-pole system can be given as $A(s) = A_0/(1+s/\omega_p) \approx \omega_u/s$ with DC gain A_0, pole ω_p and unity-gain frequency ω_u. The closed-loop transfer function is:

$$A_{CL}(s) = \frac{A(s)}{1+\beta A(s)} = \frac{1}{\beta}\cdot\frac{1}{1+s/\omega_{-3dB}} \tag{2.36}$$

with $\omega_{-3dB} = \beta\omega_u$. Neglecting the 1/f noise for the time-being (it will be discussed in the next section), for a two-stage load-compensated OTA shown in Fig. 2.2, the input-referred noise can be approximated as

$$\overline{V}_{ni}^2(f) = \frac{8kT}{g_{m1}}\gamma \tag{2.37}$$

Then, the noise power at the output V_{out} in Fig. 2.11 can be calculated as

$$P_{N-OTA} = \int_0^\infty V_{ni}^2(f).\left|A_{CL}(f)\right|^2 df = \frac{8kT}{g_{m1}}\gamma\int_0^\infty \frac{1}{\beta^2}\cdot\frac{1}{1+(f/f_{-3dB})^2}df$$

$$= \frac{8kT}{g_{m1}}.\gamma.\frac{1}{\beta^2}.\omega_{-3dB}.\frac{\pi}{2} \tag{2.38}$$

where β is the feedback factor, and ω_{-3dB} is the closed-loop bandwidth given by (2.39) and (2.40), respectively.

$$\beta = \frac{C_{I1}}{C_{S1}+C_{I1}} \tag{2.39}$$

$$\omega_{-3dB} = \beta\omega_u = \frac{C_{I1}}{C_{S1}+C_{I1}}\cdot\frac{g_{m1}}{2\pi.C_{Leff}}, C_{Leff} = \frac{C_{S1}.C_{I1}}{C_{S1}+C_{I1}} + C_C + C_{S2}(stage2) \tag{2.40}$$

Combining (2.38)-(2.40), and dividing the result by the squared integrator gain $(C_{S1}/C_{I1})^2$, the P_{N-OTA} given in (2.38) can be referred to input as

$$P_{N-OTA} = \frac{2kT}{C_{Leff}}.\gamma.\frac{1}{\beta}.(\frac{C_{I1}}{C_{S1}})^2. \tag{2.41}$$

Summing up the three noise sources given by (2.34), (2.35), and (2.41) will result in the approximated total thermal noise at the input to the first stage

$$P_{N1} \approx \frac{4kT}{C_{S1}} + \frac{2kT}{C_{I1}}(\frac{C_{I1}}{C_{S1}})^2 + \frac{2kT}{C_{Leff}}.\gamma.\frac{1}{\beta}.(\frac{C_{I1}}{C_{S1}})^2. \tag{2.42}$$

According to (2.32), the input-referred noise power is attenuated by the oversampling. As a consequence, $P_{N-in} = P_{N1}/M$. With $C_{S1} = 2$pF, $C_{I1} = 8.8$pF, $M = 250$, $kT = 4\times10^{-21}$, $\gamma \approx 1$, the total input-referred noise of -99.7dB is estimated. The in-band noise power is also calculated form *SpectreRF Pnoise*, which is equal to -96.3 dB (including 1/f noise).

To summarize, a general rule of thumb in a ΔΣ modulator design is that the kT/C noise, i.e. the first two terms in (2.42), and the amplifier thermal noise in the first stage constitute about 75% of the noise budget, whereas the quantization noise is only about 5% of the total noise [16].

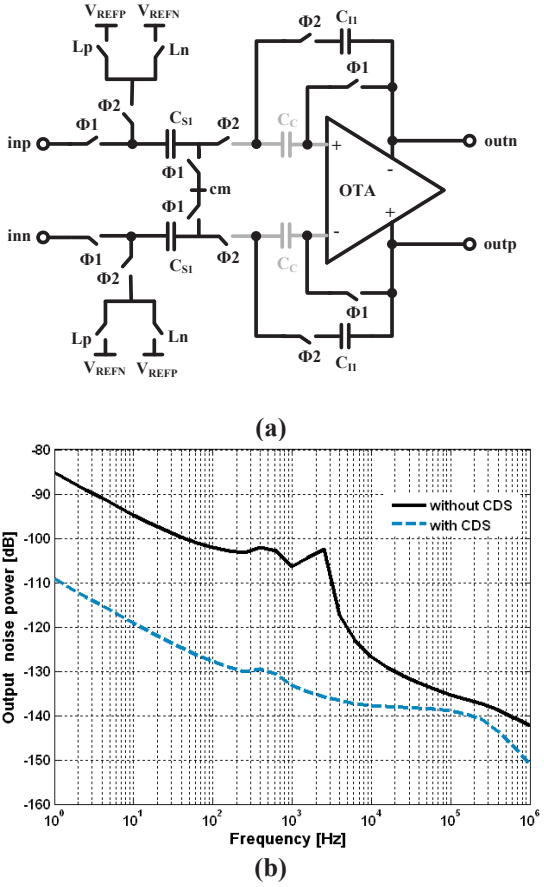


Figure 2.12: (a) The first stage integrator implemented with CDS technique for 1/f noise reduction (b) the output noise power with/without CDS technique.

2.4.2 Flicker Noise

In the noise expression derived in (2.42), the input-referred flicker noise of the OTA was neglected. A particular attention is given to the flicker noise here as it is important in low frequency applications. The 1/f noise is treated in different ways in various designs [2], [17], [18]. As shown by (2.33), the 1/f noise is inversely proportional to the device geometry. This noise in the first OTA can thus be reduced simply by increasing the size of the transistors in the input stage of the two-stage amplifier (Fig. 2.2). This approach was suitable in **Paper 1** [2] for obtaining SNR around 80dB. The same OTA was also integrated with correlated double sampling (CDS) technique [17], as shown in Fig. 2.12, to examine the impact of this technique in decreasing the 1/f noise. It is

apparent from the waveforms depicted in Fig. 2.12b that using CDS technique the 1/f noise at the output is largely reduced at the cost of area penalty, due to two C_C capacitors as large as 10pF. Also, the wideband thermal noise increases. The design in [2] avoids the usage of this approach because the 1/f noise was adequately suppressed by increasing the transistor size. As a result, the capacitive area penalty was prevented. Another approach to minimizing the flicker noise is chopper stabilization [17]. In this method, the input signal is modulated to a chopping frequency above the noise corner frequency of the OTA before the OTA flicker noise is injected to it. Subsequently, the output of the integrator is demodulated, recovering the input signal back to its original frequency.

2.5 Implementation of an Experimental Modulator

In this section, the system-level considerations, cicuit design, and experimental results of a second-order single-loop single-bit ΔΣ modulator implemented in a 65nm CMOS process are discussed (**Paper 1**). Prior to this, a short overview of existing low-power modulator techniques is explained.

2.5.1 Overview of Available Techniques

Many design efforts to date have been devoted to low-power modulator designs. As a consequence, innovative circuit thechniques have been developed to reduce the power consumption in traditional active ΔΣ converters, such as inverter-based modulator [5], [19], single-stage power-efficient amplifiers [3], [4], double-sampled integrator [20]-[22], and amplifier-sharing [23], [24]. Double-sampling technique, as a low-power solution in SC circuits, can provide twice the sampling frequency without increase in amplifier bandwidth requirement, but at the cost of more *kT/C* noise. The designs in [3] and [4] employ single-stage current mirror amplifier, shown in Fig. 2.3, to reduce the analog power. Inverter as an amplifier enables simple and low-voltage integrator design. Also class-C operation can provide low power design, in which the inverter's operating supply voltage can be less than the sum of the threshold voltages of both NMOS and PMOS transistors. The area of the modulator can be reduced significantly. The modulators in [23] and [24] make use of only one amplifier, and share it among the integrators in the time domain in order to save significant power and area.

2.5.2 Modulator Architecture

2.5.2.1 System-Level Considerations

There exist several degrees of freedom in the ΔΣ modulator design space, such as the modulator order, the OSR, and the number of quantization bits. With minimum power consumption as a key design goal, the objective is to prevent any circuit overhead and complexity. Targeting about 12-bit resolution, the system-level simulations show that a second-order single-loop topology is adequate for the required SNR and convenient to minimize circuit complexity, hence the power and area. The modulator exploits intrinsically linear single-bit quantizer. The multi-bit quantization is therefore avoided

because the internal multi-bit DAC normally requires DEM [11], [12] or data weighted averaging (DWA) logic [25], that increase the hardware complexity, hence the power consumption. Since the signal bandwidth is quite low (≤ 500 Hz), a relatively high OSR can be used without unbearably increasing the sampling frequency, which makes the thermal noise contribution to the signal band very low. This also decreases the size of capacitors in the first integrator and consequently the power consumption. With an OSR of 250 in the system-level simulation when both OTAs gain is set to 35dB, the second-order single-bit modulator achieves more than 90dB SNR, providing more than 10dB margin for 12-bit accuracy. Figure 2.5b shows the modulator architecture, and Fig. 2.8 shows the output spectrum.

2.5.2.2 Modulator Order and OSR

In this section, the trade-offs between the OSR and the order of loop filter with respect to power consumption and modulator performance are discussed. The first-order ΔΣ modulator suffers from the idle tones [11], and is naturally rejected. Also, it requires very high OSR (or sampling frequency) to meet the target SNR, which results in high power dissipation, particularly in digital blocks. In low-power design, it is beneficial to use second-order modulator topology due to its simplicity. As an alternate option, third-order topology with approximately half OSR can be used at the cost of one extra integrator, one extra common-mode feedback (CMFB) circuit in the OTA, whereas amplifiers with half GBW can be replaced in turn.

Compared to a second-order topology, a third-order (or higher-order) topology makes use of a lower OSR (or sampling clock frequency) for a given SNR. It should be pointed out that in a third-order (or higher-order) structure, the more strict scaling of loop cofficients is required to maintain the loop stability, therefore according to (2.27) the SNR is compromised in practical implementations.

For *kT*/*C*-dominated modulators as particular case (e.g., high-resolution ADCs), the sampling capacitor value, C_{S1}, in the first stage shown in Fig. 2.11 can be expressed as:

$$C_{S1} = \frac{8kT.DR}{M.V_{FS}^2} \tag{2.43}$$

where *DR* is the dynamic range, *M* is the oversampling ratio, and V_{FS} is the amplitude of a full-scale input. For a given *DR*, using half OSR in a third-order modulator translates into twice the sampling capacitor. With constant integrator gain ($a_1 = C_{S1}/C_{I1}$) in both second- and third-order topologies, the integrating capacitor, C_{I1}, also doubles, which enhances the effective capacitive loading of the OTA, hence the power consumption.

2.5.2.3 Low-Power Design Considerations

To reduce the overall power consumption, several architectural and circuit-level solutions are exploited as follows. As simplicity both in architecture and circuit building blocks is useful for ultra-low-power design, a single-loop topology with one-bit quantization is adopted. Lower-order modulator also simplifies the design of the succeeding digital decimation filter, thereby reducing the total converter power [11], [13].

The usage of low-V_{th} devices gives adequate overdrive voltage in the design of switches at the cost of more leakage or harmonic distortions [4], while removing the demand for additional circuits to boost the clock level. Low-V_{th} transistors also enable a simpler amplifier design, which mitigates the problem of low available headroom in 0.9V supply. In contrast, the digital circuits benefit from high-V_{th} transistors in order to limit the leakage consumption in the target low speed application.

Beside the choice of modulator topology, the selection of the circuit building blocks, including OTA, comparator, CMFBs, and clock generation circuitry, is also very important in power reduction (Section 2.5.3). Moreover, design efforts have been made to find the optimal analog performance parameters (e.g., dc gain and gain-bandwidth of the OTAs) in a wide optimization space. This was previously discussed in section (2.2.1).

2.5.3 Circuit Building Blocks

The modulator circuit and building blocks are discussed in this section. The OTA, the most power consuming block of modulator, was explained in section 2.2 in details. In particular, the power analysis of several amplifier topologies was accomplished in section 2.2.3, showing the two-stage load-compensated OTA a suitable topology for low speed medical applications. Figure 2.2a showed the OTA circuit.

2.5.3.1 Complete Modulator Circuit

The complete modulator circuit is shown in Fig. 2.13. Two-stage load-compensated OTAs (Fig. 2.2a) were used in the integrators. As the second integrator is less critical, the corresponding amplifier performance parameters were scaled down to minimize the analog power. Given 90dB SNR, the first sampling capacitor value, C_{S1}, is determined from (2.43) with a 0.6V reference voltage (or full scale input) and OSR equal to 250. With extra noise margin C_{S1} is calculated to be 2pF. Other capacitors are calculated to meet the loop coefficients (a_1, a_2) = (0.23, 0.3) illustrated in Fig. 2.5b. The DAC reference voltage is set to 0.6V, which is defined by V_{REFP} = 0.75V and V_{REFN} = 0.15V, respectively, in Fig. 2.13. The integrators input and output common-mode levels are set to 0.45V for maximum output swing.

2.5.3.2 Single-bit Quantizer and Latch

The single-bit quantizer is implemented by using a dynamic comparator and a SR-latch, as shown in Fig. 2.14. Since the comparator is a dynamic circuit, the modulator slow clock (250kHz) causes the leakage current to flow through the branches. To suppress this, high-V_{th} low-power devices of the used 65nm CMOS process are applied. The total power consumption of the comparator and latch is about than 10nW.

2.5.3.3 Clock Generation

On-chip clock generation is provided to produce two non-overlapping clocks with their delays from the external 250kHz sine wave [2]. As the size of switches is small, the total capacitive load that each clock output has to drive is very small. The estimated capacitive load of four clock outputs are 60, 40, 120, 120fF, respectively. Therefore, the

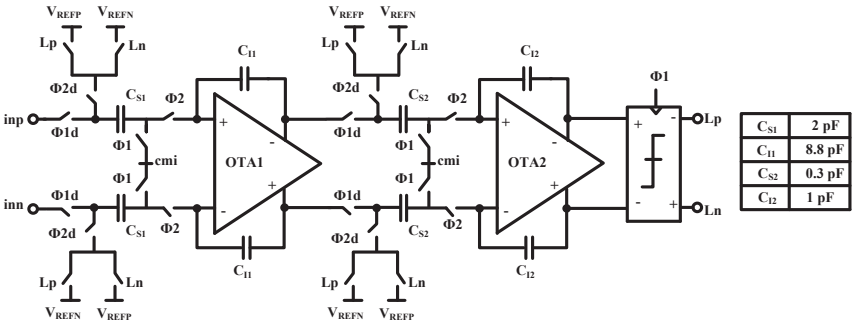


Figure 2.13: Schematic diagram of the implemented second-order single-bit modulator with two active integrators. The size of the main capacitors is included [2].

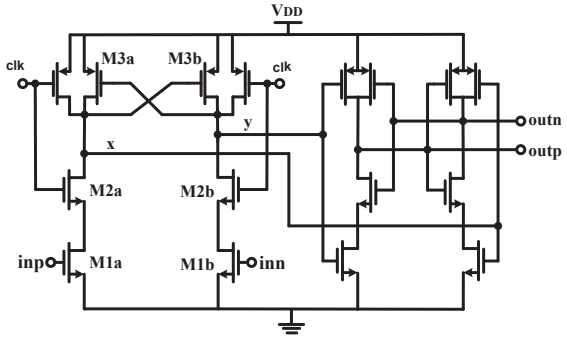


Figure 2.14: Dynamic comparator and SR latch using high-V_{th} low-power devices [2].

circuit logic gates are carefully sized and optimized for nano-watt range power consumption. High-V_{th} low-power devices with length L = 1.5µm are used to minimize the leakage currents.

2.5.4 Experimental Results

The prototype chip was fabricated in a 65nm CMOS technology. The chip micrograph is shown in Fig. 2.15. The modulator output data is captured by an oscilloscope, and then the decimation filtering and down-sampling are performed using Matlab. Figure 2.16 shows the measured power spectrum for a –4.0dBFS, 99Hz sinusoidal input. Figure 2.17 depicts the measured SNR and SNDR versus the differential input amplitude. The overall measured performance results are summarized in Table 2-3. The measured power breakdown by sources is shown in the diagram of Fig. 2.18. The analog power, including the integrators and reference voltages, composes 85% of the total power, whereas almost 50% of the total power is dissipated in the first

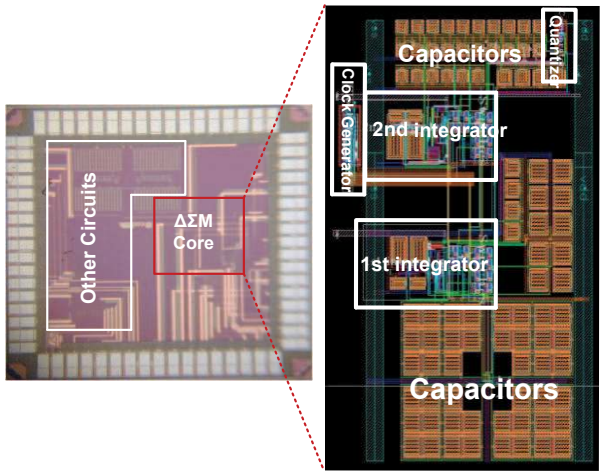


Figure 2.15: Chip micrograph and the layout details [2].

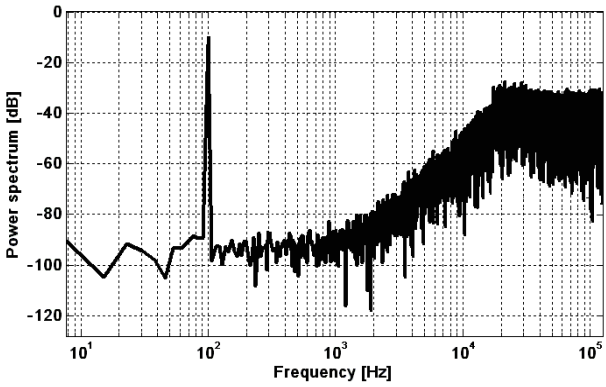


Figure 2.16: Measured output spectrum using a -4.0dBFS 99Hz input where 32768-point FFT were used [2].

integrator. It should be noted that the reference buffers necessary for the reference generation are not included in the power calculation, and so is for the modulators listed in the comparison Table 2-4.

2.6 Comparison of the Power Efficiency

The measured performance of the implemented modulator is compared to other delta-sigma modulators in Table 2-4. Two commonly used figure of merits (FOMs) are

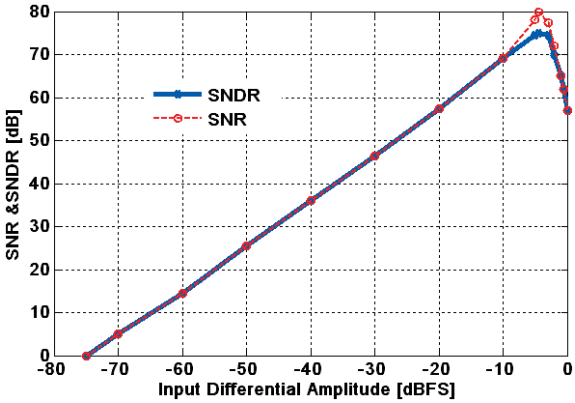


Figure 2.17: Measured SNR and SNDR versus differential signal amplitude. Below -40dBFS inputs, the SNR and SNDR values are extrapolated [2].

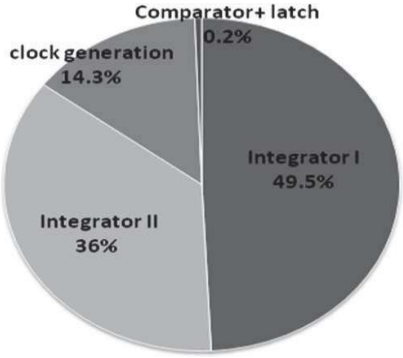


Figure 2.18: Measured power breakdown by sources [2].

defined below:

$$FOM_W = \frac{Power}{2^{(SNDR-1.76)/6.02} \times 2 \times BW} \tag{2.44}$$

$$FOM_S = DR_{dB} + 10\log(\frac{BW}{Power}) \tag{2.45}$$

where FOM_W favors low-resolution ADCs, while FOM_S favors high-DR ADCs. As shown in Table 2-4, the achieved FOMs are comparable to previously reported delta-sigma ADCs. Moreover, the designed modulator occupies one of the lowest chip area among the modulators, which is an important design factor for implantable devices.

TABLE 2-3: MEASURED PERFORMANCE RESULTS.

Technology	1P7M 65nm CMOS
Supply Voltage	0.9V
Clock Frequency	250kHz
Signal Bandwidth	500Hz
Peak SNR	80dB (13-bit)
Peak SNDR	76dB (12.3-bit)
Dynamic Range	75dB
Power	0.3μW digital 1.8μW analog
Active Area	0.033mm^2
FOM	0.407pJ/[conversion-step]

TABLE 2-4: PERFORMANCE COMPARISON WITH OTHER ΔΣ MODULATORS

Ref., Year	V_{DD} [V]	BW [Hz]	SNDR [dB]	DR [dB]	Power [μW]	Area [mm^2]	CMOS [μm]	FOM_W[a] [pJ/step]	FOM_S
[5] Chae, 2009	1.5	120	65	75	0.73	0.35	0.35	2.093	157
[5] Chae, 2009	1.2	8 k	63	76	5.6	0.003	0.35	0.303[b]	167
[22] Yang, 2012	0.5	20 k	81.7	85	35	0.57	0.13	0.088	172
[21] Kim, 2008	0.9	24 k	89	92	1500	1.44	0.13	1.36	164
[4] Roh, 2008	0.9	20 k	73	83	60	0.42	0.13	0.411	168
[26] Goes, 2006	0.9	10 k	80.1	83	200	0.06	0.18	1.21	160
[6] Roh, 2010	0.8	250	48.2	49	0.816	0.5	0.18	7.77	134
[27] Xu, 2010	1.8	1 k	80	88	9	1.84	0.35	0.551	168
[28]Michel,2012	0.3	20 k	61.4	70[c]	18.3	0.338	0.13	0.477	160
[2] Fazli, 2013	0.9	500	76	75	2.1	0.033	0.065	0.407	159

(a) FOM_W = Power/(2^{ENOB}×2×BW) known as Walden FOM
(b) Excluding clock generator
(c) DR value is unavailable, and is replaced by SNR value

2.7 Summary

In this Chapter, the low-power OTA topologies suitable for low-power delta-sigma modulator design in nanometer CMOS technologies were studied. The optimal analog performance parameters of the OTA building block were extracted from behavioral modulator simulations, aiming for power optimization. In addition, a complete power analysis of the amplifiers under study was also provided. Finally, comparison of the key

performance metrics of the designed amplifier topologies was given in Table 2-2.

The conventional distributed feedback, single-loop, modulator topology was described for first-, second-, and third-order loop filters. The concept of noise shaping and oversampling techniques were discussed by using system-level simulations. Moreover, behavioral simulations were accomplished to obtain the optimal modulator loop coefficients.

In addition to in-band quantization noise shaping, the baseband circuit noise of the succeeding blocks in the modulator forward path after the first integrator is also shaped (or low-pass filtered). The linearized model of a single-loop third-order ΔΣ modulator was used to derive the total input-referred noise power in baseband.

An experimental implementation of a second-order single-loop one-bit ΔΣ modulator in a 65nm CMOS process was explained in details in this Chapter. The modulator circuit and its building blocks were also discussed. The measured performance results and a full comparison of the implemented modulator with other published low-power modulators were presented.

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Chapter 3

Low-Power ΔΣ Modulators: Passive Approach

3.1 Introduction

This Chapter describes the design of low-power ΔΣ modulators using passive integrators. It investigates the design of the passive filter and the nonidealities associated with it. Three modulator designs are introduced employing partially passive loop filters (**Papers 6, 7**) or a fully passive filter (**Paper 6**). Passive integrators have better linearity than active integrators, and can operate under very low supply voltage without consuming any power from the supply. Aiming to reduce analog power consumption, the objective is to study the effectiveness of the switched-capacitor (SC) passive filter on the modulator performance. A second-order single-loop modulator with hybrid active-passive loop filter was implemented in a 65nm CMOS process, where the less critical second integrator is replaced by a passive one. Also, a second-order fully passive modulator was fabricated in the same chip. Both designs were tested, and the test results are discussed in section 3.4. Their performance is compared with that of a power optimized active modulator. The principles of the passive modulator using cascade of integrators feedback (CIFB) architecture, thereafter feedback architecture, are discussed first, and a thorough analysis, including the system-level signal and noise transfer functions and the circuit noise, is then discussed. Based on the design and careful analysis of the aforementioned modulators, a novel fourth-order feedforward active-passive modulator is presented with only one active stage in order to mitigate some of the fundamental problems associated with the fully passive ADCs. The term feedforward architecture is frequently used in the text to identify it from the feedback

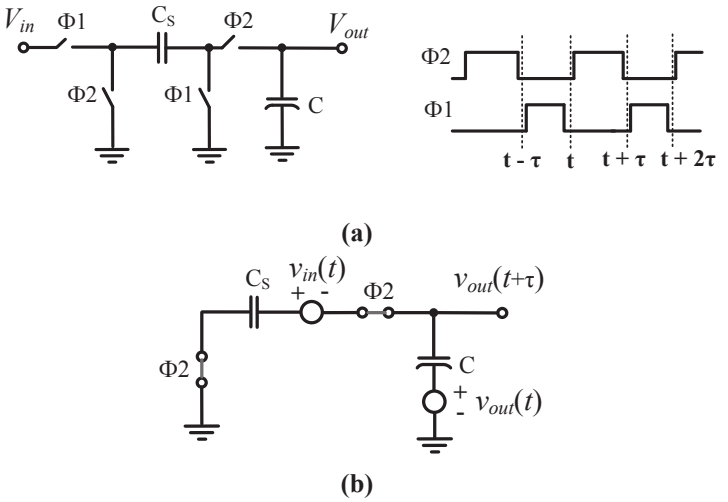

Figure 3.1: (a) Basic passive low-pass filter along with non-overlapping two-phase clock timing diagram in single-ended form (b) its arrangement during integrating phase.

architecture. A comparison of the proposed modulators with those reported previously is provided in the end of this Chapter. Also, these designs are compared with previous passive and hybrid active-passive modulators in section 3.7.

3.2 Switched-Capacitor Passive Low-Pass Filter

This section presents the fundamentals of the SC passive low-pass filter, and discusses the nonidealities associated with it, such as the integrator's loss and the effect of parasitic capacitances.

3.2.1 Basic Passive Filter

The passive low-pass filter (or integrator) is shown in its basic form in Fig. 3.1a along with two non-overlapping clocks. The filter transfer function can be derived by analyzing the circuit in time domain. In phase *Φ1* during time interval t-τ to t, the input signal $v_{in}(t)$ is sampled onto capacitor C_S, while the integrating capacitor C maintains its value from time instance t-τ, i.e. $v_{out}(t\text{-}\tau)$. As the content of C remains unchanged in this time interval, it can be expressed

$$v_{out}(t) = v_{out}(t-\tau) \tag{3.1}$$

Considering the next clock phase when *Φ2* closes (time interval t to $t+\tau$), the filter can be rearranged in a form that is shown in Fig. 3.1b. By applying superposition of two voltage sources $v_{in}(t)$ and $v_{out}(t)$, the output can be written as:

$$v_{out}(t+\tau) = \frac{C_S}{C_S + C} v_{in}(t) + \frac{C}{C_S + C} v_{out}(t) \tag{3.2}$$

Advancing one more sampling phase ahead, we get

$$v_{out}(t+2\tau) = v_{out}(t+\tau) \tag{3.3}$$

Supstituting (3.3) into (3.2), it can be modified to:

$$v_{out}(t+2\tau) = \frac{C_S}{C_S + C} v_{in}(t) + \frac{C}{C_S + C} v_{out}(t) \tag{3.4}$$

Now, applying *z*-transform on both sides, the transfer function can be calculated as:

$$\begin{aligned} H(z) = \frac{V_{out}}{V_{in}}(z) &= \frac{z^{-1}}{1 + \frac{C}{C_S} - \frac{C}{C_S} z^{-1}} \\ &= \frac{z^{-1}}{1 + \rho - \rho z^{-1}}. \end{aligned} \tag{3.5}$$

Showing the low-pass filtering characteristics, with $\rho = C/C_S$. It can be seen from (3.5) that the low-frequency dc gain $|H(z=1)|$ is unity. Substituting $z = e^{j\omega T}$ into (3.5), the 3dB bandwidth can be obtained as

$$\begin{aligned} f_{3dB} &= \frac{f_S}{2\pi(\rho + 1)} \\ &= \frac{f_S}{2\pi} \cdot \frac{C_S}{C_S + C} \end{aligned} \tag{3.6}$$

where f_s is the sampling frequency. The transfer function given by (3.5) can be reformulated as:

$$H(z) = \frac{\alpha z^{-1}}{1 - (1 - \alpha) z^{-1}} \tag{3.7}$$

where α is the integrator gain, and is equal to $C_S/(C_S+C)$. With C_S = 2pF and C = 64pF, the integrator gain is only 1/33, which is very small compared to that of an active integrator. In active integrators, this gain usually varies from 0.2 to 0.5. The ideal transfer function of an active integrator can be represented as:

$$H(z) = \frac{a z^{-1}}{1 - z^{-1}} \tag{3.8}$$

where *a* denotes the closed-loop gain and is the ratio of sampling capacitor C_S over the integrating capacitor *C*.

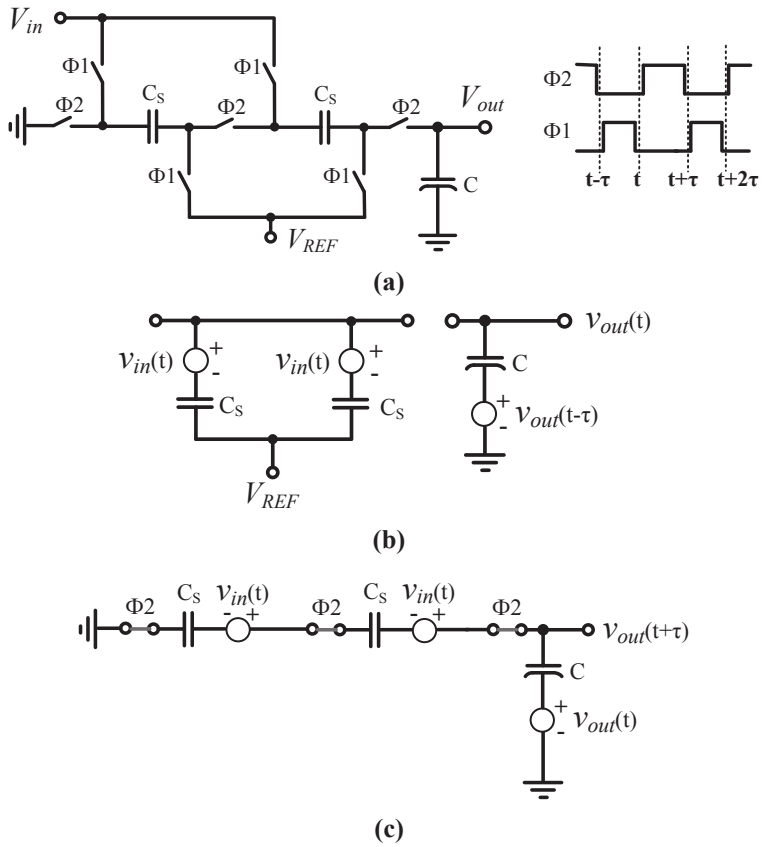

Figure 3.2: (a) Gain-boosted passive low-pass filter for N = 2, (b) its configuration in the sampling phase, *Φ1*, and (c) its configuration in the integrating phase, *Φ2*.

3.2.2 Gain-Boosted Passive Filter

The gain parameter in the loop filter plays an essential role for obtaining noise shaping. To compensate for the lack of gain in the basic filter of Fig. 3.1a, a charge redistribution scheme can be used [1] to produce passive gain at the cost of capacitive area, but in a very power-efficient manner. Figure 3.2 shows the gain-boosted passive filter using this scheme. The operation of the circuit is illustrated in Fig. 3.2b,c. During *Φ1*, the top plates of sampling capacitors C_S are charged to either V_{REFP} or V_{REFN} of the one-bit DAC, while their bottom plates are charged to the input V_{in}. During *Φ2*, the precharged capacitors are positioned in series between the filter's CM voltage (i.e. $V_{DD}/2$) and the output (Fig. 3.2c). Similar to what was carried out in the previous section, the ideal transfer function of an *N*-stage gain-boosted filter can be derived as

given by (3.9). For an arbitrary value of N, the resulting low-frequency gain of the filter, i.e. $|H(z=1)|$, is N and the single pole is placed closer to the origin as compared to the basic passive filter, resulting in higher in-band quantization-noise shaping ability in the modulator.

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{z^{-1}C_s/(C_s/N + C)}{1 - z^{-1}C/(C_s/N + C)} = \frac{z^{-1}}{1/N + \rho - \rho z^{-1}} \tag{3.9}$$

The 3dB bandwidth can be calculated as:

$$f_{3dB} = \frac{f_s}{2\pi} \cdot \frac{1}{(1 + N\rho)} \tag{3.10}$$

Comparing (3.9) with (3.5) and assuming identical capacitive ratio C/C_S, the net effect of the gain-boosted scheme on the filter transfer function is the gain increase by N, while reducing the 3dB cut-off frequency by N. It is worthwhile to point out that for a given 3dB bandwidth represented by (3.10), there is a great opportunity to decrease the size of the integrating capacitor C, the predominantly area-taking capacitor of the gain-boosted filter, by N times while the dc gain according to (3.9) will be increased. As a practical example, for a 500Hz signal bandwidth and the sampling frequency f_S equal to 500kHz, with a basic filter, according to (3.6), the value of ρ is calculated to be 158. With C_S = 1pF, this will result in an integrating capacitor C as large as 158pF. For the same bandwidth, a 5-stage gain-boosted filter turns out to have a C equal to 31.6pF, which is five times smaller.

3.2.3 Circuit Nonidealities

In this section, the impact of circuit nonidealities on the performance of both the simple low-pass filter (Fig. 3.1) and the gain-boosted low-pass filter (Fig. 3.2) is investigated. In particular, the effect of passive integrator loss and parasitic capacitances on the performance of the filter and ΔΣ modulator is outlined.

3.2.3.1 Loss in the Passive Filters

The passive integrator suffers inherently from the fundamental problem of no gain in a basic filter or low gain in a gain-boosted filter. To examine this problem, consider a simple first-order modulator, shown in Fig. 3.3, which employs a basic passive filter. The linear model of the modulator consists of a single-bit quantizer that has been modeled as a gain factor G and an additive white quantization noise. Using this linear model and the loop filter transfer function $H(z)$ given by (3.5), the noise transfer function (NTF) can be calculated as:

$$NTF(z) = \frac{1}{1 + G.H(z)} = \frac{1 + \rho - \rho z^{-1}}{1 + \rho + (G - \rho)z^{-1}} \tag{3.11}$$

From the above expression, it is apparent that the value of zero in the ideal NTF moves

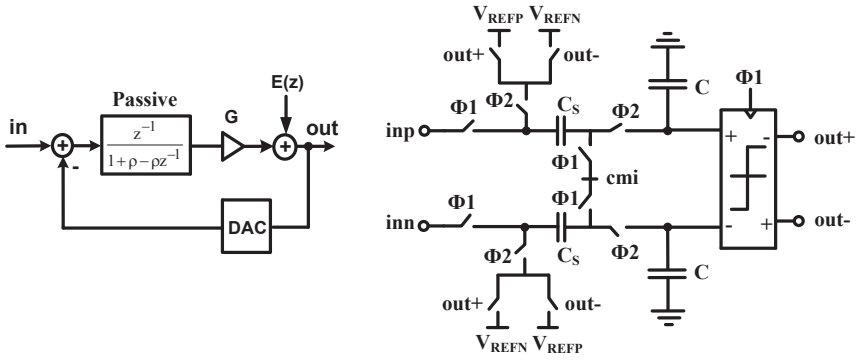

Figure 3.3: (a) Linearized model of first-order passive modulator (b) Circuit implementation [3], © 2013, IEEE.

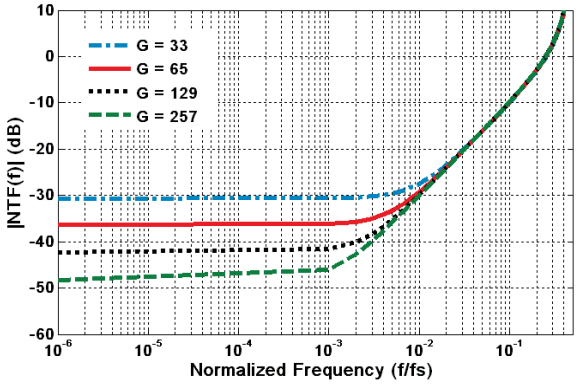

Figure 3.4: Magnitude response of the NTF of the first-order passive modulator [3], © 2013, IEEE.

from $z = 1$ (at dc) to $z = \rho/(1+\rho)$ inside the unit circle. Hence, the dc gain of the NTF, i.e. NTF(1), shifts from its ideal value of zero to $1/G$. This means that the extent of quantization-noise shaping at the low frequencies of interest largely depends on the loop gain, G. The main difference between an active and a passive ΔΣ modulator is the loop-gain distribution. The active modulator distributes the loop-gain into each pole sector among the integrators, while the passive one lumps the total loop-gain into the comparator [2]. An estimate of this gain is given by [1] in which the overall loop-gain is approximated to be unity at half the sampling frequency, $f_s/2$. Therefore, for a first-order filter characteristics of (3.5), the loop-gain is estimated to be $1/|H(z=-1)| = 1+2\rho$. The magnitude of the NTF of the first-order passive modulator is shown in Fig. 3.4.

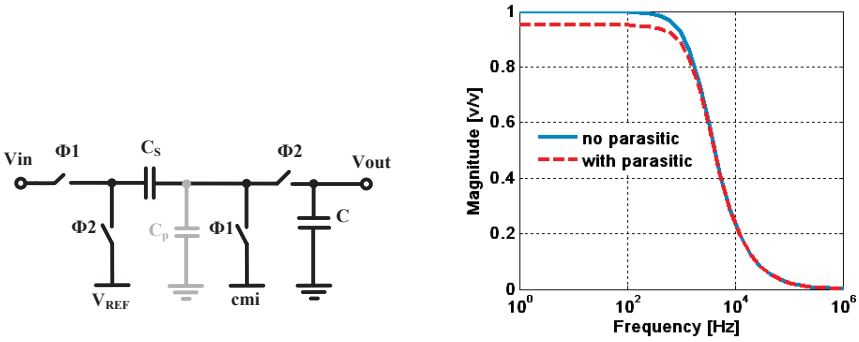

Figure 3.5: Basic passive filter including parasitics [3], © 2013, IEEE.

Obviously, the larger ρ (or capacitor ratio) increases the G, and consequently enhances the in-band noise attenuation at the cost of larger capacitive area. For example, for a G equal to 260, with C_S = 2pF a large integrating capacitor value of 260pF is required, which makes the realization of the first-order passive modulator impractical. With a second-order passive loop filter implementation, this area overhead can be mitigated significantly because the loop gain is generated by the poles of both integrators.

3.2.3.2 Impact of Parasitics on SC Passive Filter

The parasitic capacitances due to the creation of C_S and C as well as the nonlinear capacitances associated with switches can change the characteristics of the passive filter, and degrade its performance. Due to the small size of the switch (aspect ratio of 5µm/0.06µm), the parasitics associated with its implementation can be neglected. The most significant parasitics can be lumped into C_P as shown in Fig. 3.5. The filter transfer function with parasitics can be calculated as:

$$H_P(z) = \frac{z^{-1}}{1+\rho+\lambda-\rho z^{-1}} \tag{3.12}$$

where $\rho = C/C_S$ and $\lambda = C_P/C_S$. Compared to (3.5) the term λ is excessive, and is due to the parasitics. The loss and the 3dB bandwidth of the filter represented by (3.12) can be expressed as:

$$A_P(z) = \left|H_P(z=1)\right| = \frac{C_S}{C_S+C_P} < 1 \tag{3.13}$$

$$f_{3dB} = \frac{f_S}{2\pi} \cdot \frac{C_S+C_P}{C+C_S+C_P} \tag{3.14}$$

Compared to (3.6), the parasitic capacitance reduces the passband gain and shifts the 3dB frequency corner towards a higher frequency, which degrades the quantization

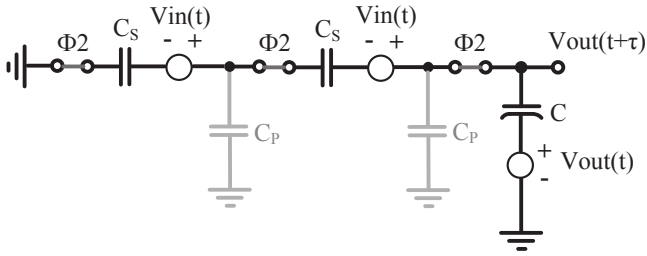

Figure 3.6: Equivalent circuit of a 2-satage gain-boosted filter with parasitic capacitances in *Φ2*.

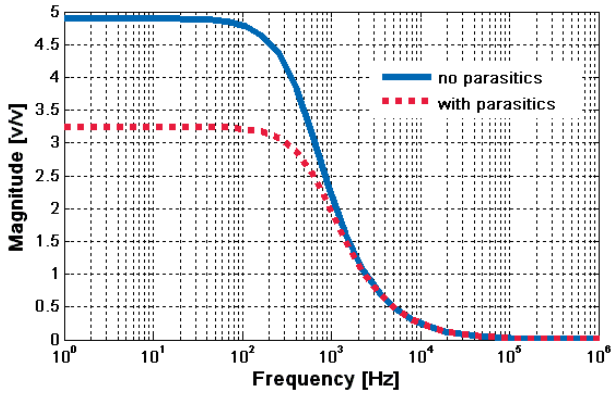

Figure 3.7: Simulated transfer function of 5-stage gain-boosted passive filter with/without parasitic capacitances [3], © 2013, IEEE.

noise suppression. With f_s = 500kHz, C_S = 2pF, C = 64pF, and the estimated C_p = 100fF, the filter transfer function with/without parasitic capacitance is simulated, and the result is plotted in Fig. 3.5. It demonstrates that in the presence of C_p the gain decreases to 0.95 from unity, while the pole moves from 2.4kHz to 2.54kHz. The results can also be verified by inserting the parameters into (3.13)-(3.14), showing a good agreement between the simulation results and calculations.

3.2.3.3 Impact of Parasitics on Gain-Boosted Filter

A 2-stage gain-boosted passive filter was shown in Fig. 3.2. The equivalent circuit in the integrating phase with parasitics lumped into internal nodes is illustrated in Fig. 3.6. For the sake of simplicity, the number of parallel sampling capacitors is taken to be 2 in this figure, while in practical realization of a second-order passive modulator, which will be discussed later in this Chapter, a 5-stage gain-boosted filter is designed. The

filter transfer function (for $N = 5$), with and without parasitic capacitances, is simulated with $f_S = 0.5$MHz, $C_S = 2$pF, $C = 64$pF, and the estimated $C_p = 100$fF. Figure 3.7 shows that in the presence of C_p, the dc gain reduces from 5 (14dB) to 3.25 (10.24dB), while the 3dB bandwidth shifts from 500Hz to 750Hz, which is a significant performance degradation. Simulation shows that using more than 5-6 stages is problematic since the gain improvement is not satisfactory in the presence of parasitic capacitances.

3.3 Comparative Analysis of Modulator Architectures

Two second-order single-loop ΔΣ modulators with 1-bit quantizer are studied in this section. The first design employs a hybrid active-passive loop filter wherein the less critical second integrator is replaced by a basic passive low-pass filter depicted in Fig.-3.1. The second design exploits a fully passive loop filter: a basic passive integrator (Fig. 3.1) in the first stage, and a 5-stage gain-boosted filter (Fig. 3.2) in the second stage. The resulting hybrid and fully passive modulators are then compared with the standard second-order active modulator presented in **Paper 1**. The active modulators were analyzed in the previous Chapter. The focus here will be only on the modulators using passive integrator(s), while a second-order active one is considered to be a reference for comparison. Hereafter, for the sake of brevity, these modulators are sometimes named with their shortened form, where $\Delta\Sigma M_{AA}$, $\Delta\Sigma M_{AP}$, and $\Delta\Sigma M_{PP}$ represent the reference active modulator, the hybrid active-passive modulator, and the fully passive modulator, respectively.

3.3.1 System-Level Considerations

Regardless of what type of low-pass filter is utilized in each integrator, the generalized linear model of a second-order single-bit modulator is shown in Fig. 3. 8, in which all noise sources are specified.

$$Y \approx X + N_1 + \frac{N_2}{H_1} + \frac{N_C}{H_1 H_2} + \frac{Q_n}{G H_1 H_2} \tag{3.15}$$

where H_1 and H_2 are the integrators transfer functions, N_1 and N_2 are the input-referred circuit noise injected at the input to each stage, respectively, while N_C and Q_n represent the comparator input-referred noise and the quantization noise. The factor G is the equivalent gain of the quantizer.

For the hybrid $\Delta\Sigma M_{AP}$, since filter H_2 has no gain, the last two terms related to N_C and Q_n do not achieve similar low-pass filtering as for the $\Delta\Sigma M_{AA}$, thereby affecting the SNR. Due to signal attenuation by the passive filter H_2 at the quantizer input, the gain G increases [2] as compared to that of the $\Delta\Sigma M_{AA}$. A higher G can be obtained by pushing the pole to lower frequencies [2], thereby achieving less quantization noise Q_n, while this would result in more circuit noise because N_C/H_1H_2 term increases.

For the passive $\Delta\Sigma M_{PP}$, by ignoring the inter-stage loading a similar linear model can be applied for noise discussions. The output is then expressed by (3.15) because G is

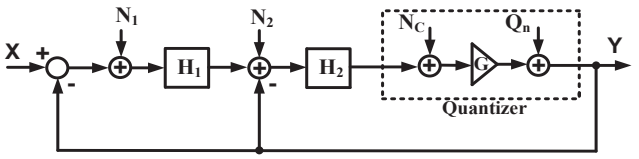

Figure 3.8: Linear model of a single-loop second-order 1-bit modulator.

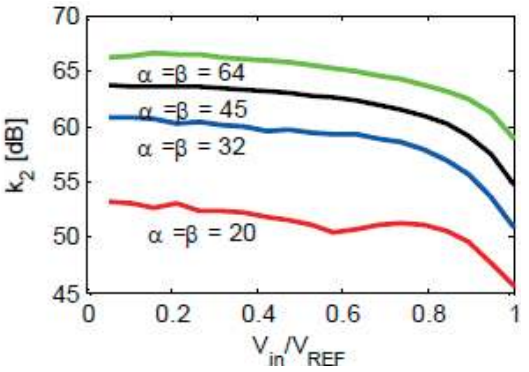

Figure 3.9: Simulated quantizer gain dependency on the normalized input amplitude and capacitor ratio α and β [3], © 2013, IEEE.

assumed to be very large. Due to no gain in both H_1 and H_2, the input signal subjects to extreme attenuation at the quantizer input. This very low signal swing indicates very large loop gain provided by the comparator. According to (3.15), higher quantization-noise suppression can be achieved by placing the poles at lower frequencies (due to larger G). Optimal pole locations then have to be decided for adequate suppression of the circuit noise N_2 and N_C. By intuition, the increase in the comparator gain can be explained in this way. For larger α, $\beta = C_i/C_{Si}$ the pole locations of the overall passive filter move towards the lower frequencies, according to (3.6), hence the gain of the filter decreases and the swing at the comparator input reduces substantially. As the comparator output does not change (it is either low or high supply rail), a larger comparator gain is realized in this way. Figure 3.9 plots k_2, the equivalent gain of the quantizer, across the input amplitude for different $\alpha = C_1/C_{S1}$ and $\beta = C_2/C_{S2}$. Thus, the single-bit quantizer in Fig. 3.8 can be modeled as an amplifier with input-dependent gain, k_2, and an additive white noise source.

3.3.2 Noise and Signal Transfer Functions

Figure 3.10 illustrates the linear model of the two second-order modulators presented in [3], whereas that of the reference active one was discussed previously in section 2.3.1. The loop coefficients are highlighted in the figure. The factor α, according to (3.7), is the integrator gain, and is equal to $C_S/(C_S+C)$ for the basic passive filter and

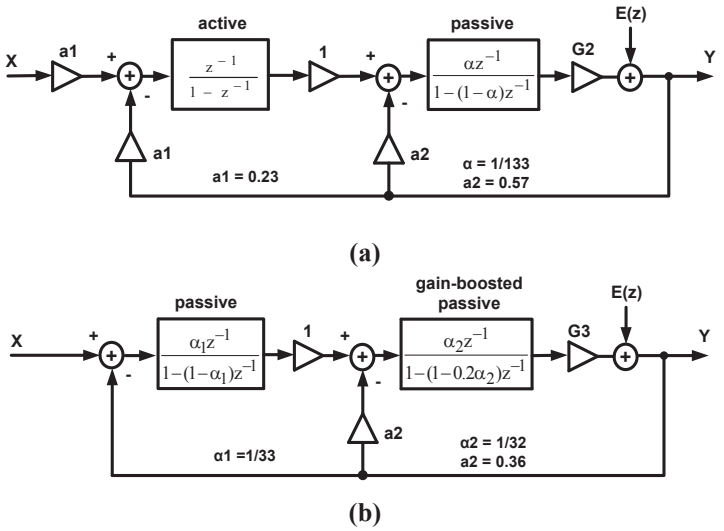

Figure 3.10: The linear model of two second-order 1-bit modulator architectures: (a) active-passive $\Delta\Sigma M_{AP}$; *a1*, *a2* = 0.23, 0.57 (b) fully passive $\Delta\Sigma M_{PP}$; *a2* = 0.36.

$C_S/(C_S/N+C)$ for the N-stage gain-boosted filter. The values of α are given in Fig. 3.10. The equivalent quantizer gain, *Gi*, differes from one architecture to another. For an active modulator designed using feedback loop topology, usually a full-scale internal integrator swings are applied, thus the quantizer gain can be estimated to be unity [4]. Due to large signal attenuation in the passive filters, the quantizer equivalent gain in $\Delta\Sigma M_{AP}$ and $\Delta\Sigma M_{PP}$ becomes non-unity, and depends on the input amplitude of the modulator. Therefore, the factors *G2* and *G3* in Fig. 3.10 are determined from the nonlinear simulation model [5]. The signal and noise transfer functions (STFs and NTFs) of the mentioned modulators are illustrated in Fig. 3.11 along with those of the reference $\Delta\Sigma M_{AA}$ modulator. Clearly seen from Fig. 3.11a, there is a -2.5dB loss in the $\Delta\Sigma M_{PP}$ design, while the other two variants provide unity signal transfer function at low frequencies. This will result in degraded SNR for the fully passive implementation. Moreover, as expected, the $\Delta\Sigma M_{PP}$ introduces higher in-band quantization-noise than the $\Delta\Sigma M_{AP}$ and the reference $\Delta\Sigma_{AA}$, which is due to the limited filter gain (in $\Delta\Sigma M_{AP}$) or no filter gain (in $\Delta\Sigma M_{PP}$). Clearly, the $\Delta\Sigma M_{PP}$ demonstrates less in-band noise attenuation, as shown in Fig. 3.11b, which results in the lowest SNR amongst the presented architectures.

3.3.3 Circuit Noise

The detailed analysis of the circuit noise of a second-order active modulator were discussed previously in section 2.4.1. Derived in (2.32), for the hybrid modulator shown in Fig. 3.10a, with $a_1 = 0.23$, $\alpha = 1/133$ and $M = 250$, the baseband circuit noise at the

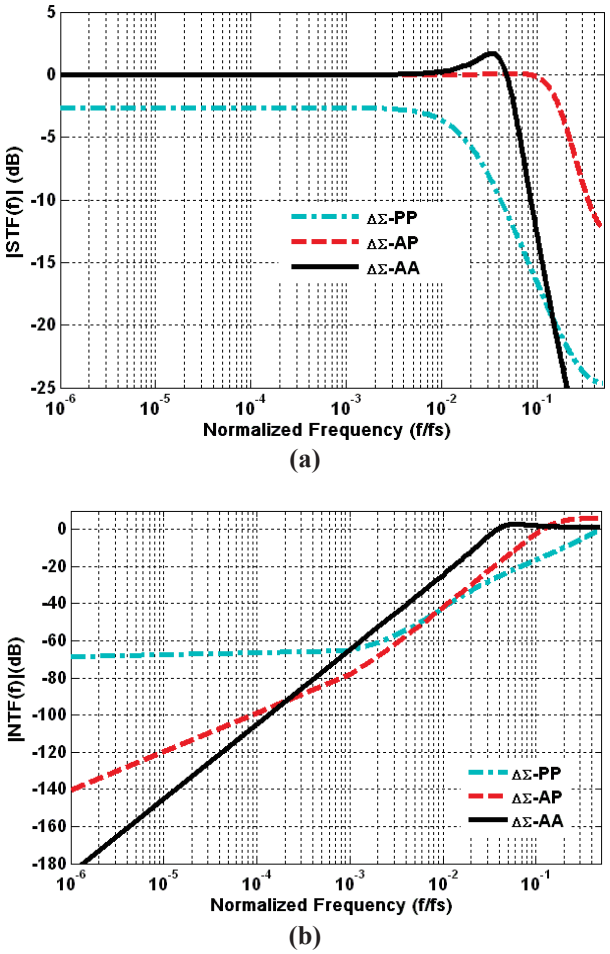

Figure 3.11: Comparison of three modulator architectures: (a) STF magnitude (b) NTF magnitude [3], © 2013, IEEE.

input of the second integrator and comparator input is attenuated by 10^{-3} and 1.7×10^{-3}, respectively, relative to the noise introduced at the input of the first integrator. Therefore, the total input-referred noise can be approximated by the noise of the first integrator. This was estimated by (2.42).

For the passive $\Delta\Sigma M_{PP}$ converter (Fig. 3.10b), there are three thermal noise sources, $P_{N1} \approx 4kT/C_{S1}$ from the first filter (H_1) with $C_1 >> C_{S1}$, P_{N2} from the second gain-boosted filter (H_2) and the comparator input-referred noise $P_{Com} = (8kT\gamma/g_m+2k_N/wlC_{ox}f)\Delta f$. Therefore, according to (3.15), the overall in-band noise power can be calculated as:

$$P_{n.tot} = P_{N1} + \frac{P_{N2}}{H_1^2} + \frac{P_{Com}}{H_1^2 H_2^2} + \frac{P_{Qn}}{G^2 H_1^2 H_2^2} \tag{3.16}$$

where the transfer function of H_1 is given by (3.5) and $H_T = H_1 H_2$ is the equivalent transfer function of the loop filter from the modulator input to the comparator input, which can be expressed as:

$$H_T(z) = H_1 H_2 = \frac{k_0 z^{-2}}{1 + k_1 z^{-1} + k_2 z^{-2}} \tag{3.17}$$

with $k_0 = \alpha_1\alpha_2\alpha_3$, $k_1 = -1-\alpha_3+\alpha_1\alpha_3+0.2\alpha_2\alpha_3$ and $k_2 = (1-\alpha_1)(1-0.2\alpha_2)\alpha_3$, where we define $\alpha_1 = C_{S1}/(C_1+C_{S1}) = 1/33$, $\alpha_2 = C_{S2}/(0.2C_{S2}+C_2) = 1/32$ and $\alpha_3 = C_1/(C_1+0.2C_{S2}) \approx 1$. The inter-stage loading between the filters is also taken into account in (3.17) whose α_3 factor indicates the inter-stage dependency. The first two terms in (3.16) is minimized by proper capacitor size such that the comparator noise becomes the predominant source of the noise. The last term of (3.16), P_{Qn}, relates to the in-band quantization noise, which is attenuated by the high-pass transfer function $1/HFG$, due to the loop gain G produced by the comparator.

3.4 Implementation of Two Modulators Using Passive Filter

3.4.1 A 0.9V 1.27µW Active-Passive Modulator

The circuit implementation of the proposed modulator is shown in Fig. 3.12 based on the topology illustrated in Fig. 3.10a. All capacitors are realized with MIM structure.

3.4.1.1 Behavioral Simulation

The amplifier performance requirements in the first integrator is simulated using a behavioral model of a second-order modulator in order to determine the minimum required dc gain and GBW for a target SNR of more than 90dB. This was discussed in section 2.2.1 in the previous Chapter. It can be seen that for noise-shaping only, the minimum gain and GBW to obtain more than 90dB SNR is about 35dB and 1.2MHz, respectively.

Another feature associated with the hybrid topology is that the integrator output swing of the passive filter is significantly reduced compared to a classic active modulator. Shown in Fig. 3.13, output of the passive integrator is obviously much smaller than the traditional active integrator in the second stage, due to the introduction of an attenuation factor equal to $C_{S2}/(C_{S2}+C_2)$ by the passive low-pass filter.

In the behavioral model, the switches are replaced by transistor-level implementation, and two small and large signals with magnitudes equal to -10dBFS and -2.92dBFS, respectively, are applied to the modulator. Due to non-linear behavior of the switches with large signals, third and fifth-order harmonic distortion appear in the output power spectra, as shown in Fig. 3.14.

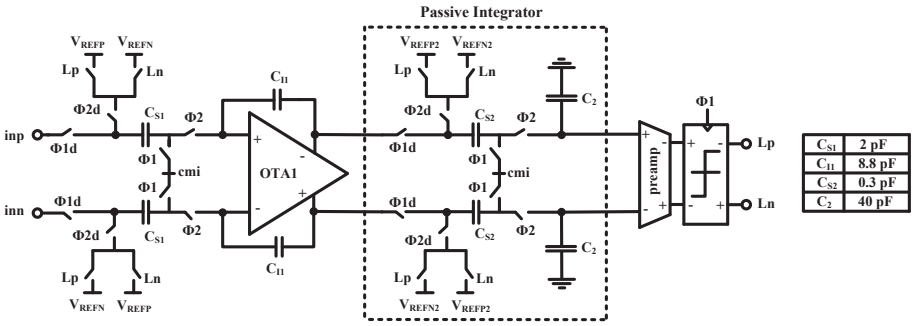

Figure 3.12: Circuit schematic of the hybrid $\Delta\Sigma M_{AP}$ employing an active integrator in the first stage and a passive integrator in the second stage [3], © 2013, IEEE.

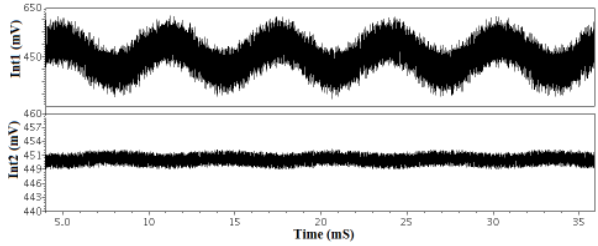

Figure 3.13: Simulated integrator output swings of the hybrid $\Delta\Sigma M_{AP}$.

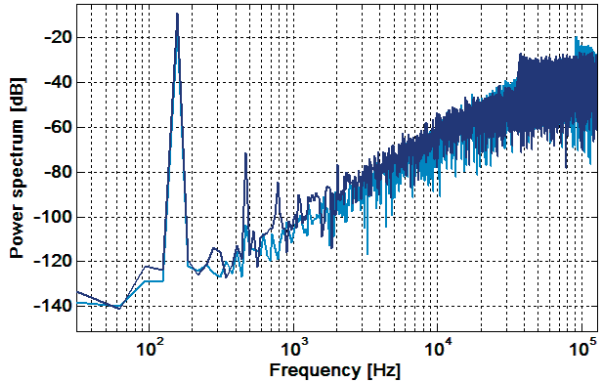

Figure 3.14: Power spectra from behavioral simulations of a second-order active-passive modulator with OSR = 256, 156Hz input and -10 and -2.92dBFS amplitudes.

3.4.1.2 Building Blocks

The OTA in the first stage of the modulator is a two-stage load-compensated topology, identical to the one used in reference active modulator. Further discussions can be found in section 2.2.3 of previous Chapter. The rest of the building blocks are discussed in the following subsections.

A. Switches and other circuits

As demonstrated in Fig. 3.15, all switches are realized by transmission gates and local switch drivers implemented by two cascaded inverters. Low-power low-V_{th} transistors are applied in order to provide wider overdrive voltage at 0.9V supply voltage, but at the cost of more sub-V_{th} leakage current. The transistors in the switches are properly sized to ensure small on-resistance, required by the RC time constant. The delayed version of the two-phase non-overlapping clock signals are also generated on-chip to reduce the charge injection between phases.

The dynamic comparator and the following SR latch are identical with the reference active modulator, which is shown in Fig. 2.14 composed by high-V_{th} transistors. Also, the clock generation circuitry is implemented on-chip. The detailed explanations can be found in [6].

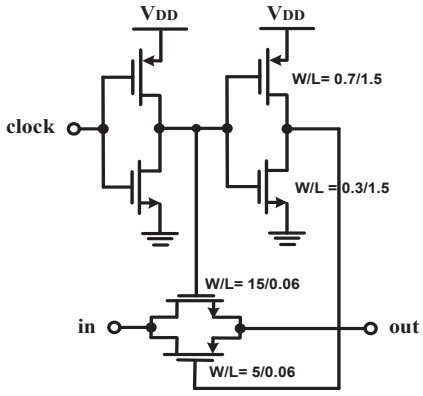

Figure 3.15: Switch implementation. The units are in μm**.**

B. Passive Filter

A fully differential implementation of the simple passive filter, shown in Fig. 3.1, is used. The capacitors are realized with MIM structure. The sampling capacitor, C_{S2}, is taken to be 0.3pF identical to the one used in the reference modulator for similar loading of OTA1, which is deterimined from the thermal noise requirement. From (3.5) with 250kHz sampling frequency, the integrating capacitor C_2 is calculated for the 3dB bandwidth to be 300Hz. The capacitors size is given in Fig. 3.12. Due to signal

attenuation by the passive filter, the reference level related to the second DAC is scaled down accordingly, and is set to 0.4V, defined by V_{REFP2} = 0.65V and V_{REFN2} = 0.25V. The reference voltage related to the first DAC is 0.6V.

C. Preamplifier

A single-stage power-efficient preamplifier with a gain-enhanced positive feedback is used, as shown in Fig. 3.16, to amplify the highly attenuated signal at the quantizer input. According to (3.16), the preamplifier noise becomes significant due to the lack of gain inside the loop filter; therefore, designing a low-noise preamplifier is a crucial task in passive ADCs. To cope with noise, the input transistors M_1 and M_2, the dominant noie sources, are sized as large as 40/0.1. The simulated input-referred noise of the preamplifier is 22.5μV_{rms}. The gain that it provides is 12dB, while it dissipates 180nW.

3.4.2 A 0.7V 0.43μW Passive Modulator

To further explore the capability of the passive filter in power reduction, a second variant of second-order modulator is presented using the feedback topology. The modulator schematic is shown in Fig. 3.17. This variant utilizes passive filters rather than power-hungry active integrators in both stages, where the second filter embeds a gain-boosting technique with a charge redistribution scheme. Since the internal swings are inherently low, due to attenuation in the passive integrators, the fully passive modulator topology is capable of working in lower supply voltage than its active counterpart. As the majority of power is consumed by digital parts, including the built-in clock generation and switch drivers, the reduction of supply voltage is very beneficial for power consumption scaling-down. The main limiting factors, however, are the switches overdrive problem and the limited headroom in the preamplifier circuit prior to the comparator. Exploiting low-V_{th} transistors provides both sufficient overdrive voltage for switches and adequate voltage headroom for the preamplifier design.

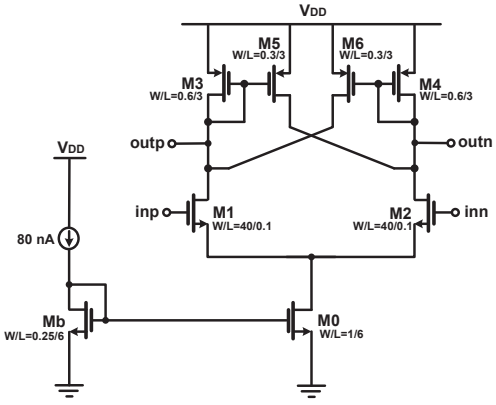

Figure 3.16: The differential preamplifier circuit [3]. Units are in μm, © 2013, IEEE.

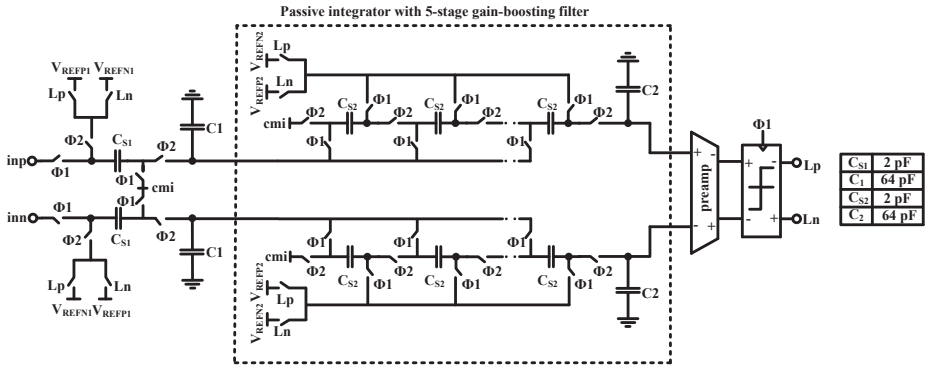

Figure 3.17: Circuit schematic of the proposed $\Delta\Sigma M_{PP}$ using fully passive loop filter. The second integrator utilizes a 5-stage gain-boosted filter [3], © 2013, IEEE.

The proposed modulator can operate at 0.7V with insignificant SNR degradation, while compared to 0.9V the measured power is reduced from 0.92μW to 0.43μW, more than 50% of its total power is saved in this way. The overall modulator trades SNR for reduced power consumption.

All of the circuit building blocks are identical to the presented active-passive modulator, which were discussed in section 3.4.1.2. In the fully passive topology, the strategy of sizing the capacitors differs from that of the $\Delta\Sigma M_{AP}$ because there is no active OTA involved in the loop filter. Therefore, the circuit noise and other nonidealities from the succeeding blocks (e.g., gain-boosted passive filter, preamplifier, and comparator) may directly influence the modulator performance. The circuit noise was analysed and estimated before in section 3.3.1. Based on this assessment, the capacitors values are calculated carefully as follows: The C_{S1} and C_{S2}, determined from the thermal noise requirement, are selected as 2pF, including a margin. The 2nd-order loop filter is designed to have two poles at 0.5kHz and 2.5kHz, respectively. Calculated from (3.6) and (3.10), the capacitors C_1 and C_2 are chosen to be 64pF. The DAC reference voltages for the first and second filters are set to 0.7V and 0.25V, respectively, while the common-mode voltage is set to $V_{DD}/2$.

3.4.3 Experimental Results

The measurement results of both modulators are summarized in Table 3-1, and the results are compared with the standard active modulator [6] implemented in the same chip. The chip micrograph is shown in Fig. 3.18. Compared to the reference $\Delta\Sigma M_{AA}$, the $\Delta\Sigma M_{AP}$ and $\Delta\Sigma M_{PP}$ occupy 2× and 4× the core area. Clearly seen, about 75% of the core area in the $\Delta\Sigma M_{PP}$ is taken by the integrating capacitors. Figure 3.19 shows the measured power spectra for both modulators. The tested SNDR versus differential input amplitude is shown in Fig. 20. The detailed power breakdown is reported in [3].

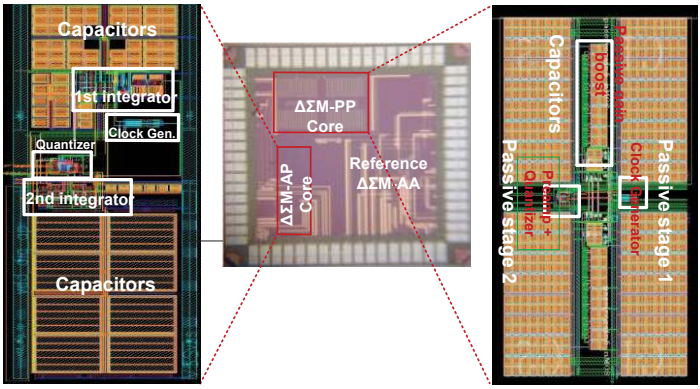

Figure 3.18: Chip photograph and layout details.

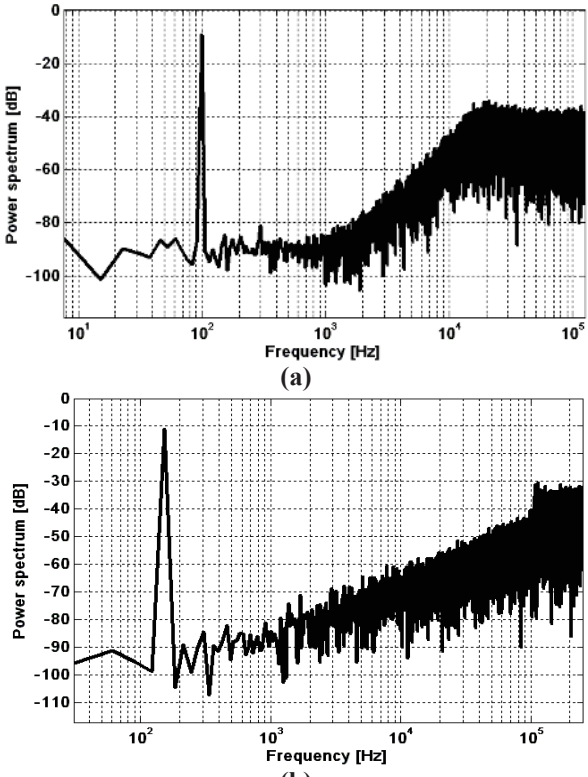

Figure 3.19: Measured spectra: (a) with $-3.1\text{dB}_{\text{FS}}$ and 99Hz sine-wave for $\Delta\Sigma\text{M}_{\text{AP}}$, and (b) with 0dB 156Hz for $\Delta\Sigma\text{M}_{\text{PP}}$ [3], © 2013, IEEE.

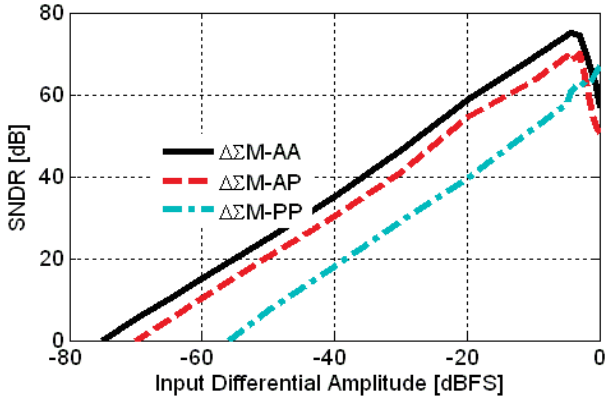

Figure 3.20: Measured SNDR versus input amplitude using a 99Hz tone, and comparison with the reference active modulator [3], © 2013, IEEE.

TABLE 3-1: COMPARISON OF THREE MODULATOR VARIANTS [3], © 2013, IEEE.

	$\Delta\Sigma M_{AA}$	$\Delta\Sigma M_{AP}$	$\Delta\Sigma M_{PP}$
Technology	1P7M 65nm CMOS		
Supply Voltage	0.9V		0.9V/0.7V
Clock Frequency	250kHz		500kHz
Signal Bandwidth	500Hz		
Peak SNR	80dB	73.5dB	70.2dB / 68dB
Peak SNDR	76dB	70dB	67dB / 65dB
Dynamic Range	75dB	70.5dB	55dB / 53dB
Power	2.1µW	1.27µW	0.92µW / 0.43µW
Active Area mm²	0.033	0.059	0.125
FOM pJ/step	0.407	0.491	0.503 / 0.296

3.5 Traditional Passive Modulators: Drawbacks

Due to lack of dc gain inside the passive loop filter, the corresponding modulator is sensitive to noise coupling, which affects the SNR. The design in [2] uses a second-order passive filter without gain, while, in turn, a three-stage preamplifier is adopted prior to the comparator to compensate for gain, which is a power hungry solution. In fact, the use of active gain in earlier stages was delayed to the final stage. The passive modulators in [1] and [7] employ gain-boosted passive filter to somehow mitigate the gain problem. But, achieving high gain requires unrealistically large capacitor area and is also more sensitive to parasitic capacitances.

The lack of gain and significant signal attenuation inside the passive loop filter make the design of high-resolution comparators and consequently high-resolution ADCs a challenging task. To revisit issues concerning the comparator design, again consider the linear model given by (3.15). The quantization noise obtains some lowpass filtering because of the loop gain G provided by the quantizer. On the other hand, for a certain SNR, the kT/C noise related to passive stages can be mitigated by properly scaling up the capacitors size, whereas the N_C is the only noise term that is not subject to any attenuation at low frequencies. N_C consists of the thermal noise and the low frequency 1/f noise of the preamplifier. To limit this, the passive modulator in [1] utilizes a preamplifier with large input devices whose W/L ratio is 200μm/1.2μm, imposing about 0.5pF of parasitic capacitance at the comparator input. Moreover, in the passive delta-sigma ADCs, the offset of the overall ADC is defined by that of the comparator [8]. Therefore, to alleviate the comparator nonidealities, several solutions have been applied in the past [8], [9] where at least one active stage was accompanied to suppress the input-referred noise and the dc offset.

Almost all of the modulators presented to date using a passive approach have been using classic feedback topology [1]-[3], [7]-[9], where the comparator design was a critical task, thereby designing the modulators with more than two cascaded passive filters were impractical. In the next section, a 4th-order modulator with input feedforward topology is proposed, which improves the swing at the comparator input and enables the use of three successive passive filters. As a consequence, the comparator design becomes much simpler without requiring a power-consuming preamplifier. The capacitive area penalty mentioned in section 3.4.3 and Table 3-1 decreases heavily due to the active integrator at the input stage.

3.6 Proposed 4th-Order Active-Passive Modulator

The ultimate purpose of this design (**Paper 7**) is to improve the ADC resolution by solving the problem of extremely low swing at the quantizer input of the classic feedback passive modulators as well as cascading more than two passive filters, while maintaining high power-efficiency and low chip area. Significant power reduction was obtained through (i) the reduced clock frequency by using a higher-order and more power-efficient loop filter, (ii) the removal of the power consuming preamplifier of the traditional feedback passive modulators [1]-[3], [7], [8] and (iii) the relaxed amplifier performance requirements in the full feedforward modulator structure [10], [11].

3.6.1 Architectural Design

The modulator uses the input feedforward topology. The feedforward topology has an extra path from the input of the modulator to the quantizer [10], [11]. This small architectural modification eliminates the signal component inside the loop filter; thereby it only processes the quantization noise [10]. This distinct feature facilitates the cascading of three power-efficient passive filters, in spite of their large attenuation. Moreover, the voltage swing at the quantizer input is the sum of the input signal and the

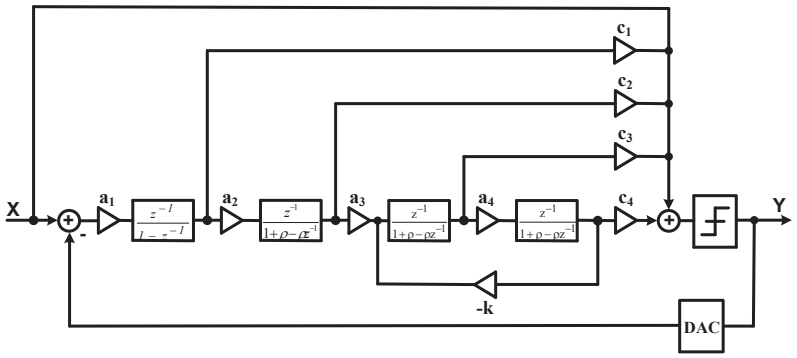

Figure 3.21: Fourth-order feedforward ΔΣ modulator with one active integrator in the first stage [12], © 2013, IEEE.

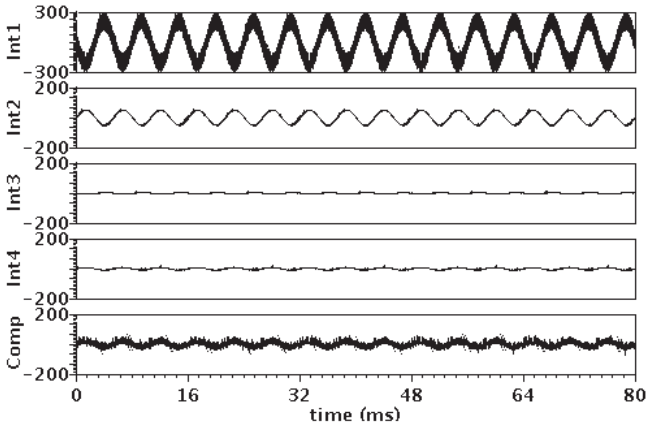

Figure 3.22: Integrators output swing. C*omp* represents the comparator input signal, and *Inti* (*i* = 1-4) represents the *i*th integrator output [12], © 2013, IEEE.

TABLE 3-2: MODULATOR COEFFICIENTS.

Filter Coefficients	Feedforward Coefficients	Resonator Coefficients
$a_1 = 0.2$	$c_1 = 2$	$k = 1/64$
$a_2 = 1$	$c_2 = 3$	
$a_3 = 1$	$c_3 = 2$	
$a_4 = 1$	$c_4 = 5$	

suppressed quantization noise, which enables the comparator design without requiring any preamplifier circuit. Figure 3.21 shows the fourth-order full input feedforward modulator topology with single-bit quantizer, where an active integrator in the first stage and three simple passive integrators in the following stages are utilized [12]. A local resonator feedback loop with a coefficient of k is used to move a pair of the NTF zeros to the edge of the signal band, resulting in SNR improvement.

The behavioral simulation shows the integrators output swing and the added swing after the summation node. Clearly seen in Fig. 3.22, despite the continual swing drop due to passive stages, the swing at comparator input is relatively large, i.e. ±40mV, owing to the input feedforward architecture. Additionally, the consecutive attenuated swings of passive filters will not harm the actual signal because the feedforward loop filter only processes the quantization noise [13]. The modulator loop coefficients were optimized from the massive behavioral simulations, as listed in Table 3-2. The coefficients related to the passive filters, i.e. a_i for i = 2,3,4, are implicitly multiplied by the $1/(1+\rho)$ factor, with $\rho = C_i/C_{si}$.

3.6.2 Circuit Design

Figure 3.23 shows the differential modulator circuit schematic. It has four integrators, one active integrator in the first stage [14], and three simple passive filters as discussed in section 3.2.1. A dynamic comparator and a latch, similar to the one in [6], are used as one-bit quantizer. The integrators input and output common-mode voltages are set to $V_{DD}/2$, i.e. 0.35V. The reference voltage is set to 0.5V, which is defined as V_{REFP} equal to 0.6V and V_{REFN} equal to 0.1V.

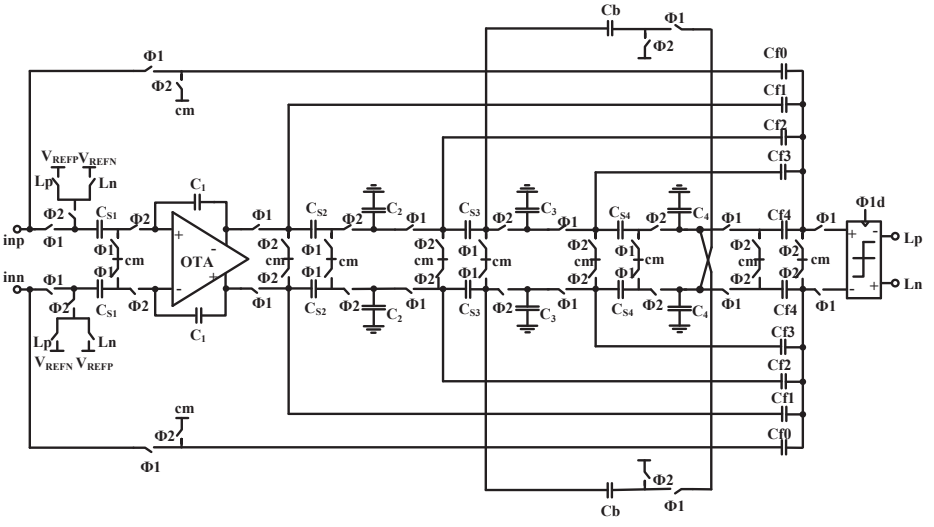

Figure 3.23: Schematic of the fourth-order active-passive delta-sigma modulator [12], © 2013, IEEE.

The main advantage of the first active stage is that it can suppress the comparator nonidealities, discussed in section 3.5, to a high extent. Additionally, the thermal noise from the succeeding passive stages is also decreased, resulting in significant capacitive area reduction.

The capacitors values are calculated to realize the optimal loop coefficients summarized in Table 3-2. C_{S1} and C_1 are determined from the kT/C noise requirement of the ADC. The capacitors C_{f0}-C_{f4} are calculated to create the feedforward coefficients. The size of the capacitors in the passive stages, i.e. C_{S2}-C_{S4} and C_2-C_4, can be significantly reduced because the preceding active integrator attenuates the related kT/C noise. Therefore, compared to the passive modulator presented in section 3.4.2, the total capacitor area is estimated to scale down by 50%. The ratios C_{Si}/C_i (i = 2,3,4) are calculated according to the optimal signal swing before the quantizer and the simulated SNDR [12]. Moreover, the resonator capacitor is determined to be 250fF to realize gain factor 1/64. The capacitors values are summarized in Table 3-3.

TABLE 3-3: CAPACITORS VALUES IN PF [12], © 2013, IEEE.

Sampling Capacitors	Integrating Capacitors	Feedforward Capacitors	Resonator Capacitor
		$C_{f0} = 1$	$C_b = 0.25$
$C_{S1} = 1$	$C_1 = 5$	$C_{f1} = 2$	
$C_{S2} = 0.25$	$C_1 = 16$	$C_{f2} = 3$	
$C_{S3} = 0.25$	$C_1 = 16$	$C_{f3} = 2$	
$C_{S4} = 0.25$	$C_1 = 16$	$C_{f4} = 5$	

3.6.3 Simulation Results

Table 3-4 summarizes the simulation results. Compared to the previous passive modulator in [3], the clock frequency is halved which is beneficial for power reduction in the ADC and the following decimating filter. Significant SNR improvement is achieved by cascading four integrators and also alleviating the problem of low swing at the quantizer input with the input feedforward architecture. It is important to point out that the total capacitor area is estimated to scale down by 50%. The sum of all capacitor values in the second-order passive ADC (Fig. 3.17) and the fourth-order active-passive modulator (Fig. 3.23) is 280pF and 138pF, respectively. The attained figure of merit (47fJ/step) makes this modulator a suitable candidate for low-voltage low-power ADC designs intended for medical applications.

3.7 Comparison of the Power Efficiency

The performance of the proposed modulators presented in this Chapter is compared with previously reported modulators using passive filter(s) in Table 3-5. Two commonly used FOMs given by (2.44) and (2.45) are applied for the comparison, where

TABLE 3-4: PERFORMANCE RESULTS AND COMPARISON WITH PREVIOUS PASSIVE MODULATOR.

	4^{th}-Order Act-Pass ΔΣM (Simulation)	$\Delta\Sigma M_{PP}$ Measurement
Technology	65nm CMOS	
Supply Voltage	0.7V	
Clock Frequency	256kHz	500kHz
Signal Bandwidth	500Hz	
Peak SNR	84dB	68dB
Peak SNDR	80.3dB	65dB
Power	400nW	430nW
Active Area mm^2	N/A	0.125
FOM fJ/step	47	296

TABLE 3-5: PERFORMANCE COMPARISON WITH REPORTED MODULATORS USING PASSIVE FILTER(S)

Ref., Year	Type	BW [Hz]	Sampling Rate[MHz]	SNDR [dB]	DR [dB]	Power [μW]	FOM_W[a] [pJ/step]	FOM_S[b]
[1] Chen, 1997	DT Passive	20k	10	67	78	250	3.41	157
[2] Chen, 2009	DT Passive	100k	104	74.1	80.5	830	1.0	159.7
[8] Yousry,2008	DT APDSM[c]	10M	640	56	54	5500	0.55	146.6
[9] Das, 2005	CT APDSM[d]	600k	256	N/A	86	5400	N/A	166.5
[3] Fazli, 2013	DT Passive	0.5k	0.5	65	65	0.43	0.3	144
[3] Fazli, 2013	DT APDSM	0.5k	0.25	70	70.5	1.27	0.49	156.5
[12] Fazli, 2013[e]	DT APDSM	0.5k	0.256	80.3	84	0.4	0.05	175

(a) FOM_W = Power/($2^{ENOB}\times2\times$BW) known as the Walden FOM
(b) FOM_S = DR(dB)+10log (BW/Power) known as the Schreier FOM
(c) DT-APSDM = Discrete-Time Active-Passive Delta-Sigma Modulator
(d) CT-APSDM = Continuous-Time Active-Passive Delta-Sigma Modulator
(e) Simulation results

FOM_W accounts for the SNDR, whereas the FOM_S considers the DR. The latter one favors high-DR ADCs. The passive $\Delta\Sigma M_{PP}$ modulator with 0.43μW power and medium resolution (68dB SNR from 0.7V) looks attractive when using FOM_W definition. When considering FOM_S, the hybrid second-order and fourth-order modulators present the FOM of 156.5 and 175, respectively, which demonstrate high power efficiency among the modulators [1]-[3], [8], [9]. In particular, the fourth-order modulator in [12] employing a feedforward architecture presents an impressive FOM when both FOM_W and FOM_S are applied.

3.8 References

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Chapter 4

Low-Voltage Low-Power ΔΣ Modulators

4.1 Introduction

The low-power ΔΣ modulators using the distributed feedback architecture and active (OTA-based) integrators (or filters) were described in Chapter 2. The low-power ΔΣ modulators using hybrid active-passive filters (**Papers 6, 7**) and a fully passive filter (**Papers 6**) were presented in Chapter 3. Both distributed feedback and input feedforward loop topologies were exploited in various designs in Chapter 3. This Chapter, however, focuses on the low-voltage design aspects of the low-power delta-sigma modulators. To do so, the low-voltage design challenges including the low switch overdrive voltage, the limited voltage headroom, the reduced signal swing and the performance degradation of the analog circuits are explained in details. Then the recent circuit techniques and innovations concerning the design of low/ultra-low voltage ΔΣ converters including the inverter-based integrator and the body-input circuits are reviewed in brief. Three modulators operating at 0.7V, 0.5V and 270mV supply voltage, presented in **Papers 3, 4, 5,** are introduced subsequently by the circuit-level approach. At the circuit-level, the low-voltage building blocks, suitable for nanometer CMOS technologies, are analyzed and presented according to the design requirements and constraints of the portable medical applications and medical implant devices. At the same time, low power consumption, as a main design requirement of these applications, is also emphasized in the design of the modulator building blocks. The full comparison of the proposed modulators to the state-of-the-art low-voltage modulators is also provided in the end of this Chapter.

4.2 Driving Force of the Supply Voltage Scaling

The main driving force of the supply voltage downscaling is the constant reduction of the minimum feature size of the modern CMOS technologies in favor of the high density and low power mainstream digital market. To maintain reliability and to avoid device breakdown, the maximum supply voltage needs to be reduced accordingly when moving to deep nanoscale processes. The supply voltage is predicted to be 0.5V for low-power digital circuits, at the 22nm technology node, by the year 2016 [1]. The V_{th} is also reduced, but not at the same rate as the supply voltage in order to limit the static leakage in digital circuits. This brings several difficulties and challenges in analog circuit design. A V_{th} of about 0.2V is forseen.

Another driving force of the supply voltage scaling-down is the great demands for low power consumption of the digital circuits. The static and dynamic power consumption for a CMOS logic gate, e.g. CMOS inverter, can be expressed as:

$$P_{static} = V_{DD} \times I_{Leakage} \tag{4.1}$$

$$P_{dynamic} \propto C_L \times V_{DD}^2 \times f \tag{4.2}$$

where V_{DD} is the supply voltage, $I_{leakage}$ is the leakage current of the gate, C_L denotes the load capacitance, and f is the operating frequency of the gate. The reduction of the supply voltage is very useful in minimizing both the static and dynamic power consumption. Particularly, the dynamic power, the main source of power dissipation in digital circuits, has a quadratic dependency to the V_{DD}. As a result, a significant power reduction can be achieved by downscaling of the supply voltage.

Apart from the technology constraints and the power requirements, another motivating drive for supply voltage reduction is the biomedical compatibility requirements [2]. Battery operated biomedical implant devices must be adopted to human body potentials, in the order of magnitude of several hundred mili-volts, to prevent additional heating in the sensitive body regions like human brain and heart.

4.3 Ultra-Low Voltage Design Challenges

4.3.1 Low Switch Overdrive

In switched-capacitor (SC) circuits like filters and delta-sigma modulators, the switch is a key component. The implementation of the switch is basically done by MOS transistors. To reduce the signal-dependent on-resistance, the CMOS switch is usually realized by parallel NMOS and PMOS transistors to form a transmission gate switch. The direct consequence of the reduced supply voltage in switch design is the low overdrive voltage, which results in increased switch on-resistance. The on-resistance for a simple MOS switch can be expressed as:

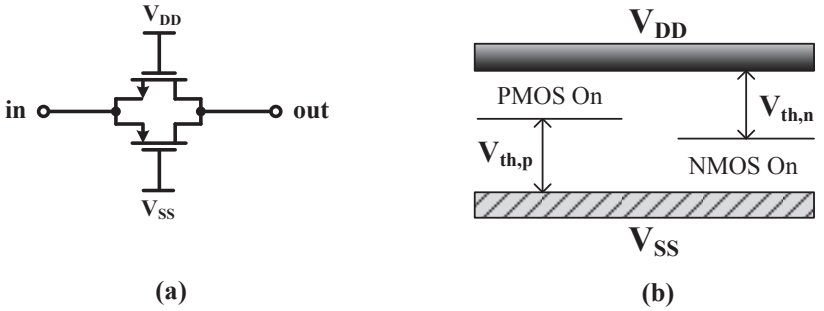


Figure 4.1: (a) Transmission gate switch (b) graphical representation of the switch operating range.

$$R_{on} = \frac{1}{\mu\, C_{ox} \frac{W}{L}(V_{GS} - V_{th})} \tag{4.3}$$

which is a function of device process parameters, geometry, and the overdrive voltage, i.e. V_{GS}-V_{th}. For a transmission gate switch, the on-resistance is the parallel on-resistance of both n-type and p-type transistors. For supply voltage higher than $V_{th,n}$+$|V_{th,p}|$ the CMOS switch is fully functional. For supply voltages lower than the sum of the threshold voltage of both transistors, this implementation no longer works. To illustrate this issue, a graphical representation of the switch operating range is shown in Fig. 4.1. The small gate voltage, due to the low supply voltage, limits the operating range of the switch. For instance, the NMOS transistor is "On" only for the input signal below V_{DD}-$V_{th,n}$, while the PMOS transistor is "On" only for the input signal higher than $|V_{th,p}|$. Both transistors are "Off" at the input mid-range. Therefore, for rail-to-rail switch operation, the supply voltage must be greater than the sum of the threshold voltages and the input signal amplitude. Higher gate voltage than the rated supply voltage has to be used for proper operation in ultra-low voltage designs. There are several solutions to overcome the problem of limited switch overdrive, e.g. low-V_{th} transistors [3]-[5], local switch bootstrapping [6]-[8], clock boosting [9]-[12], etc.

The recent development of the process technologies has provided low threshold voltage transistors, which enables higher overdriving capability for the switching transistors without using bootstrapping circuits. The low V_{th} transistor comes at the cost of additional mask and processing steps during fabrication, which is expensive. Moreover, the low V_{th} devices cause off-state leakage problem [13]-[15], which in the SC sampling circuits are signal-dependent. This nonlinear leakage current brings harmonic distrotion in the modulator output power spectrum. To reduce the effect of the nonlinear leakage or subthreshold current, an analog T-switch (AT-switch) has been introduced in [14] which offers reverse gate-source voltage V_{GS}. A subthreshold leakage suppression switch has been proposed in [15] that equalizes the voltage of the drain and

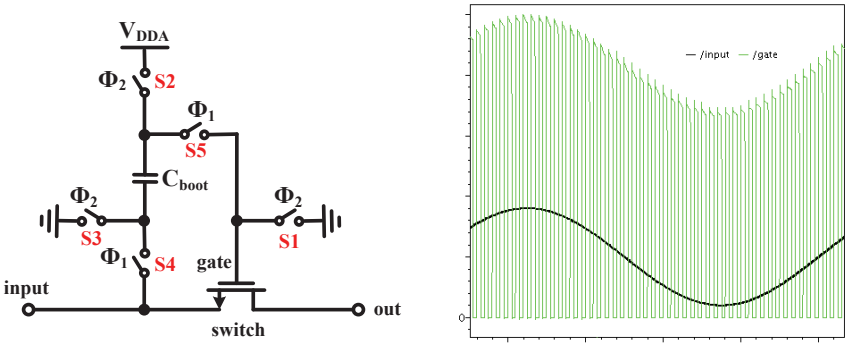


Figure 4.2: (a) Basic switch bootstrapping circuit (b) gate driving waveforms.

source terminals. The fundamental concept behind these switches can be explained simply by using the subthreshold current relationship [13], [15] given below:

$$I_{ds} \propto \frac{W}{L} . e^{\frac{V_{GS}-V_{th}}{nv_T}} . \left(1 - e^{\frac{-v_{DS}}{v_T}}\right) \tag{4.4}$$

where n and v_T represent the body effect cofficient and the thermal voltage, respectively. To suppress the leakage, the AT-switch scheme in [14] applies reverse V_{GS} reducing the first exponential term in (4.4), while the second scheme in [15] equalizes the drain and source voltage, v_{DS}, causing the last term to approach zero. The detailed transistor implementation of these switches can be found in the literatures [14] and [15].

Another solution to the switch driving problem in low-voltage environment is the local bootsrapping circuits [6]-[8]. These techniques impose large area due to large required capacitors. To adequately drive the switches, the bootsrapping circuits apply a gate-source voltage above the rated supply voltage, which can introduce reliability issue due to the gate-oxide breakdown. The basic idea of this switch is illustrated in Fig. 4.2 [16]. The circuit includes the main *switch*, a bootstrap switch, C_{boot}, and five switches S1-S5. During Φ_2, the C_{boot} is charged to V_{DDA}, and the gate of the *switch* is connected to ground which turns it off. During Φ_1, S4-S5 are closed to place the precharged capacitor potential ($\sim V_{DDA}$) across the gate and source of the switch, producing a constant overdrive voltage for the *switch* transistor. As a result, the on-resistance of the switch is decreased largely and becomes signal-independent. Therefore, the harmonic distortion due to the nonlinear leakage current are greatly suppressed. Advanced implementations of this switch can be found in [6], [17].

Another solution that alleviates the problem of low switch overdrive voltage is clock boosting. The maximum on-resistance of a CMOS switch occures when the input signal is near supply mid-level. In ultra-low voltage design environment, the on-resistance increases significantly. To sufficiently open and close the CMOS switch, the clock boosting or clock doubling scheme is used in [9] and [11] in order to provide enough

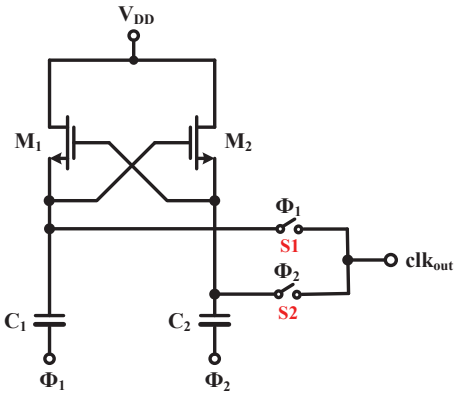


Figure 4.3: Basic switched-capacitor clock doubler circuit [19].

overdrive voltage necessary for the fast switching. Figure 4.3 shows a simplified clock doubler circuit [18], [19], in which the cross-coupled NMOS transistors, M_1 and M_2, charge the capacitors C_1 and C_2 to V_{DD}. When Φ_1 is low, the transistor M_2 turns off, while at the same time Φ_2 is high which turns the M_1 on. Therefore, the capacitors C_1 is charged to V_{DD}. When Φ_1 goes high, the top plate of C_1 is boosted to $2\times V_{DD}$. At the same time, S1 closes, which transfers the boosted voltage to the output. M_2 is switched on at this point, charging the C_2 to V_{DD}. In the next half clock cycle, when clock Φ_2 goes high, the top plate of C_2 is boosted to $2\times V_{DD}$, and will be transferred then to clk_{out} node when S2 is closed. The clock doubler circuit usually follows the clock outputs of a non-overlapping clock generation circuit [11]. For robust operation against process, voltage and temperature (PVT) variations in ultra-low voltage design, the use of the clock boosting approach [20] appears to be essential, but at the cost of larger area and higher power consumption.

4.3.2 Limited Available Voltage Headroom

The direct consequence of the supply voltage scaling-down in analog design environment is the limited available voltage headroom and low overdrive voltage for the transistors. The traditional amplifiers with differential input piar have the fundamental restriction of the low input common-mode range (CMR) because V_{th} does not scale with the same rate as the supply voltage when moving into deep submicron CMOS technologies. Therefore, the challenging task is to maintain a wide common-mode rejection ratio (CMRR) while achieving sufficient analog performance in the presence of PVT variations. In an operational amplifier, the most critical part with respect to low voltage design is the input stage. Figure 4.4 shows the classic differential input pair with NMOS and PMOS input transistors. In the input pair shown in Fig. 4.4a, the minimum allowable input voltage operating in strong inversion regime is equal to:

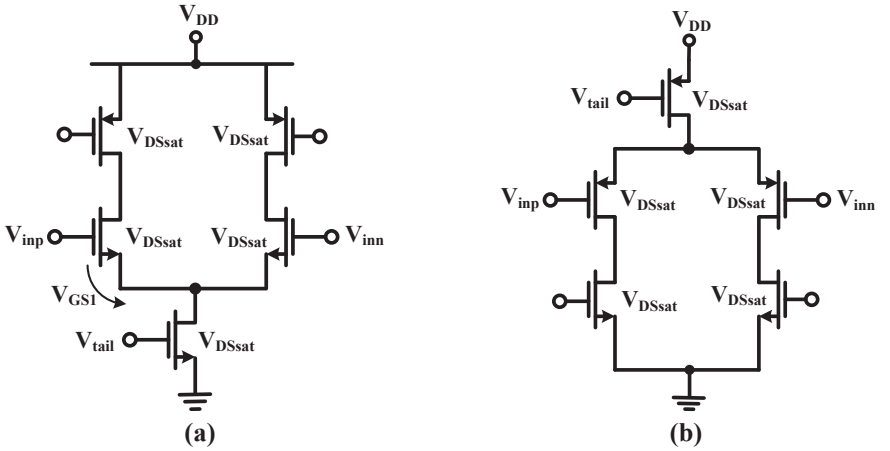


Figure 4.4: Classical differential input pairs (a) with NMOS input (b) with PMOS input.

$$\begin{aligned} V_{in_{CM}}(\min) &= V_{GS1} + V_{DSsat} + |\Delta V_{th}| \\ &= V_{th,n} + V_{OV} + V_{DSsat} + |\Delta V_{th}| \end{aligned} \tag{4.5}$$

and the maximum allowable input voltage is given by the level that places the input transistors at the edge of the triode region:

$$V_{in_{CM}}(\max) = V_{DD} - V_{DSsat} - V_{th,n} \tag{4.6}$$

with saturation voltage V_{DSsat}, overdrive voltage V_{OV} and $|\Delta V_{th}|$ as a certain process variation. With supply voltage of 0.9V, threshold voltage of 0.25V and V_{DSsat} of about 0.1V in moderate inversion region, the resulting input CMR is only 0.1V. The minimum supply voltage V_{DD} can be expressed as:

$$V_{DD,Min} = 3 \times V_{DSsat} + |\Delta V_{th}| \tag{4.7}$$

which can be lower than 0.5V. Clearly seen from (4.5) and (4.7), the minimum allowable input CM level is limited by the V_{th} and $|\Delta V_{th}|$, whereas the minimum possible supply voltage is limited by the V_{DSsat}, which unfortunately does not scale with technology [11]. Moreover, since the threshold voltage in sub-nanometer processes does not scale with the same rate as the V_{DD} for leakage suppression, the transistor overdrive voltage is mainly restricted by the V_{th}. Under subthreshold operation with V_{OV} ≈ -50mV, the threshold voltage hard limit can be alleviated to some extent, and the input CM level can be pulled down for low supply operation. Similarly, the minimum and maximum allowable input voltage operating in strong inversion region can be derived for the input pair shown in Fig. 4.4b as follows:

$$\begin{aligned} V_{in_{CM}}(\min) &= |V_{SG1}| - V_{DSsat} - V_{DSsat} \\ &= |V_{th,p}| - V_{DSsat} \end{aligned} \tag{4.8}$$

$$V_{in_{CM}}(\max) = V_{DD} - V_{DSsat} - |V_{SG1}| = V_{DD} - 2V_{DSsat} - |V_{th,p}| \quad (4.9)$$

The minimum supply voltage V_{DD} can be expressed as:

$$V_{DD,Min} = 3 \times V_{DSsat} + |\Delta V_{th}| \quad (4.10)$$

which can be under 0.5V. Obviously, $|V_{th,p}|$ is the limiting factor for scaling down the input CM level given by (4.8). Nevertheless, comparing (4.5) with (4.8) shows that the minimum achievable CM level can be decreased significantly with PMOS input-pair arrangement. In addition, the input CMR drops heavily by two saturation voltages from the power supply rail, V_{DD}.

In (4.7) and (4.10) it is assumed that the input CM level is fixed at a constant level. By regulating the input CM level according to V_{th} variation, the term $|\Delta V_{th}|$ can be canceled out [11], which therefore reduces the supply voltage by one $|\Delta V_{th}|$. Assuming a $V_{DSsat} \approx$ 100mV, the supply voltage can drop down to 300mV. As mentioned above, in very low voltage operation (below 300mV), there exist very tight and narrow ranges for the input CMR, overdrive voltage, and the maximum voltage swing that the analog amplifier can still operate with. This demands a careful analog design and approperiate circuit topologies for the robust operation against PVT variations.

To summarize, for supply voltage above 0.5V the design limiting factor is the V_{th}, whereas below 0.5V the main limitation is caused by the V_{DSsat}, which is not scalable with thechnology scaling.

In order to alleviate the mentioned issues related to the V_{th} and V_{DSsat}, several circuit techniques have been proposed such as analog design using low-V_{th} transistors [3]-[5], inverter-based amplifiers [10]-[12], bulk-driven Opamps [21]-[23], and forward body biasing technology [24]-[27].

The recent process development has provided low-V_{th} transistors, which enable simpler analog design in low-voltage operation, while in turn the digital circuits benefit from standard V_{th} transistors for leakage suppression. The use of low-V_{th} transistors can relieve the fundamental problem of limited headroom and low overdrive voltage.

The inverter-based amplifier in [10] and [11] makes use of a supply voltage lower than the sum of the threshold voltage of both NMOS and PMOS transistors. The inverter is then biased in subthreshold region, also called as a class-C inverter, in which the V_{th} constraint is eliminated, facilitating the reduction of the supply voltage. Another aspect we must emphasize here is that the V_{DSsat} is the real hard limit in very-low voltage operation (under 300mV) because the minimum supply can be set to $2 \times V_{DSsat} + V_{swing}$ [11]. V_{swing} represents the output swing that the inverter needs to operate with in a delta-sigma modulator loop filter.

Buck-driven operational amplifier is another design technique that overcomes the threshold voltage constraint and the input CMR limitation. In bulk-driven amplifier, also known as back-gate amplifier, the differential signal is given to the bulk terminal of the input transistors rather than the gate, a wide CMR is achieved in this manner.

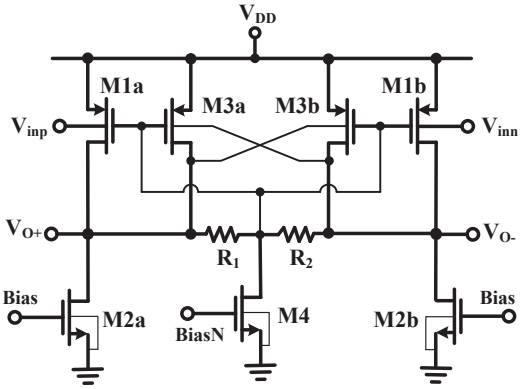


Figure 4.5: bulk-driven amplifier stage with local CMFB [22], © 2004, IEEE.

A simple single stage fully differential amplifier is shown in Fig. 4.5 in order to explain the concept of body-driven amplifier. The differential inputs are given to the bulk of M1a and M1b, and the body transconductance, g_{mb}, of these devices provides the input transconductance. M2a and M2b are NMOS load transistors acting as current sources. The tail current source has been removed entirely, which eliminates one V_{DSsat} between the positive and negative supply rails, providing larger voltage headroom. A local common mode feedback (CMFB) is provided using two resistors and two transistors, M3a and M3b. The resistors R_1 and R_2 detect the common mode voltage of the outputs, and feed it back to the gates of the PMOS transistors M1a, M1b, M3a, M3b for properly setting the bias current of each branch. A level shifting from 0.25V at the output to 0.1V at the gates is performed by sinking a small current through the transistor M4. To enhance the amplifier CMRR, the bulk of M3a and M3b is used to create a cross-coupled pair which adds up a negative conductance, $-g_{mb3}$, to the total output conductance. To clearly explain the impact of the bulk-driven cross-coupled pair on the CMRR, the differential mode DC gain and common-mode gain are derived according to (4.11) and (4.12):

$$A_{Diff} = \frac{g_{mb1}}{g_{ds1} + g_{ds2} + g_{ds3} + 1/R - g_{mb3}} \tag{4.11}$$

$$A_{CM} = \frac{g_{mb1}}{g_{ds1} + g_{ds2} + g_{ds3} + g_{m3} + g_{mb3} + g_{m1}} \tag{4.12}$$

where g_{mbi}, g_{mi} and g_{dsi} are the body transconductance, the gate transconductance, and the output conductance of the ith transistor in the amplifier, respectively. The negative conductance in (4.11) assists in boosting the differential DC gain, whereas the term $g_{m3} + g_{mb3}$ helps to reduce the CM gain of (4.12), both help to increase the CMRR absolute value because it is calculated as $|A_{Diff}/A_{CM}|$. As a result, the local CMFB circuit enables an inherent common-mode rejection, whereas a large input CMR is achievable from a

0.5V supply voltage equal to the V_{th} of the standard device in 0.18μm process. By cascading two equal gain stages shown in Fig. 4.5, and applying the Miller compensation concept for the frequency compensation, a two-stage amplifier with higher attainable DC gain can be constructed [28], [29].

There are several drawbacks associated with the use of bulk-driven transistors compared to the gate-driven transistors. The main drawback is that the body transconductance is much lower than the gate transconductance with the same device dimention and bias current. Therefore, it is prone to more input-referred noise. As a result, larger device dimention and bias current have to be used to obtain the same transconductance as the gate-input device, which significantly increases the power consumption.

In addition to the gate, the channel behavior of a MOS transistor can also be regulated from the body terminal. In the forward body bias technique utilized in [26] and [27], the body terminal of the PMOS devices are tied to $V_{DD}/2$ (the modulator CM voltage) to further reduce the threshold voltage. The threshold voltage of MOSFET is well-known as:

$$V_{th} = V_{th0} + \gamma(\sqrt{|V_{SB}| + |2\phi_f|} - \sqrt{|2\phi_f|}) \tag{4.13}$$

where V_{th0} is the threshold voltage with $V_{SB} = 0$, γ is the body-effect coefficient, ϕ_f is the *Fermi* potential, and V_{SB} is the voltage difference between body and source terminals. By increasing V_{SB} the threshold voltage decreases. As a practical example, the PMOS transistors in the preamplifier circuit [27] in **Paper 4** use a $V_{SB} = V_{DD}/2$ in order to reduce $V_{th,p}$ for operation at 0.5V supply. It should be noted that when a forward bias voltage is applied across the body-source junction, there exists a potential risk of latch-up, which requires a careful and serious design consideration. As a result, for a robust circuit operation, too much forward biasing of body-source junction must be avoided.

4.3.3 Decreased Signal Swing

As the supply voltage reduces in a certain process, the same does for the amplifier output swing. To illustrate this, consider the simplest amplifier in a common source configuration with a MOS load, as shown in Fig. 4.6. The maximum peak-to-peak output swing, $V_{out,pp}$, is V_{DD}-$2V_{DSsat}$. With constant V_{DSsat} of the technology, a decrease in V_{DD} will result in a reduced output swing. For instance, with a V_{DD} of 0.5V and V_{DSsat} of 0.15V, the output swing is only 0.2V, which is not sufficient for many applications.

The output swing of an OTA directly determines the output swing of the integrators, which indeed defines the reference voltage of the target ΔΣ modulator. As a consequence, the maximum input signal, $V_{in,max}$, that determines the dynamic range (DR) of the ADC at a given input-referred noise floor P_n is limited by the reference voltage directly or the OTA swing indirectly. The DR can be derived as:

$$DR = 10\log\frac{V_{in,\max}^2 / 2}{P_n + P_D} \tag{4.14}$$

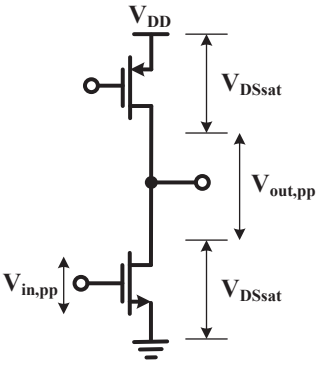


Figure 4.6: Illustration of the input and output voltage swing in a basic common source amplifier with MOS load.

where P_D is the input-referred distortion performance. Obviously seen from (4.14), the low supply voltage introduces challenges to high DR delta-sigma ADC designs. To maintain the same dynamic range in low supply voltage, the noise floor has to be decreased and the distortion performance must be improved, which in both cases the ADC will require higher current consumption, or more power dissipation.

4.3.4 Analog Performance Degradation

The decrease of the supply voltage obviously results in performance degradation in the active componets, and ultimately the ADC. Due to limited headroom, cascoding does not exist in low-voltage analog design. Also, keeping all stacked transistors in moderate or strong inversion region is impossible. Therefore, the transistor characteristic degrades in the weak inversion, which reduces the analog performance parameters such as DC gain and GBW. To boost these parameters cascade of amplifying stages has to be chosen, which is more power hungry. Especial low-power circuit techniques are required to enhance the performance.

4.4 Low-Voltage Modulator Circuits and Techniques

In this section, the most recent advancements of the low-voltage low-power ΔΣ modulator designs are discussed briefly with special emphasis on low voltage operation. The main circuit-level techniques and architectural approaches for reducing the supply voltage of the modulators will be highlighted. In the section (4.5), the author contributions to the field are also included. The design challenges in low-voltage environment discussed in section 4.3 can be classified into two main categories: some issues are related to the design of the sampling switch, while others are associated with

the design of analog circuits. The state-of-the-art modulators that will be discussed in this section are to tackle the issues in one or both categories. A 0.7V ΔΣ modulator using class-C inverter as an amplifier has been introduced by Chae in [10], which employs boosted clock signals in order to mitigate the switch driving problem. A 250mV ΔΣ modulator using class-C inverter biased near threshold voltage has been proposed by Michel in 2012 [11], which exploits a clock boosting scheme to alleviate the problem of the low switch overdrive voltage. The ΔΣ modulator operating at 0.5V supply voltage in [14] makes use of the low V_{th} (0.1V) devices of a 0.15µm FD-SOI process, in which the subthreshold leakage current due to the low V_{th} switches is suppressed by special switching scheme, so called analog T-switch (AT-switch).

4.4.1 Inverter-Based SC Integrator

Inverter is the simplest amplifier composed of only two transistors. The tail current source in typical OTA topologies is omitted inherently in the inverter structure with the penalty of loss in the CMRR, but in turn the minimum supply voltage can be decreased down to $2\times V_{DSsat}$, irrespective of the output signal swing. It is important to mention that the limiting factor in supply voltage scaling-down is the V_{DSsat}, and is independent of the V_{th}. The V_{DSsat} is about 0.1V-0.15V. At the edge of the strong inversion, it is 0.15V, whereas in the weak inversion it is 0.1V, independent of the process type, the value of V_{th}, and the transistor dimension [28]. To reduce the minimum operating voltage of the traditional modulators, the OTA in the integrator can be replaced by a simple inverter.

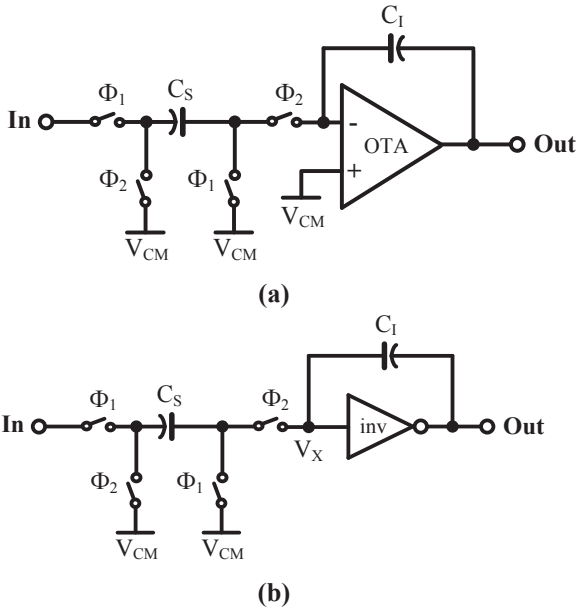


Figure 4.7: (a) Conventional SC integrator using OTA (b) SC integrator using inverter [10], © 2008, IEEE.

OTA composes the main building block of the ΔΣ modulators, and determines the major part of the total power consumption. To reduce the power consumption, an inverter can be used as an alternative to the power-hungry OTA. Recalling from (4.1), the static short circuit current drawing from V_{DD} to ground limits the use of the inverter for supply voltages greater than the sum of V_{thn} and V_{thp}. For power supply voltages lower than $V_{thn}+|V_{thp}|$, it behaves as a class-C inverter that minimizes the static current. Figure 4.7 shows the SC integrators using OTA and inverter. Unlike the OTA, the inverter has only one input terminal. The SC inverter-based integrator then does not have a virtual ground as a reference at its input. The reference node depends on the inverter's input offset, which degrades the integrator performance. As a result, the unknown offset value at node V_X has to be cancelled out by using an offset cancellation scheme like auto-zeroing technique [30]. In applications where low voltage operation is not essential, cascode inverter can be replaced in order to boost the dc gain, but at the cost of reduced signal swing [31].

Correlated double sampling (CDS) as an auto-zeroing technique has been used in [10] to cancel out the offset and to produce a virtual ground similar to a conventional integrator using OTA (Fig. 4.7a). The offset cancellation comes at the cost of a bulky C_C capacitor as big as the feedback capacitor C_I. Figure 4.8a shows the inverter-based integrator with embedded offset-cancellation technique. Additional capacitor C_C is added to store the offset value in the sampling phase, ϕ_1. During ϕ_1, when the input is sampled onto C_S, the inverter is configured in a unity-gain arrangement, storing the offset voltage into C_C capacitor. During ϕ_2, the stored charge in C_S is transferred through C_I feedback capacitor. A negative feedback is then formed through C_I, pushing the node V_g to a signal ground.

As mentioned before, the inverter has no tail current source, which causes the biasing condition to be undefined and the CMRR to be poorer. In fact, it is the input CM level that determines the bias current. At the very low voltage operation, the input CM voltage is largely sensitive to supply voltage variation, resulting in shift in the bias current. As a consequence, the analog performance parameters such as the dc gain, GBW, and slew rate are affected. The integrator shown in Fig. 4.8 can be used in a pseudo-differential configuration to mitigate the lost CMRR problem and to surmount the drawback of the undefined operating bias voltage by using a SC CMFB [32]. Figure 4.10 shows the pseudo-differential integrator. A simple power-efficient SC CMFB is utilized, as shown in Fig. 4.10b. In ϕ_1 phase, the C_M is discharged to ground, while in ϕ_2 phase two C_M capacitors make a CM detector, detecting the common-mode level of the two integrator outputs and feeding the signal to the virtual ground node, V_g.

Both single-ended integrator shown in Fig. 4.8 and the pseudo-differential integrator shown in Fig. 4.10 introduce a half clock delay to the signal, a distinct difference between the conventional full delay integrator and an offset-canceled inverter-based integrator. Therefore, the half clock delay of the loop filter is compensated in the DAC feedback branch in the digital domain by means of a half delay latch. The realized first-order modulator using half clock delay integrator and half delay element in the feedback path is shown in Fig. 4.9 for clarification.

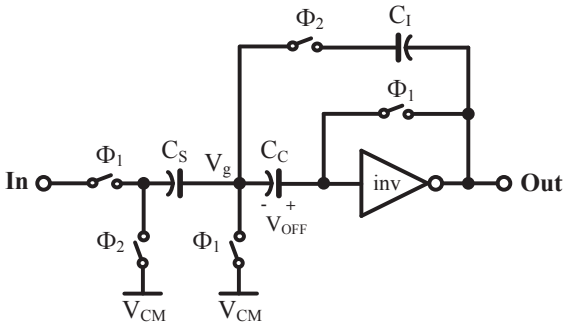


Figure 4.8: Inverter-based SC integrator using offset cancellation [10], © 2008, IEEE.

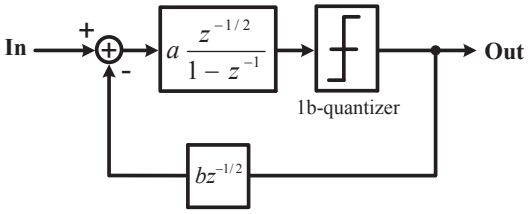


Figure 4.9: First-order modulator topology using half clock delay integrator and half delay DAC element.

4.4.2 0.5V SC Integrator Using Low V_{th} Transistors

Low V_{th} devices facilitate the design of switches and analog building blocks because more overdrive voltage and headroom are available. The main bottleneck is that the switch with low V_{th} device is leakier. In particular, the nonlinear leakage current in the sampling switch is signal-dependent and any nonlinear behavior causes distortion to the signal. The 0.5V modulator proposed by Ishida in [14] introduces an AT-switch scheme that mitigates the subthreshold leakage problem associated with the use of low V_{th} devices. The process that has been used in this implementation is a 0.15µm FD-SOI process with a 0.1V threshold voltage. Figure 4.11 shows the SC integrator with AT-switch scheme. The AT-switch consists of two switches *SW1* and *SW2*. In the sampling switch *SW1*, the transmission gate is replaced by two analog T-switch (Ma1-Ma3 and Mb1-Mb3), wherein two series-connected NMOS or PMOS are controlled by the additional transistor, Ma1 or Mb1, at their intermediate nodes. The AT-switch works in a way that a negative V_{GS} is applied across the gate-source terminal, which according to (4.4) reduces the first exponential term. Therefore, the overall subthreshold current decreases. Figure 4.11 shows the leakage reduction by applying an intermediate voltage of $V_{DD}/2$ in each T-switch. In the sampling phase, a reverse voltage is applied to one of

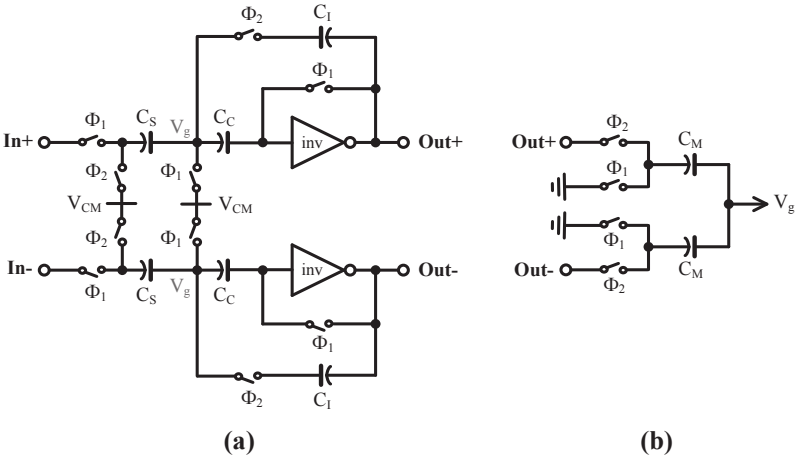


Figure 4.10: (a) Pseudo-differential integrator (b) SC CMFB. In phase ϕ_1, the C_M is discharged to ground, while in phase ϕ_2 two C_M capacitors detect the CM level [10].

the MOS switches Mc1 or Mc2 to block the leakage. For example, when the input voltage is V_{DD} (or V_{SS}), the voltage at node A is approximately V_{DD} (or V_{SS}), therefore with $\Phi 2d = V_{SS}$ and $\overline{\Phi 2d} = V_{DD}$ a reverse V_{GS} is applied to Mc2 (or Mc1). In addition, the MOS switch M_e corresponding to the *SW4* in Fig. 4.11b is also reversely biased because the voltage at node B is $V_{DD}/2$ while its gate is connected to $\Phi 2 = V_{SS}$.

In the integrating phase, a $V_{DD}/2$ potential is connected between Ma2 (or Mb2) and Ma3 (Mb3) through Ma1 and Mb1, resulting in a reverse voltage across Ma3 and Mb3, regardless of that the input is V_{DD} or V_{SS}. At the same time, the MOS switch Md corresponding to the *SW3* is also reversely biased because the gate is connected to $\Phi 1 = V_{SS}$ and the source is tied to analog ground $V_{DD}/2$.

It should be noted that the natural way to decrease the switch off-state current is to increase the length of a transistor significantly, which intolerably enhances the switch on-resistance. Therefore, novel solutions are required to suppress the sub-V_{th} leakage without unacceptably increasing the on-resistance. The AT-switch approach is one of such efforts that effectively limits the leakage current due to a low V_{th} transistor, but compared to a conventional SC integrator, shown in Fig. 4.11a, it employs twice the number of transistors and the complementary clock phases ($\overline{\Phi 1d}$ and $\overline{\Phi 2d}$) should also be generated.

Two 0.5V first-order ΔΣ modulators using conventional sampling scheme and the presented AT-switch have been implemented on silicon within the same chip. The experimental results provided in [14] and [33] show that with the use of the AT-switch the harmonic distortion seen by the conventional circuit due to the nonlinear leakage current of low V_{th} is greatly suppressed. The signal-to-noise and distortion ratio (SNDR) by analog T-switch exceeds that of the conventional switch by 8.1dB.

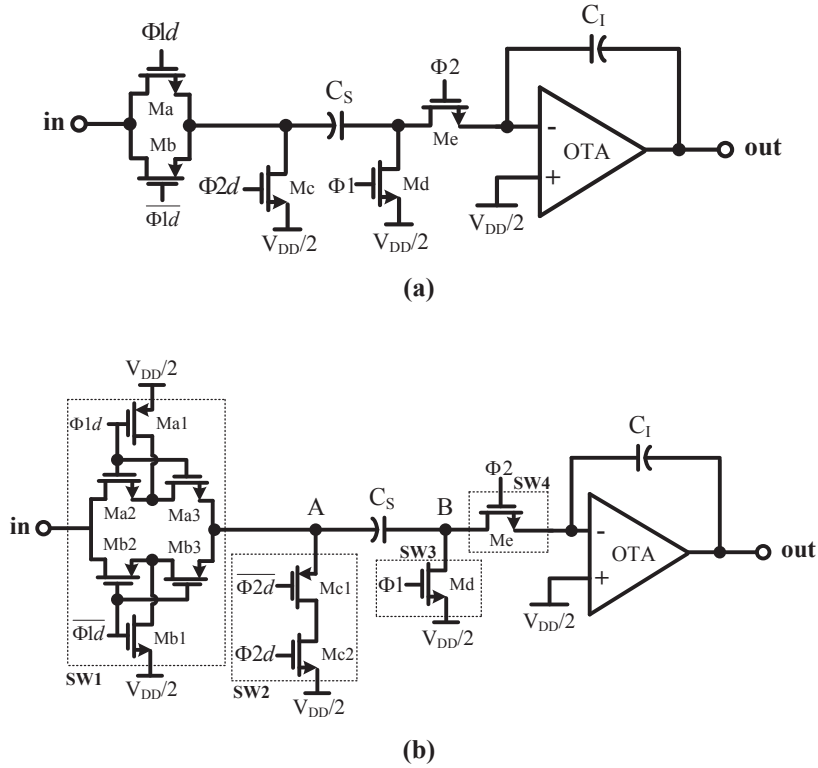


Figure 4.11: Schematic of (a) the conventional SC integrator and (b) the SC integrator using AT-switch scheme. Ma1-Ma3 and Mb1-Mb3 are T-switch. All MOS switches are driven by non-overlapping clocks with full swing from V_{SS} to V_{DD} [14], © 2006, IEEE.

4.4.3 0.5V CT Integrator Using Body-Input OTA

The combination of the reduced supply voltage and high device threshold voltage of future nanoscale processes [1] poses serious challenges on analog circuit design due to the limited overdrive voltage and available headroom. True low-voltage analog circuit design are addressed in this work [29] without using special low V_{th} devices [3]-[5] or internal voltage boosting [6]-[8]. The 0.5V operation is enabled by using body-input amplifiers, a body-input gate-clocked comparator, and a return-to-open DAC scheme.

The 0.5V ΔΣ modulator employs a continuous-time (CT) implementation, which is superior to its discrete-time (DT) counterpart in two senses: (i) the design of the switch, a challenging component in the low-voltage integrator design, is completely eliminated

in the RC-integrator (or CT integrator), relieving the settling time constraints in the OTA. Therefore, the bandwidth requiremnets of the OTA will be more relaxed compared to the SC realization, an advantage in the low power design. To conclude, the key advantage of the CT modulator implementation is the removal of the switch, that is very difficult to design around or below 0.5V supply voltage; (ii) the CT modulator has an inherent anti-aliasing filtering that greatly mitigates the requirements on the preceding filters [34]. On the other hand, the CT modulators suffer from the clock related nonidealities such as the clock jitter [35], [36] and excess loop delay [37]. The discussions related to these issues are out of the scope of this thesis. The focus here is merely on the circuit techniques and architectural improvement that enable the low-voltage operation.

Figure 4.12 shows a differential RC-integrator using a bulk-input OTA and a return-to-open (RTO) DAC. The clock signal Φ is the sampling clock which is used in the dynamic comparator, while Φ_{DAC} is the DAC clock signal delayed from Φ to allow the comparator outputs to settle completely. The RTO DAC scheme used in the RC integrator eliminates the additional switch connected to V_{CM} = 0.25V, as shown in Fig. 4.13, in order to enable low voltage design. The corresponding switch that resets the DAC output node to zero, with gate and source connected to 0.5V and 0.25V voltages and with |Vth| of only 0.2V, is not functional because of the weak overdrive voltage of only 50mV. In return-to-zero (RZ) signaling (in the Φ_{RZ} interval) the DAC output node is reset to a DC level (V_{CM} = 0.25V in this work) to clear the node from the data dependent charges (transients) which improves the linearity of the modulator. In the RTO scheme, however, the DAC output nodes in Φ_{RZ} interval is open-circuited and remains floating. Therefore, no current flows from the DAC output node to the integrator capacitor, C_I, meaning that the floating end of R_{DAC} resistor is connected to the input CM level of the integrator OTA. This implies return-to-zero functiality without applying the additional RZ switch.

The RC-integrator shown in Fig. 4.12 applies a two-stage body-input (or bulk-driven) OTA, whose first and second stages make use of identical amplifier topology, as demonstrated in Fig. 4.5. Despite the very low voltage operation, the relatively high power consumption and large area prevent the corresponding delta-sigma modulator to achieve high power efficiency, evaluated by the typical figure-of-merit (FOM). The reason is that the body-input transistors require approximately five times more current than the gate-input transistors to obtain an equal input transconductance, g_m. Several other drawbacks were also enumerated previously in section 4.3.2 for the body-input amplifiers.

The comparator in this work [29] uses the body terminal of the input transistors as input, while the gate is clocked at the rate of the sampling frequency. Figure 4.14 shows the circuit schematic. It comprises a preamplifier and a latch, which are clocked by Φ and $\overline{\Phi}$, respectively. When Φ is low, the differential input with CM level of $V_{DD}/2$ is amplified by the body transconductance of the M1a and M1b. The latch comprising the M3a, M3b, M4a, and M4b is composed of the simple back-to-back inverters with body inputs.

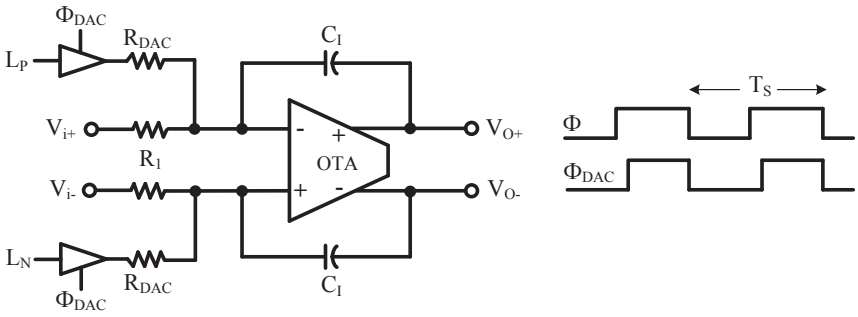


Figure 4.12: Fully differential CT integrator. L_P is the digital output of the modulator and L_N is the complementary digital output.

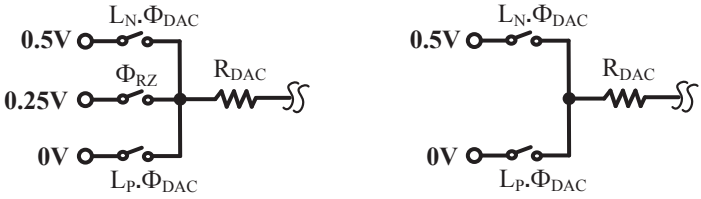


Figure 4.13: Illustrative diagram of the return-to-zero (RZ) DAC (left) and return-to-open (RTO) DAC (right).

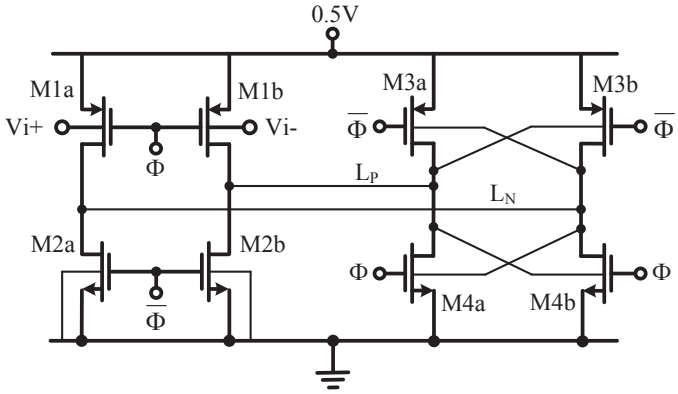


Figure 4.14: Schematic of the body-input gate-clocked comparator. L_P and L_N represent the modulator digital outputs [29], © 2007, IEEE.

The modulator uses a 3rd-order cascade-of-integrators feedback (CIFB) topology designed and implemented in 0.18μm triple-well CMOS technology using only standard MOS transistors. Clocked at 3.2MHz, the modulator achieves 76dB peak SNR, 74dB peak SNDR over a 25kHz signal bandwidth from a 0.5V supply voltage. It consumes 300μW total power.

4.5 Proposed Low-Voltage Low-Power ΔΣ Modulators

The recent circuit techniques, advancements and innovations concerning the design of low/ultra-low voltage ΔΣ converters were reviewed in brief so far. The low-voltage design challenges were also discussed. This section presents the design of three modulators operating at 0.7V, 0.5V and 270mV power supply voltages by the circuit-level approach in a digital 65nm CMOS process. The aim is to tackle the challenges that were addressed in section 4.3. At the circuit-level, low/ultra-low voltage building blocks suited for advanced nanometer CMOS technologies will be designed and analyzed according to the performance requirements in the medical applications and medical implant devices.

4.5.1 A 0.5V 250nW Passive ΔΣ Modulator

A 0.5V ultra-low-power 2nd-order DT modulator is presented in **Paper 4** intended for medical implant devices. To enable operation near 0.5V supply voltage, the conventional active integrators are replaced by the power-efficient SC passive (OTA-less) integrators. The modulator building blocks, including the preamplifier, the comparator and latch and the clock generation circuit are adapted to operate at 0.5V power supply. A low-noise and gain-enhanced single-stage preamplifier is developed using a partially body-driven technique. The low-pass passive filter of the second integrator is gain-boosted using a charge redistribution amplification scheme, producing a passive voltage gain of 5 (or 14dB). The designed modulator can also function at 0.45V with input CM voltage of 0.225V, but the SNR drops significantly to 52dB, due to the very low available overdrive voltage for the switches and the comparator's speed and performance degradation.

As explained in section 4.4, the body-input OTA and body-input gate-clocked comparator in [29], [38] and the class-C inverter amplifier in [10], [11] were two recent design efforts that eliminate the constraint on the V_{th}, leading to an ultra-low voltage operation of 0.5V and 0.25V, respectively. A body-input OTA requires several time larger bias current than a gate-input OTA to obtain an equal g_m, thereby preventing this modulator to achieve a high power-efficiency. In addition, the inverter amplifier biased near V_{th} in [11] needs special biasing and CMFB circuits that can operate with 0.25V supply voltage. Moreover, the modulator requires charge pump [39] clock boosting circuits that can elevate the clock level for sufficient switch driving, thereby increasing the circuit complexity and thus the total power consumption of the target modulator. Both mentioned low-voltage techniques are relying on the power-hungry active filters

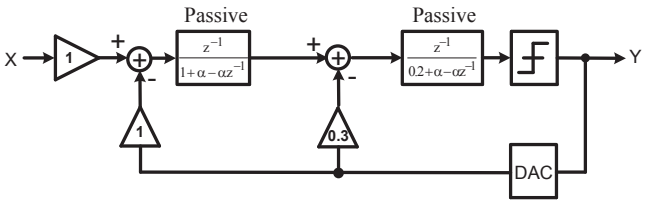


Figure 4.15: Block diagram of the scaled single-loop second-order modulator topology. Factor α in a passive integrator is defined as the ratio of the integrating capacitor C_i and sampling capacitor C_{Si}, i.e. $\alpha = C_i / C_{Si}$.

in which analog circuit design is a challenging task in 0.25V-0.5V supply voltage, due to the limited headroom and small signal swing. The aim of this work is to design a 0.5V ultra-low-power (below 1μW) ΔΣ converter by avoiding power-hungry active integrators and the power penalty associated with the additional circuit overhead.

4.5.1.1 Modulator Architecture

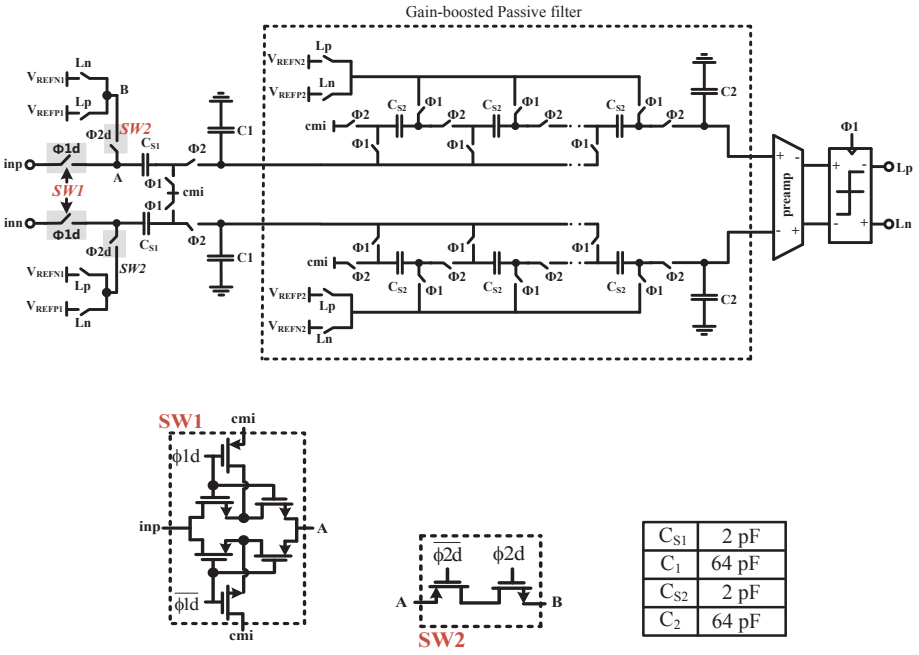
Figure 4.15 shows the scaled modulator topology in that a second-order, single-loop, distributed feedback topology with one-bit quantizater is selected due to its simplicity and linearity. The linearity requirement is more relaxed as no amplifier is involved in the passive loop filter. Therefore, a full scale amplitude can be applied at the modulator input without being overloaded because the signal components in the passsive and prior to the one-bit quantizer experience a large attenuation. Due to this attenuation, the DAC reference level related to the second stage can be scaled down proportionally to improve the loop stability. The loop coefficients are chosen to be *a1*, *b1*, *a2*, *b2* = 1, 1, 1, 0.3. The low signal bandwidth (up to 500 Hz) of the target medical application allows the usage of a relatively large oversampling ratio (OSR), reducing the contribution of the *kT*/*C* noise to the signal band. In this way, also the capacitor size of the passive integrators and consequently the power consumption can be reduced.

4.5.1.2 Low-Voltage Building Blocks

The overall modulator schematic is shown in Fig. 4.16. It comprises the following building blocks that will be explained in details in this section: the passive low-pass filter, the gain-enhanced preamplifier, the single-bit quantizer, the switches and non-overlapping clock generation circuitry.

A. Low-Voltage Passive Low-pass Filter

The SC passive filters are very suitable for the low voltage operation as long as a sufficient overdrive voltage is provided for the switches to operate correctly. In other words, the limited switch overdriving problem is the only obstacle in designing the low-voltage passive filters. This switching problem can be mitigated simply by the use of low V_{th} transistors or by boosting the clock voltage at the gate of the switch. The first



C_{S1}	2 pF
C_1	64 pF
C_{S2}	2 pF
C_2	64 pF

Figure 4.16: Schematic of the second-order passive ΔΣ modulator proposed in **Paper 4** [27]. The labeled *SW1* and *SW2* switches represent the analog T-switch with low V_{th} transistors. The rest of the switches are transmission gate type. © 2013, IEEE.

integrator in Fig. 4.16 consists of a simple passive filter which is composed of the C_{S1} and C_1 capacitors. The second integrator, composed of the C_{S2} and C_2 capacitors, uses a gain-boosted filter using charge redistribution scheme. The main sampling switch, i.e. *SW1*, employs analog T-switch [14], discussed in section 4.4.2, in order to suppress the nonlinear leakage current of the low V_{th} transistors in the switches. The operation mechanism, fundamentals, and circuit nonidealities of the passive low-pass filters were discussed in details in Chapter 3.

Figure 4.17 shows the gain-boosted passive filter [40] used in the second stage of the modulator (Fig. 4.16). Special attention should be given to the switch design. Using simple NMOS switch with low V_{th} (~0.15V), the marked switch overdrive is near zero when the input signal is at its peak, i.e. 0.4V. Therefore, to correctly open and close the switch, a transmission gate switch seems to be essential. The minimum overdrive when V_{IN} offset is 0.2V/0.25V is 0.15V/0.1V, much higher than that of a basic NMOS switch.

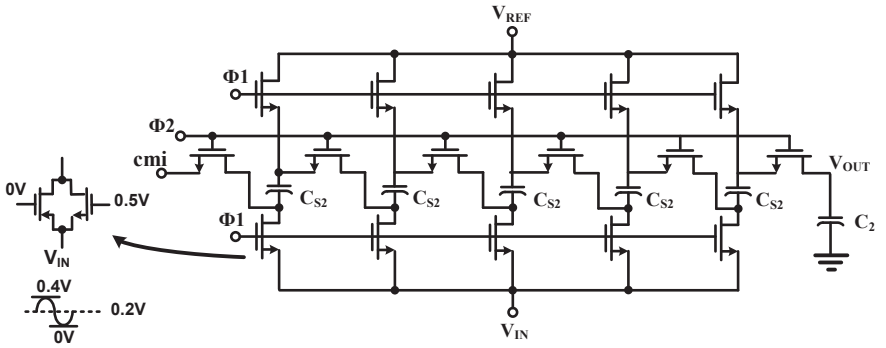


Figure 4.17: Passive low-pass filter using charge redistribution gain-boosted scheme. Single-ended is shown for simplicity. All switches driven by *Φ1* are transmission gate [27], © 2013, IEEE.

B. Partially Body-Driven Gain-Enhanced Preamplifier

The one-bit quantizer in the modulator, as shown in Fig. 4.16, is realized by a dynamic comparator followed by a SR latch, which is preceded by a single-stage preamplifier to amplify the attenuated signal after the passive filters. Since no active gain involves in the passive stages, except for a small gain of 14dB in the gain-boosted filter, the circuit noise from the quantizer becomes important as well. As a result, a low-noise preamplifier needs to be designed. The preamplifier circuit is shown in Fig. 4.18a. The output CM is set to $V_{DD}/2$.

The preamplifier exploits low V_{th} transistor to provide more headroom at 0.5V. Also, the body of the PMOS transistors, M3-M6, is tied to $V_{DD}/2$ to further decrease the threshold voltage. No additional bias voltage is required for this purpose as the modulator CM voltage can be used here.

The original circuit, without using body biasing and cross-coupled connections of V_{op} and V_{on} at body of M5-M6, achieves a simulated DC gain of 12dB, 9dB, and 4dB from 0.9V, 0.5V, and 0.4V, respectively, with input CM voltage of $V_{DD}/2$. The DC gain degrades at lower supply voltages due to reduced headroom and changes in transistors operating region. To compensate for the reduced gain, partially body-driven gain-boosting technique is adopted in the circuit. The circuit employs two positive feedbacks due to the cross-coupled connection of the output nodes *Vop* and *Von* to both drain and body of opposite transistors in M5 and M6, resulting in negative conductance equal to $-g_{m5,6}-g_{mb5,6}$. The gain can be expressed as follows:

$$A_{DM} = \frac{g_{m1,2}}{(g_{ds1,2} + g_{ds3,4} + g_{ds5,6} + g_{m3,4}) - (g_{m5,6} + g_{mb5,6})} \tag{4.15}$$

where g_{mi} and g_{dsi} represent the transconductance and output conductance of *i*th

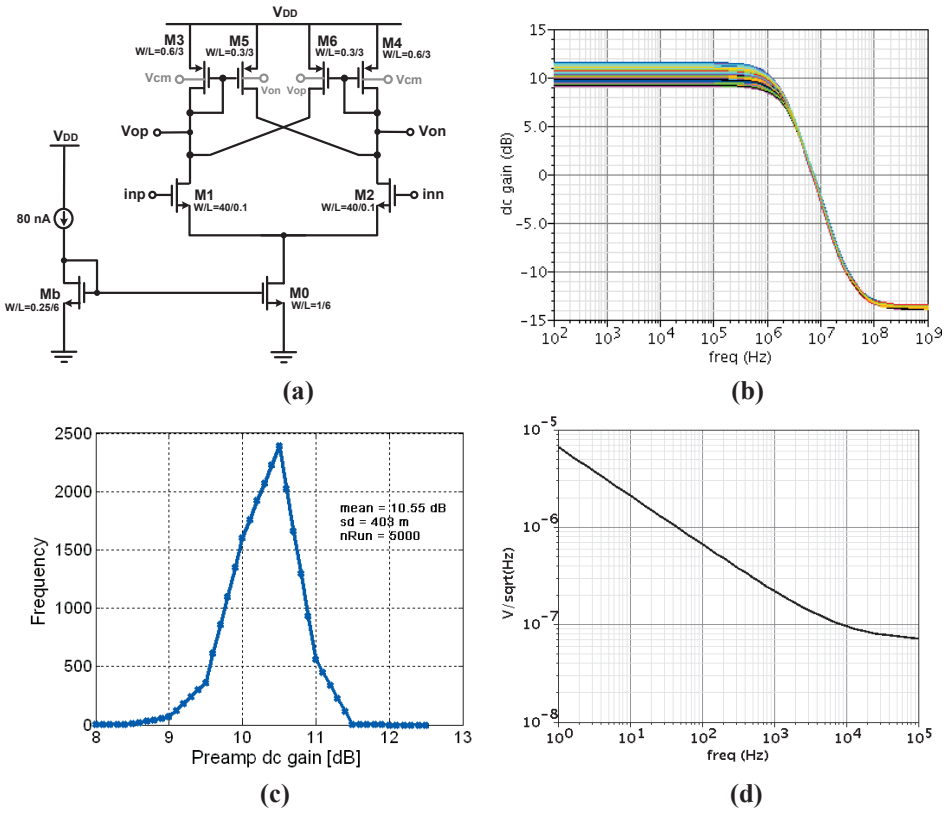


Figure 4.18: (a) Circuit schematic of the preamplifier. Units are in µm. (b) Simulated Bode plot of the preamplifier DC gain (c) Simulated histogram of DC gain (d) Simulated input-referred noise spectrum [27], © 2013, IEEE.

transistor, respectively. The size of M_5-M_6 are chosen so that $g_{m5,6}+g_{mb5,6}$ is 70% of the term $g_{ds1,2}+g_{ds3,4}+g_{ds5,6}+g_{m3,4}$. With this choice the preamplifier is stable and the gain is enhanced to 10.6dB at 0.5V supply, without additional power dissipation. Furthermore, the input devices are designed in subthreshold regime that provides larger g_m at lower bias current. To prove the circuit robustness, a Monte Carlo simulation is run for 5000 runs to show the impact of mismatch and process variations. The results are shown in Fig. 18b,c. The worst-case gain is 9.2dB (Fig. 18b), while the mean value of the histogram indicates a gain of 10.6dB (Fig. 18c).

The size of the input devices is selected to be 40/0.1 so as the flicker noise is reduced and a large g_{m1} is produced that limits the thermal noise, kT/g_{m1}, both at the cost of more power. Figure 18d shows the simulated input-referred noise. Integrating under the area of power spectral density (PSD) from 0.5Hz to 500Hz yields the total intput-

referred noise of 6.7μV_{rms}. The thermal noise level is 72nV/$\sqrt{Hz}$.

C. Clock Generation Circuitry

Ultra-low-power non-overlapping clock generation is used as designed in [41], but low V_{th} transistors operating at subthreshold regime are utilized to enable ultra-low voltage operation down to 0.3V. The total power consumption of the digital circuits, including clock generation and switch local drivers, is 92nW, which is 37% of the total power. The use of low V_{th} for low-voltage operation imposes extra leakage consumption.

D. Low-Voltage Single-Bit Quantizer

The one-bit quantizer is realized by a preamplifier, as shown in Fig. 4.18a, and a dynamic comparator followed by a cross-coupled inverter latch, as shown in Fig. 4.19. To enable ultra-low-voltage operation: (i) only two transistors are stacked; (ii) the tail current source is omitted at the cost of worse mismatch in the input pair; (iii) low V_{th} transistors are used in despite of being leaky; (iv) the body terminal of all PMOS devices are tied to $V_{DD}/2$ to further decrease the V_{th}.

4.5.1.3 Overall Modulator Circuit

Figure 4.16 shows the overall modulator circuit. By managing overdrive problem and nonlinear leakage current of the low V_{th} switches, the passive integrator is preferred to the active integrator for ultra-low-voltage operation. With sampling frequency f_s the 3dB bandwidth frequency is estimated as $f_sC_{S1}/(2\pi C_1)$ and $f_sC_{S2}/(2\pi .5.C_2)$ for the first and second filters, respectively. The capacitors C_1 and C_2 are selected as 64pF so that the second-order loop filter has two poles at 0.5kHz and 2.5kHz. The DAC reference level is set to 0.5V and 0.15V, respectively, for the first and second stage. The proposed modulator designed in 65nm CMOS was simulated with 500kHz clock. Table 4-1 summarizes the simulation results. The modulator achieves 79dB and 71dB peak SNR and peak SNDR, respectively, under PVT and 0.5V supply. Figure 4.20 shows the simulated power spectrum. The distortion comes due to the low V_{th} leaky switches.

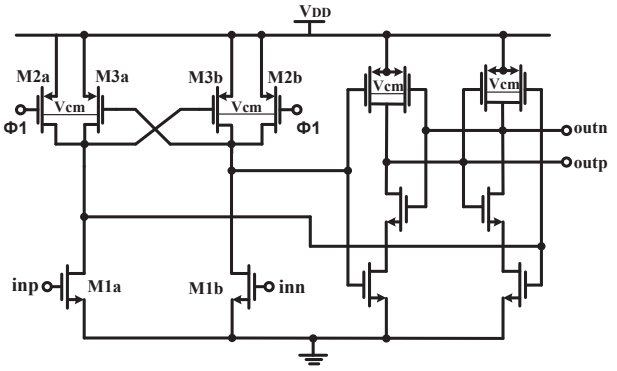


Figure 4.19: 0.5V comparator and latch using low V_{th} devices [27], © 2013, IEEE.

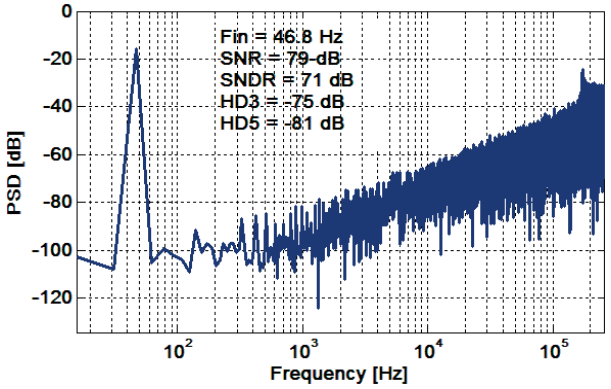


Figure 4.20: Output power spectrum using 120mV (-6.4dBFS) input amplitude. 32768-point FFT was used. The SNDR is 58dB over 1.2kHz signal bandwidth.

TABLE 4-1: SIMULATED PERFORMANCE RESULTS [27], © 2013, IEEE.

Supply Voltage	**0.5V**	**0.45V**
Technology	65nm CMOS	
Clock Frequency	500 kHz	
Signal Bandwidth	500 Hz	
Differential Input Range	1.0 V_{PP}	0.9 V_{PP}
Peak SNR[a]	79 dB	55 dB
Peak SNDR	71 dB	47 dB
Dynamic Range[b]	84 dB	60 dB
Power	250 nW	200 nW
Temperature Range	0-100 ºC	0-100 ºC
FOM[c]	0.086 pJ/step	1.09 pJ/step
(a) Peak SNR obtained at 120mV input amplitude or -6.4dBFS input		
(b) SNR with FS input is 84dB, while SNDR is 54dB.		
(c) FOM = Power/(2^{ENOB}×2×BW) where *BW* is signal bandwidth		

4.5.2 A 270mV 0.85µW ΔΣ Modulator Using Gain-Boosted Inverter-Based Amplifier

This section discusses an ultra-low-voltage low-power switched-capacitor ΔΣ modulator, presented in **Paper 5**, running at a supply voltage as low as 270mV for medical implant devices. The OTAs in the integrators of the traditional sigma-delta modulator and the adequate driving of the switching transistors usually determine the

lowest modulator's supply voltage. Conventional circuit topologies and stacking more than two transistors are not available in supply voltage below 0.5V, due to very low overdrive and voltage headroom.

Inverter is the simplest amplifier which can operate with supply voltage lower than the sum of the absolute threshold voltages of the NMOS and PMOS transistors [10], [42]. The DC gain and GBW of the CMOS inverter degrade significantly at supplies far below the nominal $V_{thn}+|V_{thp}| = 0.62$V, which need to be enhanced for a robust and high-performance modulator. Figure 4.21 shows the variations of the DC gain and GBW with respect to supply voltage, where the gain and GBW are reduced drastically under 0.35V. The input and output CMs are set to $V_{DD}/2$ for the maximum swing. Chae and Han proposed an inverter-based modulator in [10] using cascode inverter for boosting the gain, as shown in Fig. 4.22b. The minimum V_{DD} for cascode inverter is $4\times V_{DSsat} + V_{swing}$. For V_{DSsat} and V_{swing} equal to 0.1-0.15V and 0.1V, respectively, a $V_{DD} \geq 0.6$V can be tolerated. As a result, cascoding is not present for the gain boosting for $V_{DD} \leq 0.5$V.

Recalling from section 4.3.2, for a simple inverter the minimum supply is $2\times V_{DSsat} + V_{swing}$, which is about 0.25-0.3V. But, the drawback is the reduced gain. In the following, a new gain-enhanced inverter-based OTA will be presented.

4.5.2.1 Current-Mirror Inverter-Based Amplifier (IBCM)

The proposed inverter-based amplifier consists of a class-C inverter and a current-mirror output stage. Figure 4.22 shows the basic inverter, the cascode inverter, and the proposed current-mirror inverter-based amplifier. The aim is to boost the gain, GBW, and slew rate (SR) simultaneously by mirroring a small fraction of the bias current of the inverter M_1-M_2 to the output branch. The gain and GBW can be expressed as:

$$A_0 = (g_{m1} + g_{m2}) \times k \times R_{out} \tag{4.16}$$

$$GBW = \frac{(g_{m1} + g_{m2}) \times k}{2\pi C_L} \tag{4.17}$$

where g_m is the transconductance of the input transistor, R_{out} is the output resistance, and k represents the current ratio of the current-mirror M_3-M_4, defined as $(W/L)_{M4}/(W/L)_{M3}$. As seen from (4.16) and (4.17), both gain and GBW are theoretically enhanced k times as compared to a basic inverter shown in Fig. 4. 22a. Large device size in M_1-M_2 has to be avoided because it creates large parasitic capacitors, which can limit the OTA performance [42]. SR is an important parameter in the amplifier of a ΔΣ modulator. When a large positive input is present at the inverter input during integration phase, the PMOS is shut off and the bias current flows entirely from the NMOS and the current mirror M_3-M_4. Therefore, the current coming out of the compensation capacitor C_L is k times the bias current. This is illustrated in Fig. 4. 23. The SR can be defined as:

$$SR = \frac{I_{C_L}|_{Max}}{C_L} = \frac{k \times I_D}{C_L} \tag{4.18}$$

which shows that it is enhanced by k times as compared to the basic CMOS inverter.

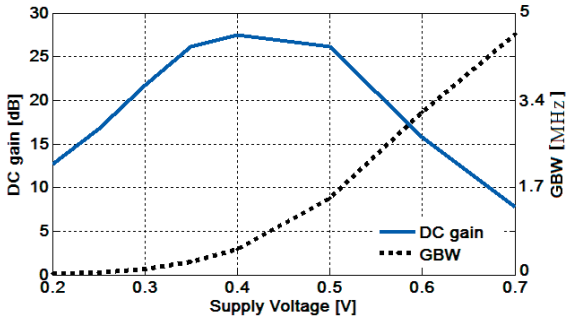


Figure 4.21: Characteristics of a CMOS inverter: DC gain and GBW variations versus V_{DD}. $(W/L)_{NMOS} = 1\mu m/0.8\mu m$, $(W/L)_{PMOS} = 10\mu m/0.8\mu m$, $C_{load} = 3pF$. Input and output CMs are set to $V_{DD}/2$.

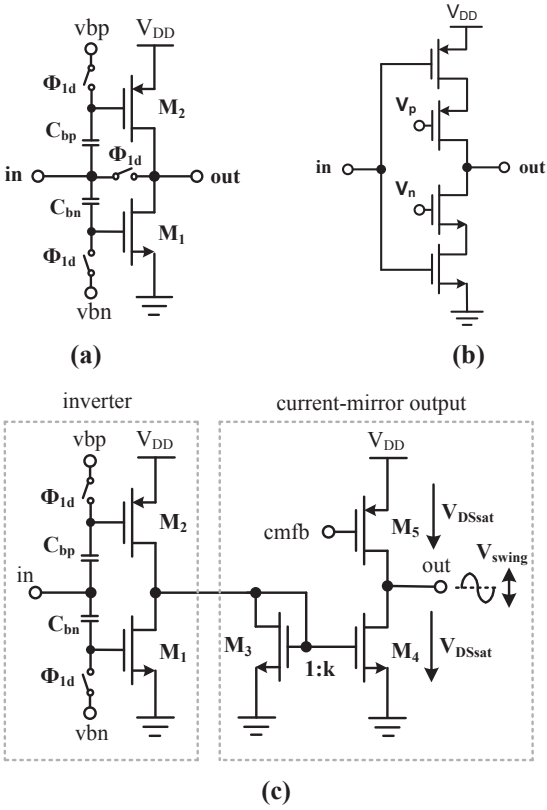


Figure 4.22: Circuit schematics of (a) conventional CMOS inverter (b) Cascode inverter, and (c) proposed gain-boosted inverter-based current-mirror OTA. The SC biasing scheme using floating capacitors is also shown.

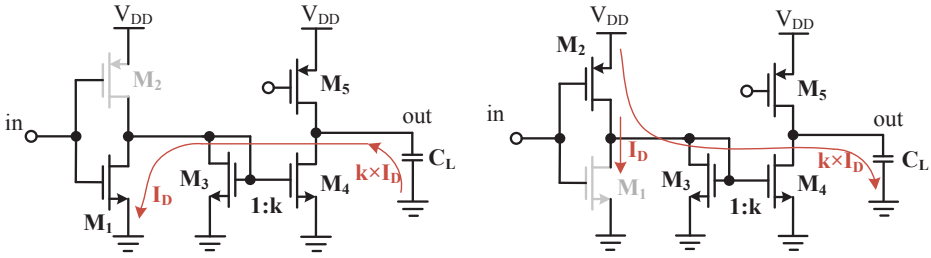


Figure 4.23: Slewing the current at compensation capacitor C_L for a large positive (left) and negative (right) inputs. I_D is the bias current of the inverter.

With current-mirror gain-enhancement technique the simulated DC gain and GBW of the inverter increase to 40dB and 1.9MHz from 22dB and 0.48MHz, respectively, from a 0.27V supply and a 3pF load capacitance. The phase margin is about 66º.

SC biasing scheme is used in the inverter using two floating capacitors shown in Fig. 4.22c. The capacitors C_{bn} and C_{bp} are periodically refreshed in $\Phi 1$ phase [11], and function as floating batteries between input and gates in order to properly bias the gate of the transistors independent of the input CM voltage. The output CM voltage is set to $V_{DD}/2$ by using an energy-efficient SC CMFB [4] circuit that derives the gate of M_5.

A drawback of the proposed amplifier is that it exhibits more input-referred thermal noise than the conventional inverter, related to the g_{m3} of the transistor M_3. Therefore, M_3 has to be carefully sized so that the thermal noise to be minimized. Also, the non-dominant pole, i.e. $g_{m3}/2\pi C_C$, due to C_C the parasitic capacitance at the gate of M3, must be placed more than 3 times the GBW for reasonable phase margin, 66º in this design. The diode-connected transistor M_3 slightly loads the inverter, which decreases the inverter pure gain. But, the combination of the inverter and the current-mirror stage enhance the overall gain sufficiently. The input-referred thermal noise power of the conventional inverter (Fig. 4.22a) and the gain-enhanced inverter (Fig. 4.22c) can be expressed as:

$$\overline{V_{n,inv}^2} = \frac{4kT\gamma}{g_{m1}+g_{m2}}, \left[v^2/Hz\right] \tag{4.19}$$

$$\overline{V_{n,GB-inv}^2} = \frac{4kT\gamma}{g_{m1}+g_{m2}}\left(1+\frac{g_{m3}}{g_{m1}+g_{m2}}\right), \left[v^2/Hz\right] \tag{4.20}$$

where γ is 1/2 for weak inversion region. Compared to (4.19), the (4.20) has an additional term associated with M_3. Since the CDS technique, as an auto-zeroing technique, is used in the corresponding integrator, the low frequency flicker noise is attenuated at the cost of increased white noise floor due to the noise folding accompanied with sampling [30]. The foldover thermal noise in the flicker-noise-cancelled integrator is the dominant source of the noise, in which the thermal noise is

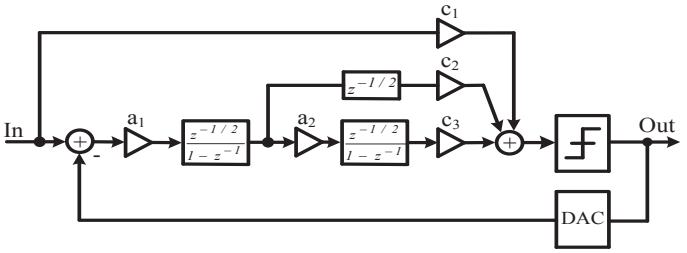


Figure 4.24: Modulator architecture using input feedforward topology.

amplified by a factor of GBW/f_s, with sampling frequency f_s. As a result, the input-referred noise of the simple inverter and the gain-boosted inverter given by (4.19) and (4.20) can be modified as the following:

$$\overline{V_{n-Fold,inv}^2} = \frac{GBW}{f_s}.\frac{4kT\gamma}{g_{m1}+g_{m2}},\left[v^2/Hz\right] \tag{4.21}$$

$$\overline{V_{n-Fold,GB-inv}^2} = \frac{GBW}{f_s}.\frac{4kT\gamma}{g_{m1}+g_{m2}}(1+\frac{g_{m3}}{g_{m1}+g_{m2}}),\left[v^2/Hz\right] \tag{4.22}$$

4.5.2.2 Modulator Architecture

As discussed in section 4.3.3, the output swing is of great importance in ultra-low-voltage and low-power designs. The integrator swing determines the modulator's reference voltage, as a consequence, the modulator dynamic range (DR), and ultimately the power consumption. The minimum supply voltage of an inverter, i.e. $2\times V_{DSsat}$ + V_{swing}, is limited by the required swing. The limited swing therefore translates into the demanding requirement of a low-swing loop topology. Figure 4.24 shows the modulator architecture. A second-order input feedforward topology has been used. In contrast to conventional feedback topology, the input feedforward structure offers the integrators to process only the quantization noise, therefore, the integrators signal swing can be reduced significantly, making the feedforward architecture suitable for ultra-low-voltage operation. The reduced internal signal swing also encourages lower required SR in the OTAs, which enables low-power consumption. The loop coefficients are optimized with behavioral simulations as (a_1 a_2 c_1 c_2 c_3) = (0.1 0.6 1 7 1). Half-delay integrators are adopted in this structure to realize the CDS technique for inverter's offset cancellation as well as low frequency flicker noise attenuation.

4.5.2.3 Modulator Circuit and Simulation Results

Figure 4.25 shows the circuit schematic of the designed second-order SC ΔΣ modulator using the proposed inverter-based OTA, shown in Fig. 4. 22. The IBCM amplifier in feedback configuration does not provide a virtual ground at the integrator input node as it has only one input terminal. Combined with CDS technique that eliminates the offset and attenuates the 1/f noise, two instances of IBCM amplifiers are

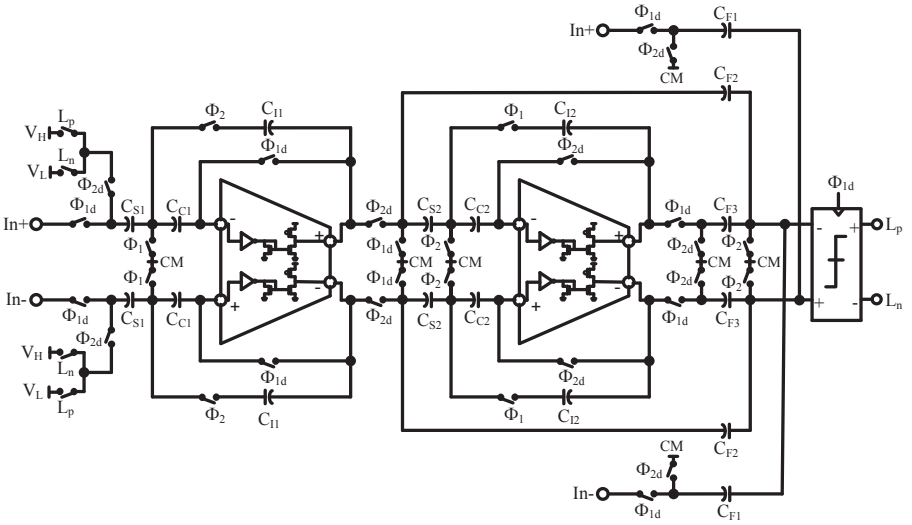


Figure 4.25: Modulator circuit.

used to create a pseudo-differential integrator with a virtual ground. When the first integrator samples the input in C_{S1} and the offset voltage in C_{C1}, the second integrator is transferring the charge to the integrating capacitor C_{I2} and vice versa. As a result, there is a half clock period delay between the integrators, which is shown in the architecture of Fig. 4.24. The half-clock delay element in the internal forward path is realized by SC implementation. The summation at the comparator input is realized with parallel capacitor branches including C_{F1}, C_{F2}, and C_{F3} capacitors. The capacitor sizes are summarized in Table 4-2.

Ultra-low-power non-overlapping clock generation is used as designed in [27] with low V_{th} transistors operating at subthreshold regime that enable operation down to 0.27V. The clock outputs are then boosted by a charge pump clock doubler [39]. In order to open and close the switches properly, transmission gate switches are used which are driven by the clock doubler output. The total power consumption of the clock generation circuitry including clock doublers is only 37nW from a 270mV supply.

Floating capacitors C_{bp} and C_{bn} between the input and gates of inverter are used to define the operating point of the inverter M_1-M_2, as shown in Fig. 4.22, while a SC energy-efficient CMFB circuit is utilized [4], which drives the gate of M_5 to set the output CM level at $V_{DD}/2$ for maximum swing.

The proposed modulator was designed and simulated in a 65nm process. Figure 4.26 shows the output power spectrum for a -2dBFS, 265Hz sine-wave input. The differential input signal range is $500mV_{pp}$. The modulator performance is summarized in Table 4-3. The total power consumption is 0.85μW at a 270mV power supply, in which the digital power is only 9%. The resulting FOM is 0.31pJ/conversion by

calculating FOM = Power / 2^{ENOB}×2BW. The modulator can work up to 0.5V power supply.

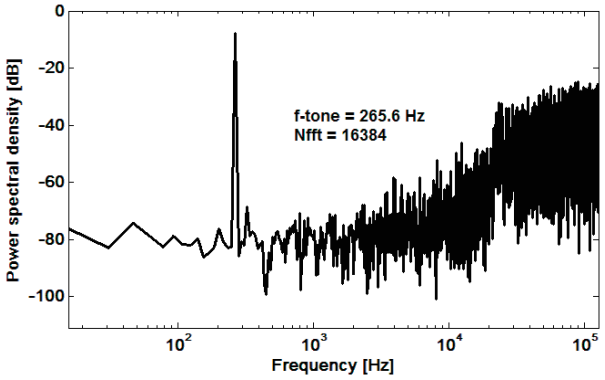


Figure 4.26: Output power spectrum.

TABLE 4-2: CAPACITOR SIZES OF THE FEEDFORWARD MODULATOR.

Sampling capacitors	Integrating capacitors	Feedforward capacitors
		C_{F1} = 1 pF
C_{S1} = 1 pF	C_{I1} = C_{C1} = 10 pF	C_{F2} = 7 pF
C_{S2} = 0.6 pF	C_{I2} = C_{C2} = 1 pF	C_{F3} = 1 pF

TABLE 4-3: SIMULATED PERFORMANCE RESULTS.

Supply Voltage	**0.27V**
Technology	65nm CMOS
Clock Frequency	256 kHz
Signal Bandwidth	1 kHz
Differential Input Range	$0.5V_{PP}$
Peak SNR	64.4dB
Peak SNDR	61dB
Dynamic Range	65dB
Power	0.85µW
FOM[a]	0.31pJ/step
(a) FOM = Power/(2^{ENOB}×2×BW) where *BW* is signal bandwidth, and ENOB = (SNR-1.76)/6.02.	

4.5.3 A 0.7V ΔΣ Modulator with Partly Body-Driven and Switched Op-amps

This section discusses a third-order DT delta-sigma modulator presented in **Paper 3** using partly body-driven and switched op-amps (SO) for measurement of bio-potential signals, such as EEG and ECG, in portable medical applications. The AT-switch with low V_{th} devices in **Paper 4** and the clock doubling scheme used in **Paper 5** were two effective solutions for mitigating the limited switch overdrive problem in low voltage design. SO technique [43] adopted in **Paper 3** is another common solution that alleviates the switching problem by eliminating the critical switches, thereby enabling 0.7V operation without using low V_{th} devices and clock boosting scheme. The SO approach reduces the speed of the modulator because of the necessary time the amplifiers need to settle when switched on. As a result, it is not a suitable technique in high speed applications. In low-speed medical applications, however, it is shown to be an effective solution for power reduction. The amplifier DC gain degrade significantly in lower supply voltages, therefore, a body-driven gain-boosting scheme is used to compensate for the reduced gain. Also, body forward biasing technique adopted in the amplifiers and comparator further decreases the V_{th} of the PMOS transistors, resulting in more headroom for 0.7V circuit design.

4.5.3.1 Modulator Architecture

The system-level modulator topology is shown in Fig. 4.27a. A third-order conventional feedback loop filter structure using half clock delay integrators, related to SO integrator, is used with single-bit quantization. Half-delay elements are inserted in the feedback paths in order to compensate for the half clock delay in the SO integrator. The modulator is carefully scaled and the loop coefficients are determined from the stability requirement and the signal linearity constraint.

4.5.3.2 The Switched Opamp Technique

The technique aims for solving the switch-driving problem in low voltage design. There are two classes of switches in a SC integrator: switches that have one terminal connected to CM voltage, and the floating switches like sampling switches (Fig. 4.27b). The former can always be turned on, but the latter is problematic because the related switches have to pass rail-to-rail signal range. As in the sampling phase the Opamp is turned off, the output node leaves out floating, and therefore the critical floating switches next to the amplifiers can be entirely eliminated.

4.5.3.3 Body-Driven Gain-Enhanced OTA

A fully differential power-efficient and gain-boosted two-stage amplifier is developed with load frequency compensation. The load-compensation is preferred to the Miller compensation because it avoids extra power for driving the Miller capacitor [41]. Figure 4.28 shows the circuit schematic of the switched amplifier. To reduce the power, the input CM level is set to $V_{DD}/2$, which is limited by the gate-source voltage of M1a-M1b and the drain-source voltage of M0. The input transistors are driven in the weak

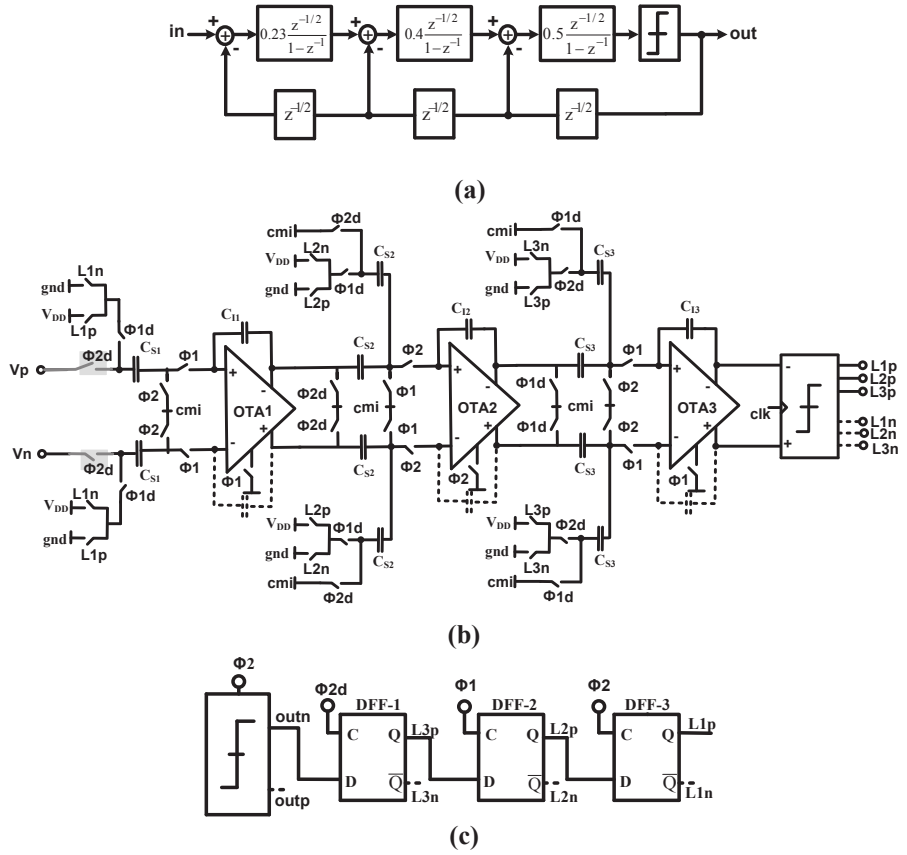


Figure 4.27: (a) Modulator architecture with coefficients 0.23, 0.4, 0.5. (b) Circuit schematic, (c) latches realizing the half-clock delay DAC elements [44], © 2013, IEEE.

inversion region that produces a larger g_m. Since for a given bias current the g_{mw} of the weak inversion transistor is almost five times larger than the g_m of the strong inversion [45], the main transistors M1a-M1b, M3a-M3b, and M6a-M6b are biased in the weak inversion to achieve greater DC gain and GBW, while all other transistors are biased in the moderate inversion region. This also helps to reduce the thermal noise, $4kT\gamma/g_{mwi}$, of the mentioned transistors, due to $g_{mw} = 5\times g_m$. the factor γ is 1/2 in the weak inversion region, and 2/3 in the strong inversion region. The absence of cascoding in the low voltage analog domain brings the rail-to-rail output swing, but at the cost of reduced gain. To enhance the gain without drastic power increase, a body-driven gain-boosting technique is applied at the output nodes using cross-coupled pair at the body of M6a-M6b. This introduces a negative conductance equal to $-g_{mb6}$ that increases the output resistance, thereby enhancing the overall gain. The DC gain can be expressed as:

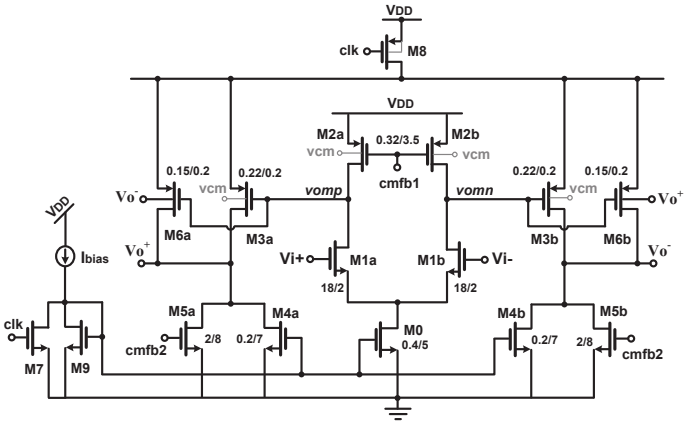


Figure 4.28: The proposed load-compensated switched amplifier using body-driven gain-enhancement technique. The PMOS body is connected to $V_{cm} = V_{DD}/2$ to reduce the threshold voltage. Sizes are given for the first OTA [44], © 2013, IEEE.

$$A_0 = \frac{g_{m1}}{g_{ds1} + g_{ds2}} \cdot \frac{g_{m3} + g_{m6}}{g_{ds3} + g_{ds4} + g_{ds5} + g_{ds6} - g_{mb6}} \tag{4.23}$$

The M6a and M6b are sized such that the g_{mb6} is about 65% of the term g_{ds3}+g_{ds4}+g_{ds5}+g_{ds6}. With the gain-enhancement technique, the typical DC gain and GBW of the first OTA are boosted to 50.4dB and 1.12MHz, respectively, from 39.6dB and 670kHz. To minimize the power, all OTAs and CMFB circuits are turned off in their sampling phase. Switches M7-M8 are introduced for this purpose. Also, for extra power saving, the OTA performance parameters related to the second and third integrators are scaled down, as summarized in Table 4-4, because their impact is less critical.

4.5.3.4 Modulator Circuit

Figure 4.27b shows the complete modulator circuit. The first, second, and third integrators are active in *Φ1*, *Φ2*, *Φ1* phases, respectively, resulting in half-clock delay integrators. The compensating half-delay elements are shifted to the feedback paths as it is much easier to design the power-efficient clocked latches in the digital domain. The integrators input and output CM levels are set to $V_{DD}/2$ for the maximum input and output swing. The input sampling switch is realized as transmission gate, whereas the rest of switches are basic MOS transistor. To obtain sufficient overdrive voltage in the input switch, the signal range is limited between 0.1-0.6V. A third-order loop filter is used to minimize the OSR or the clock frequency, hence the digital power consumption. The modulator clocked at 128kHz (OSR equal to 128) achieves 87dB peak SNDR at 600nW total power consumption operating at a 0.7V supply voltage.

TABLE 4-4: TYPICAL SIMULATED PERFORMANCE OF THE AMPLIFIERS.

	OTA1	OTA2, OTA3
DC Gain (dB)	50.4	48
GBW (MHz)	1.12	0.77
Phase Margin (°)	60	70
Static Power (nW)	347	280

4.6 Comparison

A performance comparison among the proposed modulators in [12], [27], [44] and the state-of-the-art low-voltage modulators is summarized in Table 4-5, where a typical FOM is used as defined below:

$$FOM = \frac{Power}{2^{(SNDR-1.76)/6.02} \times 2 \times BW} \tag{4.24}$$

The designed modulators achieve comparable FOM compared to the state-of-the-art modulators. In particular, the design in **Paper 5** [12] is capable of operating at supply voltage down to 270mV using the class-C inverter-based OTAs, whose reduced gain is enhanced by a current-mirror stage. This modulator shows one of the lowest V_{DD} reported to date. The achieved FOM is comparable with the results from the higher-supply-voltage modulators. The 0.5V passive modulator presented in **Paper 4** attains an ultra-low power consumption of only 250nW, and a high energy-efficiency of 86fJ/step, making it a suitable candidate for the medium resolution converters.

4.7 Summary

This Chapter concentrated on ultra-low-power ΔΣ modulators design with especial focus on low/ultra-low voltage operation. The majority of 0.5-0.7V modulators presented in sections 4.4 and 4.5 utilize low-voltage OTA topologies [14], [23], [26], [29], [46]. But, below 0.5V no modulator has been reported to date using conventional OTAs, due to the extremely low overdrive and output swing. At the same time, the tail current source of the input stage cannot be omitted for acquiring acceptable CMRR, except for the body-input amplifier with built-in CM rejection [29], which places a hard break for the V_{DD} reduction. To overcome this limitation, CMOS inverter were introduced as an OTA at the loss of CMRR. The minimum V_{DD} was reduced to 250mV in [11] and 270mV in **paper 5**. Also, the problem associated with low overdrive and small swing was eliminated by replacing the active OTA-based integrator with passive OTAless integrator in **Paper 4** at the cost of reduced noise shaping property, resulting

in a 0.5V design. The switch-overdriving problem in low/ultra-low voltage operation can be mitigated with low V_{th} transistors [3]-[5], local switch bootstrapping [6]-[8], or clock boosting [9]-[12].

ABLE 4-5: COMPARISON OF PROPOSED ΔΣ MODULATORS WITH STATE-OF-THE-ART LOW-VOLTAGE DESIGNS

Ref., Year	V_{DD} [V]	BW [Hz]	SNDR [dB]	SNR [dB]	Power [μW]	f_S [MHz]	CMOS [nm]	FOM[a] [pJ/step]
[10][b] Chae, 2008	0.7	20k	81	84	36	4	180	0.098
[29][c] Pun, 2007	0.5	25k	74	76	300	3.2	180	1.46
[15][d] Roh, 2009	0.6	20k	81	82	34	1.92	130	0.092
[26][e] Zhang, 2011	0.6	20k	79.1	80.1	28.6	2.56	130	0.097
[47][f] Ahn, 2005	0.6	20k	81	81	1000	3.072	350	2.73
[46] Yang, 2012	0.5	20k	81.7	82.4	35.2	1.25	130	0.088
[11] Michel, 2012	0.25	10k	61	64	7.5	1.4	130	0.477
[14][g] Ishida, 2005	0.5	8k	39.6	44	75	2.0	150	60.1
[27][h] Fazli, 2013	0.5	0.5k	71	79	0.25	0.5	65	0.086*
[12][i] Fazli, 2013	0.27	1k	61	64.4	0.85	0.256	65	0.31*
[44] Fazli, 2012	0.7	0.5k	87	91.5	0.6	0.128	65	0.033*

(a) FOM = Power/(2^{ENOB}×2×BW) where *BW* is signal bandwidth
(b) Using class-C inverter (c) CT and body-input amplifier
(d) Utilize subthreshold-leakage switches
(e) CT feedforward architecture with gain-enhanced partially body-driven amplifiers
(f) Switched-RC integrator (g) leakage suppression AT-switch using low V_{th}
(h) Passive integrator with AT-switch in input sampling (i) Gain-boost inverter-based current-mirror OTA and clock boosting
*** includes only simulation results**

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Chapter 5

Low-Power Dual-Mode ΔΣ Modulator

5.1 Introduction

Multi-band ADCs have attracted a lot of interest in realizing multi-mode transceivers in mobile communications [1], [2]. For multi-band applications, ΔΣ modulators are preferred because they provide robust and cost-effective designs with performance trade-offs with respect to oversampling ratio (OSR) and power consumption. This Chapter describes the design of a dual-mode ΔΣ modulator for a low-power medical application [3].

The design of a low-power variable bandwidth amplifier (VBA) (**Papers 8**) whose gain-bandwidth product (GBW) can be tuned is described in this Chapter. The VBA is built from a two-stage load-compensated amplifier, in which its GBW can be programmed in three different levels. Another practical application is a low-pass filter with tunable cut-off corner intended for analog front-end of the biomedical sensor interface [4] or neural recording integrated circuit (IC) [5]. The concept, circuit design and the related design challenges of the implemented tunable bandwidth OTA are discussed in details. The chip test results will be described subsequently.

As a practical example, a dual-mode single-clock-rate delta-sigma modulator is introduced, as presented in **Papers 9**, in order to optimize both the integration area and the power consumption. The dual-mode modulator combines the designed VBA with an adjustable OSR for the sensing/measuring stages of a cardiac pacemaker [6]. The designed flexible ADC poses minimum circuit overhead, in that two digital control bits are used to set the required GBW in the VBAs while a simple divided-by-2 digital circuit is provided to generate half sampling clock frequency internally from the

reference input clock. The simulated performance results of the flexible ΔΣ modulator in two functional modes will be discussed in this Chapter.

5.2 Variable Bandwidth Amplifier

5.2.1 Concept

As discussed in Chapter 2, the two-stage load-compensated amplifier were selected among the existing OTA topologies in the target low-current (100-200nA) and low-speed (less than 1MHz) application, due to its power-efficiency, rail-to-rail output swing, and minimal load capacitance for an optimum GBW and phase margin. Figure 5.1 shows the two-stage amplifier with load-compensation. Another interesting property of the used amplifier topology is that its GBW or 3dB bandwidth can be multipied by two/three when switching on/off the replicas of the second stage, whereas its load capacitance is kept constant. This is explained in the following manner. Assume that the nondominant pole is located beyond 3×GBW for a safe phase margin, the DC gain and GBW of the two-stage load-compensated OTA can be expressed as:

$$A_0 = g_{m1}R_{out1} \times g_{m5}R_{out2} \tag{5.1}$$

$$GBW = \frac{g_{m1}g_{m5}R_{out1}}{2\pi C_L} \tag{5.2}$$

where g_{mi} is the transconductance of the ith transistor, R_{outi} is the output resistance of the ith stage of the OTA, and C_L is the output load capacitance. It is further assumed that all transistors operate in the moderate inversion region. Clearly seen from (5.2), increasing the g_{m5} by 2× or 3× would enhance the GBW accordingly by a factor of 2 or 3. It should be noted that this is not feasible by $2\times g_{m1}$ or $3\times g_{m1}$ indeed because the term $g_{m1}R_{\text{out1}}$ will ultimately remain constant. As a consequence, the gain represented by (5.1) holds constant when tuning the bandwidth by g_{m5} term in (5.2), assuming an ideal second-order model with transistor operating in saturation. This principle is used to construct a variable bandwidth amplifier according to the block diagram shown in Fig. 5.2a. The Gm1 and Gm2 blocks represent the first and second stage of a two-stage amplifier (Fig. 5.1), respectively. Two control switches (*ctrl1* and *ctrl2*) connect and disconnect the replica stages. Consider the case that both switches are off, the unity-gain frequency of the VBA is then assumed to be GBW. When *ctrl1* turns on, ideally a unity-gain frequency of 2×GBW can be obtained. Similarly, when both *ctrl1* and *ctrl2* turn on, ideally a unity frequency of 3×GBW can be achieved. In this way, a two-stage amplifier with second stage replicas is built that can produce three levels of unity-gain frequency at GBW, 2×GBW, 3×GBW. The complete circuit schematic of the resulting VBA is shown in Fig. 5.2b. The *ctrli* switches are realized by MOS transistors M7, M8, and M9 in order to switch on/off the replica stages. When the control signal *ctrli* goes low, the PMOS switches M7 and M9 are on and the NMOS switch M8 is off connecting the Gm2 cell to the supply voltage V_{DD} and the SC common-mode feedback circuit.

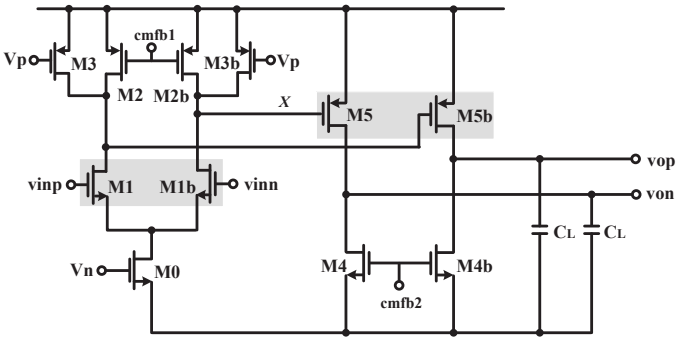
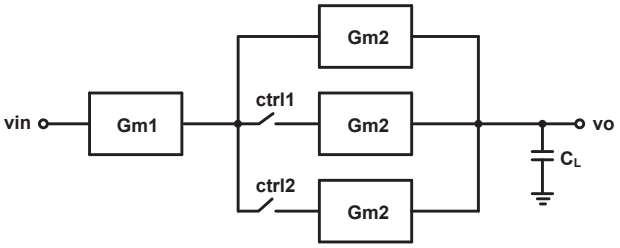
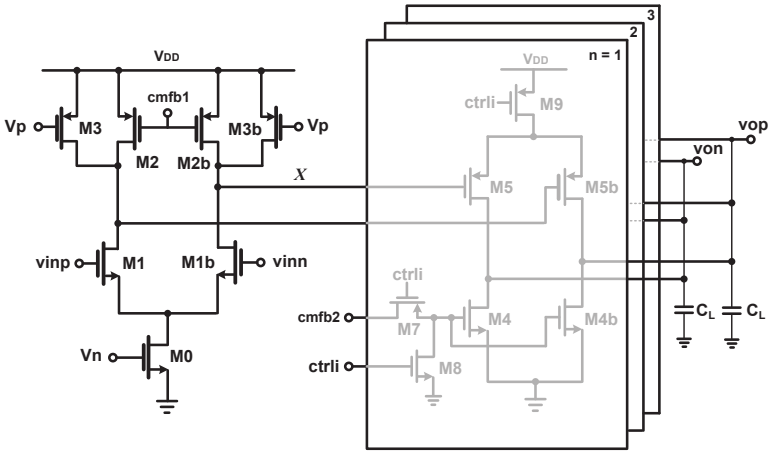


Figure 5.1: Two-stage load-compensated OTA.



(a)



(b)

Figure 5.2: (a) Block diagram (b) differential circuit schematic [3], © 2013, IEEE.

5.2.2 Design Considerations

The dominant and non-dominant poles of the VBA shown in Fig. 5.2 can be expresses as:

$$P_d = \frac{1}{2\pi.R_{out2}C_L} \tag{5.3}$$

$$P_{nd} = \frac{1}{2\pi.R_{out1}C_C} \tag{5.4}$$

R_{outi} is the output resistance of the ith stage, C_L is the output load, and C_C is the parasitic capacitance at node x, which is mainly from the gate-source capacitor of the M5 or M5b. Idealy, for a single-pole characteristic when all non-dominant poles are sufficiently away from the unity-gain frequency (f_u), the GBW and cut-off frequency of the VBA is multiplied by n, where n is the number of the Gm2 cells connected in parallel (Fig. 2.2b). In practical circuit implementation, this is restricted by the frequency response problem. Connecting more Gm2 cells would increase the C_C and hence pulles the non-dominant pole given by (5.4) closer to f_u, that reduces the phase margin. To preserve a safe phase margin (more than 60°), the non-dominant pole has to be placed at least three times of the f_u. To do so, according to (5.3) and (5.4), the parasitic capacitance C_C should be minimized by keeping the size of the M5 (or M5b) lower, the R_{out1} must be kept smaller at the cost of more current in the first stage, or the load C_L has to be taken sufficiently large. The latter one improves the phase margin, but it decreases the GBW, which needs more power consumption to set it at the required level. Obviously, there is trade-off here between the power consumption and the phase margin.

Another important consideration in the VBA design is the load capacitor. Since the GBW is heavily dependent on the C_L according to (5.2), the GBW and phase margin are simulated with respect to the load variation in the full bandwidth mode (*ctrl1= ctrl2=* 0). The simulation results are illustrated in Fig. 5.3. With 10% load variation at the worst case, the GBW and phase margin change 192Hz and 2°, respectively, which can be tolerated by the designed VBA.

5.2.3 Experimental Results

The proposed amplifier was designed and implemented in a standard CMOS 65nm technology. The chip micrograph is shown in Fig. 5.4. It occupies a 150μm×50μm core area. An off-chip unity-gain buffer is used to buffer the output. Figure 5.5 shows the measured frequency response with an estimated 8pF load, including the capacitances of the wiring, the pad, and the buffer's input. The VBA presents three programmable unity-gain frequencies at 0.9MHz, 1.7MHz, and 2.3MHz with a consistent DC gain of 56dB. The corresponding cut-off frequencies are 320Hz, 600Hz, and 850Hz, respectively. The power consumption including the CMFB and biasing circuits is 180nW and 315nW, respectively, operating in low and full bandwidth modes.

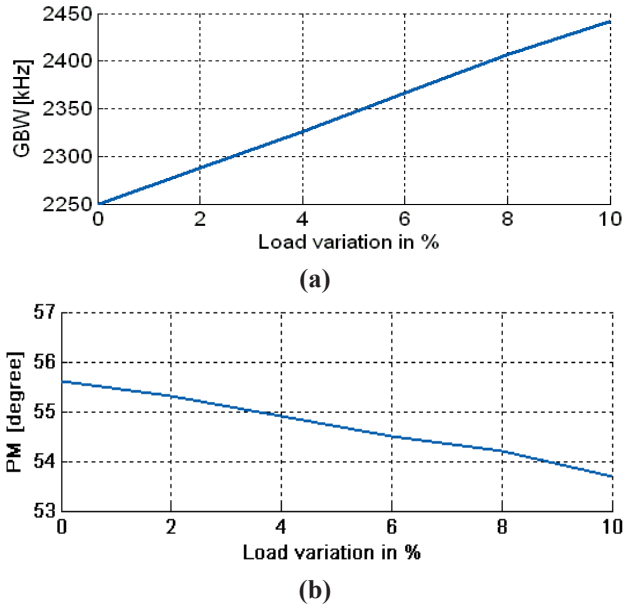


Figure 5.3: (a) GBW and (b) phase margin variations versus the load variation [3], © 2013, IEEE.

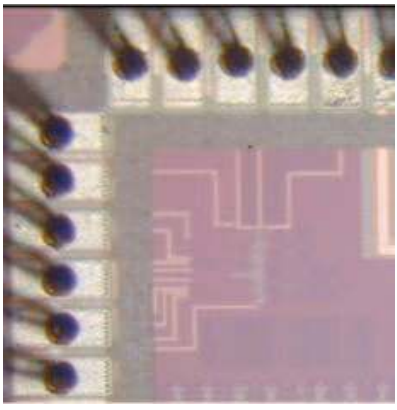


Figure 5.4: Chip micrograph.

The transient response is measured from a unity-gain feedback setup with 100MΩ resistance (three resistors at the input, feedback path and biasing) and a 8pF load. Figure 5.6 demonstrates the measured transient responses of the implemented VBA for two

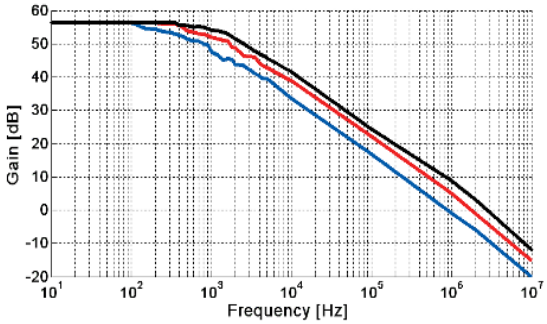


Figure 5.5: Frequency response in three bandwidth settings with 56dB dc gain.

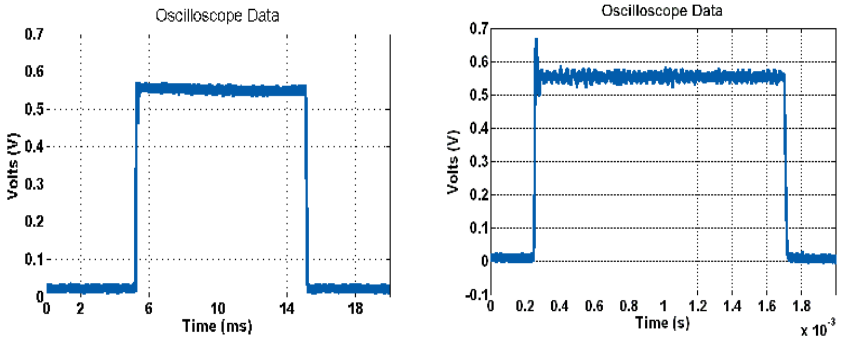


Figure 5.6: Measured transient responses of the VBA in low bandwidth setting with a 50Hz input (left) and full bandwidth setting with a 250Hz input signal (right).

TABLE 5-1: PERFORMANCE COMPARISON WITH OTHER LOW VOLTAGE OTA DESIGNS

Ref., Year	DC gain [dB]	GBW [MHz]	Load Cap. [pF]	Phase Margin [°]	Power [μW]	Supply Voltage [V]	FOM[a] [MHz.pF/A]
[7] Roh, 2010	45	0.049	0.68	90	0.4	0.8	66×10^3
[8] Chatterjee, 2005	62	10	20	60	75	0.5	1333×10^3
[9] Lin,2007	62	160	2	67	250	0.8	1024×10^3
[10] Yao, 2003	52	1.2	18	60	8	0.8	2160×10^3
[3] Fazli, 2013[b]	56	2.3	8	57	0.315	0.9	3286×10^3

(a) FOM = $(GBW\times C_L)/ I_{VDD}$. (b) This work includes only the simulation results.
(b) The results related to the full bandwidth setting are included.

bandwidth settings when a 580mV$_{PP}$ input is applied at the input. The phase margin is 70° in low bandwidth setting, whereas it decreases to 57° in the full bandwidth mode. The full performance comparison is given in Table 5-1. The implemented VBA amplifier provides a better figure of merit than the other low power amplifiers.

5.3 Dual-Mode ΔΣ Modulator

The design of a dual-mode delta-sigma modulator is discussed in this section. Two low-power ADCs are required for the sensing and measuring stage of the cardiac pacemaker [6], according to the specification given in Table 5-2. The ultimate goal is to optimize both the integration area and the power consumption, the two essential design parameters for an implantable device. In the dual-mode ΔΣ modulator presented in [1], the classic single-bit second-order architecture was chosen to digitize the GPRS signals. An OSR equal to 195 was used to attain 84dB of DR. A multi-bit third-order modulator using cascaded (MASH 2-1) structure was chosen to digitize the WCDMA signals. The advantage of the MASH 2-1 structure is that it can re-use the "GPRS modulator". Moreover, the loop coefficients are switched to different quantities when shifting from GPRS mode to WCDMA mode. This poses additional capacitive area due to the realization of two different sets of coefficients. An OSR = 10 is used to attain 70dB of DR. In the dual-mode ΔΣ modulator presented in [2], the classic second-order single-bit architecture was chosen to digitize both the GPS and WCDMA signals. Unlike the design in [1], neither the loop architecture nor the coefficients are reconfigured, thereby avoiding circuit complexity and area penalty. The DR targets are 84dB over 100kHz GSM band and 50dB over 1.92MHz WCDMA band. To meet these DR requirements in both bands, the sampling clock frequency is chosen from the wider input bandwidth, i.e. 1.92MHz, to be 48MHz, resulting in an OSR of 25. Taking a large OSR equal to 240 in GSM mode to attain 84dB of DR over 100kHz bandwidth will terminate to a 96MHz sampling frequency, which is twice that of the other mode. Therefore, the shift from WCDMA to GSM mode is merely done by dividing the sampling clock by two. This is beneficial in terms of the reduced complexity in the clock generation circuitry. As seen above, the flexibility usually comes with circuit overhead and additional power consumption. The target dual-mode modulator discussed here is an attempt to making a smart solution that can minimize both the circuit complexity and the power penalty.

5.3.1 Circuit

The scaled topology of the modulator is shown in Fig. 5.7a. The modulator inherits several advanced features of the second-order implementation in [11], such as the loop architecture and order, the loop coefficients, the amplifier topology, the dynamic comparator and on-chip clock generation circuitries. Moreover, the same system-level and low-power design considerations are applied in this work. Therefore, the majority of the circuit building blocks and the relevant discussions are omitted here to avoid redundancy. The reader is encouraged to refer to the **Paper 1** or the related discussions that can be found in section 2.5 (Chapter 2). The major differences of the flexible ΔΣ

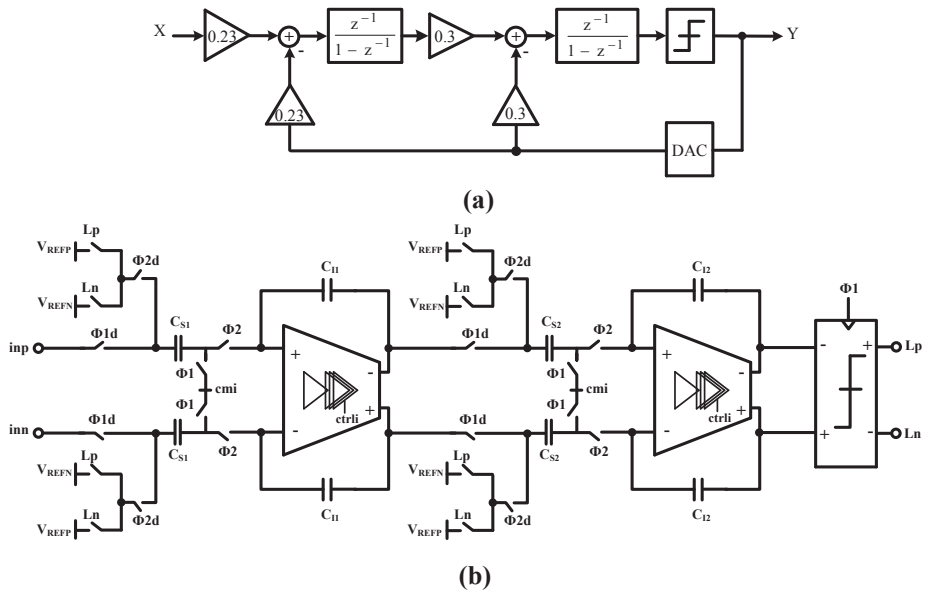


Figure 5.7: (a) Block diagram of the modulator (b) circuit schematic.

TABLE 5-2: SPECIFICATION OF THE ADCS

	Mode I	**Mode II**
	Sensing stage	Measuring stage
ENOB	≥ 10-bit	≥ 12-bit
Signal bandwidth	0.1Hz-250Hz	0.1Hz-50Hz

modulator shown in Fig. 5.7 with that presented in [11] are the use of the tunable-GBW OTAs (or VBAs in short) rather than the simple two-stage amplifiers and the use of adjustable OSR. The design exploits the OSR as in [1] and [2], whereas the 3dB bandwidth or the unity-gain frequency of the VBAs in the integrators is tuned to either low-bandwidth or full-bandwidth mode, according to the mode of operation. When it functions in mode II, the VBAs are tuned in their low-bandwidth mode by switching off the replica stages in order to save analog power consumption. The circuit schematic of the dual-mode modulator employing the presented VBAs is shown in Fig. 5.7b. To meet the resolution requirements in both bands, as summarized in Table 5-2, the sampling clock frequency is chosen from the Mode II (over 50Hz bandwidth) to be 32kHz, resulting in an OSR of 320, which is sufficient to attain more than 12-bit resolution. Taking an OSR equal to 128 for mode I over 250Hz bandwidth terminates to a 64kHz sampling frequency, which is twice that of mode II. This option is adequate for attaining

an effective number of bit (ENOB) more than 10-bit. The choice of the sampling frequencies to be a multiple of 32 makes it very easy to provide a 64kHz master clock input and then produce the other sampling frequency, i.e. 32kHz, by a division-by-2 using a D-FF. This can significantly reduce the complexity of the clock generation circuitry. The use of a relatively large OSR in Mode II (equal to 320) enables the large suppression of the low frequency noise such as 1/f noise, hence eliminating the need for special circuit techniques (e.g., chopper stabilization and CDS) in the first integrator. Also, the simulated input-referred noise of the first VBA is $27\mu V_{rms}$ [3], well below the least significant bit (LSB) of the mode-II's modulator. The first sampling capacitor value is determined according to the requirement of the higher resolution mode (i.e. Mode II). With OSR equal to 320, 92dB of DR, and a full scale input amplitude of 0.3V, the first sampling capacitor value, C_{S1}, is calculated to be 1.8pF. With a safe margin it is taken to be 2pF. The sampling capacitor size in the second integrator is reduced a lot (0.3pF) because the thermal noise of this stage is greatly attenuated by the gain of the first stage. The values of the integrating capacitors C_{I1} and C_{I2} are selected as 8.8pF and 1pF, respectively, in order to realize the specified loop coefficients in the block diagram of Fig. 5.7a.

5.3.2 Simulation Results

The proposed modulator is designed in a standard 65nm CMOS and is simulated with a 64kHz input clock signal. The differential input range is 1.2V with 0.6V reference level. The peak SNDR for both functional modes is obtained from a 200mV signal amplitude with an offset voltage of 0.45V. The simulated SNDR with respect to input amplitudes is illustrated in Fig. 5.8. The input sine-waves amplitude for this measurement is –3.52dBFS with 109.4Hz and 15.6Hz for mode I and II, respectively. Table 5-3 summarizes the simulation results. Clearly seen in the low bandwidth mode, despite the higher OSR and hence better resolution, the power-efficiency improves a lot. Compared to Mode I, the FOM is almost half, which is mostly due to the reduced GBW in the VBAs, thereby decreasing the analog power significantly.

TABLE 5-3: PERFORMANCE SUMMARY

	Mode I	**Mode II**
Technology	65nm CMOS	
Supply Voltage	0.9V	
Reference Voltage	0.6V	
Signal bandwidth	250Hz	50Hz
Sampling Frequency	64kHz	32kHz
VBA Operation Mode	Full Bandwidth	Low Bandwidth
Oversampling Ratio	128	320
Peak SNDR	67.3dB	85dB
Power Consumption	990nW	685nW
FOM	1.05pJ/step	0.47pJ/step

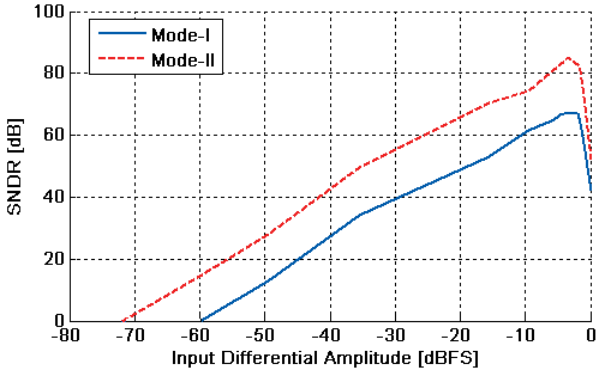


Figure 5.8: SNDR versus differential signal amplitude [3].

5.4 Summary

A novel dual-mode delta-sigma modulator was presented in this Chapter using a variable bandwidth amplifier that can support two low frequency bands. The ultimate goal is to optimize both the power consumption and the integration area. Unlike the dual-mode modulator design by Dezzani in [1] which reconfigures both the architecture and the loop coefficients, this design heavily decreases the hardware complexity by keeping the architecture the same for both bands as in [2] while the gain-bandwidth requirement of the VBA can be appropriately adjusted for each functional mode. Moreover, the choice of the sampling frequencies to be a multiple of 32, i.e. 32kHz and 64kHz, can significantly reduce the complexity of the clock generation circuitry, and hence the power consumption. It is believed that the power efficiency of the presented flexible modulator can further be optimized, particularly when only doubling the sampling frequency, two replicas of Gm2 stage, shown in Fig. 5.2a, are sufficient for the mode I. In other words, it is possible to adjust the VBA's GBW in medium bandwidth rather than full bandwidth mode. Moreover, the ratio of the sampling rate over the GBW of the mode I and II is 28 and 36, respectively. This is somewhat an overdesign in the transistor-level, and is believed that can be decreased by a factor of two for the real chip implementation. Nevertheless, the achieved simulated FOMs (0.47 and 1.05pJ/step) are comparable with previously reported modulators. The author encourages the reader to refer to the comparison data given in Table 2-4.

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Chapter 6

Conclusions and Future Work

6.1 Conclusions

The analog-to-digital converter (ADC) is a key building block in the sensing stage of the implantable biomedical devices. To reduce the overall power consumption, it is desirable to integrate the entire analog front-end, ADC and digital processor in a single chip. While digital circuits benefit substantially from the technology scaling-down, it is becoming more and more challenging to meet the stringent requirements on linearity, dynamic range, and power-efficiency at lower supply voltages in traditional ADC architectures. Recent research work on the low-power, low-voltage, high performance ΔΣ modulator design in 65nm CMOS technology has been presented in this thesis. In the modulators design, both circuit level and architecture level approaches are presented.

This thesis investigates the design of power-efficient high-resolution ΔΣ modulators at very low frequencies. In total, eight discrete-time (DT) modulators have been designed in a 65nm CMOS technology. This includes: two active modulators, two hybrid active-passive modulators, one fully passive modulator, two ultra-low-voltage modulators operating at 0.5V and 270mV supply voltages, and a dual-mode ΔΣ modulator using variable bandwidth amplifiers.

In Chapter 2 the design of low-power ΔΣ modulators using traditional feedback architecture and active (OTA-based) integrators are introduced. Then the design, power analysis, and comparison of several OTA topologies, suitable for low-power ΔΣ modulator, are explained (**Papers 1, 2**). By introducing oversampling and noise-

shaping, the basic operation principle of the ΔΣ modulator is presented. The circuit noise of an implemented second-order single-bit modulator is then analyzed. An experimental second-order single-bit ΔΣ modulator (**Papers 1**) is presented where special measures are taken in the circuit design to reduce the power consumption. The peak SNR of the modulator reaches 80dB in a 500Hz signal bandwidth. The total power consumption is only 2.1μW under a 0.9V power supply. The measurement results and the achieved high figure of merit have proven the possibility of implementing high-performance low-power ΔΣ ADC in nanometer CMOS technologies using traditional feedback topology and standard active loop filter.

In Chapter 3 the usefulness of the passive filter in power reduction and the performance trade-offs with respect to the standard active modulators are presented. The design of passive filter and the nonidealities associated with it is investigated, and then three modulator designs employing partially passive filter (**Papers 6, 7**) and a fully passive filter (**Papers 6**) are introduced. A second-order single-loop modulator with hybrid active and passive loop filter is implemented in a 65nm CMOS process, where the less critical second integrator is replaced by a passive one. Also, a second-order fully passive modulator is fabricated in the same test chip. Both designs are measured, and the test results are discussed. The first design achieves a peak SNR of 73.5dB while it consumes 1.27μW under a 0.9V power supply. The second design attains a peak SNR of 68dB from a 0.7V supply voltage. These modulators reach a high figure of merit, 0.49pJ/step and 0.296pJ/step respectively, which have proven the suitability of the proposed implementations for low-power medical applications. Based on the design and careful analysis of the aforementioned modulators, a novel fourth-order feedforward active-passive modulator is presented with only one active stage, which mitigates some of the fundamental problems associated with traditional passive ADCs. This design is the first active-passive design using full feedforward topology. Clocked at 256kHz, the modulator consumes only 400nW of power under a 0.7V supply voltage. A peak SNR of 84dB and a peak SNDR of 80.3dB have been reached in a 500Hz signal bandwidth. The proposed fourth-order feedforward modulator presents an impressive figure of merit when both Walden and Schreier FOMs are applied.

In Chapter 4, the focus of the low-power delta-sigma modulator design is on low-voltage and ultra-low voltage operation. The low-voltage design challenges and main obstacles are explained. Then the recent circuit techniques and innovations concerning the design of low/ultra-low voltage ΔΣ converters are reviewed in brief. Three ΔΣ modulators (**Papers 3, 4, 5**) operating with 0.7V, 0.5V and 270mV power supplies are introduced. At the circuit-level, the low-voltage building blocks suitable for nanometer CMOS technologies are analyzed and presented. At the same time, the low-power design, as an ultimate objective of the medical applications, is outlined. A third-order single-loop ΔΣ converter using switched-opamp and partially body-driven gain-enhanced amplifiers has been presented (**Paper 3**). The peak SNDR of the modulator reaches 87dB in a 500Hz signal bandwidth. The total power consumption is 600nW under 0.7V supply voltage. The 0.5V passive modulator presented in **Paper 4** with two other modulator designs in [1] and [2] are the three lowest operating supply voltage

modulators reported to date. It reaches higher figure of merit as compared to designs in [1] and [2]. The modulator consumes 250nW while attaining 71dB of SNDR. The resulting 86fJ/conversion-step proves this modulator an ideal topology for medium-resolution conversion in medical application. The modulator presented in **Paper 5** proposes a unique gain-boosting approach in the absence of transistor cascoding. The modulator consumes 850nW under 270mV power supply, while achieving 61dB of SNDR in a 1kHz signal bandwidth.

In Chapter 5, the design of a low-power variable bandwidth amplifier (**Papers 8**) whose unity-gain frequency can be tuned in three different levels is described. A practical application is in the analog front-end of the biomedical sensor interface [3] or neural recording integrated circuit (IC) [4], where low-power low-pass filters with a tunable cut-off corner are required. The concept, circuit design and related design challenges of the implemented tunable bandwidth OTA are presented. The chip test results are then explained. The VBA achieves three GBW levels of 0.9MHz, 1.7MHz, and 2.3MHz with a consistent DC gain of 56dB. The total power consumption is 180nW and 315nW in the low-bandwidth and full-bandwidth modes. As a practical example, a dual-mode single-clock-rate delta-sigma modulator is introduced in **Papers 9** in order to optimize both the integration area and the power consumption. The dual-mode modulator combines the designed VBA with an adjustable oversampling ratio (OSR) for the sensing/measuring stages of a cardiac pacemaker. The flexibility in the designed ADC comes with minimum circuit overhead and power penalty.

Both the circuit level and the system level approaches of the low-power low-voltage ΔΣ ADC designs in 65nm CMOS, spanning from 270mV to 0.9V supply voltage and ranging from 250nW to 2.1μW power consumption, are presented in this thesis. By applying these approaches to the ΔΣ ADC design, several test chips have proven the possibility of designing high-performance low-power low-voltage converters in nanometer CMOS technologies.

6.2 Future Work

The presented 0.5V modulator [6] consumes 250nW of power, which 90nW of this is the power dissipation in the low-voltage preamplifier. Hence, the preamp circuit can be totally removed, and the presenting gain can simply be merged with a dynamic power-efficient comparator with a higher gain in order to reduce the total power. Furthermore, by using clock boosting scheme such as the one used in **Paper 4** [7] the operating supply voltage can be decreased to 300-400mV depending upon the DR requirement, which significantly scales down the digital power, the major source of power in the current design. The normal comparator can be replaced by a buck-input gate-clocked comparator [1]. Clearly, there is a trade-off between the DR and the total power consumption when scaling down the supply voltage.

A fourth-order active-passive DT delta-sigma modulator with only one active stage was presented in **Paper 7** [8] using feedforward structure. To achieve a higher resolution, the input active integrator can incorporate a CDS technique in order to

reduce the 1/f low-frequency noise and to cancel out the dc offset voltage. Moreover, the loop filter can be extended to a fifth-order modulator using a combined feedback and feedforward loop topologies. A simple first-order passive filter realized by a distributed feedback architecture with a local feedback DAC, as shown in Fig. 3.3b, can be added between the fourth-order feedforward loop and the single-bit quantizer. This small amodification can enhance the loop stability, and the modulator SNR.

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Part II

Publications

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