Indonesian Journal of Electrical Engineering and Computer Science
Vol. 20, No. 2, November 2020, pp. 727~735
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v20.i2.pp727-735

Low power design of ultra wideband PLL using 90 nm CMOS technology

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Article Info

Article history:

Received Mar 1, 2020
Revised Apr 19, 2020
Accepted May 4, 2020

Keywords:

Charge pump
Low pass filter
Phase frequency detector
Phase locked loop
Voltage controlled oscillator

ABSTRACT

The rapid growth of the electronic system has become one of the challenges in the high performance of Very Large Scale Integration (VLSI) design and has contributed to the evolution of Phase Locked Loop (PLL) system design as one of the inevitable and significant necessities in the modern days. This design focus on the development of PLL system that can operate at a high performance within the Ultra-Wideband (UWB) frequency but consume low power that may be useful for future device implementation in the communication system. All proposed sub modules of PLL is highly suitable for low power and high speed application as each of them consumes overall power consumption around 2 µW until 1 mW with frequency from 3.1 GHz to 10.6 GHz. All the design architecture, schematic, simulation and analysis are implemented using Synopsys Tool in 90 nm CMOS technology. Through the overall analysis, it can be concluded that this proposed sub modules design of the PLL system has better performance compared to previous work in terms of power consumption and frequency.

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1. INTRODUCTION

A PLL system is a closed loop feedback control system that is capable of generating a clock signal that has a fixed relationship to the reference clock signal. The main concept of this system is to match the reference and the feedback signals in phase which is the lock condition by comparing both signals [1]. Figure 1 shows the block diagram of PLL that consists of three sub module blocks namely Phase Frequency Detector (PFD), Charge Pump (CP) and Loop Filter (LF) and Voltage Controlled Oscillator (VCO).

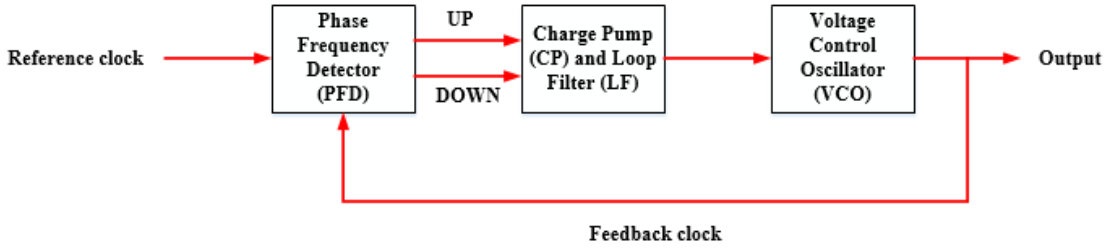

Figure 1. Basic block diagram of PLL system [2]

Designing a high performance that can operate data at very fast speed within a short time and low power dissipation is demanding nowadays especially for the portable and wireless devices that used battery powered. It is because people adored to have a device that capable to be handled and carried away easily from one to another place. Thus, the devices that can operate faster and having a long-lifetime was a total demand. So it is a challenge to design PLL system that focus in minimize power consumption while maintaining high frequency of UWB.

Some studies have been done regarding on the PLL system using various sub module blocks where in [3-6] shown some improvement in terms of frequency but however, it could not achieve the low power issue efficiently. To overcome the low power issue, a PLL system with various sub module of high speed phase frequency detector, conventional charge pump with second order low pass filter and single ended differential pair of voltage controlled ring oscillator with three stages delay cell has been chosen as the optimization method to improve the PLL system. The overall power consumption of the PLL system can be reduced mainly by minimizing the power consumption in charge pump and VCO circuit where both circuits can contribute about 20% to 50% of total power consumption of the PLL. By reducing this power consumption, the contribution of the charge pump and VCO could lead to a reduction of the overall power consumed by the PLL system. This paper is organized as follows: in Section 2, the description of the PLL circuit with various sub modules and illustrations of related mathematical modeling are described. Then, the overall result of the PLL system used in this study is discussed in Section 3. Lastly, summary and conclusion are presented in Section 4.

2. RESEARCH METHOD

2.1. Phase frequency detector

Phase frequency detector is one of the important blocks in the PLL system. Figure 2 shows the block diagram of PFD where it is used to compare the phase and frequency difference of the two clock input signals which are clock reference and clock from VCO where the reference clock (CLK_{ref}) acts as first clock input and the feedback signal that coming from VCO (CLK_{vco}) as the second clock input. By depending on the phase and frequency difference of the two clock input signals, it will provides two output signals that are UP and DOWN are generated. The output of PFD is then fed to the charge pump to generate the related control signal for VCO.

A proposed design of PFD circuit known as High Speed Phase Frequency Detector (HSPFD) is present in Figure 3. Compared to traditional PFD [7] that used two D Flip-flop, two inverters and an AND gate at the feedback path, the proposed HSPFD circuit consists of two D Flip-flop, two inverters and two NAND gates that acts to reduce power consumption and reach high speed by detect both rising and falling edges of the input signals.

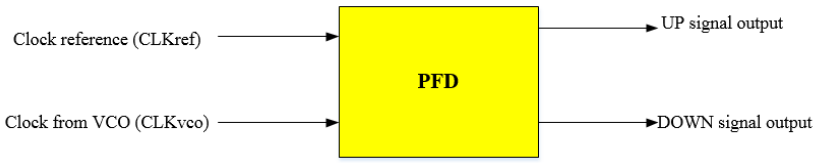

Figure 2. Block diagram of PFD [8]

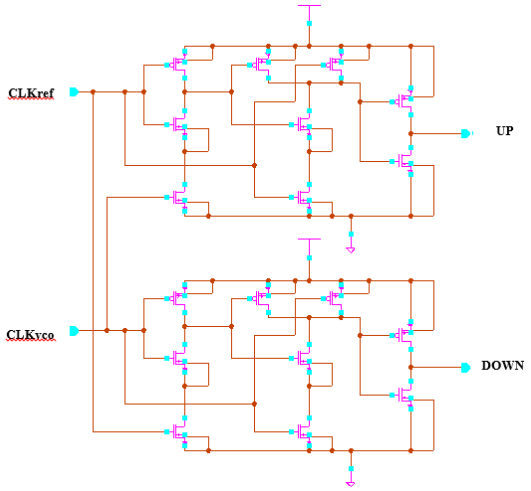

Figure 3. High speed phase frequency detector (HSPFD) circuit

2.2. Charge pump

Charge pump is an essential building block in PLL where it is controlled by three states of PFD. The main function of the charge pump is to convert the phase or frequency difference information from the PFD into an analog signal that will be fed to the input loop filter [9]. The charge pump injects, subtracts, or stored charge across a capacitor in the low pass filter by depending on the output of a sequential of PFD circuit. Figure 4 shows the basic architecture of charge pump where it consists of current source and switches. The output signal of the charge pump is then connected to low pass filter that will integrates the charge pump output current to an equivalent VCO control voltage (Vctrl). When S1 is closed, current flow into the low pass filter and increasing the control voltage to VCO. While when S2 is closed, current flow out of the low pass filter and decreasing the control voltage to the VCO [10]. Figure 5 shows the Conventional charge pump circuit that consists of 15 transistors where this circuit is used to combine two output form PFD that are UP and DOWN into a single output that will be pumped into a loop filter.

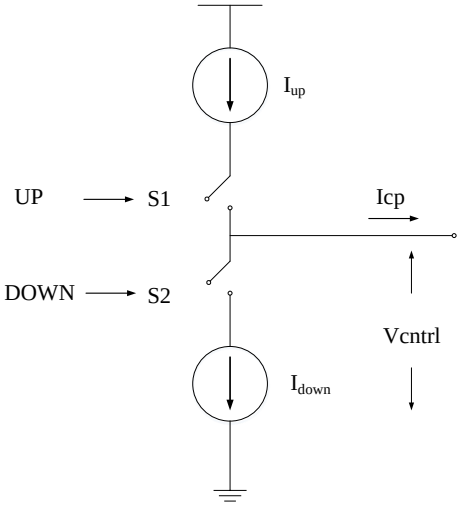

Figure 4. Basic architecture of charge pump [10]

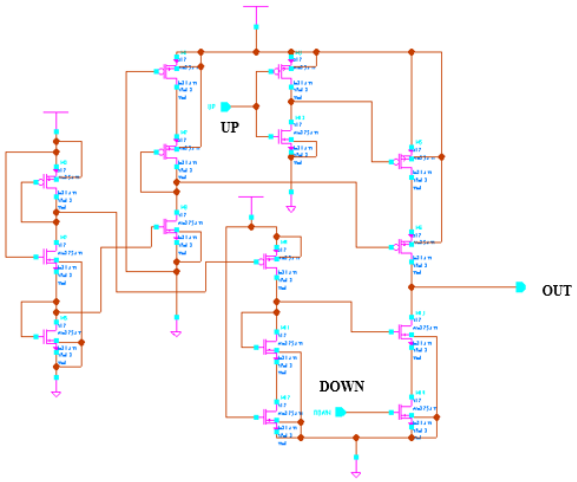

Figure 5. Conventional charge pump circuit

2.3. Loop filter

For the loop filter, it needs to be chosen carefully to avoid irrelevant values because the actual circuit of loop filter is generally remarkably simple but it has a major impact on the performance of the loop. Loop filter is functioning as a converter to convert the current coming from the charge pump to control voltage that is directly connected to VCO to control the frequency of VCO [11]. Figure 6 shows second order passive filter circuit that used in this paper where it consists of a resistor and a capacitor in series and other capacitor is used to reduce spikes which is parallel to both of them.

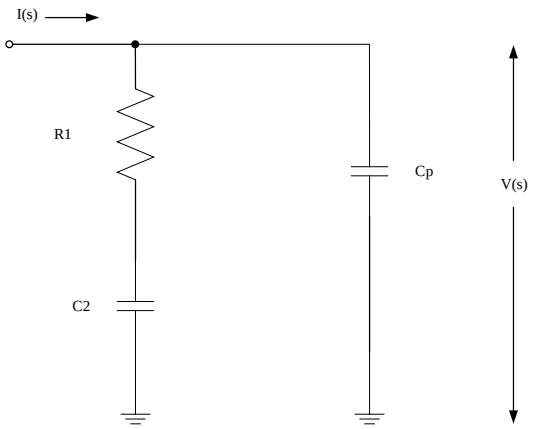

Figure 6. Second order passive filter [11]

By refering to the method introduced by Ken Holladay [11], the value of capacitance and resistance are calculated from the following equations.

$$F_{step} = F_{osc\,max} - F_{osc\,min} \quad (1)$$

$$N = \frac{F_{osc\,max}}{F_{step}} \quad (2)$$

$$F_N = \frac{2 \times BP_{PLL}}{2\pi \times \left(\xi + \frac{1}{4\times\xi}\right)} \quad (3)$$

$$C_2 = \frac{I_{CP}\times K_{VCO}}{N\times(2\pi\times F_N)^2} \quad (4)$$

$$R_1 = 2 \times \xi \times \sqrt{\frac{N}{I_{CP}\times K_{VCO}\times C_2}} \quad (5)$$

$$C_1 = \frac{C_2}{10} \quad (6)$$

where F_{step} represents the frequency step while $F_{osc\,max}$ and $F_{osc\,min}$ represents the maximum oscillator frequency and the minimum oscillator frequency from the frequency range while N represents the multiplication factor. In (3), F_N represents the natural frequency while BP_{PLL} represents the loop bandwidth and ξ represents the damping factor. In (4), I_{CP} and K_{VCO} represents the charge pump current and VCO sensitivity. Meanwhile, from (4), (5) and (6), the value of capacitor C_1 is defined by calculating the value of C_2 and R_1 . Table 1 shows the summary of parameter for second order low pass filter.

Table 1. Parameter of second order passive filter

Parameter	Values
Frequency range, F_{osc}	3.1 GH – 10.6 GHz
VCO sensitivity, K_{vco}	10 KHz
Charge pump current, I_{cp}	5 µA
loop bandwidth, BP_{PLL}	100 KHz
Damping factor, ξ	0.707
Frequency step, F_{step}	7.5 GHz
Natural frequency, F_n	30.013 KHz
Multiplication factor, N	1.4133
R_1	7.53662 MΩ
C_1	99.493 fF
C_2	0.99493 pF

2.4. Voltage controlled oscillator

Voltage controlled oscillator or known as VCO is a crucial block because the VCO performance governs many aspects of the performance of the whole PLL system. It is also able to produce an oscillating frequency from an input voltage. In VCO, the number of stages can affect the output frequency of VCO. By changing the number of stages, the oscillation frequency of VCO could be boosted. The increasing of number of staged may improve the phase noise as the phase noise was being filtered at each stage [12]. But, the VCO design with higher number of stages will increase the complexity of circuit and at the same time rise the power consumption [13]. Figure 7 shows the block diagram of voltage controlled ring oscillator (VCRO) that using single-ended differential pair configuration ring oscillator with three delay stages [14] and Figure 8 shows the proposed VCRO schematic circuit design with three delay stages that consist of an inverter and three delay stages.

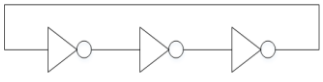

Figure 7 Block diagram of VCRO [14]

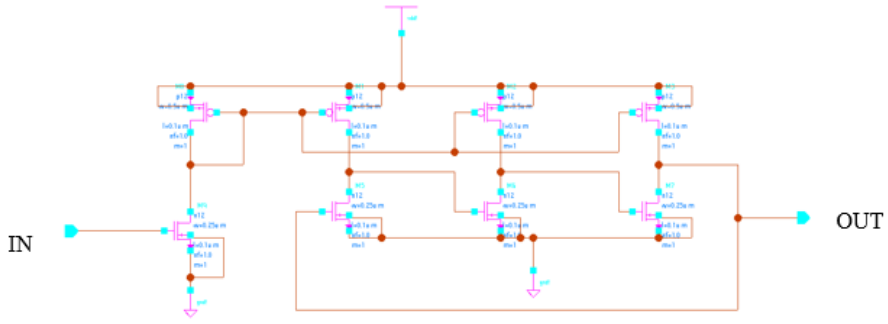

Figure 8 Schematic circuit of VCRO

3. RESULTS AND ANALYSIS

The schematic circuit of all sub module designs have been designed using Schematic Editor of 90 nm CMOS technology of Synopsys Tool. The setting of the simulation was done by using Simulation and Analysis Environment (SAE) while the output waveform was evaluated and analyzed by using WaveViewTool. The discussion of each sub module explained in sub section below.

3.1. High speed phase frequency detector (HSPFD)

The proposed design of PFD was operated at 1.2 V power supply, 1 GHz input frequency and load capacitance of 0.01 pF. There is three different output condition that occurs in the PFD that are lock condition, CLK_{ref} leading and CLK_{vco} leading. In Figure 9, both UP and DOWN are in lock condition where both input CLK_{ref} and CLK_{vco} are set in the same delay time that is 0.5 ns. Figure 10 shows the simulation waveform when the CLK_{ref} is in leading condition where CLK_{ref} is leading with 0.5 ns delay time and followed by CLK_{vco} in 100 ps. When the CLK_{ref} leading, it will charge upper D Flip-flop and cause output signal UP high. While Figure 11 shows the CLK_{vco} leading condition where this condition is vice versa from the CLK_{ref} leading condition. When CLK_{vco} is leading with 0.5 ns delay time and followed by CLK_{vco} in 100 ps, it will charge lower D Flip-flop and resulting output DOWN high. Table 2 shows the comparison of power consumption and frequency between the proposed design and previous studies design.

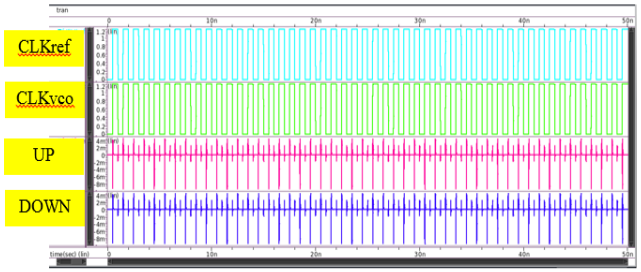

Figure 9. Output waveform in lock condition

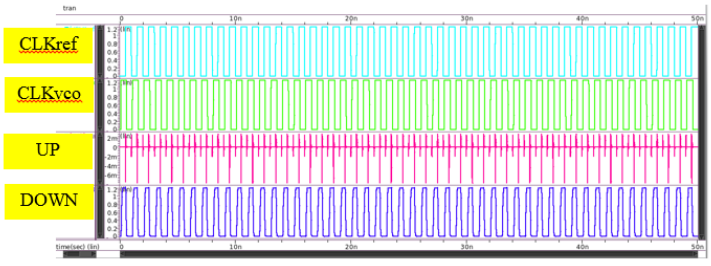

Figure 10. Output waveform in CLK_{ref} leading condition

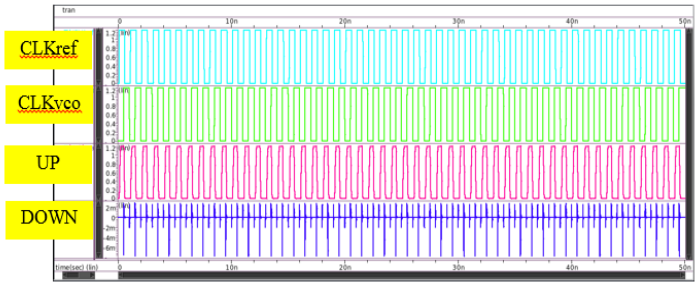

Figure 11. Output waveform in CLK_{VCO} leading condition

Table 2. Comparison of the proposed PFD design with previous studies

No	Power (µW)	Frequency (GHz)
Proposed Design	1.512	3.3
[15]	0.116	1
[16]	8.513	1
[17]	79	0.1
[18]	6.951	1
[19]	10	1.5

3.2. Conventional charge pump with second order passive filter

Figure 12 and Figure 13 shows the output waveform in charging or discharging condition. When the input UP is high and input DOWN is low, the output of the charge pump is in charging condition. While the discharging condition occurs when the input UP is low and input DOWN is high. In this proposed design, the power supply is set to 1.2 V and load capacitance of 0.01 pF is used for simulation analysis. While for Table 3 shows the comparison of power consumption and frequency between the proposed design and previous techniques used in charge pump and loop filter.

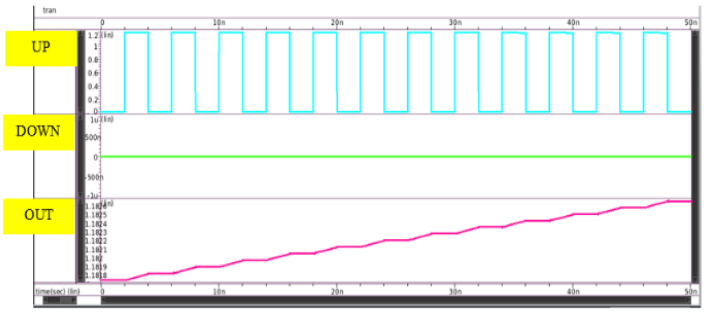

Figure 12. Output waveform in charging condition

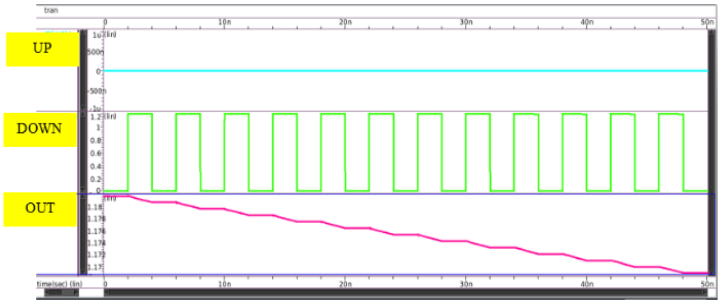

Figure 13. Output waveform in discharging condition

Table 3. Comparison between the proposed charge pump and loop filter with previous studies

No	Power (µW)	Frequency (GHz)
Proposed Design	1.235	3.2
[20]	2.07	4.7
[21]	5	1.53
[22]	37	0.5
[23]	6.76	2.2
[24]	6.69	-

3.3. Single ended differential pair of voltage controlled ring oscillator (VCRO)

Figure 14 shows the output waveform of single ended differential pair of VCRO with three stages delay cell where voltage supply of 1.2 V, voltage control of 2 V along with 6 GHz of initial sinusoidal frequency, 1 V amplitude and 2 pF of load capacitance were supplied to the input of VCRO. The simulation setting of transient analysis starts at 0.5 ns and stops at 3 ns and gives result of smaller voltage and same shape to the output of VCRO because the used of three stages of delay cell where it invert the input pulse of VCRO three times and gives the output waveform as Figure 14. While Table 4 shows the comparison of VCRO in different technology.

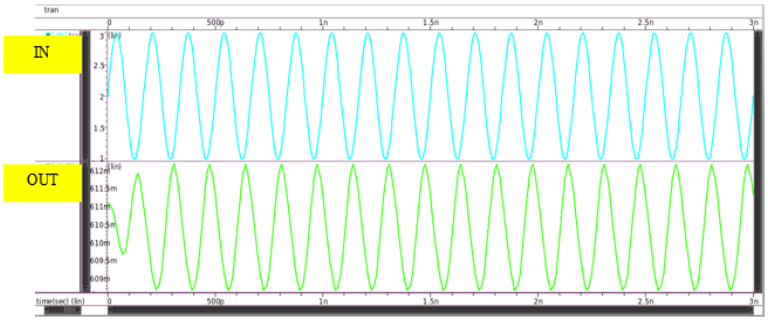

Figure 14. Output waveform in discharging condition

Table 4. Comparison of VCRO in different technology

No	Power (µW)	Frequency (GHz)
Proposed Design	687	6.5-7.138
[25]	1050	0.9-1.25
[26]	835	3.328-4.606
[27]	750	3.500-4.500
[28]	50	3.500-4.500

4. CONCLUSION

This paper has presented a PLL design with different sub modules that has been designed and implemented using Synopsys Tools in 90 nm CMOS technology. The proposed design reveals the behavior of each sub modules in the PLL system that obtain power consumption around 2 µW until 1 mW and UWB frequency from 3.1 GHz to 10.6 GHz that has great potential to be implantable in wireless and communication system. The power consumption achieved for HSPFD is 1.152 µW, while power consumption for Conventional Charge Pump with Second Order Passive Filter and VCRO are 1.235 µW and 687 µW. At the same time, the proposed design of HSPFD and for Conventional Charge Pump with Second Order Passive Filter achieved frequencies of 3.3 GHz and 3.2 GHz. While for VCRO, it is able to operate in the range of 6.5 to 7.138 GHz.

ACKNOWLEDGEMENTS

The authors would like to express gratitude for financial support and contributions from Ministry of Education (MOE) Malaysia under Fundamental Research Grant Scheme (FRGS) vot number 1630.

REFERENCES

[1] S. M. Jung, and J. M. Roveda, "Design of low jitter phase-locked loop with closed loop voltage controlled oscillator." *Wireless and Microwave Technology Conference (WAMICON), 2015 IEEE 16th Annual*, pp. 1-4, 2015.

[2] S. Maji, and S. M. S. K. Saw. "Phase Locked Loop–A Review," *International Journal of Engineering Research & Technology (IJERT), CMRAES-Conference Proceedings*, vol. 4, no. 2, 2016.

[3] S. V. R. Kaipu, K. Vaish, S. Komatireddy, A. Sood, and M. Goswami, "Design of a low power wide range phase locked loop using 180nm CMOS technology," *Signal Processing and Communication (ICSC), 2016 International Conference*, pp. 443-447, 2016.

[4] B. Yuan, and H. Liu, "A generalized low power and lower jitter charge pump PLL," *Microwave and Millimeter Wave Circuits and System Technology (MMWCST), 2013 International Workshop*, pp. 471-474, 2013.

[5] S. W. Chu, and C. K. Wang, "An 80 GHz wide tuning range Push-push VCO with boosted full-wave rectification technique in 90 nm CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 22, no. 4, pp. 203-205, 2012.

[6] K. P. Thakore, H. P. Parmar, and N. M. Devashrayee, "Low power and low jitter phase frequency detector for phase lock loop," *International Journal of Engineering Science and Technology*, vol. 3, no. 3, pp. 1998-2004, 2011.

[7] Tonk, Anu. "A comparative review and analysis of different phase frequency detectors for phase locked loops," *International Journal of Engineering Research and General Science* vol. 3, no. 6, pp. 618-632, 2015.

[8] K. P. Thakore, H. P. Parmar, and N. M. Devashrayee, "High speed PFD with charge pump and loop filter for low jitter and low power PLL" *International Journal of Electronic and Computer Technology (IJECT)*, vol. 2, no. 2, pp. 55-59, pp. 397-405, 2011.

[9] Metange PN, Khanchandani KB. "Analysis and design of high performance phase frequency detector, charge pump and loop filter circuits for phase locked loop wireless applications," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 4, no. 2, pp. 397-405, 2016.

[10] A. Agrawal, R. Khatri, "Design of low power, high gain PLL using CS-VCO on 180nm Technology," *International Journal of Computer Application*, vol. 122, no.18, pp. 26-30, 2015.

[11] K. Holladay and F. Microelectronics, "Design a PLL for a specific loop bandwidth," *EDN Network*, vol. 45, no. 21, pp. 173–175, 2000.

[12] B. Goyal, S. Suman, and P. K. Ghosh, "Design and analysis of improved performance ring VCO based on differential pair configuration," *2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT)*, pp. 3468–3472, 2016.

[13] R. Nandini, and S. R. Himadri, "Comparison of low power phase frequency detectors for delay locked loop," *International Journal of Engineering Research and Technology* vol. 2, no. 1, pp. 1-7, 2013.

[14] M. Vishwanath, and E. Sanjay, "A high-speed, low power consumption D Flip Flop for high speed frequency detector and frequency divider," *International Journal of Electronics and Communication Engineering and Technology* vol. 5, no. 8, pp. 185-193,2014.

[15] F. B. N. Al Amin, N. Ahmad, and M. H. Jabbar, "A low power CMOS phase frequency detector in high frequency PLL system," *Journal of Physics: Conference Series*, vol. 1049, no. 1, pp. 1-8, 2017.

[16] S. B. Rashmi, and S. S. Yellampalli, "Design of Phase Frequency Detector and Charge Pump for High Frequency PLL," *International Journal of Soft Computing and Engineering*, vol. 2, no. 2, pp. 88-92, 2012.

[17] J. W. Park, "Integrated high voltage boost converter with LC filter and charge pump," *Microelectronic International*, vol. 31, no. 1, pp. 54-60, 2013.

[18] I. Toihria, "Design of an effective charge pump-phase locked loops architecture for RF applications," *International Journal of Coumputer Application*, vol. 74, no. 3, pp. 38–44, 2016.

[19] K. K. Patel, N. D. Patel, and K. P. Thakore, "Charge pump, loop filter and VCO for phase lock loop using 0.18 µm CMOS technology," *Journal of VLSI and Signal Processing*, vol. 2, no. 4, pp. 21-25, 2013

[20] N. Ahmad, N. A. B. Ishaimi, and M. H. Jabbar, "Charge pump and loop filter for low power PLL using 130nm CMOS technology," *Journal of Physics: Conference Series*, vol. 1049, no. 1, pp. 1-10, 2017.

[21] M. Ali, M. Sawan, *et al*, "FM-UWB transmitter for wireless body area networks: Implementation and simulation," *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2395–2398, 2016.

[22] M. Ali, H. Shawkey, and A. Zekry, "A 750µW 3.5–4.5GHz FM-UWB transmitter," *J. Electr. Syst. Inf. Technol.*, vol. 2, no. 1, pp. 133–140, 2015.

[23] M. Ali, H. Shawkey, and A. Zekry, "Ultra-low power 3.5-4.5GHz FM-UWB transmitter," *2013 Saudi Int. Electron. Commun. Photonics Conf. SIECPC 2013*, pp. 5–8, 2013.

[24] N. Ahmad, M. K. K. B. Ibrahim, and M. H. Jabbar, "Low Power Ultra-Wideband VCRO in 130nm CMOS Technology," *Journal of Physics: Conference Series*, vol. 1049, no. 1, pp. 1-9, 2017.

[25] R. Ranjan, A. Raman, and N. Kashyap, "Low Power and High Frequency Voltage Controlled Oscillator for PLL Application," *2019 6th International Conference on Signal Processing and Integrated Networks (SPIN)*, pp. 212-214, 2019.

[26] S. Chauhan, *et al*, "CMOS Design and Performance Analysis of Ring Oscillator for Different Stages," *International Journal of Engineering Trends and Technology (IJETT)*, vol. 32, no. 5, pp. 234–237, 2016.

[27] S. Suman and P. B. P. Singh, "Design of Temperature Sensor Using Ring Oscillator," *International Journal of Scientific & Engineering Research*, vol. 3, no. 5, pp. 1-7, 2012

[28] B. S. Patro, J. K. Panigrahi, and S. K. Mandal, "A 6-17 GHz linear wide tuning range and low power ring oscillator in 45nm CMOS process for electronic warfare," *2012 International Conference on Communication, Information & Computing Technology (ICCICT)*, pp. 1-4, 2012.

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