Low-Power High-Level Synthesis for Nanoscale CMOS Circuits

Saraju P. Mohanty · Nagarajan Ranganathan
Elias Kougianos · Priyadarsan Patra

Low-Power High-Level Synthesis for Nanoscale CMOS Circuits

Springer

Saraju P. Mohanty
University of North Texas
Denton, TX
USA

Nagarajan Ranganathan
University of South Florida
Tampa, FL
USA

Elias Kougianos
University of North Texas
Denton, TX
USA

Priyadarsan Patra
Intel Corporation
Hillsboro, OR
USA

ISBN: 978-0-387-76473-3 e-ISBN: 978-0-387-76474-0
DOI: 10.1007/978-0-387-76474-0

Library of Congress Control Number: 2008920380

Printed on acid-free paper

9 8 7 6 5 4 3 2 1

springer.com

To Uma, my sisters and my parents.

To Radhika, Sheela, Shiva and my parents.

To Diane and my family.

To Anu, Ashish, Adarsh and my parents Harihar and Padmabati.

Preface

Low-Power High-Level Synthesis for Nanoscale CMOS Circuits shows very-large-scale integration (VLSI) researchers and engineers how to minimize the different types of power consumption of digital circuits. This text provides the fundamentals of high-level (also called behavioral- or architectural-level) synthesis of digital circuits. In addition, this text provides adequate knowledge in the design of low-power CMOS circuits. Students will acquire a sufficient understanding of the different methodologies of power reduction while taking into account process variations during characterization and modeling.

This self-contained text is directed to nanoscale VLSI design engineers, graduate students in electrical engineering and computer scientists who are about to start their research in high-level VLSI design. It is also an important comprehensive source for microelectronics engineers who would like to understand the different aspects of power reduction. The text assumes basic knowledge of algorithms and familiarity with digital circuit design. Since the research focus in this field is continually progressing, students will acquire sufficient knowledge after studying this book so as to be able to understand more specialized literature on their own. Each chapter has simple relevant examples for a better grasp of the principles presented. Several algorithms are given to provide a better understanding of the underlying concepts. However, the goal of this book is to train the students to develop algorithms rationally.

The text provides a sufficient amount of fundamentals to become familiar with the terminology of the field. The main objective is to achieve in-depth knowledge in a few topics instead of a shallow, broader presentation. The purpose and objective of low-power high-level synthesis is explained in Chapter 1. The initial chapters deal with the basics of high-level synthesis (Chapter 2), power (Chapter 3) and power estimation (Chapter 4). In subsequent parts of the text, a detailed discussion of methodologies for the reduction of different types of power is presented: power reduction in Chapter 5, energy or average power reduction in Chapter 6, peak power reduction in Chapter 7 and transient power reduction in Chapter 8. As the dimensions of CMOS devices decrease to nanometer scale to adhere to Moore's law, different leakage mechanisms are observed. Different schemes to minimize various forms of leakage in ICs are presented in Chapter 9.

S.P. Mohanty
Denton, TX
USA

Acknowledgments

Saraju P. Mohanty acknowledges the full support and encouragement from the Department of Computer Science and Engineering at the University of North Texas. This book derives a lot of material from the very-large-scale integration (VLSI) design courses that he teaches there as well as from his doctoral dissertation. The author is very thankful to his students for providing constant valuable feedback. Saraju P. Mohanty also thanks Dr. Krishna Kavi, the Department Chair and Dr. Oscar García, Founding Dean of the College of Engineering. He acknowledges the faculty and staff of the Department of Computer Science and Engineering for their generous support.

Nagarajan Ranganathan would like to express his gratitude to the Department of Computer Science and Engineering at the University of South Florida. He acknowledges with gratitude the research contributions of all his current and past students.

Elias Kougianos expresses his gratitude to the Department of Engineering Technology at the University of North Texas. In particular, he thanks the Department Chair, Dr. Nourredine Boubekri, for the collegial environment that he fosters in the department.

Priyadarsan Patra is grateful to Intel Corporation for fully supporting his authorship and for providing a world-class environment. He thanks his colleagues at the Strategic CAD Labs and the Microprocessor Technology Labs of Intel, where he has worked, and other colleagues from the leading product groups, for providing perspectives that have influenced what is good in this book.

The authors are grateful to Dr. Uma Choppali who has helped immensely in the preparation of figures in the book as well as Ms. Otilia Sánchez, M.A. Both of them have read the entire manuscript thoroughly and provided excellent editorial comments.

The publication of this book would not have been possible without the support of the Springer staff. We would like to thank Alex Greene and Katelyn Stanne for their promptness and patience in answering all our questions.

The authors are greatly indebted to their families for their patience, understanding and support during the innumerable hours of preoccupation with the writing of this book. Authors Saraju P. Mohanty and Elias Kougianos would like to acknowledge NSF award number 0702361.

Contents

List of Figures

List of Tables

Acronym Definition

ACO	Ant colony optimization
ACS	Ant colony scheduling
AF	Activity factor
AHD	Average Hamming distance
ALAP	As late as possible
ALU	Arithmetic logic unit
AMPL	A mathematical programming language
ARF	Autoregressive filter
ARMA	Autoregressive moving average
ASAP	As soon as possible
ASIC	Application-specific integrated circuit
ATG	Automatic test generation
BFS	Breadth first search
BN	Boolean network
BPF	Band-pass filter
BSIM	Berkeley short channel insulated gate model
BTBT	Band-to-band tunneling
CAD	Computer-aided design
CCLC	Cross-coupled level converter
CDFG	Control data flow graph
CFG	Control flow graph
CG	Compatibility graph
CLT	Central limit theorem
CMOS	Complementary metal oxide semiconductor
CMP	Chemical mechanical polishing
CPF	Cycle power function
CPLD	Complex programmable logic device
CPU	Central processing unit
CVD	Chemical vapor deposition
DCN	Diffusion-connected network
DCT	Discrete cosine transform
DCU	Dynamic clocking unit
DCVS	Differential cascade voltage switch
DFC	Dynamic frequency clocking
DFG	Data flow graph

DFM	Design for manufacturing
DG	Distribution graph
DIBL	Drain-induced barrier lowering
DPCD	Dynamic programmable clock divider
DPM	Dynamic power management
DSP	Digital signal processing
DT	Dynamic threshold
DVS	Dynamic voltage scaling
DWT	Discrete wavelet transform
EDA	Electronic design automation
EDP	Energy delay product
ESL	Electronic system level
ESTG	Extended state transition graph
EWF	Elliptic wave filter
FDS	Force directed scheduling
FET	Field effect transistor
FFT	Fast Fourier transform
FIFO	First in first out
FIR	Finite impulse response
FN	Fowler–Nordheim
FPGA	Field programmable gate array
FSM	Finite state machine
FU	Functional unit
GAS	Genetic algorithm scheduling
GDS	Generalized data stream
GIDL	Gate-induced drain leakage
GIS	Geographic information system
GTS	Game-theory (based) scheduling
HCDG	Hierarchical conditional dependency graph
HDL	Hardware description language
HL	High to low
IC	Integrated circuit
IDCT	Inverse discrete cosine transform
IEEE	Institute of Electrical and Electronics Engineers
IIR	Infinite impulse response
ILP	Integer linear programming
I/O	Input/output
IP	Intellectual property
IR	Infrared
ITRS	International Technology Roadmap for Semiconductors
LBS	List-based scheduling
LECTOR	Leakage control transistor
LCT	Leakage control transistor
LH	Low to high
LP	Linear programming

LUT	Look-up table
MC	Multicycling
MCM	Monte Carlo method
MESVS	Minimum energy schedule with voltage selection
Mκ	Multiple dielectric
MMV	MPEG motion vectors
MOSFET	Metal oxide semiconductor field effect transistor
MOVER	Multiple operating voltage energy reduction
MOX	Multiple oxide
MPEG	Moving Picture Experts Group
MT	Multiple threshold
MU	Memory unit
MV	Multiple supply voltage
MVDFC	Multiple supply voltage and dynamic frequency clocking
MVMC	Multiple supply voltage and multicycling
MVSF	Multiple supply voltage and single frequency
MWIS	Maximum weight independent set
Nano-CMOS	Nanoscale CMOS
NFA	Nondeterministic finite automata
NBTI	Negative bias temperature instability
NMOS	Metal oxide semiconductor, n type
NoC	Network on a chip
NOP	No operation
NP	Nondeterministic polynomial
ODT	On-die termination
PC	Personal computer
PCB	Printed circuit board
PDA	Personal digital assistant
PDP	Power delay product
PDSS	Profile-driven synthesis system
PI	Primary input
PLA	Programmable logic array
PLL	Phase-locked loop
PMOS	Metal oxide semiconductor, p type
PSB	Processor side bus
PSF	Process scaling factor
RAM	Random access memory
RC	Resource constrained (scheduling)
RF	Radio frequency
ROM	Read-only memory
RTL	Register transfer level
SAS	Simulated annealing scheduling
SDL	Set dominant latches
SoC	system on a chip
SOI	Silicon on insulator
SP	Signal probability

SRAM	Static random access memory
STG	State transition graph
SVDFC	Single supply voltage and dynamic frequency clocking
SVMC	Single supply voltage and multicycling
SVSF	Single supply voltage and single frequency
TC	Time constrained
TDP	Thermal design power
TLB	Translation look-aside buffer
TLM	Transaction-level modeling
TSS	Tabu search scheduling
UDFG	Unscheduled data flow graph
VHDL	VHSIC Hardware Description Language
VHSIC	Very-high-speed-integrated circuit
VLSI	Very-large-scale integration
VT	Variable threshold
WDF	Wave digital filter
YACC	“Yet another compiler” compiler