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Low Power High Performance SRAM Design Using VHDL

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Abstract- Data retention and leakage current are among the major area of concern in today's CMOS technology. In this paper 6T SRAM cell has been analyzed on the basis of read noise margin (RNM), write noise margin (WNM), read delay, write delay, and data retention voltage (DRV). Implementation and simulation is carried out using VHDL. The word "static" indicates that the memory retains its contents as long as power remains applied. SRAM indicates that locations in the memory can be accessed, i.e. written or since it is volatile memory and preserves data only while power is continuously applied. Each bit in SRAM is stored in four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote '0' and '1'. Two additional access transistors serve to control the access to a storage cell during read and write operations. It thus typically takes six MOSFETs to store one memory bit. The data retention voltage for 6T SRAM cell comes to be 252.3mV. The higher read delay is attributed to the fact that dual threshold voltage technology has been in it in the order to reduce the leakage current. Write delay has found to be 8.57 ps.

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Low Power High Performance SRAM Design Using VHDL

Mahendra Kumar[1], Kailash Chandra[2]

Abstract- Data retention and leakage current are among the major area of concern in today's CMOS technology. In this paper 6T SRAM cell has been analyzed on the basis of read noise margin (RNM), write noise margin (WNM), read delay, write delay, and data retention voltage (DRV). Implementation and simulation is carried out using VHDL. The word "static" indicates that the memory retains its contents as long as power remains applied. SRAM indicates that locations in the memory can be accessed, i.e. written or since it is volatile memory and preserves data only while power is continuously applied. Each bit in SRAM is stored in four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote '0' and '1'. Two additional access transistors serve to control the access to a storage cell during read and write operations. It thus typically takes six MOSFETs to store one memory bit. The data retention voltage for 6T SRAM cell comes to be 252.3mV. The higher read delay is attributed to the fact that dual threshold voltage technology has been in it in the order to reduce the leakage current. Write delay has found to be 8.57 ps.

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I. Introduction

For nearly 40 years CMOS devices have been scaled down in order to achieve higher speed, performance and lower power consumption. Due to their higher speed SRAM based Cache memories and System-on-chips are commonly used. Due to device scaling there are several design challenges for nanometer SRAM design. Now we are working with very low threshold voltage and ultra– thin gate oxide due to which leakage energy consumption is getting increased. Besides this data stability during read and write operation is also getting affected. In order to obtain higher noise margin along with better of the performance new SRAM cells have been introduced [4]. In most of these cell read and write operation are isolated to obtain higher noise margin. In large memory capacity RAM chips, active power reduction is vital to realizing low-cost, high-reliability chips is because it allows plastic temperature.

Hence, various low power circuit technologies concerning reductions in charging capacitance, operating voltage, and static current have been developed. As a result, active power has been reduced at every generation despite a fixed supply voltage, increased chip size, and improved access time.

II. SRAM Cells

A SRAM cell must be designed in such a way, so that it provides a non destructive read operation and a reliable write operation. In the conventional 6T SRAM cell this condition is fulfilled by appropriately sizing all the transistors in the SRAM cell. Sizing is done according to the cell ratio (CR). Traditional SRAM cells are symmetrically composed of transistors with identical leakage and threshold characteristics.

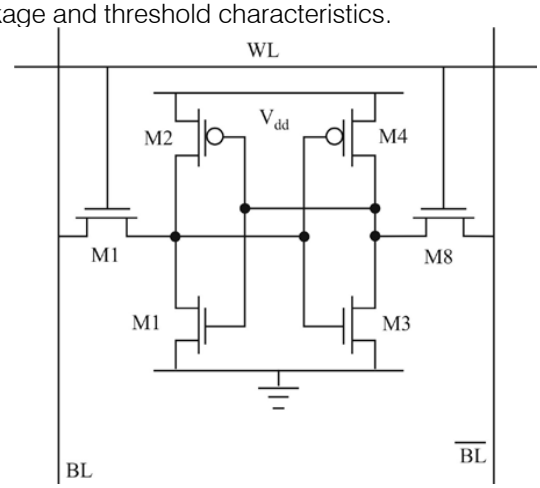

Figure 1. Six-transistor SRAM cell.

The two lines between the inverters are connected to two separate bit-lines via two n-channel pass-transistors (left and right of the cell). The gates of those transistors are driven by a word-line. The 6T SRAM cell has a differential read operation. This means that both the stored value and its inverse are used in evaluation to determine the stored value. Before the onset of a read operation, the word line is held low (grounded) and the two bit lines connected to the cell through transistors M5 and M6 are pre-charged high (to Vdd). Since the gates of M5 and M6 are held low, these access transistors are off and the cross-coupled latch is isolated from the bit lines. If a '0' is stored on the left

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storage node, the gates of the latch to the right are low. That means that transistor M3 (see figure.1) is initially turned off. In the same way M2 will also be off initially since its gate is held high. This results in a simplified model, shown in fig.2 for reading a stored '0'.

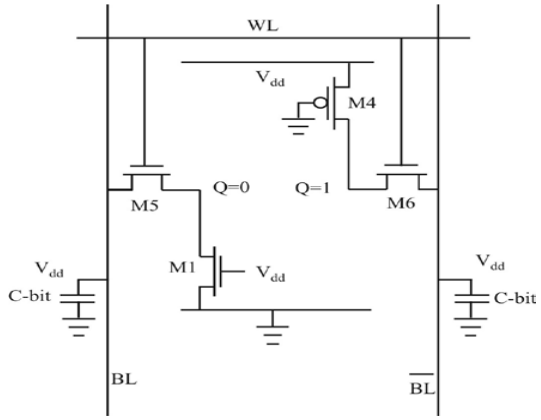

Figure 2. Six-transistor SRAM cell at the onset of read operation (reading '0').

The cell capacitance has here been represented only through the value held by each inverter (Q=0 and Q=1 respectively). The next phase of the read operation scheme is to pull the word line high and at the same time release the bit lines. This turns on the access transistors (M5 and M6) and connects the storage nodes to the bit lines. It is evident that the right storage node (the inverse node) has the same potential as BL and therefore no charge transfer will be take place on this side. The left storage node, on the other hand, is charged to '0' (low) while BL is pre-charged to VCC. Since transistor M5 now has been turned on, a current is going from C-bit to the storage node. This current discharges BL while charging the left storage node.

For a standard 6T SRAM cell, writing is done by lowering one of the bit lines to ground while asserting the word line. To write a '0' BL is lowered, while writing a '1' requires BL to be lowered. As in the previous example of a read, the cell has a '0' stored and for simplicity the schematic has been reduced in the same way as before. The main difference now is that the bit lines no longer are released. Instead they are held at Vdd and Gnd. If we look at the left side of the memory cell (M1-M5) it is virtually identical to the read operation (fig.3). Since both bit lines are now held at their respective value, the bit line capacitances have been omitted. During the discussion of read operation, it was concluded that transistor M1 had to be stronger than transistor M5 to prevent accidental writing. Now in the write case, this feature actually prevents a wanted write operation. Even when transistor M5 is turned on and current is flowing from BL to the storage node, the state of the node will not change.

As soon as the node is raised, transistor M1 will sink current to ground and the node is prevented from reaching even close to the switching point. So instead of writing a '1' to the node, we are forced to write a '0' to the

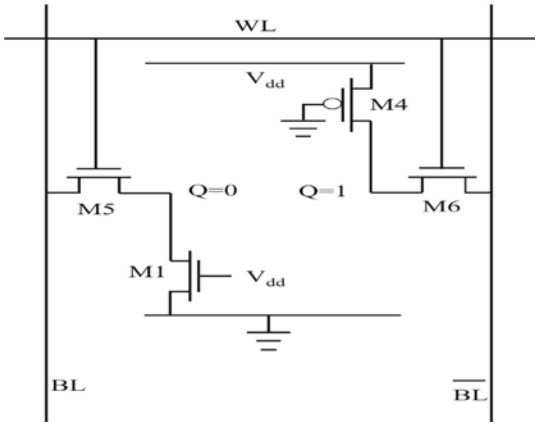

Figure 3. Six-transistor SRAM cell at the onset of write operation (writing '0','1').

inverse node. When the word line is raised M6 is turned on and current is drawn from the inverse storage node to BL. At the same time, M4 is turned on and as soon as the potential at the inverse storage node starts to decrease, current will flow from VCC to the node. In this case M6 has to be stronger than M4 for the inverse node to change its state. The transistor M4 is a PMOS transistor and inherently weaker than the NMOS transistor M6 (the mobility is lower in PMOS than in NMOS). Therefore, making both of them minimum size, according to the process design rules, will assure that M6 is stronger and that writing is possible. When the inverse node has been pulled low enough, the transistor M1 will no longer be open and the normal storage node will also flip, leaving the cell in a new stable state. The sizing for 6T SRAM cell can be used for comparisons

III. Simulation Results

A static RAM with six transistors, making a flip flop circuit with bistable states is widely used. The bistability of the SRAM cell can be observed using its eye property. In order to hold data, the static noise margin (SNM), defined by the size of the eye and should be kept large. The specification of SNM is such that are liable eye property is maintained despite the process fluctuations, variations in the operating conditions such as temperature and voltage, and bit-line noise. Since SNM becomes small with the reduction of the supply voltage, it becomes weaker against the threshold-voltage variation. In order to obtain high SNM, higher threshold voltage and high beta ratio are beneficial. By increasing the beta ratio, the slope becomes steeper and the eye becomes larger. This

Func. Block	Macrocell	Inputs	Product Terms	Pins
FB1	16 / 18	18 / 36	44 / 90	5 / 9
FB2	14 / 18	27 / 36	21 / 90	6 / 9
FB3	15 / 18	32 / 36	71 / 90	5 / 8
FB4	16 / 18	31 / 36	52 / 90	7 / 8

Table1- Functional blocks of Static RAM

increase of beta ratio results in an area increase. Higher threshold voltage makes the eye larger, though it must be kept lower than half of Vdd. If Vth becomes much larger than half of Vdd, the eyes disappear and SRAM does not work properly.

Moreover, in the case of a memory array (for example, 512 cells connected together on a single bit line), the OFF-state current and the gate-leakage current of the transfer gate will appear from each bit in a bit line despite the word line being off. When the integral value of this OFF-state current and the gate-leakage current becomes comparable to the cell current, which is supposed to be turned on by the word line, the reading operation will fail. Therefore, both small leakage of the transfer gate and large cell current are required. A longer gate length for transfer transistor and a wide width for driver are stable but result in a reduced density. Using Xilinx ISE 10.1 release version, the implementation of memory write cycle is successfully performed. First of all source for process implementation is selected. It allows opening new source. On opening new source, VHDL module and file name is selected. Next step is to define the module, which can be defined by giving port name and direction (in/out/inout). Now project navigator creates a new Skelton source with a given specifications. After finishing, writing the program and saving it, implementation process allows synthesizing. During synthesize-XST, RTL schematic view of Signal 'clk16x' mapped onto global clock net GCK1. The complement of 'clk16x' mapped onto global clock net GCK3.Global output enables net(s) unused. There are 61 macrocells in high performance mode (MCHP).There are 0 macrocells in low power mode (MCLP). The following fig. 4 shows RTL schematic view of Static RAM.

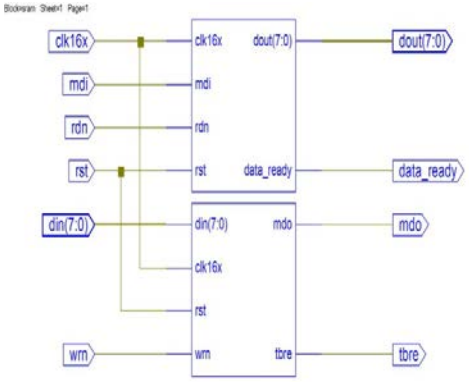

Figure 4. Internal architecture of Static RAM.

Filter report states about functional blocks and he detail of function blocks is illustrated in following table 1.

Non destructive read out characteristics of SRAM never require restoration of cell data, allowing the elimination of a sense amplifier on each data line. To obtain a fast read, the cell signal on the data line is made as small as possible, transmitted to the common U0 line through the column switch, and amplified by a sense amplifier. Since the cell signal is developed as the ratio voltage of data-line load impedance to cell transistors, a ratio current ZDC flows along the data line during word-line activation. Here, data-line charging current is negligibly small due to a very small AV, (= 0.1 V N 0.3 V), although it is prominent for write operation. Thus the current for read operation is expressed as

$$I_{DD} \cong [mi_{DC}\Delta t + C_{PT}V_{INT}]f + I_{DCP}.$$

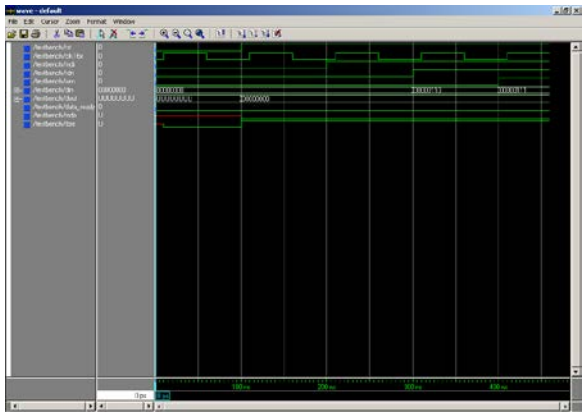

Figure 5. Simulation waveform of Static Ram.

Table 2. Signals and ports of Static RAM

Type	Name
Input Port	rst
Input Port	clk16x
Input Port	mdi
Input Port	rdn
Input Port	wrn
Input Port	din [7:0]
Output Port	dout [7:0]
Output Port	data_ready
Output Port	mdo

Due to larger width of pull down transistors in6T SRAM cell, finger type layout has been used for it.
Layout for different SRAM cell is shown in figure 6.

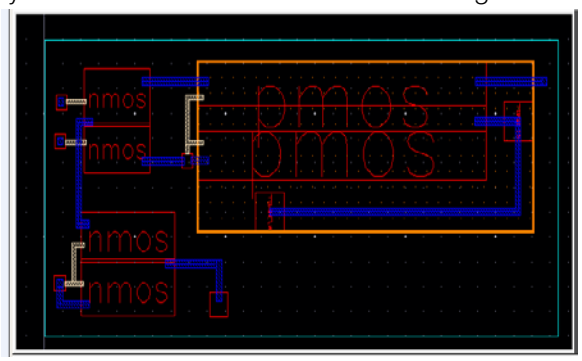

Figure 6. Layout of 6T SRAM cell.

The experimental evaluation includes analysis of power dissipation, delay and static noise margin. It is shown in following table 3.

Table 3 Experimental evaluation of basic six transistocell

S.No.	Write zero power (μW)	Write one power (μW)	Write zero delay (ns)	Write one delay (ns)	Static noise margin (mV)
1.	232.2	44	0.75	0.84	360
2.	246.8	49	0.89	0. 92	387
3.	223.4	39	0.68	0.81	323
4.	219.7	37	0.61	0.76	319

IV. Conclusions & Remarks

An innovative 6T SRAM cell concept has been proposed and validated in 45nm MCFET technology. The simulation results have shown the great potential of the proposed approach for optimizing both the cell stability and the power consumption (higher than 25%) without any area penalty and for the same read access time. The concept is well adapted for all applications, low power and high performance. Thus, IREAD can be adjusted (weakened or reinforced) for the same cell size by increasing or reducing the number of stacked silicon films. The proposed approach can also be extended to nano-Wires technology or Si Bulk technologies with a selective dip of the STI to generate trigate structures on the edges of active area, where a greater width is needed.

The trend of SRAM technology is moving towards high-density, high-speed and low-power. Higher density and higher speed are achieved by scaling. Reduction of the gate oxide leakage current is essential to achieve high-speed keeping low standby current. Pattern formation processes, lithography and dry etching are the main concerns to miniaturization. Low power consumption is achieved by reduction of the power supply and invention of the circuit design. New technology, such as Cu interconnects and low 'K' dielectrics are introduced for high-speed operation. For lower cost and higher performance, the fabrication process is moving towards single-wafer processing in 300-mm wafer size. Process integration for the single-wafer process is the key to future technology. Failure analysis also requires innovation for future devices.

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