



Low Power High-Speed Folding ADC based Partial Discharge Sensor for Wireless Fault Detection in Substations

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Abstract

Partial discharge is a well-established metric for condition monitoring and assessment of high-voltage plant equipment, such as switchgear, transformers and transmission lines. Traditional techniques for the detection of partial discharge pulses involve physical connection of sensors to the device under observation, requiring separate sensors for each item of plant, which can be costly and time consuming. Wireless partial discharge measurement provides an attractive alternative, since sensors can monitor multiple items of plant simultaneously. However, direct sampling of the received UHF partial discharge pulse is unsuitable for a scalable wireless sensor network, due to the high cost and power consumption required for high-speed data conversion. A sensor is proposed that utilizes a pipelined, sample-and-hold based, folding analogue to digital converter structure that features low power consumption when no signal is present, making it suitable for low-power data conversion of radiometric partial discharge. A proof of concept circuit has been developed using discrete components to evaluate the performance of the system with 8-bit resolution at 25 MSa/s and 56 mW of power consumption.

1. Introduction

Partial discharge (PD) is a fault that occurs within the insulating material of high-voltage (HV) equipment. PD is defined by the IEC60270 standard as “localized electrical discharge that only partially bridges the insulation between conductors and which can or cannot occur adjacent to a conductor. Partial discharges are in general a consequence of local electrical stress concentrations in the insulation or on the surface of the insulation. Generally, such discharges appear as pulses having a duration of much less than 1 microsecond” [1]. Traditional methods of detecting and monitoring PD, such as high-frequency current transformers (HFCT) and transient earth voltage (TEV) sensors [2-6], provide detailed information of the PD events under measurement, such as apparent charge and frequency spectra, allowing for evaluation of the PD fault type and progression assessment to be evaluated [7].

However, these techniques are only capable of monitoring local sources of PD within a single piece of plant, due to the close coupling required between the sensor and the equipment under test. Thus, separate sensors are required for each piece of plant to be monitored, which limits the scalability of such a network due to cost and complexity.

Radiometric PD monitoring avoids these limitations, as sensors are not restricted to monitoring single items of plant, making a system simpler and cheaper to install and scale. Traditional radiometric techniques, such as time-of-arrival (TOA) and time-difference-of-arrival (TDOA) [8-13] provide accurate wireless location estimation, but require high-speed analogue-to-digital (ADC) sampling rates in excess of 1 GSa/s in order to resolve the minute time differences between signals received at each sensor. Synchronization is also required between sensors, making implementation on a large-scale difficult.

A sensor node based on received signal-strength (RSS) only has the benefits of ease of installation, unsynchronized operation and a lower required conversion sample-rate; therefore, making a fully-scalable RSS-based wireless sensor network (WSN) an attractive solution to large-scale PD detection and monitoring. Various RSS-based PD sensors have been reported previously [14-20] which utilize envelope responding power detectors to remove the high frequency component of the received radiometric PD. Thus, the required conversion rate is dramatically reduced. However, for acceptable accuracy a sample-rate of at least 20 MSa/s is required [21], which still places some constraints on power consumption.

Proposed is a radiometric sensor, intended for use in a large-scale PD monitoring WSN, that uses a high-speed sample-and-hold (S/H) based folding ADC for data conversion. The ADC is designed to only consume significant power when a PD pulse is received.

2. Folding ADC Architecture

The folding ADC architecture consists of a cascade of folding amplifiers (FA) which each provide a non-linear

response that folds the input signal around half the input range. Each folding stage contains a comparator to determine which region the input signal is within, providing a Gray-coded bit-per-stage conversion process [22], as shown in Figure 1.

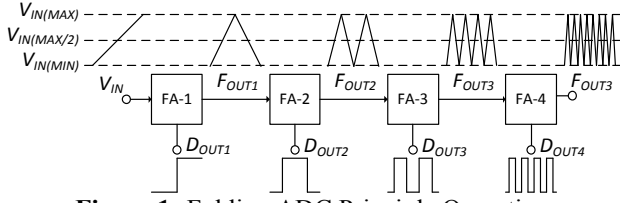


Figure 1: Folding ADC Principle Operation.

Due to this bit-per-stage response, folding ADCs typically feature low complexity compared to other high-speed architectures [23-24], such as pipelined and flash ADCs, and are therefore lower in cost and power consumption. A restriction with the standard folding ADC is the speed at which a signal needs to propagate through the series-connected FA stages, requiring high bias currents for high-speed operation, and therefore, high power consumption. This is addressed with the inclusion of S/H sections in between FA stages to reduce the required response time to that of a single stage [25]. However, this is at an increase in circuit complexity due to the addition of S/H amplifiers. The ADC architecture utilized in the proposed radiometric PD sensor incorporates the S/H function within the FA stages, therefore reducing the required power consumption and circuit complexity. The input signal is applied to a S/H amplifier which drives a series of 7 S/H FAs. Each stage is clocked from the FPGA by a complementary clock signal, which ripples the signal through each pipelined S/H FA. The LSB is obtained using a comparator. The FAs and comparator are referenced to half the input range. The output of each stage is clocked into the FPGA, which contains alignment logic to adjust each bit to the correct sample, and Gray-code to binary conversion.

3. Proposed PD Sensor

The proposed high-speed folding ADC-based wireless PD sensor, shown in Figure 2, comprises of a RF front-end section, a signal processing section, a micro-controller and a wirelessHART mote for data transmission.

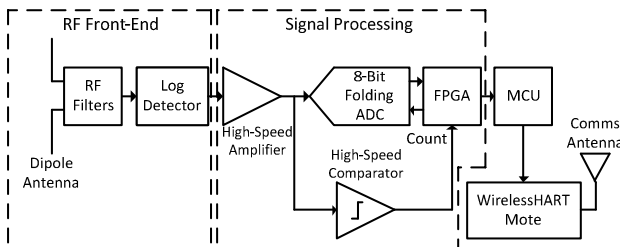


Figure 2: High-Speed ADC-based Wireless Sensor Block Diagram.

The RF front-end is composed of a dipole antenna, band-pass and band-stop filters, a logarithmic power detector and a high-speed amplifier. The radiometric PD signal is received via the dipole antenna, which is selected since an omni-directional response is required. The band-pass filter limits the measurement range of the sensor to 30-320 MHz,

whilst the band-stop filter removes potential interference from locally transmitted signals in the 70-250 MHz band. This results in two measurement bands at 30-70 MHz and 250-320 MHz.

The logarithmic power detector, used for increased receiver sensitivity, removes the high-frequency components of the received signal and produces an output which is proportional to the power in dBm of the signal envelope. The envelope detected signal is then AC-coupled to remove the DC offset of the detector, and scaled back to the 0-3 V signal range by a high-speed non-inverting amplifier. Figure 3 shows a received PD signal generated by a HVPD picocoulomb PD calibrator, and the output of the logarithmic detector for the received PD pulse.

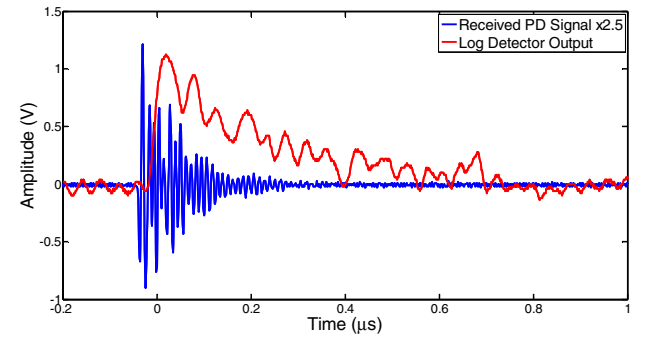


Figure 3: Received PD signal multiplied by 2.5 and logarithmic detector output.

The amplified signal is then applied to the signal conditioning section, which contains the high-speed folding ADC, a high-speed comparator and an FPGA. The comparator output is driven to a logic high level when the received PD event is above a set threshold level. This is applied to the FPGA, which immediately begins to clock the ADC with a bi-phase non-overlapping signal. The received PD signal is then sampled via the ADC at a rate of 25 MSa/s. An internal mono-stable circuit in the FPGA ensures that sampling is performed over a 1 μs period to ensure the entire pulse is acquired. Any samples taken after the pulse cause a minimal error to the PD measurement since the output of the detector is AC-coupled. The FPGA also ‘counts’ the number of PD events received each time the comparator output triggers signal acquisition.

After a PD event is received and sampled, the samples and current counter value of received events are transmitted to the micro-controller. The micro-controller then performs the calculation shown in (1) and (2) in order to convert the logarithmic power samples to linear values in mW and calculate the total energy of the received PD.

$$P_i = \frac{(V_{DET(i)} + V_{DET(DC)})}{Slope} + P_{DET(INT)} \quad (1)$$

$$E_i = E_{i-1} + \Delta T \sum_{i=1}^n 10^{\frac{P_i}{10}} \quad (2)$$

where P_i , $V_{DET(i)}$ and E_i are the received power, detector output voltage and total energy at point i respectively, E_{i-1} is the energy at the previous data point, ΔT is the time between samples, n is the number of data points, and $A_{V(N)}$,

$V_{DET(DC)}$, $Slope$ and $P_{DET(INT)}$ are the non-inverting amplifier voltage gain, detector DC offset voltage, detector slope and detector intercept power (in dBm). The average energy is then calculated for all received pulses up to the latest received event. After a predetermined period, the average energy and event counter value are transmitted to a central HUB via the wirelessHART mote.

4. Results

The proposed sensor node was tested by placing the PD calibrator source approximately 1 m from the sensor node and transmitting a radiometric PD-like signal via a 10 dB attenuator pad to simulate an increased distance. The PD signal was then received and processed by the sensor. The receiving antenna and detector output were sampled at a rate of 1 GSa/s via a digital storage oscilloscope (DSO). The energies were then calculated from the sampled received PD signal, the sampled detector output and the sensor output, Figure 4. For test purposes, the sampled data was transmitted directly to a PC via a UART to USB converter. The data was then processed directly on the PC.

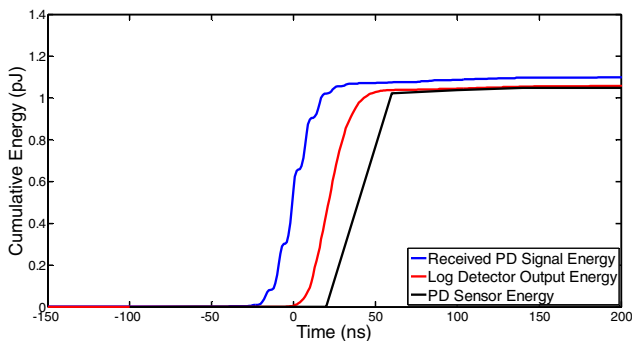


Figure 4: Calculated Energies from Sampled, Detector and Sensor Outputs.

The energies calculated via the received PD signal, the detector output and the sensor output were 1.11 pJ, 1.06 pJ and 1.04 pJ respectively, with an error of -0.21 dB between the detector output and received PD, and an error of -0.26 dB between the sensor output and received PD, which is minimal compared to the reduction in power consumption.

5. Conclusion

The proposed high-speed folding ADC-based PD monitoring sensor is designed to consume significant power only when a pulse is present, with a power consumption of approximately 56 mW from a 3.6 V supply when no signal is present. The sensor has been tested in a laboratory environment with an error of only -0.26 dB compared to the received PD signal sampled at the antenna output.

6. Acknowledgements

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7. References

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