Low-Power Low-Phase-Noise Differentially Tuned Quadrature VCO Design in Standard CMOS

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***Abstract*—This paper describes the design and optimization of voltage controlled oscillators with quadrature outputs. Systematic design of fully integrated *LC*-VCOs with a high inductance tank leads to a cross-coupled double core *LC*-VCO as the optimal solution in terms of power consumption. Futhermore, a novel fully differential frequency tuning concept is introduced to ease high integration. The concepts are verified with a 0.25-μm standard CMOS fully integrated quadrature voltage-controlled oscillator (VCO) for zero- or low-IF DCS1800, DECT, or GSM receivers. At 2.5-V power supply voltage and a total power dissipation of 20 mW, the quadrature VCO features a worst-case phase noise of −143 dBc/Hz at 3-MHz frequency offset over the tuning range. The oscillator is tuned from 1.71 to 1.99 GHz through a differential nMOS/pMOS varactor input.**

***Index Terms*—Differential tuning, LC-tank, phase noise, quadrature, VCO.**

I. Introduction

MOBILES in telecommunications systems such as DCS1800 or GSM900 offer from generation to generation higher performances and longer standby times at a lower cost. Multimode multiband capability, supporting, e.g., DCS1800, GSM900 and DECT, and in the near future UMTS, becomes very important. Receiver architectures like zero-IF or low-IF offer flexibility and low cost through high integration. The tough combination of the very low phase noise specifications with very low power consumption (battery operation) pushes designers to use *LC*-VCOs. A great research effort has been invested in the design of integrated voltage-controlled oscillators (VCOs) using integrated or external resonators, but as their power consumption is still unacceptable, today's mobile phones commonly use external *LC*-VCO modules [1], [2]. As in low-IF [3] or zero-IF transceivers, quadrature signals (0° and 90°) are needed for I/Q-(de)modulation, it is important to offer quadrature generation at a minimal power consumption. This work aims at the overall optimized design of integrated VCOs providing quadrature outputs and fulfilling the phase-noise specifications for GSM and DCS1800 at a power consumption comparable to, or even lower than, external VCO modules.

The paper is organized into seven sections. Section II covers systematic *LC*-VCO design for low power and low phase noise. Section III discusses fully integrated design. The quadrature generation issues are discussed in Section IV. Section V treats the novel differential tuning. Section VI presents the prototype design and measurements, followed by the conclusion in Section VII.

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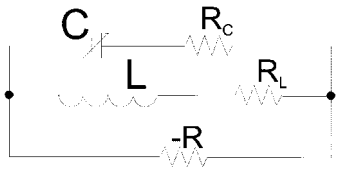

Fig. 1. Basic *LC*-VCO.

II. *LC*-VCO Design

A. LC-VCO Basics

A general *LC*-VCO can be symbolized as in Fig. 1. The oscillator consists of an inductor L and a capacitor C, building a parallel resonance tank, and an active element $-R$, compensating the losses of the inductor (R_L in Fig. 1) and the losses of the capacitor (R_C in Fig. 1). As the capacitance C is proportional to a tuning input voltage, the circuit results in a VCO with angular center frequency

$$\omega_c = \frac{1}{\sqrt{LC}}. \tag{1}$$

The capacitor C in Fig. 1 not only consists of a variable capacitor to tune the oscillator, but it also includes the parasitic or fixed capacitances of the inductor, the active elements, and the load (output driver, mixer, prescaler, etc.). VCO designs for mobile telecommunications demand the extremely tough combination of low phase noise and low power, explaining the avalanche of publications on this topic. Many publications [4]–[6], [3], [7], [8] treat the phase noise mechanisms in bipolar and MOS VCOs. As the systematic tank design used in this work is quite different to the approach used in recently published very low phase noise VCO design [9], the next section recapitulates the energy consideration theorem and Leeson's empirical phase-noise expression. These expressions are unconditionally valid for a large signal oscillator and lead to the optimized design of Section VI.

B. Design for Low Power

Recalculating capacitor and inductor losses to one single resistor, the *LC*-tank resonator simplifies to Fig. 2. Using the energy conservation theorem, the maximal energy stored in the inductor must equal the maximal energy stored in the capacitor

$$\frac{CV_{\text{peak}}^2}{2} = \frac{LI_{\text{peak}}^2}{2} \tag{2}$$

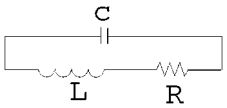

Fig. 2. Basic *LC* resonator tank.

with $V_{\rm peak}$ the peak amplitude voltage across the capacitor and $I_{\rm peak}$ the peak amplitude current through the inductor. Now we can calculate the loss in the tank as

$$P_{\rm loss} = RI_{\rm peak}^2 = C\frac{R}{L}V_{\rm peak}^2 \tag{3}$$

or with (1)

$$P_{\rm loss} = RC^2\omega_c^2 V_{\rm peak}^2 = \frac{R}{L^2\omega_c^2}V_{\rm peak}^2. \tag{4}$$

As the power consumption of a VCO must compensate at least the losses in the tank, these equations lead to some interesting conclusions for the power consumption of any *LC*-VCO.

1) It is not surprising that power loss decreases linearly for lower series resistances in the resonance tank. These equations demonstrate that for some given unavoidable series resistance in the coil, there is still the degree of freedom to increase the inductance in order to decrease the power loss.
2) Normally the frequency of oscillation is specified and cannot be changed. In this case, (4) clearly shows that power consumption decreases *quadratically*, if the tank inductance can be increased. Measurements (also simulations) on several fully integrated *LC*-VCOs, using the topology of Fig. 1, show a decreasing power consumption when tuned at higher frequencies, as predicted by (3).

C. Design for Low Phase Noise

Already in 1966, Leeson [10] published the following heuristic expression for the phase noise of an *LC*-VCO:

$$S_{\rm SSB} = F\frac{\rm kT}{2P_{\rm sig}}\frac{\omega_c^2}{Q^2\Delta\omega^2} \tag{5}$$

where Q is the loaded quality factor of the tank, $\Delta\omega = 2\pi\Delta f$ is the angular frequency offset, and F is called the device noise excess factor or simply noise factor. The equation was verified in [7], providing insight in the noise factor F. Equation (5) shows that one obvious way to reduce phase noise is to increase $P_{\rm sig} \propto V_{\rm peak}^2$. As Q goes in quadratically, (5) also clearly shows that the most effective way to lower phase noise is to use an *LC*-tank with a higher Q. Conventional inductor $Q = -{\rm Im}(y_{11})/{\rm Re}(y_{11})$ is useless as it equals to zero at tank resonance. With Barkhausen oscillation criterion, the phase stability definition for Q appears to be the most appropriate for the oscillator application (see [11] for a very thorough explanation and comparison of Q definitions). The phase stability quality factor is defined as

$$Q_{\rm PS} = -\frac{\omega_c}{2}\frac{d\phi}{d\omega}\bigg|_{\omega=\omega_c}. \tag{6}$$

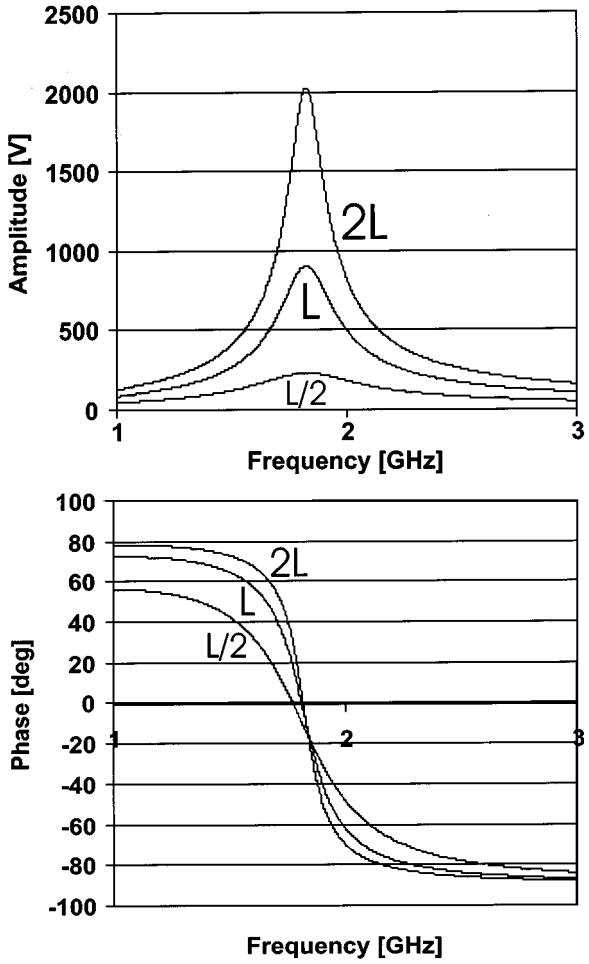

Fig. 3. *LC*-tank bode plot.

Keeping in mind that $\phi = 0$ at $\omega_c, Q_{\rm PS}$ for the *LC*-tank of Fig. 2 can easily be simplified to

$$Q_{\rm PS} = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{7}$$

or with (1)

$$Q_{\rm PS} = \frac{L}{R}\omega_c. \tag{8}$$

To provide a less mathematic insight, Fig. 3 shows the amplitude and phase plot for an *LC*-tank, keeping constant resonance frequency for different L/C ratios. A higher L/C ratio results in the phase domain into a steeper phase rolloff, or into a tank rejecting stronger any phase deviation. The amplitude representation shows, that higher L/C ratios correspond to smaller bandpass filters, or more selective filters. In practice, an upper limit for the L/C ratio is set by the required frequency tuning range. The minimal tuning range is determined by the combination of the specified frequency bands with the tolerances of the VCO components.

Substituting (8) into (5)

$$S_{\rm SSB} = F\frac{\rm kT}{2P_{\rm sig}}\frac{R^2}{L^2\Delta\omega^2} = F\frac{\rm kT}{V_{\rm peak}^2}\frac{R^3}{L^2\Delta\omega^2} \tag{9}$$

TABLE I
LOW-POWER LOW-PHASE-NOISE OPTIMIZATION SUMMARY

	low power	low phasenoise
L	maximize	maximize
C	minimize	minimize
R	minimize	minimize
Amplitude	minimize	maximize

it is remarkable that phase noise is not dependent on ω_c, or phase noise over tuning range should be constant, if $V_{\rm peak}$ can be kept constant through an amplitude control mechanism. Equation (9 leads to a very different tank, compared to [9] stating that phase noise only depends on the effective tank resistance. Equation (9) clearly shows that, despite the unavoidable high series resistances in standard CMOS processes, phase noise still can be optimized.

The conclusions of this section are summarized in Table I.

III. FULLY INTEGRATED DESIGN

A. Optimized LC-Tank

From the previous section, it is clear that an *LC*-tank with maximal L/R and L/C ratio is needed. The best available inductors are external inductors. These external components feature very high Qs, but their use is limited by the bondwires, the package and pad parasitics, and the electrostatic discharge (ESD) protection networks. Especially when aiming at highly integrated zero-IF receivers, board coupling becomes a very critical issue. For reasons of manufacturability and cost, a fully integrated solution will be the first choice, if power consumption can be reduced to an acceptable level (e.g., to the power consumption of external modules [1]). As the main goal of this work is a VCO with quadrature outputs, the complete power of VCO and interfacing and quadrature generation circuitry must be compared, which is the topic of Section IV.

The power consumption of a fully integrated solution can be reduced through an optimization of the fully integrated tank using the following design options:

- *MOS varactor*. MOS transistors are used as varactors [12] because of their high $C_{\rm max}/C_{\rm min}$. This enables an *LC*-tank with higher L/C ratio. For maximal varactor Q, a minimal length of 0.25 μm should be preferred to minimize the resistive paths in the channel. However, to decrease the effect of the fixed overlap gate–source and gate–drain capacitances and to increase $C_{\rm max}/C_{\rm min}$, MOS varactor length is set to 0.35 μm. A multifingered folded layout is used for minimal gate resistance or maximal varactor Q.
- *high winding count*. With n the number of turns in a coil, the coil inductance $L \propto n^2$ and the coil series resistance $R_s \propto n$, so a higher n will improve the R^3/L^2 ratio from (9) by n. An upper boundary for n comes from the fact that the winding-to-winding capacitance also increases with n.
- *differential coil*. The use of one differential coil, instead of two single coils [13], exploits the coupling factor to increase the inductance, leading to a higher L/C ratio. As the differential coil is used in a balanced configuration, the middle capacitance of the lumped model (Fig. 5) is cancelled out. This effectively increases the differential self-resonance frequency and the differential $Q_{\rm PS}$.
- *special coil layout*. The differential coil is further optimized through a special coil layout as shown in Fig. 4. The middle tap of the coil is the outer winding in the layout. It is laid out wider to reduce the ohmic resistance of this winding, without any capacitive penalty as its capacitance is at common mode. This increases L/R largely as the outer winding is the longest one. The inner windings are thinner, this decreases the capacitive load at the RF nodes of the oscillator increasing L/C and the differential self-resonance frequency.

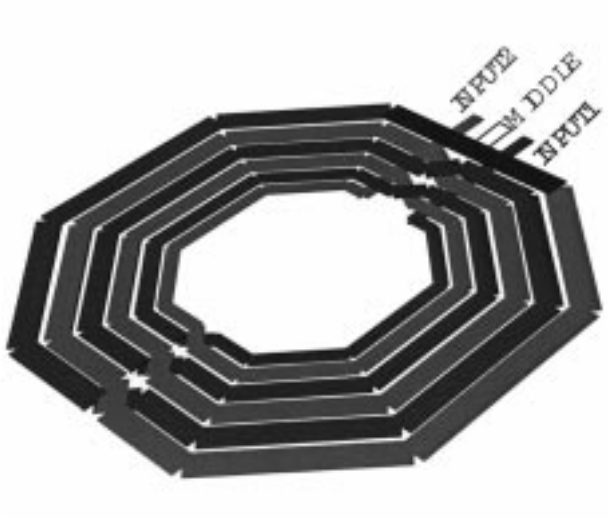

Fig. 4. Coil layout.

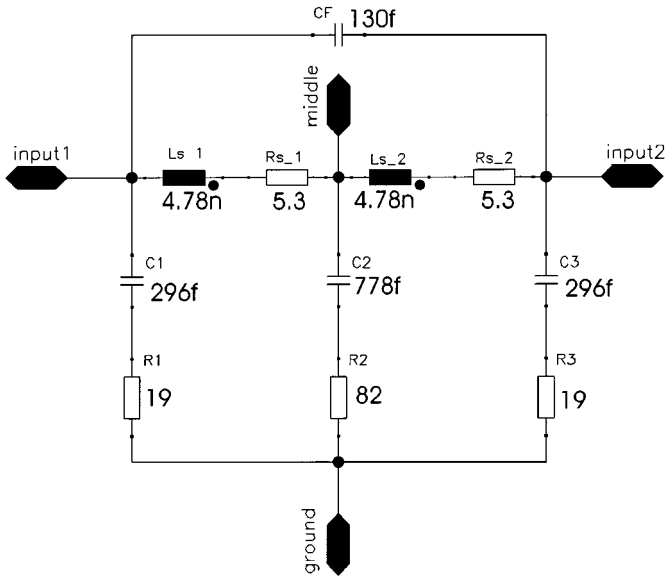

Fig. 5. Lumped circuit model for the coil.

The main drawback of this complex coil layout is that the accuracy of the lumped model needed to design the oscillator to the specified frequency and tuning range only can be extracted out of measurements. To avoid two silicon runs, the coil from

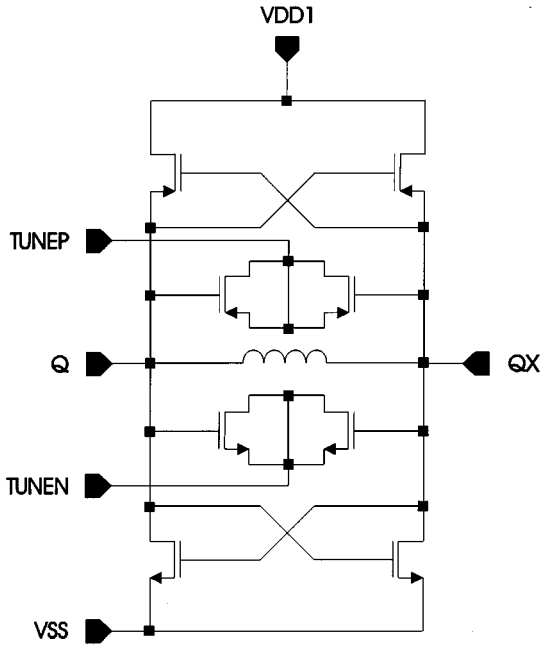

Fig. 6. Current reusing VCO topology.

[14] was reused. The 1.3-GHz coil was scaled to 1.8-GHz, through a linear geometry downscaling of the layout. The components of the lumped model were adapted according their physical meaning. The size of the resulting coil for 1.8-GHz applications is 260 μm by 260 μm. The coil was separately characterized using s-parameter structures. The lumped model extracted from the measurements is presented in Fig. 5. As the resimulation of the lumped model and the measured s-parameters match quasi-perfectly from 100-MHz to 3-GHz, the resistive losses dominate in this coil design, and no skin effect or eddy current losses had to be modeled. In balanced mode, $Q_{\rm PS}$ is about 8 in the 1.8-GHz frequency range.

B. Design of the Active Part

For the realization of the negative resistance, the combination of nMOS and pMOS transistors, as can be found, e.g., in [6], was chosen as it reuses the dc current. Furthermore, the current source was omitted to maximize the signal swing (Fig. 6). Omitting the current source has a few more advantages. It eliminates an important phase-noise source [7]. As all VCO-core transistors are put in a gigahertz-switching bias condition [15], flicker noise terms apparently are reduced by about 10 dB comparing measurement and simulation for several measured designs using this topology. The main disadvantage of omitting the current source is the increased sensitivity to the power supply (higher frequency pushing). This effect can be reduced by the integration of a voltage regulator. This topology can be redrawn to the combination of two digital inverters and an *LC*-tank. Other possible disadvantages of this very digital structure are the increased spectral impurity of the oscillator signal and the less symmetrical waveforms [6], resulting in an increased upconversion of flicker noise. Both effects can be damped by the bandpass characteristic of a well-designed resonance tank.

Finally, this topology (with or without current source) guarantees to limit all gate voltages to the supply voltage. In contrast to many VCO designs using a coil at power supply to obtain a VCO swing of twice the power supply voltage, this topology allows a reliable operation over many years within the process limits and inherently avoids degeneration effects due to, e.g., hot-electron effects.

IV. Quadrature Generation

Three design options are available to generate quadrature signals.

1) Combination of VCO, polyphase-filter (or *R-C C-R* filter), and output buffers (or limiters) as used in, e.g., [16], [17].
2) VCO at double frequency followed by master–slave flipflops.
3) Two cross-coupled VCOs as proposed in [18].

The first option needs four output buffers or limiters consuming a lot of power. If buffers are inserted between VCO and filters, even more power is needed; if the filters are directly connected to the VCO tank, tank capacitance is increased, leading to higher power consumption (4) and worse phase noise (9). Furthermore, a lot of chip area is needed, as the filters need good matching.

The second option has the smallest area. This option needs a VCO designed at double frequency, which should not consume more power, as a higher $Q_{\rm PS}$ for integrated tanks at higher frequencies is achievable (Inductance scales down linearly when sizing down an integrated coil, coil capacitance scales down quadratically, so L/C improves). However, the master–slave flipflops, which have to be designed for the doubled frequency, consume too much power in current widely used CMOS technologies (0.25 μm). As soon as next technology generations (0.18 μm, 0.12 μm) become available, this could change very rapidly. If primary design concern is low cost or small area, then this solution clearly must be preferred, as the VCO designed at double frequency features a smaller coil and the area of the master–slave flipflops in submicron CMOS is negligible.

The third option comes at the cost of double VCO area. This option outperforms the other solutions in terms of power consumption, as soon as a well-designed VCO core consumes less power than the four output buffers or limiters of the first option, or as soon as the VCO core consumes less power than the master–slave flipflops designed for double frequency needed to realize the second option. The two-core solution, furthermore, provides a very high voltage swing, which eases the design of prescaler and mixer circuits connected to the VCO. This consideration can also be extended to VCOs using external high-quality inductors. When using external inductors, a lot of current must be spent to amplify the VCO signal to drive the polyphase filters (external VCO at nominal frequency) or to drive the flipflops (external VCO at double frequency).

V. MOS Varactor Tuning

The nMOS varactors have a very steep capacitance over voltage characteristic, as shown in Fig. 7. Through gate folding, a very high measured Q at 2 GHz over gate and source/drain voltage was obtained (Fig. 8). As varactor Q is much higher than inductor Q, the MOS varactors can be considered as ideal

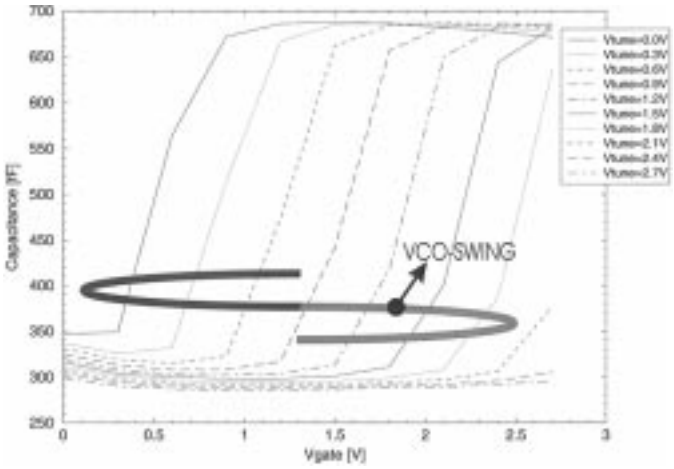

Fig. 7. Measured nMOS varactor CV characteristic.

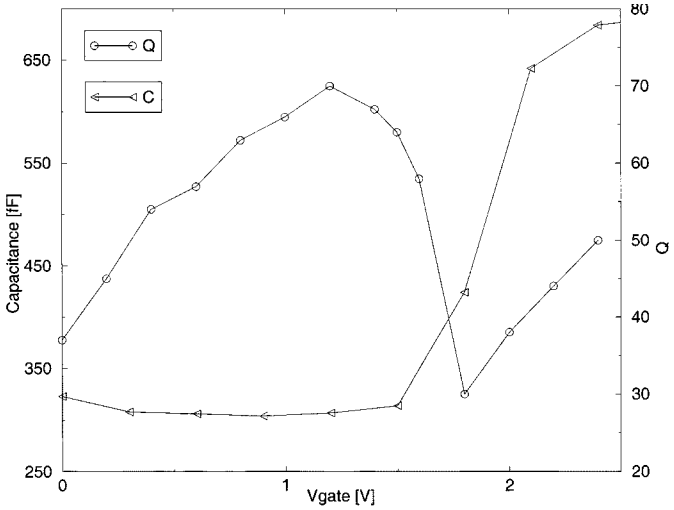

Fig. 8. Measured nMOS varactor CV & Q@2 GHz for $V_{\rm tune} = 1.2$ V.

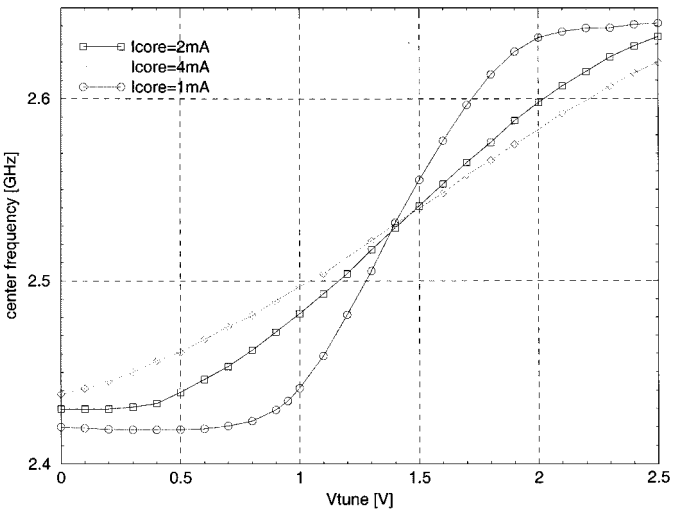

Fig. 9. Frequency tuning for different oscillator amplitudes.

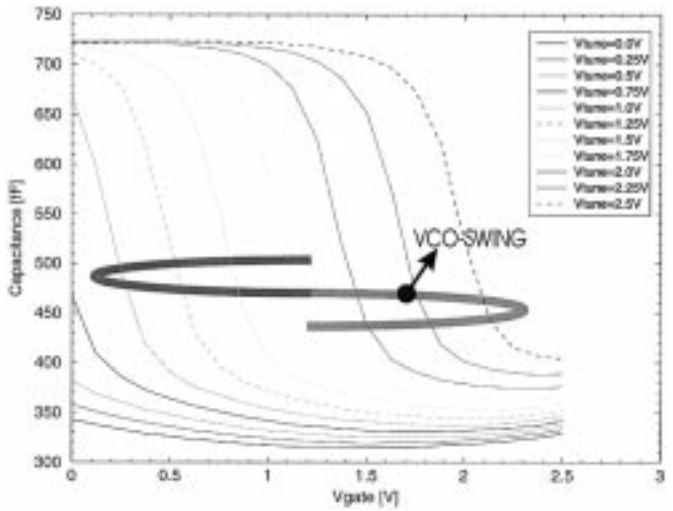

Fig. 10. Measured pMOS varactor characteristic.

capacitors. To linearize the oscillator tuning characteristic, the varactors are directly coupled to the large signal swing over the inductors. The frequency is indirectly set through the backgate voltage $V_{\rm tune}$ of the MOS transistors (Fig. 7 or 11). As shown in Fig. 7, the steep curve can be shifted through the tuning voltage $V_{\rm tune}$ on the backgates (labels as in Fig. 11). As the oscillator has a very large signal swing (nearly full power supply or 2.5 V), the effective capacitance of the varactor is averaged over each period. The resulting capacitance varies linearly with $V_{\rm tune}$ in a range defined by the oscillation amplitude, a picture of a typical resulting frequency characteristic is given in Fig. 9. The capacitance variation over each oscillation period results in harmonic distortion of the oscillator sine. Although this distortion is partially rejected by the high Q of the *LC*-tank, it is probably a source of increased flicker noise upconversion. Also, pMOS transistors can be used as varactors (measured data in Fig. 10). VCO gain ($K_{\rm vco}$, [MHz/V]) and VCO gain linear region depend on the signal swing of the oscillator and the ratio $C_{\rm min}/C_{\rm max}$ of the varactor (Fig. 9). $C_{\rm max}$ is obtained in strong inversion mode and depends on the oxide thickness $t_{\rm ox}$ of the MOS gates; it is identical for nMOS and pMOS, $C_{\text{max-pMOS}} = C_{\text{max-nMOS}}$. Varactor $C_{\rm min}$ is obtained in weak inversion mode [19], and depends on the complex channel doping profile, including LDD and HALO implants. In the submicron CMOS process used here, the ratio $C_{\text{min-pMOS}}/C_{\text{min-nMOS}} \cong 0.85 \cong 1$ (the number is process dependent). Finally, the signal swing, of course, is identical for pMOS and nMOS varactors. So a parallel connection of nMOS and pMOS varactors enables in first order a (quasi-) differentially tuned VCO with equal but opposite signed gain $K_{\rm vco}$ to nMOS and pMOS tuning input.

VI. Prototype Design and Measurements

As for the 0.25-μm CMOS process available for this design, the cross-coupled quadrature VCO definitely outperforms the other quadrature solutions in terms of power consumption. It was combined with the differential tuning concept leading to the final schematic of the prototype IC, presented in Fig. 11. The 1.5-Ωcm low-ohmic substrate nonepi standard CMOS process offers four thin aluminum metal layers. This is the worst-case scenario for coil design, comparing with bipolar, BiCMOS, or GaAs RF technologies. In the integrated inductor, the three top

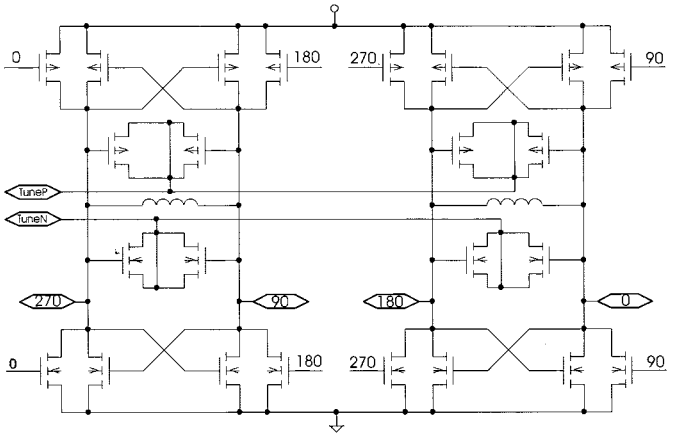

Fig. 11. Quadrature VCO schematic.

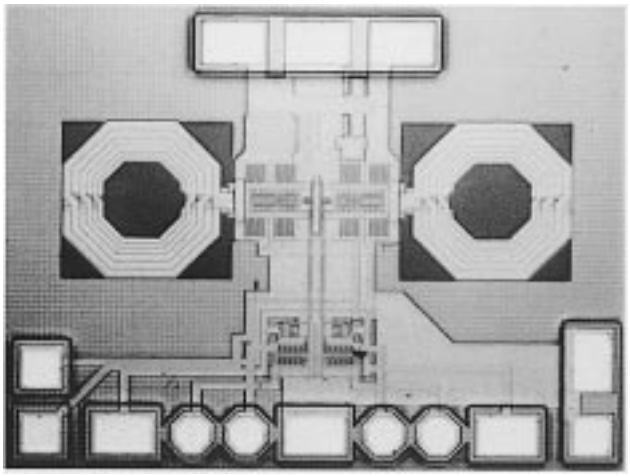

Fig. 12. Chip photo of VCO.

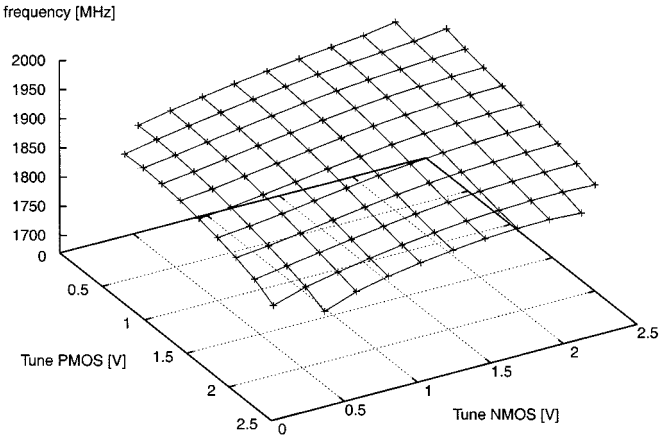

Fig. 13. VCO tuning range.

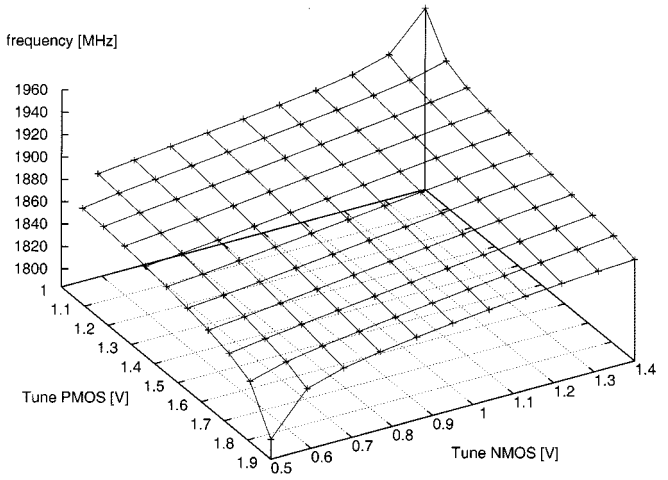

Fig. 14. Zoomed VCO tuning range.

metals were put in parallel to reduce the series resistances. For maximal speed and minimal tank capacitive load, all transistors (not including the varactors) lengths were set to minimal length of 0.25 μm. Excessive white noise [20]–[23] could become a strong argument in more advanced submicron processes to choose lengths greater than minimal.

The widths of the MOS transistors of the cores were dimensioned to obtain sine waveforms of maximal amplitude and of maximal symmetry, using ordinary SPICE transient simulations. Also by means of transient simulations, optimal core cross-coupling width was set to one third of the width of the core transistors. If the cross coupling is made too weak, a two-tone oscillation is possible; if it is made too strong, power is wasted and extra parasitics load the tanks. Due to the high Q of the tank, all MOS widths and currents can be kept small. The chip photo in Fig. 12 shows the perfectly symmetrical layout. Testchip die size is 1500 μm by 700 μm.

The 3-D tuning characteristic of the VCO is presented in Figs. 13 and 14. As the slope is very linear, it is well suited for a frequency synthesizer realization (PLL). Phase noise was measured using Europtest PN9000 equipment (delay line method); the result is presented in Fig. 15. A quadrature accuracy of ~ 3° was measured. This number is mainly due to limited accuracy

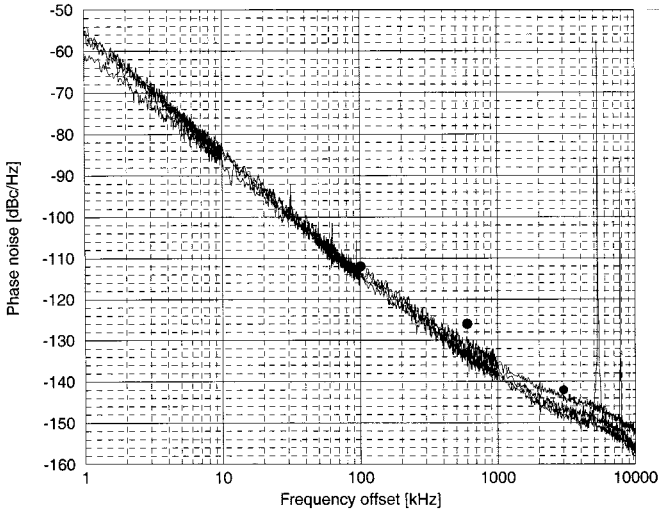

Fig. 15. Measured phase noise over frequency tuning at 2.5-V power supply, 7.8-mA core current. Dots indicate GSM requirements.

of the measurements, e.g., a bondwire length mismatch of only 0.2 mm (≅0.2 nH) leads to ~ 1° phase mismatch. Table II gives a summary of the measured performance.

TABLE II
MEASURED QUADRATURE VCO PERFORMANCE SUMMARY

Center frequency	1.72GHz-1.99GHz
Tuning range	280MHz (17%) differentially
Phase noise	< -143dBc/Hz@3MHz
Quadrature mismatch	$< 5°$
Power	20mW (7.8mA @ 2.5V)
Technology	standard 0.25μm CMOS
Area	1.1mm^2 (incl. pads)

TABLE III
PERFORMANCE OF SOME RECENTLY PUBLISHED FULLY INTEGRATED VCOS, PHASE NOISE IS RECALCULATED TO 1.8 GHz AT 3 MHz OFFSET, FOM AS DEFINED IN (10)

VCO	Tech. [μm]	Power [mW]	Phasenoise [dBc/Hz]	FOM [dBc/Hz]
[24]	0.7	6	-130	-177.8
[25]	0.25	24	-132	-174.1
[26]	0.8	66	-132	-171.1
[9]	0.25	32.4	-141	-181.5
(this)	0.25	20	-143	-185.5

A normalized phase noise has been defined as a figure of merit (FOM) for oscillators:

$$\mathrm{FOM} = S_{\mathrm{SSB}} \left(\frac{\Delta f}{f_0} \right)^2 P_{\mathrm{vco}}/\mathrm{mW} \tag{10}$$

where P_{vco} is the total VCO power consumption. This results in a FOM of -185.5 dBc/Hz for this design. In Table III, some recently published VCOs are listed. It shows that this design has a state-of-the-art phase-noise performance at an extremely low power dissipation, especially when considering that all other designs need additional power to generate quadrature outputs.

VII. CONCLUSION

The design problem to minimize the overall power consumption of a VCO with quadrature outputs is solved using two cross-coupled fully integrated high-inductance VCO cores. A prototype quadrature *LC*-VCO for 1.8 GHz was designed in 0.25-μm standard digital CMOS. A differential tuning range of 280 MHz was obtained through the use of nMOS and pMOS varactors. Measured worst-case phase noise is -143 dBc/Hz at 3 MHz. This VCO fulfills GSM and DCS1800 receive phase noise requirements at a power consumption of only 20 mW.

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