Low-Power Low-Voltage VLSI Operational Amplifier Cells

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***Abstract*—VLSI operational amplifier cells that approach the physical limitations of bandwidth, gain, and power consumption are described. To this purpose, several HF compensation architectures are presented, such as parallel Miller, multipath nested Miller, and multipath hybrid nested Miller.**

I. Introduction

HIGHER element densities in VLSI circuits entails lower power consumption per functional circuit cell. Further, smaller element dimensions entail the use of lower supply voltages necessitated by the lower breakdown voltages across the isolation barriers. It is anticipated that supply voltages will go down from the present 4.5–5 V to 2.7–3 V, further to 1.8–2 V, and ultimately to 0.9–1 V. Finally, the increasing use of battery or solar powered electronics will also demand lower supply voltages, such as 1.8 V or even 0.9 V, as well as lower power consumption.

These trends affect the fundamental limits in the design of analog circuits. The bandwidth (B) and gain (A) are restricted by minimum supply currents and voltages.

Less fundamental, but nevertheless real, are the problems which must be solved in designing complete new analog circuit architectures that allow supply voltages of down to 1.8 or even 0.9 V. The foregoing implies the design of power-efficient rail-to-rail (R-R) class-AB output stages and efficient overall topologies for bandwidth and gain.

In this paper, first, we present in Section II how to design voltage efficient input stages. In Section III, we develop the design of current-efficient output stages. In Section IV, we consider the bandwidth over power limitations of low-voltage single-stage operational amplifiers. For more gain, more stages are required. In Section V, architectures for low-power low-voltage two-stage operational amplifiers using Miller compensation are given. In Section VI, the nested Miller compensation is given for three-stage amplifiers, and in Section VII, the hybrid nested Miller compensation is presented for four-stage amplifiers. The clue in the last two sections is not to lose bandwidth while adding more stages in cascade by adopting a multipath architecture. Conclusions are given in Section VIII.

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II. Voltage-Efficient Input Stages

To process signals with the maximum signal voltage at a certain supply voltage, we require R-R input stages. An application example is an operational amplifier connected as an R-R voltage buffer amplifier. Even if we do not actually need the full R-R range, it may often be preferred to process input voltages close to either the ground rail or the single-supply rail.

The design of R-R input stages must satisfy the following requirements:

1) To reach the negative supply rail, PNP or P-channel transistors must be used while keeping their collector or drain voltages close to the ground voltage.
2) To reach the positive supply rail, NPN or N-channel transistors must be used while keeping their collector or drain voltages close to the supply voltage.
3) To achieve the full R-R range, the signals of the P- and N-type input transistors must be summed and processed in such a way that the transconductance of the complete input stage is constant over the full R-R range. If the transconductance should change, the frequency behavior would be suboptimal. This would require more quiescent current in the output stage.

This section presents designs that satisfy the above requirements.

The common-mode (CM) input voltage range of a P-channel differential CMOS input stage is restricted to a range from the negative rail voltage up to the level of the positive rail voltage minus the gate-source voltage V_{GS} and the saturation voltage V_{Dsat} of the tail-current source, as shown in Fig. 1. The CM input range of an N-channel input stage is restricted to a range from the positive rail voltage down to V_{GS} and V_{Dsat} above the negative rail voltage. If we want to obtain an R-R input range we must combine both complementary stages and allow at least one of the stages to function. This gives a lower limit to the supply voltage $V_{\text{sup, min}}$ of R-R input stages of

$$V_{\text{sup, min}} = 2V_{GS} + 2V_{Dsat}. \tag{1}$$

The minimum supply voltage for R-R operation is about 1.8 V for CMOS, depending on the technology. At supply voltages down to 0.9 V, the CM input voltage range can still include one of the rail voltages.

The complementary input stages can be combined and their output currents added by the summing circuit shown in Fig. 2. The four transistors M_5–M_8 function as two folded current followers, while the pair M_6, M_8 simultaneously functions as a current mirror.

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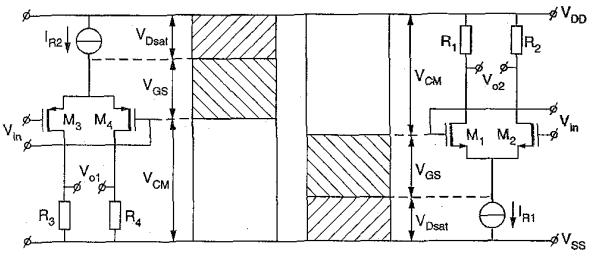

Fig. 1. Common-mode input voltage range of a P-channel and N-channel differential CMOS input stage.

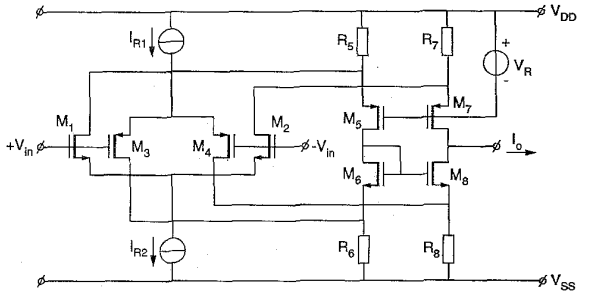

Fig. 2. R-R CMOS input stage consisting of a complementary input stage and summing circuit.

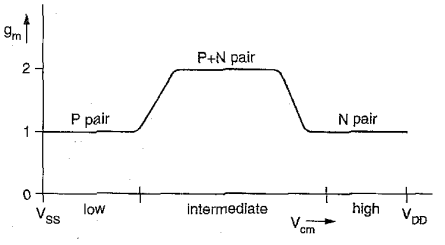

Fig. 3. Transconductance g_m versus the common-mode input voltage of a CMOS or bipolar R–R input stage.

However, one problem remains. The transconductance of the combination changes from that of the P-channel pair, up to that of the sum of both pairs, and down to that of the N-channel pair, when going from the negative rail voltage V_{SS} toward the positive rail voltage V_{DD}, as shown in Fig. 3.

In bipolar technology, the transconductance of the combination can be elegantly kept constant by keeping the sum of the tail currents of the complementary stages constant. The reason is that the transconductance g_m is proportional to the collector current I_C, according to

$$g_m = \frac{qI_C}{kT} \tag{2}$$

where q is the electron charge, k Boltzmann's constant, and T the absolute temperature. Fig. 4 shows a possible realization in which a current switch Q_5 guides one tail current I_{B1} either to the PNP pair Q_3, Q_4 or to the NPN pair Q_1, Q_2 through a current mirror Q_6, Q_7 [1], [2].

If we apply CMOS technology to the circuit shown in Fig. 4, the total transconductance would also be constant if the input transistors are biased in weak inversion. However, if they are biased in strong inversion, a 40% higher transconductance will

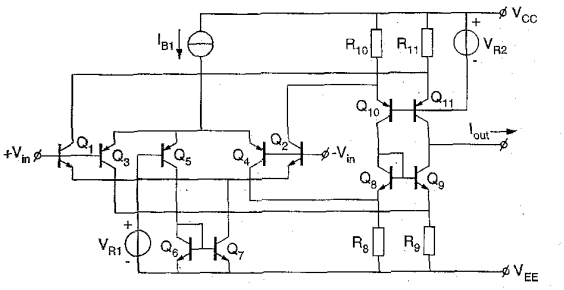

Fig. 4. R-R bipolar input stage with equalization of the transconductance by a 1:1 tail-current control.

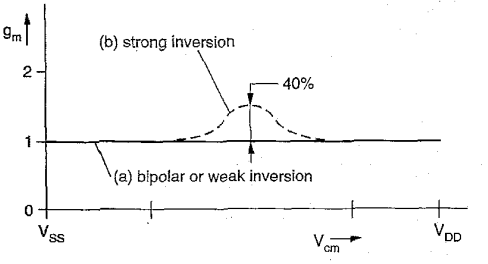

Fig. 5. Relative transconductance of a R-R input stage with 1:1 tail-current control: (a) with bipolar or CMOS in weak inversion and (b) with CMOS in strong inversion.

result in the situation where Q_5 conducts half of the current to one pair and the other half to the second pair. This is shown in Fig. 5. The reason is that the g_m of CMOS transistors is proportional to the square root of its drain current I_D in strong inversion according to

$$g_m = \sqrt{2\mu C_{ox} \frac{W}{L} I_D} \tag{3}$$

where W is the width and L the length of the transistors, μ the mobility of the charge carriers, and C_{ox} the normalized gate capacitance. In weak inversion, however, the g_m is linearly proportional to its current, as with bipolar transistors. To keep the total transconductance constant in strong inversion, we would ideally have to keep the sum of the gate-source voltages of both pairs constant, according to

$$g_m = \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \tag{4}$$

where V_{TH} is the threshold voltage, which is more complicated to achieve [3].

A simpler solution is shown in Fig. 6, where two current switches M_5 and M_8 and two 1:3 current mirrors M_6, M_7 and M_9, M_{10} supply each of the pairs with four times the normal tail current when the other pair is switched off [1], [3]. The resulting transconductance is shown in Fig. 7. The variation in the g_m is reduced to 15%, and with modified mirrors to lower values. At low supply voltages the functioning of both mirrors at the same time must be prevented, otherwise positive loop gain will excessively increase the bias current and the g_m.

It should be noted that the input offset voltage of R-R input stages varies from that of the P pair to that of the N pair when crossing the current-switching reference voltage. This change in offset causes the CMRR to deteriorate to a certain extent

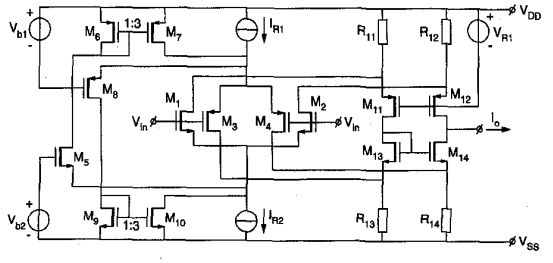

Fig. 6. R-R CMOS input stage with equalization of the transconductance by a 1:3 tail-current control.

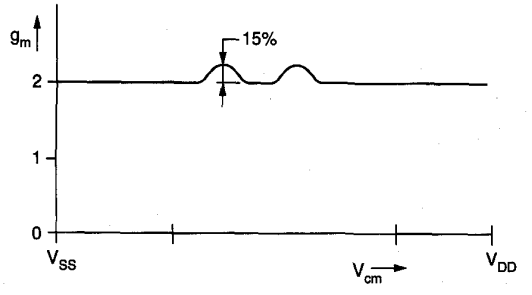

Fig. 7. Equalized transconductance of a R-R input stage with 1:3 tail-current control with CMOS transistors in strong inversion.

in the CM range around the reference voltage. Autocalibration is a way to improve this.

A. Conclusion

High performance input stages can be designed in CMOS which feature a R-R CM input voltage range at a constant transconductance. A minimum supply voltage of about 1.8 V is required for R-R operation. At supply voltages down to 0.9 V, the CM range can still include one of the rail voltages.

III. Voltage- and Current-Efficient Output Stages

Output stages for low-voltage low-power applications must satisfy three requirements:

1) The output voltage range must be R-R, to efficiently use the supply voltage.
2) The biasing must be in class-AB, to efficiently use the supply current.
3) The output transistors must be directly driven by the preceding stages without delay from the class-AB control circuit, to accommodate the highest bandwidth/supply power ratio.

This section presents designs that satisfy the above requirements.

An efficient class-AB biasing must satisfy:

1) high ratio between maximum current $I_{\max}$ and quiescent current I_{quiesc} for high efficiency.
2) a minimum current $I_{\min}$ that is not much smaller than the quiescent current I_{quiesc} to obviate HF distortion.
3) smooth AB transition to obviate LF distortion.

Fig. 8 shows the characteristics we wish to obtain.

Conventional feedforward biased output stages, as shown in Fig. 9, do have an efficient class-AB biasing, but fall short

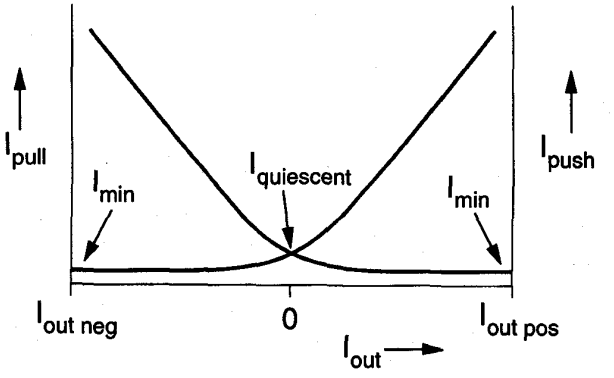

Fig. 8. Desired characteristic of the push and pull currents as a function of the output current of a class-AB stage.

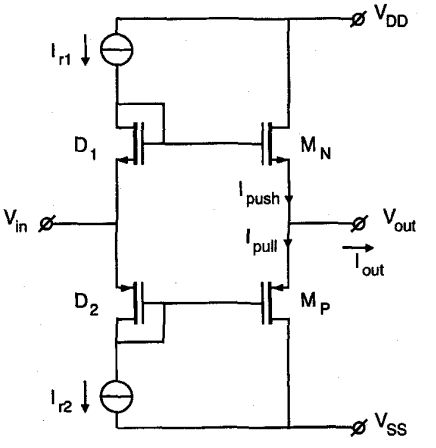

Fig. 9. Conventional CMOS common-drain stage with feedforward class-AB bias control.

of the R-R voltage range by at least two diode voltages and two drain-source saturation voltages, because their output transistors are connected in a common-drain configuration. The output transistors in R-R output stages must be connected in a common-source configuration to the ground and to the supply rail, respectively. This complicates the class-AB biasing circuit. Fig. 10 shows a common-source circuit derived by a transformation from Fig. 9. The floating voltage sources $V_s/2$ are not so simple to realize, but they depict what is desirable.

In both circuits of Figs. 9 and 10 the translinear loop consisting of the gate-source voltages of the output transistors M_P and M_N and the diode-connected transistors D_1 and D_2 secures that the sum of the gate-source voltages of M_P and M_N remains constant so that the push and the pull currents I_{push} and I_{pull} have a square-law relation according to Fig. 8. The question of how to realize the principle depicted in Fig. 10 remains.

The first feedforward biasing approach to the principle depicted in Fig. 10 is given in Fig. 11. The output transistors M_P and M_N are biased with transistors M_1 and M_2 through coupling resistor R_2, so that the sum of the gate-source voltages of M_P and M_N remains constant. The voltage across R_2 tracks that across R_1, which is equal to the supply voltage V_{DD} minus the diode voltages of D_1 and D_2. A disadvantage

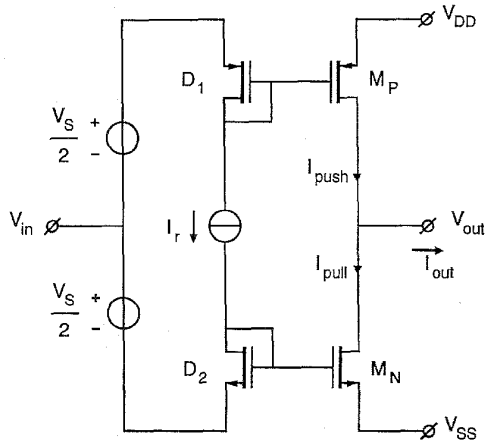

Fig. 10. R-R CMOS common-source stage with feedforward class-AB bias control.

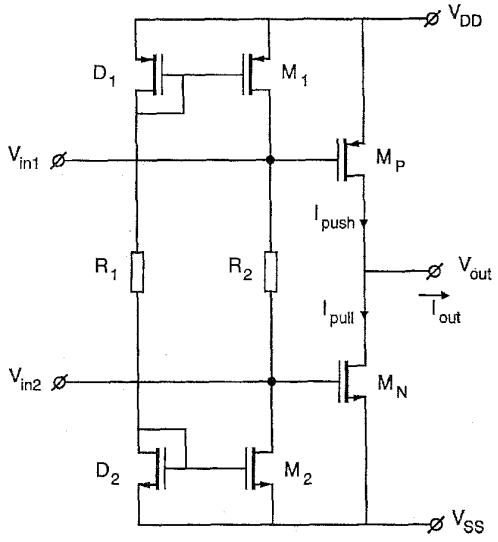

Fig. 11. R-R CMOS output stage with resistive-coupled feedforward class-AB control.

of the circuit shown in Fig. 11 is the relatively large loss of power in the resistors R_1 and R_2. The minimum voltage for this circuit is determined by the series connection of R_2, M_P, and M_N, which minimally amounts to 1.8 V.

When we give each output transistor a separate translinear loop, we have the circuit shown in Fig. 12 [6]. In order to prevent the loss of driving current in M_3 and M_4, these transistors are connected head to tail in a mesh. The positive feedback in this circuit is exactly 1, thus eliminating their source impedance loads on the input terminals for common-mode movement of their source voltages. The class-AB relation is so well fixed that the circuit can easily be driven with one input source instead of with two. The only drawback is that the circuit cannot operate at supply voltages lower than the series connection of the gate-source voltages of the output transistors and a saturation voltage. The lowest allowable supply voltage can be between 1.8–2.7 V, depending on the maximum allowable output current and technology.

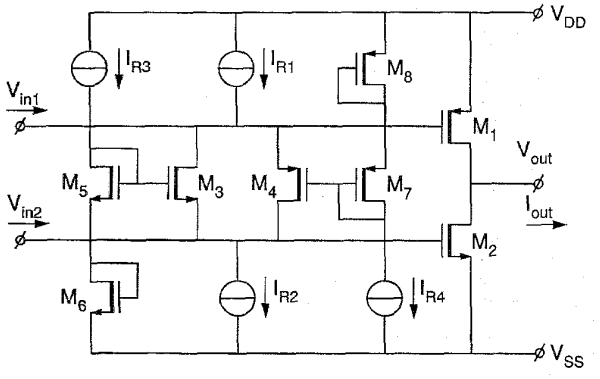

Fig. 12. R-R CMOS output stage with transistor-coupled feedforward class-AB control.

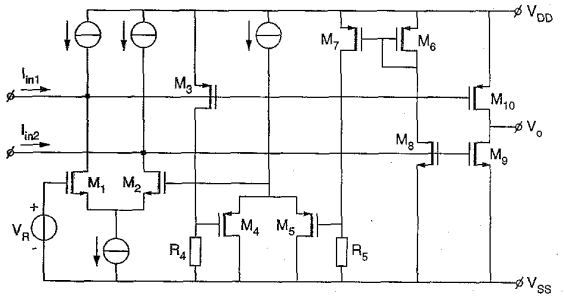

Fig. 13. R-R CMOS output stage with minimum selector and feedback class-AB control.

When we want to combine the features of accurate class-AB biasing and low supply voltage, we can apply feedback-biased class-AB control [3]. An output stage with such control is shown in Fig. 13. The gate-source voltages of the output transistors are represented by the voltages across resistors R_4 and R_5. These voltages are compared by the transistor pair M_4, M_5. The smaller voltage is transferred to the input of a control amplifier M_1, M_2 to control the bias, such that the smaller of the two push or pull output currents is regulated at a constant value [4], [5]. The class-AB control is so firm that the circuit can also be driven with one input source instead of with two. The driving current which is not needed on one side is automatically steered to the other side through the control amplifier. The resistors R_4 and R_5 can be replaced by saturated MOS transistor channels. The circuit which is shown in Fig. 13 results in accurate class-AB biasing at low supply voltages of 0.9–1.8 V, depending on the maximum output current.

A. Conclusion

We have seen that current-efficient R-R output stages can be realized. The supply voltages can be as low as 1.8 V with feedforward bias control and 0.9 V with feedback bias control. A ratio of 100 or higher between the maximum output current and the quiescent current can be obtained.

IV. Single-Stage Amplifiers

Single-stage amplifiers are very popular in VLSI circuits because of their excellent high-frequency behavior. This

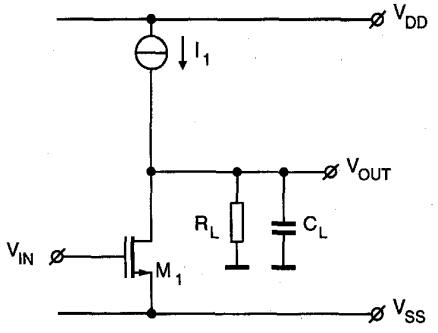

Fig. 14. Basic single-stage amplifier.

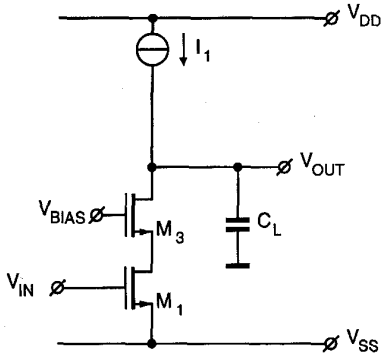

Fig. 15. Basic single-stage amplifier with cascode.

makes them very suitable for application in high-performance switched-capacitor circuits and analog-to-digital converters. Because of the single-stage topology there is no need for frequency compensation and the amplifiers are inherently very compact. In this section, we first discuss the two key parameters of amplifiers, bandwidth and gain. We discuss some possibilities to improve the gain. Finally, we consider a few circuit examples.

A simplified circuit diagram of a single-stage amplifier is shown in Fig. 14. The amplifier has only one dominant pole and the circuit is therefore always stable when feedback is applied. The unity-gain frequency B_0 of the single-stage amplifier is simply determined by the transconductance g_m and the load capacitance C_L

$$B_0 = \frac{g_m}{2\pi C_L}. \tag{5}$$

The dc voltage-gain A_0 of the amplifier is determined by the transconductance and the load resistance R_L, which also incorporates the output impedance of the transistor

$$A_0 = g_m R_L. \tag{6}$$

We see that both key parameters are directly controlled by the transconductance. Further, the gain can also be controlled by the output impedance of the transistor when it is not loaded by a low resistive load. For a CMOS transistor with a width over length ratio W/L of 100 and drain currents I_D larger than roughly 10 μA we find the unity-gain frequency as

$$B_0 = \sqrt{2\mu C_{ox}\frac{W}{L}} \cdot \frac{\sqrt{I_D}}{2\pi C_L} \approx \frac{\sqrt{I_D}}{60 C_L}. \tag{7}$$

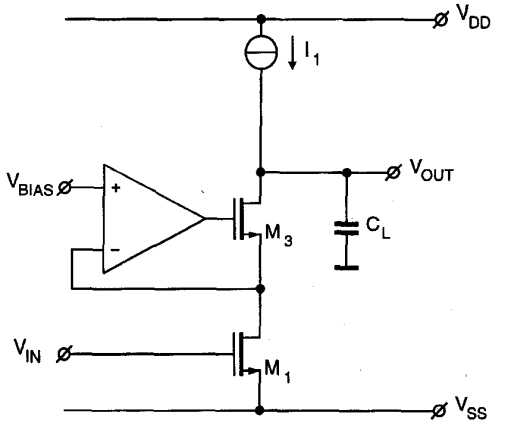

Fig. 16. Basic cascoded single-stage amplifier with gain boosting.

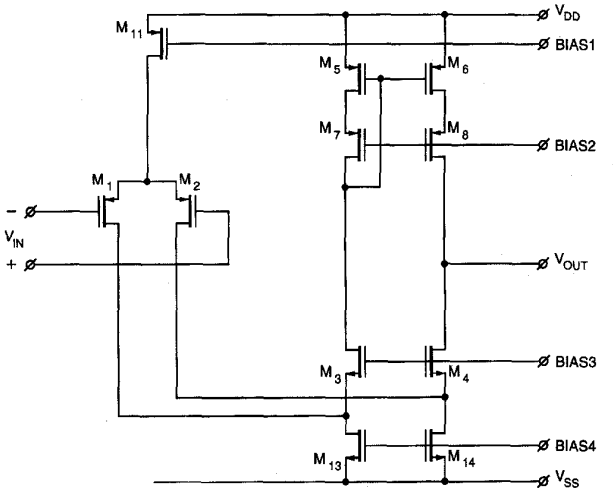

Fig. 17. Complete single-stage amplifier with folded cascode.

Dividing by the supply power gives the bandwidth to power ratio

$$\frac{B_0}{P_{\text{sup}}} = \frac{1}{60 V_{\text{sup}}\sqrt{I_D} C_L}. \tag{8}$$

The W/L ratio of a CMOS output transistor is usually in the order of about 100 to handle the output current and to reach enough bandwidth. For a current of 10 μA and a load capacitance C_L of 10 pF the CMOS single-stage amplifier has a bandwidth of 4 MHz. The gain of the single transistor depends on the length L. For a length of 2 μm the gain is usually in the order of 40 dB. Since this is too low for most purposes, methods have to be employed to improve the gain.

The gain can be improved by cascading more stages. Cascading more stages makes frequency compensation necessary and results in lower bandwidths. Amplifiers with two or more stages and frequency-compensation techniques are discussed in the following sections. Another way to achieve sufficient gain is to improve single stages. The output impedance of the stage can be increased by using a cascode, M_3, as shown in Fig. 15. The output impedance is then increased by a factor equal to the voltage gain of the cascode transistor. This results

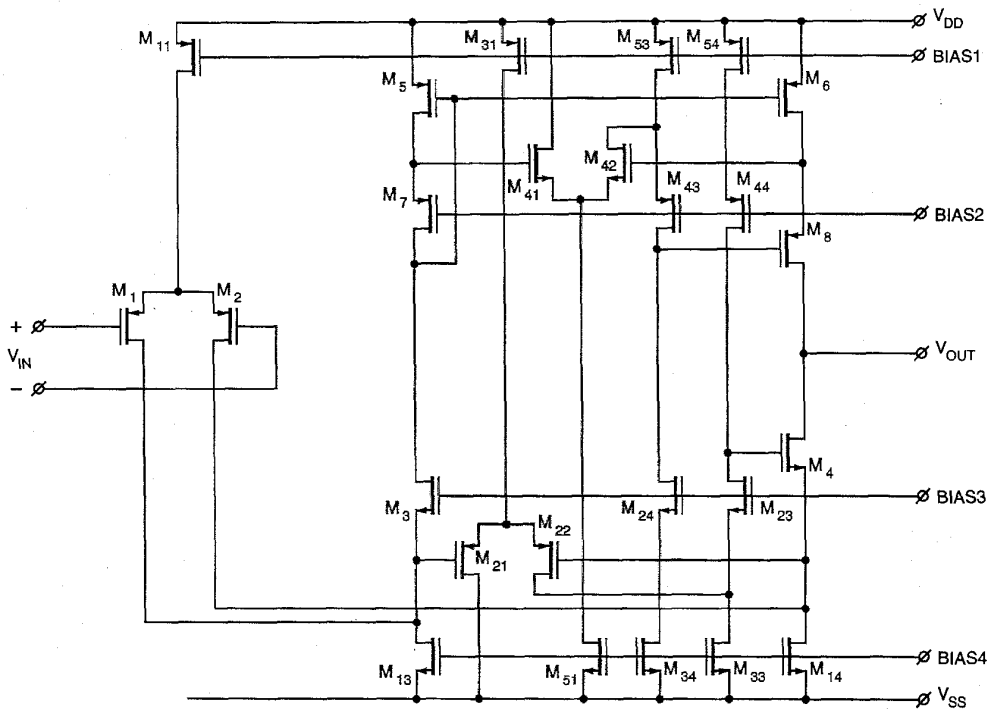

Fig. 18. Complete single-stage amplifier with gain boosting.

in an overall gain of

$$A_0 = g_{m1}r_{o1} \cdot g_{m3}r_{o3} \tag{9}$$

where g_{m1} is the transconductance of M_1, r_{o1} the small signal output resistance of M_1, g_{m3} the transconductance of M_3 and r_{o3} the small signal output reistance of M_3.

When trying to reach very high frequencies the lengths of the transistors will be very short thereby reducing the output impedance so that the gain A_0 as given by (9) is still too low. Then gain boosting can be employed to further improve the output impedance. The gain-boosting technique uses an auxiliary amplifier to create local feedback around the cascode as shown in Fig. 16 [7], [8]. Thus the output impedance of the cascode is boosted by the gain A of the auxiliary amplifier. The resulting gain of the overall amplifier is approximately

$$A_0 = g_{m1}r_{o1} \cdot g_{m3}(r_{o3} \cdot A). \tag{10}$$

Next we discuss implementations of single-stage amplifiers that use cascodes and gain boosting to achieve sufficient gain. The first example is shown in Fig. 17. It consists of a differential PMOS input stage M_1, M_2 followed by NMOS folded cascodes M_3, M_4. This arrangement yields a common-mode input voltage range that includes the negative supply rail. The differential signal is converted into a single-ended signal using current mirror M_5, M_6 which is cascoded by cascodes M_7, M_8. The minimum supply voltage is limited by the stacking of a gate-source voltage and two saturation voltages. Therefore a supply voltage of 0.9–1.8 V, depending on technology, is required.

The next step is to incorporate gain boosting in the amplifier [8]. A circuit with gain boosting is shown in Fig. 18. The general structure of this amplifier is the same as the previous circuit, consisting of input stage M_1, M_2 followed by folded cascodes M_3, M_4 and differential-to-single-ended conversion using current mirror M_5, M_6 with cascodes M_7, M_8. However, the cascodes, M_4 and M_8 which are connected to the output, are now boosted using auxiliary amplifiers consisting of transistors M_{21}–M_{23} and M_{41}–M_{43}, respectively. The auxiliary amplifiers again consist of a folded cascode amplifier with differential input stages M_{21}, M_{22} and M_{41}, M_{42}, respectively, and cascodes M_{23} and M_{43}, respectively. The current sources M_{34} and M_{54} are cascoded using M_{24} and M_{44}, respectively, to maintain the high gain of the auxiliary boosting amplifiers. The minimum supply voltage is now limited by the stacking of a gate-source voltage and three saturation voltages and thus a minimum supply voltage of about 1.8 V is required, depending on technology.

The same circuit structure can be used to realize a fully differential amplifier as shown in Fig. 19 by replacing the current mirror M_5, M_6 by current sources. The node connected to the drains of cascodes M_3 and M_7 now becomes the inverting output. These cascodes can be boosted by making the auxiliary amplifiers fully differential by using the output that was not used in the previous circuit as shown in Fig. 18 [9]. The auxiliary boosting amplifiers M_{21}–M_{23} and M_{41}–M_{43} now boost the gain of two cascodes, M_3, M_4 and M_7, M_8, respectively. The common-mode input voltage of the boosting amplifiers M_{21}–M_{23} and M_{41}–M_{43} is set using transistors M_{20} and M_{40}, respectively, and reference voltages V_1 and

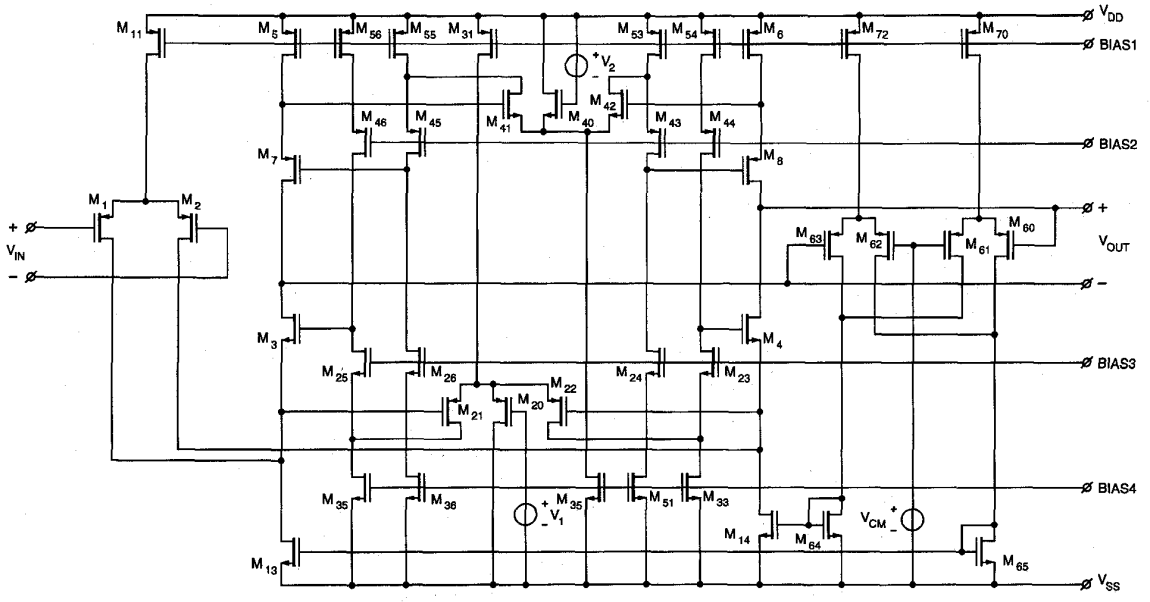

Fig. 19. Fully differential single-stage amplifier with gain boosting and common-mode feedback control.

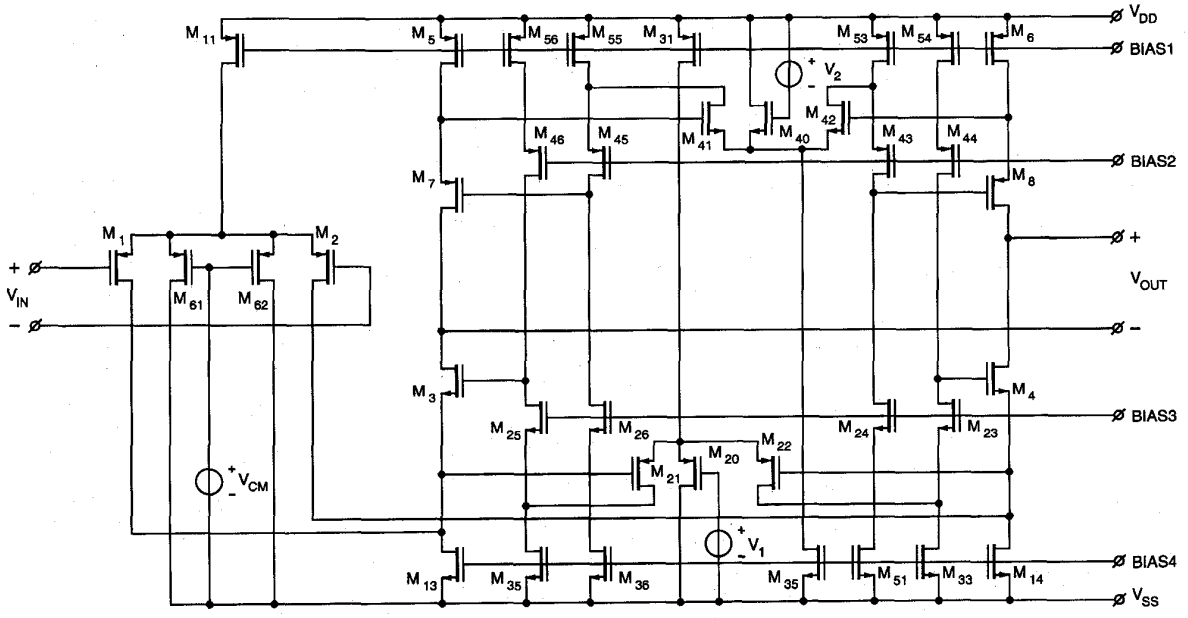

Fig. 20. Fully differential single-stage amplifier with gain boosting and common-mode feedforward control.

V_2. To control the common-mode voltage of the differential amplifier, the output common-mode voltage is sensed and compared to a reference voltage V_{CM} and a feedback loop is used to fix the common-mode voltage. This is implemented in the circuit shown in Fig. 19 [10]. The output voltage at the noninverting and the inverting output is measured and compared to the reference voltage using differential pairs M_{60}, M_{61} and M_{62}, M_{63}, respectively. The outputs of these differential pairs are summed to create two currents that depend on the common-mode output voltage. The feedback loop is obtained by using these currents to generate the bias currents of cascode M_3 and M_4. Another way to control the common-mode voltage is to use a feedforward common-mode control as shown in Fig. 20 [8]. In this circuit, transistors M_{61} and M_{62} connected to a reference voltage V_{CM} are added. Together with the input transistors M_1 and M_2 and the feedback around the amplifier, a control circuit is obtained that is basically identical to the previously discussed common-mode feedback control circuit. Through the amplifier feedback transistors, M_1 and M_2 sense the voltages at the outputs and compare these voltages to reference voltage V_{CM} using transistors M_{61}, M_{62}. The drain currents of M_1 and M_2 contain the common-mode signal which is fed into cascode M_3 and M_4.

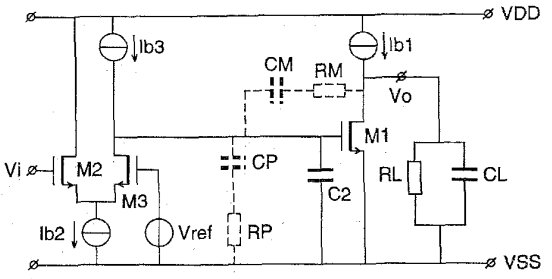

Fig. 21. Basic two-stage amplifier.

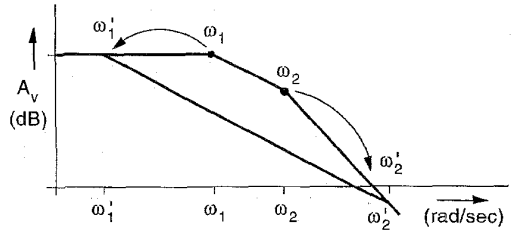

Fig. 22. Bode plot of the two-stage amplifier with Miller compensation.

The minimum supply voltage of the last two circuits is again limited by the stacking of a gate-source voltage and three saturation voltages and thus a minimum supply voltage of about 1.8 V is required, depending on technology.

V. Two-Stage Operational Amplifiers

In many applications the gain of a single stage amplifier is not sufficient; especially when it is loaded with relatively small resistors at its output. In addition, if a single-stage amplifier with folded cascodes has to drive large output currents, the saturation voltage of the cascode can be very high, and therefore limit the output voltage swing. To overcome the previously mentioned problems, a two-stage configuration can be used.

Fig. 21 shows a basic two-stage amplifier. It consists of an N-channel differential input stage M_2–M_3, and a common-source output stage, M_1. The bandwidth of a two-stage amplifier is equal to the geometrical mean of the two stages [11]. Because the circuit has two dominant poles, stability problems are likely to occur in a feedback configuration. To obviate closed-loop instability, the phase margin should be about 60°, which corresponds to a Butterworth position of the poles in a unity-gain feedback application. Hence, the bandwidth is given by

$$B = \sqrt{\frac{B_1 B_2}{2}} \tag{11}$$

where B_1 and B_2 are the bandwidths of the first and second stages, respectively. For CMOS stages operating in strong inversion, the bandwidth is given by

$$B = \frac{\mu C_{ox} \dfrac{W}{L} (V_{GS} - V_{TH})}{\pi \sqrt{2 C_2 C_L}} \tag{12}$$

where it is assumed that the input stage and output stage have the same transconductance.

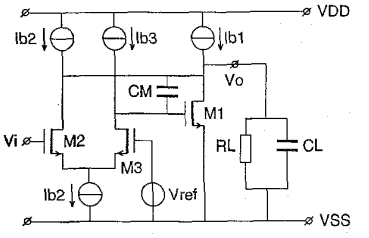

Fig. 23. Basic two-stage amplifier with multipath Miller zero cancellation.

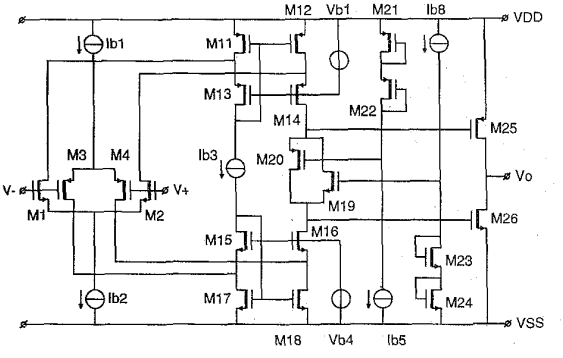

Fig. 24. Basic topology of the compact two-stage amplifier. The currents in the output transistors are regulated by a feedforward class-AB control.

Dividing by the supply power, results in

$$\frac{B}{P_{\text{sup}}} = \frac{2}{\pi (V_{GS} - V_{TH}) V_{\text{sup}}} \frac{1}{\sqrt{2 C_2 C_L}}. \tag{13}$$

From (13) it can be concluded that for the best bandwidth-to-supply power ratio, the gate-source voltage minus the threshold voltage should be as low as possible. It should be noted that for very low biasing levels, the transistors enter their weak inversion mode. In this case the term V_{GS}–V_{TH} should be replaced by two times the thermal voltage. The factor two depends on the weak inversion slope factor and might therefore differ from process to process.

The splitting of the poles to obtain a 60° phase margin is shown in Fig. 22. The poles can be split by either inserting a Miller $R_M C_M$ network, or by applying a parallel $R_P C_P$ network. The main advantage of the parallel network is that the maximum bandwidth-to-supply power ratio according to (13) can be obtained. The bandwidth can even be larger than that of a single-stage amplifier, because the internal capacitor C_2 is, in general, much smaller than the load capacitor. A drawback of parallel compensation is that the compensation method relies on matching with the load impedance. As the load of an operational amplifier is more or less user defined, it becomes almost impossible to compensate an amplifier by using parallel compensation. In addition, process variations make it even more difficult to compensate an amplifier accurately.

Miller compensation results in a much worse bandwidth-to-supply power ratio than parallel compensation. This is because the bandwidth is limited to that of the output stage. It is given by

$$B_0 = \frac{g_{m2}}{C_M} = \frac{1}{2} \omega_2' = \frac{1}{2} \frac{g_{m1}}{C_L} \tag{14}$$

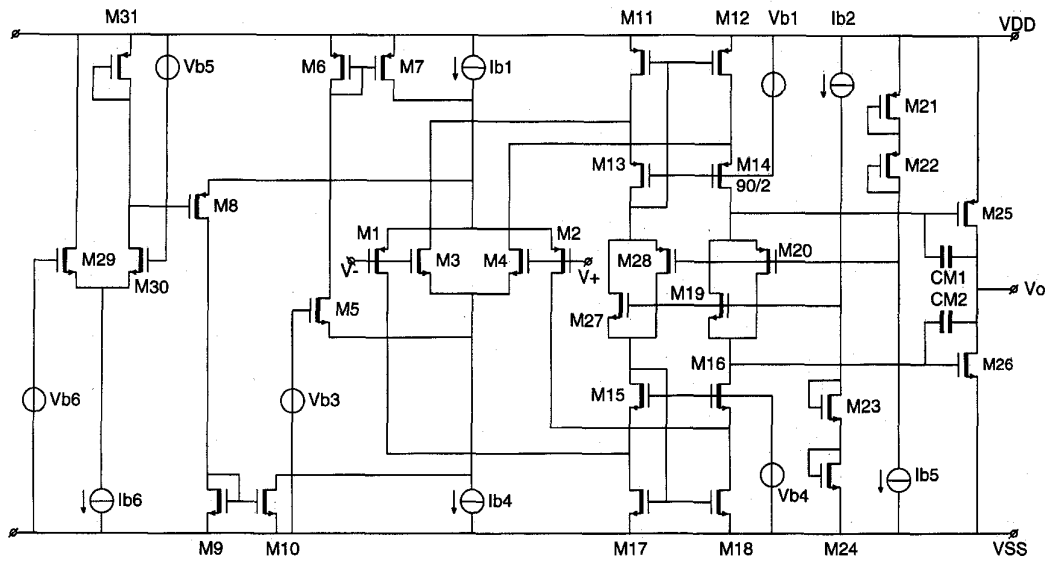

Fig. 25. A realization of the compact two-stage amplifier.

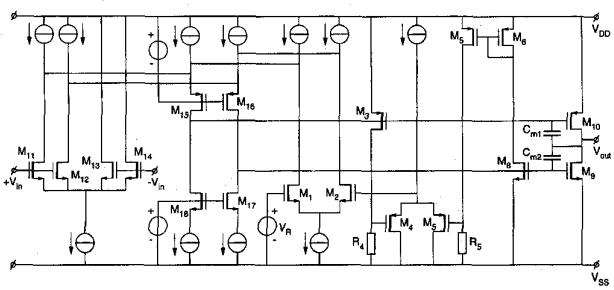

Fig. 26. A realization of a two-stage amplifier with class-AB feedback control.

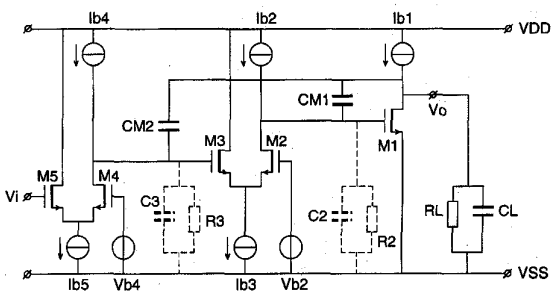

Fig. 27. Basic topology of a three-stage amplifier with nested Miller compensation.

where g_{m1} is the output stage transconductance. In general, this bandwidth is much lower than the bandwidth given by (12), because the load capacitor is much larger than the interstage capacitor. In contrast to parallel compensation, Miller compensation is robust against parameter variations, which makes it the best compensation technique for two-stage amplifiers.

A drawback of Miller compensation is that, at high frequencies the Miller capacitor introduces a direct feedforward path to the output. As a consequence, a right half-plane zero occurs in the open-loop transfer function of the amplifier. This zero can cause considerable phase shift, and thereby decrease the phase margin of the opamp. An effective way to eliminate this zero is the multipath Miller zero cancellation, as shown in Fig. 23 [19]. M_3 drives the output transistor while M_2 drives the output node. The current through M_2 compensates the feedforward current through the Miller capacitor. Hence, the output does not experience any effect from the feedforward path, and thus the right half-plane zero is eliminated.

Fig. 24 shows an example of a two-stage amplifier topology [12], [13]. It consists of a R-R input stage M_1–M_4, a summing circuit, M_{11}–M_{18}, and a R-R output stage with feedforward class-AB control, M_{19}–M_{24}. The summing circuit contains two current mirrors, which are biased by a floating current source, I_{b3}. This provides a constant current in the cascodes M_{14} and M_{16}, independent of the bias currents of the input pairs. The class-AB driver, M_{19} and M_{20}, is biased by these cascodes. This obviates a contribution to the noise and offset of two independent current sources, which would otherwise be necessary to bias the floating class-AB driver.

Using the topology described above, a complete amplifier has been realized, as is shown in Fig. 25 [13]. The amplifier is compensated using the above-described Miller technique. To obtain a constant transconductance over the common-mode input range, two three-times current mirrors, M_6–M_7 and M_9–M_{10}, have been added to the input stage. To prevent the current switches from forming a positive feedback loop at very low supply voltages, the differential pair, M_{29}–M_{30}, has been added to the g_m-control. If the supply voltage approaches a critical value, the gate voltage of M_8 is moved toward the positive supply rail. Thus M_8 is always off at very low supply voltages, and hence the positive feedback loop can never become active. The floating current source is realized by M_{27}–M_{28}. The value of the current source is set by two translinear loops, M_{11}–M_{28}–M_{22}–M_{21} and M_{17}–M_{27}–M_{23}–M_{24}. The floating current source has the same architecture as the class-AB control. Therefore, the supply voltage dependency of the class-AB control, due to

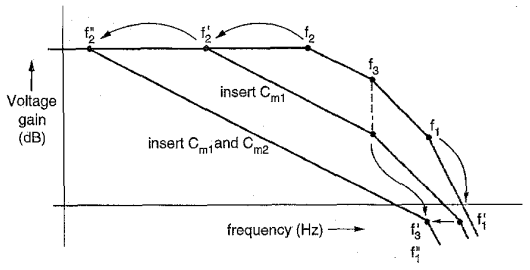

Fig. 28. Bode plot of a three stage amplifier with nested Miller compensation.

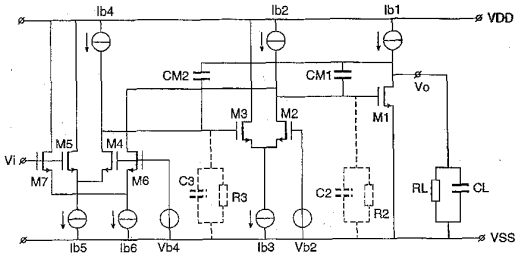

Fig. 29. Basic topology of a three stage amplifier with multipath nested Miller compensation.

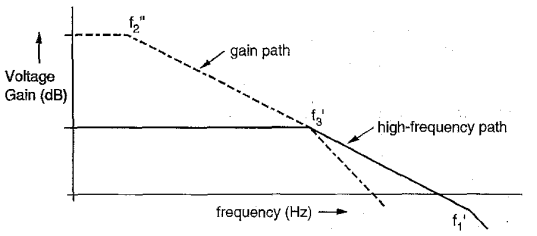

Fig. 30. Bode plot of a three stage amplifier with multipath nested Miller compensation.

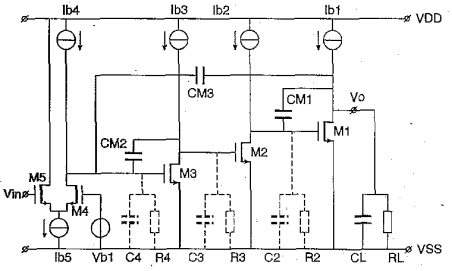

Fig. 31. Basic topology of a four-stage amplifier.

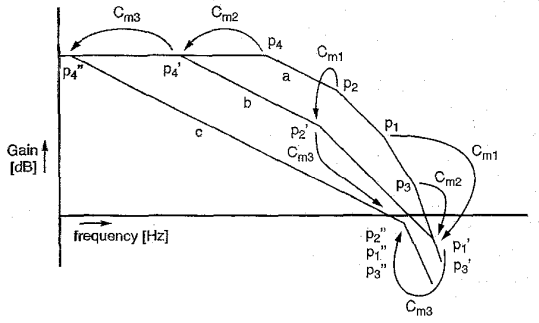

Fig. 32. Bode plot of a four-stage amplifier with hybrid nested Miller compensation.

the finite drain-source impedances, is automatically compensated.

The minimum supply voltage of this amplifier is limited by the R-R input stage and the feedforward class-AB control. It requires at least two stacked gate-source voltages and two saturation voltages. Thus, a supply voltage of about 1.8 V is required, depending on technology.

Fig. 26 shows a second example of a two-stage amplifier. It contains an N-channel input stage, M_{11}–M_{14}, which is able to sense common-mode voltages around the positive supply rail. It also contains a folded cascoded summing circuit, M_{15}–M_{18}, and an output stage with class-AB feedback control, M_1–M_{10}. Again, Miller compensation is applied to compensate the amplifier. It is implemented by means of the capacitors, C_{M1} and C_{M2}.

The minimum supply voltage of this amplifier is limited by the class-AB feedback amplifier. It requires at least two saturation voltages on top of one gate-source voltage. Thus the supply voltage of this amplifier can be considerable lower than that of the previous one. It should be noted that, if this amplifier were equipped with a R-R input stage, it would require the same minimum supply voltage as the amplifier shown in Fig. 25.

VI. Three-Stage Operational Amplifiers

The gain of a two-stage amplifier can be further increased by placing an additional gain stage between the input and the output stage. This intermediate stage is often used to reduce noise and offset contributions by the output stage.

The basic topology of a three-stage operational amplifier is shown in Fig. 27. It contains an input stage, M_4–M_5, an intermediate stage, M_2–M_3, and an output stage, M_1. Each stage introduces a dominant pole at its output. A simple and robust method to compensate this amplifier is the nested Miller compensation technique [2], [14]. Fig. 28 explains the principles of this compensation technique. The output and intermediate stage can be conceived as a two-stage amplifier with two dominant poles, f_1 and f_2. The capacitor C_{M1} closes the first Miller loop which splits f_1 and f_2 to f_1' and f_2', respectively. The pole f_1' is 3 dB below the unity-gain frequency. Therefore, the intermediate and output stage can now be treated as one stage with one dominant pole f_2'. The Miller splitting can now be repeated by inserting C_{M2}. This capacitor splits the poles f_3 and f_2', resulting in one dominant pole at f_2''.

To move the poles into Butterworth positions, the amplifier has to be dimensioned such that

$$B_{0,2} = \frac{g_{m3}}{C_{M1}} = \frac{1}{2} f_1' = \frac{1}{2} \frac{g_{m1}}{C_L} \tag{15}$$

$$B_{0,3} = \frac{g_{m5}}{C_{M2}} = \frac{1}{4} f_1' = \frac{1}{4} \frac{g_{m1}}{C_L} \tag{16}$$

where $B_{0,2}$ is the unity-gain frequency of the intermediate stage and the output stage when the first Miller loop is closed.

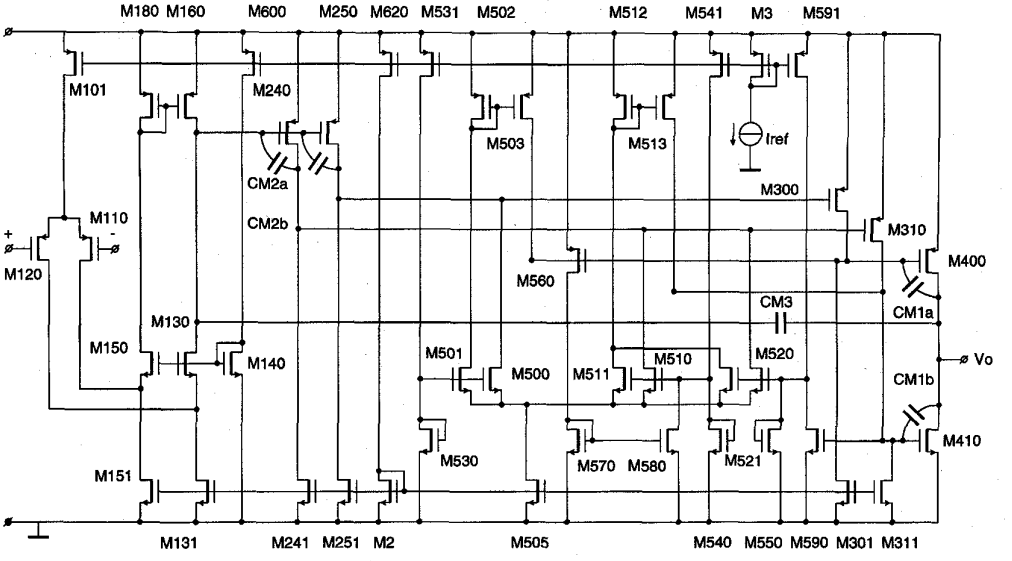

Fig. 33. A realization of a four-stage amplifier with hybrid nested Miller compensation.

$B_{0,3}$ is the unity-gain frequency of the three stage amplifier when the second Miller loop is closed.

The nesting of capacitors is relatively simple and can be repeated. A drawback is that each time a Miller capacitor is inserted, the unity-gain frequency decreases by a factor of two, as can be concluded from (15) and (16).

The loss of a factor two in the unity-gain bandwidth can be avoided by using the multipath nested Miller compensation structure, as shown in Fig. 29 [15], [16]. The circuit consists of a three stage nested Miller opamp and an additional input stage, M_6–M_7. This input stage bypasses the intermediate stage, M_2–M_3. The result is an amplifier which has the gain of three stages and a two-stage high-frequency path. Fig. 30 shows the magnitude plot of the multipath nested Miller compensation. The gain and the high-frequency path can easily be matched by making the unity-gain frequencies of both paths equal. Thus

$$\frac{g_{m7}}{C_{M1}} = \frac{g_{m5}}{C_{M2}}. \tag{17}$$

This matching of transconductance and capacitances can be very accurate.

VII. Four-Stage Operational Amplifiers

In applications where an operational amplifier has to be able to drive a large output current, the gates of the output transistors have to be able to reach the supply rail. In the two- and three-stage amplifiers discussed above, the gate swing of the output transistors was limited by either cascodes or differential pairs. Especially in a very low-voltage environment, the gate swing can be very low, which limits the drive capability of the opamp. For this reason in low-voltage amplifiers which have to deliver large output currents, cascodes, or differential pairs cannot be used to drive the output transistors. Further, in processes with very low threshold voltages, only one saturation voltage fits between the gate and the source of an output transistor. This also blocks the use of cascodes or differential pairs immediately before the output stage [17].

The amplifier topology of Fig. 31 can be used to overcome both problems [18]. It consists of three cascaded common-source amplifiers, M_1–M_3, and a differential input stage, M_4–M_5. Each stage introduces a dominant pole at its output. As can be readily seen, there is only one saturation voltage on top of the gate-source voltage of an output transistor. This maximizes the gate swing of the output transistors. Hence, the amplifier is able to drive relatively large output currents, even in a low-voltage environment. Further there is only one saturation voltage within a gate-source voltage which makes the amplifier suitable for processes with very low threshold voltages.

This amplifier cannot be compensated by using the Nested Miller compensation, because of the inverting nature of the gain stages. However, hybrid nested Miller compensation does the job [17]. Fig. 32 explains the hybrid nested Miller technique. The amplifier can be considered as two cascaded two-stage amplifiers, M_3–M_5 and M_1–M_2, each having two dominant poles. Both two-stage amplifiers can be compensated by inserting the Miller capacitors C_{M1} and C_{M2}. The result is a four-stage amplifier with two dominating poles, located at p_4' and p_2'. The remaining two poles can be split by closing the outer Miller loop. The result is a straight 20 dB roll-off up to the unity gain frequency.

The hybrid nested Miller compensation should be dimensioned such that it obeys the following expressions:

$$\frac{g_{m2}C_{M3}}{C_{M1}C_{M2}} = \frac{1}{2}\frac{g_{m1}}{C_L} \tag{18}$$

and

$$\omega_u = \frac{g_{m5}}{C_{M3}} = \frac{1}{4}\frac{g_{m1}}{C_L}. \tag{19}$$

Dimensioning the hybrid nested Miller compensation according to (19), corresponds to a maximal flat amplitude response of the amplifier with unity-gain feedback.

As follows from (19), the unity-gain frequency of the amplifier is a factor two lower than that of a two-stage amplifier. This reduction of bandwidth can be prevented by applying the multipath compensation technique to the amplifier, as explained in the previous section.

Fig. 33 shows a realization of a four-stage operational amplifier with hybrid nested Miller compensation. The amplifier consists of a P-channel differential input pair, M_{110} and M_{120}, followed by folded cascodes, M_{130} and M_{150}, allowing sensing of common-mode voltages near the negative supply rail. The current mirror, M_{160} and M_{180}, provides the differential to single-ended conversion. M_{240}–M_{250}, M_{300}–M_{310} and M_{400}–M_{410} are the common-source amplifiers. The hybrid nested Miller compensation is inserted according to the principle shown in Fig. 31. The quiescent current in the output transistors is controlled by the class-AB feedback control, M_{500}–M_{591}. This class-AB control works similar to the circuit described in Section III [17]. The minimum supply voltage is limited by the stacking of a gate-source voltage and a saturation voltage and can be as low as 0.9 V.

VIII. Conclusion

The fundamental limits in analog circuit design are affected by the trend in VLSI circuits toward higher element densities. To make efficient use of the supply current and the supply voltage, power efficient class-AB output stages and efficient overall topologies for bandwidth and gain are very important. Bandwidth and gain in relation to power consumption have been discussed for single-stage amplifiers up to amplifiers consisting of four stages. Several circuit examples with a single-stage topology, a two-stage Miller topology, a three-stage nested Miller topology, and a four-stage hybrid nested Miller topology have been discussed.

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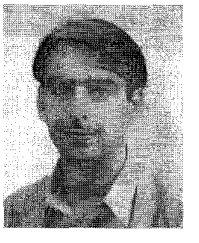

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