Low power pipelined FFT processor architecture on FPGA

ABSTRACT

Fast Fourier Transform (FFT) processor is the hardware implementation for FFT algorithms for Discrete Fourier Transform (DFT) which compute any signal in time domain to frequency domain. This processor plays an important role in many applications such as digital video broadcasting, wireless sensor network and many more digital signal processing applications, which requires a small area and low power processor. Pipelined FFT processor design on FPGA will speed up the design process and flexibility. This paper provides a survey of three types of pipelined FFT architecture, radix-8, radix-4 single path feedback (R4SDF) and radix-4 single-pasth delay commutator implemented on FPGA. The simulation part is done via Modelsim and verification through Matlab. While the implementation is done via Quartus on the Altera Cyclone IV FPGA board. The performance of these FFT processor is studied. The result shows that radix-8 pipelined FFT have higher power dissipation compared to R4SDF and R4SDC, however R4SDC design has low area design compared to the rest. Overall, all pipelined FFT processor designs are functioning accordingly.

Keyword: FFT; FPGA; Pipelined; Power; Radix-4; Radix-8