# Low-Power Programmable Gain CMOS Distributed LNA

Frank Zhang, *Student Member, IEEE*, and Peter R. Kinget, *Senior Member, IEEE*

***Abstract*—A design methodology for low power MOS distributed amplifiers (DAs) is presented. The bias point of the MOS devices is optimized so that the DA can be used as a low-noise amplifier (LNA) in broadband applications. A prototype 9-mW LNA with programmable gain was implemented in a 0.18-$\mu$m CMOS process. The LNA provides a flat gain, $S_{21}$, of 8 $\pm$ 0.6 dB from DC to 6.2 GHz, with an input impedance match, $S_{11}$, of $-16$ dB and an output impedance match, $S_{22}$, of $-10$ dB over the entire band. The 3-dB bandwidth of the distributed amplifier is 7 GHz, the IIP3 is $+3$ dBm, and the noise figure ranges from 4.2 to 6.2 dB. The gain is programmable from $-10$ dB to $+8$ dB while gain flatness and matching are maintained.**

***Index Terms*—Distributed, low-noise amplifier (LNA), low power, ultrawideband (UWB), variable gain.**

## I. Introduction

A BROADBAND low-noise amplifier (LNA) is a critical component of the ultra-wideband (UWB) receiver [1] and cognitive radio [2]. Recent publications have reported ways to obtain flat gain for UWB through resistive feedback [3] and filter-match techniques [4], [5]. This paper investigates the use of distributed amplifiers in the context of UWB applications [6] and introduces a design methodology geared toward low power operation.

The main advantages of a distributed amplifier (DA) are its intrinsic broadband frequency response that goes all the way down to DC, and good input and output impedance matching. But so far, high power consumption and large area have limited its application space. However, when one considers the tradeoff between the five main design parameters of an LNA: power drain, gain, bandwidth, noise, and linearity, it becomes evident that the traditional way of biasing a MOS DA in strong inversion, is not the best choice for reducing power consumption and optimizing the overall performance.

In this paper we discuss the design of a very low power three-stage MOS DA biased in moderate inversion (M.I.). We compare integrated broadband amplifier architectures in Section II and conclude that DAs are a valid option for LNA design. In Section III, we discuss the tradeoffs in DA designs and introduce a design methodology aimed for low power consumption while maintaining gain, noise, and distortion performance. Using this design methodology, a three-stage MOS DA is designed in Section IV. The measured results of the DA is summarized in Section V and its performance is compared with other broadband amplifier circuits in Section VI.

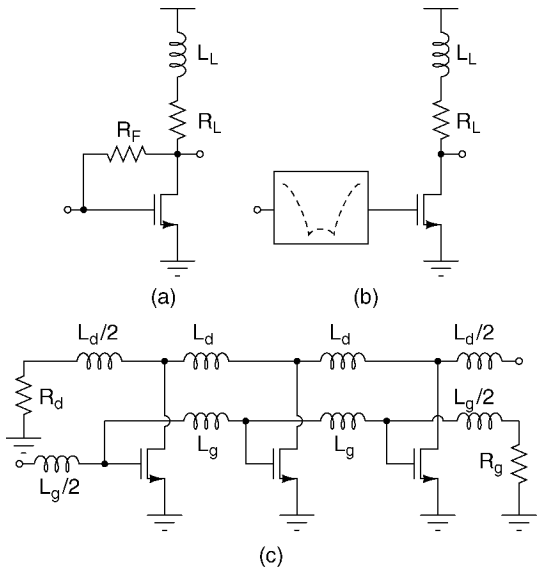


Fig. 1. Comparison of broadband amplifier architectures. (a) Resistive shunt feedback. (b) Input filter matching network. (c) Distributed amplifier.

## II. Broadband Amplifier Comparison

For an amplifier to be considered broadband, it must satisfy at least two simultaneous criteria [7]: good input matching to a standard impedance (typically 50 $\Omega$), and flat gain across a wide bandwidth. Broadband input matching is difficult for common-source/emitter-type amplifiers due to the capacitive nature of the transistor input. The matching requirement sets an upper limit on the size of this capacitance and thus the size of the transistor. This locks the amplifier gain and current consumption in a direct tradeoff.

The amplifier architecture, shown in Fig. 1(a), employs shunt-shunt feedback around a common-source stage to achieve a broadband matching and a low noise figure. However, the shunt feedback architecture is bounded by the input capacitance, and therefore it is difficult to achieve a very broad bandwidth. For example in [3], an external inductor was required to achieve broader input matching. The filter-match architecture [4], [5], shown in Fig. 1(b), integrates the capacitive input of a narrowband amplifier into an on-chip bandpass filter to achieve broadband input match. As a result, the size of the transistor is no longer coupled to the impedance matching requirement. This

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The authors are with the Department of Electrical Engineering, Columbia, University, New York, NY 10027 USA (e-mail: kinget@ee.columbia.edu).

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architecture works well with UWB's 3–10 GHz specification since gain and impedance matching at low frequencies is not required. A SiGe bipolar example of this amplifier is found in [5] with high gain and low noise figure; its CMOS counterpart [4] consumes less power, but has less gain and higher noise figure.

This paper investigates the distributed amplifier (DA) as an alternative to the architectures mentioned above. In a distributed amplifier, shown in Fig. 1(c), the input and output capacitances of the transistors are combined with on-chip inductors to form pseudo-transmission lines. Pseudo-transmission lines have properties similar to that of real transmission lines up to the cutoff frequency, $f_c$, of the line [7]. This provides impedance matching over a broad bandwidth as well as a broadband gain equal to the sum of the scalar gains from each stage. Theoretically, the gain of the DA can be increased indefinitely by adding more stages while maintaining the bandwidth [8]. However, passive losses in the pseudo-transmission lines and area constraints have limited the number of stages in practice.

DAs have often been dismissed in low-noise amplifier applications due to high power consumption and high noise figure. The reason most DAs have high power consumption is due to the pursuit of the highest gain-bandwidth product possible, which however does not result in the optimal overall performance when used as an LNA. In addition, it is often assumed that the noise figure of the DA is high due to the noise from the gate line termination resistor. However, as [9] demonstrated, the reverse gain of the DA shields the noise of the gate termination resistor from the output, and therefore the noise figure (NF) is not bounded by a 3-dB floor except at very low and very high frequencies.

The following sections describe a systematic design methodology for distributed amplifiers under power consumption constraint and demonstrate the performance of a low-power prototype circuit designed using this methodology.

## III. Distributed Amplifier Performance Tradeoffs

In this section, we examine the properties of the DA, including gain, bandwidth, number of stages, transistor region of operation, noise, and linearity, and identify parameters critical to the performance tradeoffs.

### A. DA Gain

In Fig. 2, two pseudo-transmission lines are formed by integrating the intrinsic gate and drain capacitances, $C_g$, and $C_d$, of the transistors with inductors $L_g$ and $L_d$, respectively.

When the amplifier is driven with a sinusoidal input signal, $V_s$, as shown in Fig. 2, the voltage at each gate node can be represented by a phasor with a magnitude of $V_{\text{in}}$, and a phase delay equal to a multiple of $\beta_g$. The phase delay, $\beta_g$, is frequency dependent and is equal to $\omega\sqrt{L_gC_g}$, where $\omega = 2\pi f$. Since the magnitude of the voltage signal at each gate node is the same, the drain current, $I$, of each transistor is also the same assuming transistors have the same size and bias. The current at the drain node of each stage splits evenly toward the drain termination resistor, $R_d$, and the output resistor, $R_{\text{out}}$. Fig. 2 shows the current from the first stage as it travels on the drain line toward the output. This current experiences a delay equal to a multiple of

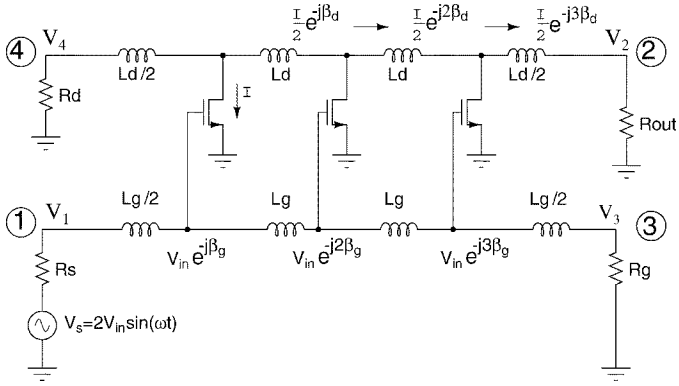


Fig. 2. Forward and reverse gain of a DA.

$\beta_d = \omega\sqrt{L_dC_d}$ as it passes through each stage, similar to the voltage on the gate line.

By setting the gate line delay and drain line delay equal ($\beta_g = \beta_d$), the currents from different stages arrive at the output resistor, $R_{\text{out}}$, in phase (constructive interference), therefore maximal gain is achieved. On the other hand, the currents flowing toward the drain termination resistor, $R_d$, arrive at $R_d$ out of phase (destructive interference), and the gain is minimum.

Fig. 2 shows the DA as a 4-port network, with gain in the forward direction (① → ②) and attenuation in the reverse direction (① → ④); port ③ is a terminated port. The forward voltage gain from port ① → ②, $G_F$, shown in (1), is valid for all frequencies [9].

$$G_F = \frac{V_2}{V_1} = \frac{g_m R_{\text{out}}}{2} \frac{\sin\left(\frac{N}{2}(\beta_d - \beta_g)\right)}{\sin\left(\frac{1}{2}(\beta_d - \beta_g)\right)} \tag{1}$$

where $N$ is the number of stages, e.g., $N = 3$ in Fig. 2, and $g_m$ is the transconductance of a single stage. Similarly, the reverse gain from port ① → ④, $G_R$, is given by

$$G_R = \frac{V_4}{V_1} = \frac{g_m R_d}{2} \frac{\sin\left(\frac{N}{2}(\beta_d + \beta_g)\right)}{\sin\left(\frac{1}{2}(\beta_d + \beta_g)\right)}. \tag{2}$$

Applying the condition for maximal forward gain by substituting $\beta_g = \beta_d$ into (1) and (2) reduces them to their simpler forms, shown in (3) and (4), respectively:

$$G_F = \frac{N g_m R_{\text{out}}}{2} \tag{3}$$

$$G_R = \frac{g_m R_d}{2} \frac{\sin(N\beta_g)}{\sin(\beta_g)}. \tag{4}$$

The reverse gain, $G_R$, is a function of frequency, and has a bandstop response.

Fig. 3 shows the ratio, $G_R/G_F$, for different number of stages, assuming $\beta_d = \beta_g$. This ratio is plotted against frequency, $f$, instead of phase delay, $\beta$, to illustrate the effect of reverse gain on the frequency response of the DA. $f$ and $\beta$ are related by $f = \beta/(2\pi\sqrt{LC})$. As expected, at DC, the forward gain and reverse gain are the same since the drain current splits evenly toward the drain termination resistor and the output.

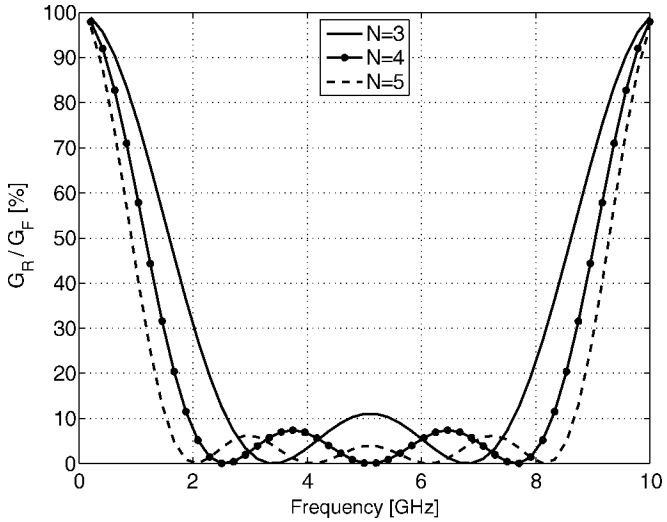


Fig. 3. Reverse gain compared to forward gain.

However, within the amplifier midband, the reverse gain is very small due to the destructive interference of the drain currents at the drain termination resistor, $R_d$.

By using the appropriate value of $g_m$, the expressions for gain in (1) and (2) are valid for MOS transistors biased from weak inversion (W.I.) to strong inversion (S.I.).

### B. DA Bandwidth

As discussed earlier, a broadband amplifier's bandwidth is essentially limited by its input matching requirement. In the case of the DA, input impedance matching is achieved by designing the characteristic impedance of the gate line, $R = \sqrt{L_g/C_g}$, equal to the source impedance, $R_s$, usually 50 Ω. To avoid unwanted reflection from the gate line, the gate-termination resistor, $R_g$ is also set equal to the gate characteristic impedance, $R$. If output impedance matching to 50 Ω is also required, then the characteristic impedance of the drain line, $\sqrt{L_d/C_d}$, and drain termination resistor, $R_d$, are set to 50 Ω as well. This simple way of achieving broadband impedance matching is a direct benefit of the intrinsic broadband nature of the pseudo-transmission lines. However, deviation from ideal transmission line characteristics at frequencies approaching that of the cutoff frequency, $f_c$, of the pseudo-transmission line eventually limits the DA bandwidth. The cutoff frequency, $f_c$ of the gate line is defined as

$$f_c = \frac{1}{\pi\sqrt{L_g C_g}} = \frac{1}{\pi R C_g}. \tag{5}$$

The impedance matching property of the gate or drain line degrades as the cutoff frequency is approached. As a rule of thumb, impedance matching better than −10 dB cannot be achieved for frequencies above ∼86% of $f_c$ [10]. The cutoff frequency is rewritten in (5) so that $C_g$ is the only variable. It is evident that for pseudo-transmission lines to obtain a given bandwidth for a given characteristic impedance, $R$, there is an upper limit on the size of the capacitance $C_g$.

TABLE I
EFFECT OF MOS BIAS TRADEOFFS ON DISTRIBUTED LNA PERFORMANCE FOR A FIXED CURRENT

| MOS Bias Trade-offs | | | | | Distr. LNA Performance | | | |
|---|---|---|---|---|---|---|---|---|
| W/L | Op. | $V_{GS}-V_T$ | $\frac{g_m}{I}$ | $f_T$ | G | IIP3 | NF | BW |
| ⇑ | W.I. | ⇓ | ⇑ | ⇓ | ⇑ | ⇔ | ⇓ | ⇓ |
| ⇓ | S.I. | ⇑ | ⇓ | ⇑ | ⇓ | ⇑ | ⇑ | ⇑ |
| Desired | | | | | ⇑ | ⇑ | ⇓ | ⇑ |

Many distributed amplifier designs use a maximal gain-bandwidth product (GBW) as the design target:

$$\text{GBW} = G_F f_c = \frac{N g_m}{2\pi C_g} = N f_T \tag{6}$$

where $f_T$ is the unity gain frequency of the transistor, and we have assumed $R_{\text{out}} = R_s = R$. The upper bound of GBW is proportional to $N$ and $f_T$, and we will analyze these two parameters next.

### C. Number of Stages N

$N$ cannot be made very large since it is limited by the attenuation caused by losses in the on-chip inductors. In Fig. 2, we assumed that the magnitude of the voltages at each gate node is the same. However, the series resistance of a real inductor attenuates the voltage signal as it travels toward the gate termination resistor, $R_g$. As a result, later stages contribute less gain compared to earlier stages and the signal on the drain line is attenuated. It can be shown that there is a maximal $N$ for a given amount of attenuation from the inductors, after which any gain from an additional stage is offset by the losses in the on-chip inductors [7]. In technologies such as GaAs where high Q inductors are available, the number of stages can be five or more. In standard CMOS technologies, the losses in inductors are much higher, and the number of stages is rarely made more than four.

Although there is very little flexibility in selecting $N$ in a CMOS DA design, the other parameter in the GBW equation, $f_T$, is bias dependent and can be varied by the designer (the maximum $f_T$ is process-dependent and is fixed for a given technology). We examine the biasing options for a MOS transistor next.

### D. Choice of Transistor Operation Regions

A MOS device can be biased in different regions of operation distinguished by the degree of inversion in the channel [11]. With the current consumption fixed, the $g_m$ efficiency $(g_m/I)$, overdrive $(V_{GS} - V_T)$, aspect ratio $(W/L)$, and unit-gain frequency $(f_T)$ are tightly coupled [12]. Table I summarizes the tradeoffs in MOS biasing for a fixed current. If we choose to bias the MOS device toward W.I., then the overdrive needs to be reduced, the aspect ratio needs to be increased, and doing so reduces the unit-gain frequency but increases the $g_m$ efficiency, $g_m/I$.

On the contrary, if we want to achieve high $f_T$ for a fixed current, the device needs to be biased in strong inversion. Most DA designers have chosen this design approach to achieve the maximal GBW.

A maximal GBW has its limitations as an LNA design target. Current consumption, linearity, and noise are all critical for an LNA, but are not reflected in GBW. Therefore, we now analyze a DA's overall performance including linearity and noise under a fixed current consumption constraint.

### E. DA Power Consumption

The total power consumption of the DA is

$$P_{\rm dc} = NIV_{\rm dd} = I_{\rm total}V_{\rm dd} \tag{7}$$

where $I$ is the current through one stage and $I_{\rm total}$ is the total current for the DA, and $V_{\rm dd}$ is the supply voltage. We will use this expression in the overall performance evaluation later.

### F. DA Noise

The noise characteristic of MESFET DAs has been analyzed in [9] and the analysis can be adapted for MOSFET DAs as well. In order to understand the contribution of noise from various noise sources, the different gain paths in a DA have to be revisited. It is evident from Fig. 2 that port ① and port ③ are symmetrical. In other words, just as $G_R$ attenuates the signal going to the drain termination (port ④), the thermal noise from the gate termination resistor going to the output (port ②) is attenuated by $G_R$. Due to the "sinc" shape of this attenuation factor, the gate termination resistor noise appears at the output only at very low and very high frequencies but not in the midband frequency.

Another source of noise is the drain termination resistor, but since the noise does not go through the gain stages, its contribution to the total output noise is small. Within the amplifier midband, noise contribution comes mainly from the transistors.

Since gate-induced noise becomes prominent only at higher frequencies [9], we can approximate the noise factor, $F$, in the passband by considering only the drain current noise. The expression for $F$ [9], adapted for MOSFET DA, is shown below and the detailed derivations can be found in Appendix I:

$$F - 1 \approx \frac{4\gamma}{NRg_m} \tag{8}$$

where $\gamma$ is a drain noise modeling constant [13] equal to approximately 1/2 in W.I. and 2/3 in S.I.. The important observation is that noise factor reduces for larger $g_m$ and larger number of stages, $N$.

### G. DA Linearity

Broadband low-noise amplifiers are more prone to intermodulation distortion since large interferers are often in-band and are not attenuated by a band-selection filter as in the case of narrowband amplifiers. Therefore, we examine the IIP3 of a DA as a measure of its linearity in this section. In a DA, assuming the two-tone input signal frequencies are close, then the third-order intermodulation distortion products from individual stages propagate to the output approximately in phase and are summed just as the output signal currents. As a result, the ratio of distortion products to signal for one stage of the DA can be used as the worst-case estimate of the total distortion to signal ratio of the DA. The linearity of a DA is analyzed in a similar fashion as the noise, and the detailed derivations can be found in Appendix II. To the first order, the IIP3 of a MOS DA is

$$\text{IIP3} \approx \begin{cases} \frac{(2n\phi_t)^2}{R} & \text{(W.I.)} \\ \frac{4(V_{GS}-V_T)}{3\alpha R} & \text{(S.I.)} \end{cases} \tag{9}$$

where $n$ is the subthreshold slope [14], and $\phi_t$ is $kT/q$. In the S.I. formula, $\alpha$ is a parameter for modeling mobility degradation and has the unit of $[V^{-1}]$ [14]. From (9), it is evident that IIP3 is constant in W.I., and is directly proportional to the overdrive $V_{GS} - V_T$ in S.I..

From (3), (7)–(9) we observe that the overall LNA performance is dependent on the following common parameters: $g_m/I$, $V_{GS} - V_T$, and $N$. We investigate the role of these parameters in the performance tradeoffs next.

### H. DA Performance Tradeoffs

A good LNA has high gain (high $G$), good linearity (high IIP3), low noise (low $F$), and low power consumption (low $P_{\rm dc}$). Large bandwidth (high BW) is also desired, but as seen in (6), is restricted by the technology's maximum $f_t$. However, as technology scales and the maximum $f_t$ increases, distributed LNA performance tradeoff becomes more flexible. Therefore, we investigate techniques to improve the overall performance of the LNA assuming extra bandwidth is available. We used the following unit-less figure-of-merit (FOM) to gauge the total performance of the LNA:

$$\text{FOM} = \frac{G \cdot \text{IIP3}}{(F-1)P_{\rm dc}}. \tag{10}$$

Substituting the corresponding equations from the previous sections, the FOM of the DA in W.I. and S.I. is

$$\text{FOM} \approx \begin{cases} I_{\rm total}\frac{R}{2\gamma V_{\rm dd}} & \text{(W.I.)} \\ I_{\rm total}\left(\frac{g_m}{I}\right)\frac{R}{3\alpha\gamma V_{\rm dd}} & \text{(S.I.).} \end{cases} \tag{11}$$

where the substitutions $g_m/I = 1/(n\phi_t)$ and $g_m/I = 2/(V_{GS} - V_T)$ are used for W.I. and S.I., respectively. A closed-form expression for the FOM in moderate inversion (M.I.), which is in between W.I. and S.I., is difficult to obtain due to the partial drift, partial diffusion behavior of the device current in that region [11]. The gain and NF characteristic of the DA moving from W.I. to S.I. is monotonic, whereas the IIP3 improves somewhat in the M.I. region [14].

Referring back to Table I, for a fixed current budget, $I_{\rm total}$, the $W/L$ of the device can be changed to move toward W.I. or S.I., and the overall performance of a DA changes accordingly. From (11), the FOM in S.I. is improved by increasing the $g_m/I$, which corresponds to reducing the overdrive, $V_{GS}-V_T$, and increasing the $W/L$; this moves the bias point toward W.I. operation. The FOM in W.I. is constant, and can not be improved further, so

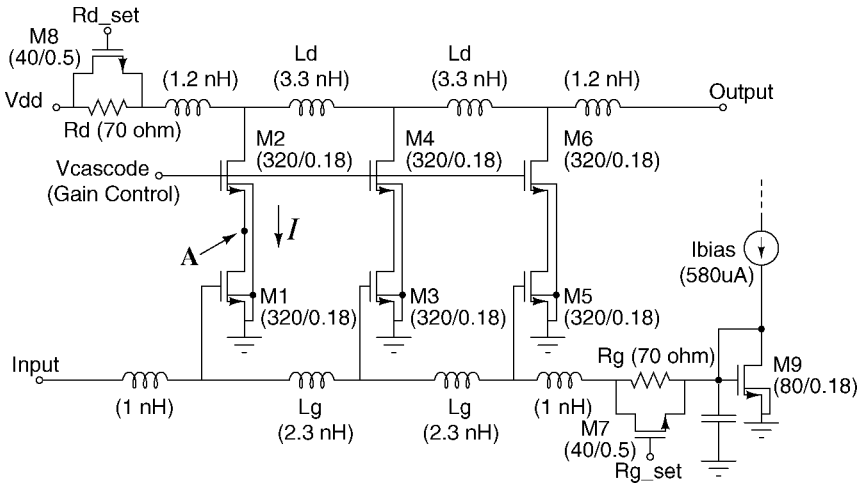


Fig. 4. Schematic of the three-stage distributed amplifier.

to obtain a good tradeoff between the different DA performance parameters we need to bias the transistors as close to W.I. as possible. However, operation toward W.I. requires a large $W/L$ which implies a lower $f_T$ and thus larger $C_g$ for a given $g_m$. The desired set of amplifier specifications for gain, noise, distortion, and most importantly, bandwidth, in combination with the technology performance will determine how close this optimized biasing can be achieved. We will describe our prototype circuit next as an example of this design methodology.

## IV. Prototype Circuit Design

To enable a good comparison with other CMOS UWB LNA designs, we set a total power consumption of 9 mW and a maximal area of 1.2 mm$^2$ as the design target, as in [4]. The area constraint sets the maximum number of stages for the DA to 3. The goal of the prototype circuit is to achieve a bandwidth of at least 7 GHz in 0.18-$\mu$m CMOS. The detailed schematic of the three-stage programmable gain DA is shown in Fig. 4.

The design procedure for the three-stage DA is as follows. First, the cutoff frequency of the gate line is calculated from the required bandwidth of 7 GHz: $f_c \approx 8.1$ GHz. Second, the maximum gate capacitance is calculated from (3): $C_{\mathrm{gmax}} \approx 780$ fF. Next, using the minimum length, the maximum width of the transistor, M1, is determined for the worst-case process corner: $W1_{\max} \approx 410$ $\mu$m. The widths of the transistors are then selected based on the constraint set by the cascode node (discussed in the next section) and the gate-induced noise (discussed in Appendix I). Finally, the inductor values are determined from $C_g$, $C_d$, and the selected $R$ ($R = \sqrt{L/C}$), which is 50 $\Omega$ for both the gate and drain lines. The "half-inductors," $L_g/2$ and $L_d/2$ are used to provide the correct input and output impedance matching.[1] Similar to the impedance of real transmission lines, the impedance of the pseudo-transmission line varies along its length, but is equal to its characteristic impedance, $R$, at the image points [7]. The "half-inductor" extends the pseudo-transmission lines to their image points where they are matched to the resistive source, load, or termination.

*1) Cascode Transistor Sizing:* A cascode structure is necessary to improve reverse isolation and at the same time eliminate the Miller multiplication of $C_{gd}$ of the input devices, M1, M3, and M5, and the associated reduction in bandwidth. However, the side effect of using large width transistors and low bias current is that the cascode node, labeled "A" in Fig. 4, can now limit the frequency response of the circuit. The current signal at the drain of M1 can go into either $g_{m2}, C_{gs2}, C_{sb2}$, or into $C_{db1}$. $C_{sb2}$ and $C_{db1}$ are junction capacitances that have become significant due to the large transistors used to obtain the high $g_m$ efficiency.

Some processes offer deep-nwell nFETs with a local substrate connection, which eliminates $C_{sb2}$. However, now the capacitance associated with the large deep-nwell required to contain the large transistor shunts away the signal at the cascode node at high frequencies. Another concern is that the doping inside the deep n-well is higher than the bulk which results in higher capacitance values. Therefore, regular bulk nFET devices resulted in a better performance for our design.

The width of M2 needs to be optimized to achieve the desired frequency response. The pole at node A, $f_A$, is

$$f_A = \frac{g_{m2}}{2\pi(C_{gs2} + C_{sb2} + C_{db1})} = \frac{f_{T2}}{\left(1 + \frac{C_{sb2}}{C_{gs2}} + \frac{C_{db1}}{C_{gs2}}\right)} \quad (12)$$

where $f_{T2}$ is the unity-gain frequency of M2. The length of M2, L2, is chosen to be minimum to obtain the highest $f_{T2}$. For fixed current and minimum L2, $f_{T2}$ increases with decreasing width, W2. $C_{sb2}/C_{gs2}$ is constant, and $C_{db1}/C_{gs2}$ increases with decreasing W2. The competing requirement for W2 in the numerator and denominator of (12) implies that an optimal width for M2 exists. From simulation, the optimal value for W2 was found to be slightly less than W1; the value was close enough to W1 (320 $\mu$m) that for layout convenience, 320 $\mu$m was also used for W2.

[1]From our circuit and EM simulations, we found that the inclusion of M-derived sections [7] did not improve the input and output impedance matching significantly, therefore we did not include those sections which would have required four extra inductors and capacitors.

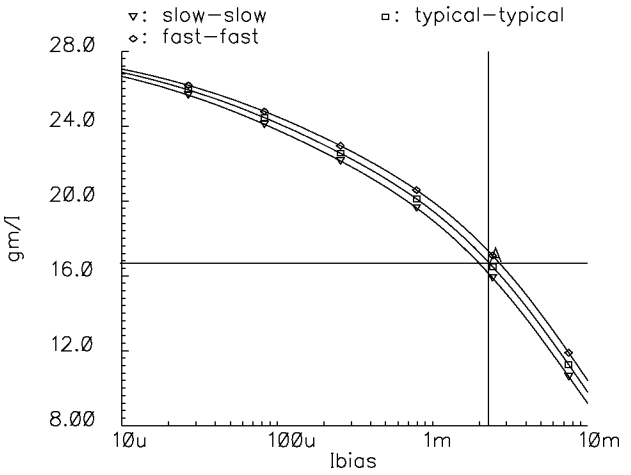


Fig. 5. Simulated $g_m/I$ versus $I$ for different process corners. The crosshair marks the bias point of the DA.

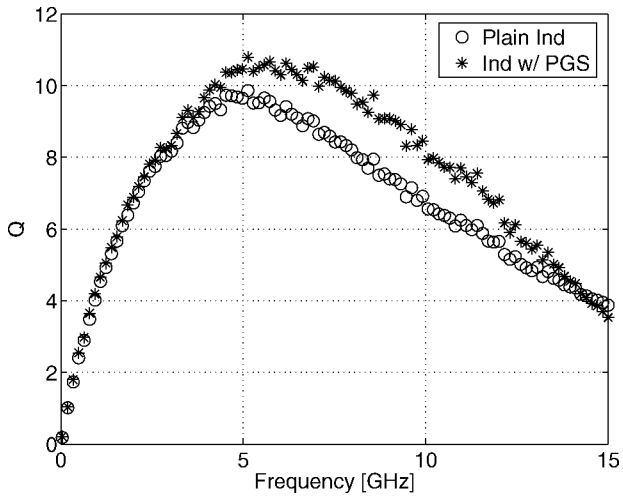


Fig. 6. Measured Q of inductor with and without patterned ground shield.

*2) DA Robustness:* The magnitude response of the DA in the passband is robust against process variation because its gate and drain lines are essentially doubly-terminated $LC$-ladders, which are known for their low sensitivity to their component values [15]. However, magnitude response's insensitivity to individual $L$'s and $C$'s (as derived in [15]) does not imply that the frequency characteristic of the DA is immune to systematic process variations. In the case of the DA, a systematic shift in capacitance[2] of the transmission lines in the same direction results in a different characteristic impedance, $\sqrt{L/C}$. However, a $\pm 20\%$ variation in capacitance, $C$, results in only $\sim \pm 10\%$ variation in the characteristic impedance, $R$. This variation is small when compared to the fact that an return loss specification of $< -15$ dB with respect to 50 $\Omega$ tolerates a much wider range of $R$ values from as low as 35 $\Omega$ to as high as 70 $\Omega$.

Variations in termination resistance due to systematic process variation becomes important when gain flatness down to DC is desired, e.g., in cognitive radio applications. However, for UWB applications, gain flatness down to DC is not required. To achieve gain flatness below 1 GHz the termination resistors need to track $\sqrt{L/C}$, and to account for the worst case where $R_g(R_d)$ and $C_g(C_d)$ skew in the same direction, adjustable termination resistors shown in Fig. 4 are used; M7 and M8 are zero-$V_T$ devices biased in triode region. The parallel combination of M7(M8) with a 70-$\Omega$ polysilicon resistor provides the flexibility to adjust the termination resistance to achieve flat gain below 1 GHz. Zero-$V_T$ devices were used instead of regular devices to obtain a wider range of resistance values for the adjustment. Zero-$V_T$ devices are part of the standard library and do not require extra masks or post-processing.

*3) DA Bias:* The biasing strategy for the three-stage DA is to maintain a stable $g_m/I$, and therefore a stable FOM in (11), over process. Current bias shown in Fig. 4 is used to ensure that the desired current flows through each stage by mirroring the current from a reference. The reference current is provided by an external current source, but can also be set by an accurate (off-chip) resistor along with a voltage reference circuit. Fig. 5 shows the small variation in $g_m/I$ versus bias current over different process corners. A $\pm 10\%$ variation in bias current results in only $\pm 2.3\%$ variation in $g_m/I$ using current bias. The simulated overdrive voltage for the input transistors of the DA is 20 mV, which places the transistors in the region of moderate inversion [11].

*4) DA Programmable Gain:* Programmable gain is a useful feature for the LNA because it can be used along with baseband circuitry in an automatic gain control (AGC) loop. The AGC prevents large input signals from saturating the receiver front-end and amplifies small signals to above the detectable level. A distributed amplifier has the important property that gain and broadband matching can be dealt with separately. When the cascode voltage, $V_{\text{cascode}}$, is reduced, M1 moves from operation in saturation toward triode, the $g_{m1}$ reduces, and the gain of the amplifier can be varied. At the same time, for a substantial range in $V_{\text{cascode}}$, the variation in the total gate capacitance remains small and therefore good impedance matching is maintained.

*5) DA Inductor Design:* The attenuation in the gate and drain pseudo-transmission lines is dominated by the resistive loss in the inductors. In CMOS process, loss in the inductors is partially due to electrical field leaking into the low resistivity substrate. A patterned ground shield (PGS) [16] under the inductor provides a low resistivity return path for the electric field therefore improves the Q of the inductor. We used polysilicon PGS with Metal-1 ground tie for the inductors in the distributed amplifier. Measured results from the inductor test structure[3] shown in Fig. 6 demonstrate the improvement in Q. The complete DA layout including all the metal interconnects was optimized using an electromagnetic simulation tool (EMX). The extracted multiport S-parameter file captures the coupling between the gate and drain pseudo-transmission lines as well as the extra parasitic capacitance from the interconnects. The stages of the DA were laid out as close as possible while keeping the coupling sufficiently small. For small-signal analysis, the extracted S-parameter file was simulated with transistor models. Figs. 7–9 illustrate the

[2]Inductance depends on layout geometry, and therefore varies little with process.

[3]Due to area constraint, the smallest inductor in the DA (1 nH) was used for the test structure.

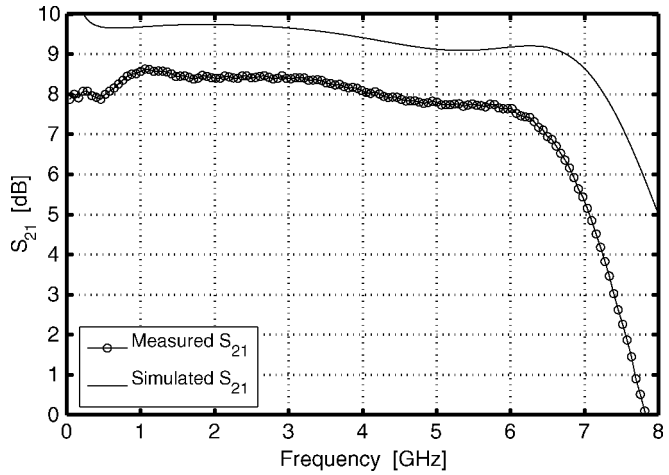


Fig. 7. Simulated (slow-slow corner) and measured $S_{21}$.

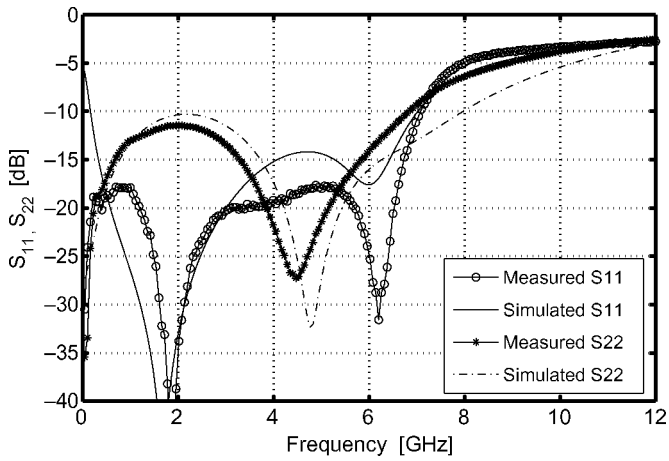


Fig. 8. Simulated (slow-slow corner) and measured $S_{11}$ and $S_{22}$.

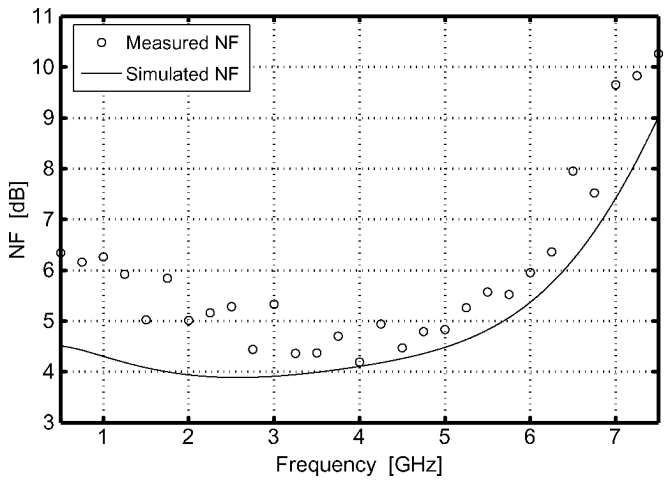


Fig. 9. Simulated (slow-slow corner) and measured noise figure.

good matching between simulated and measured results. For large-signal simulations, the equivalent lumped pi-model of the inductors was generated and simulated with transistors.

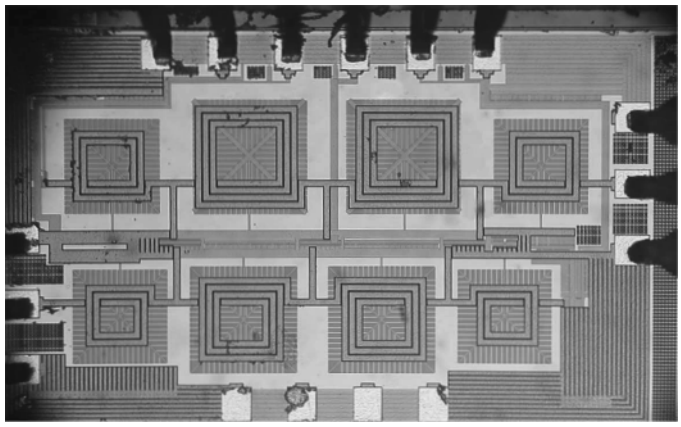

Fig. 10. Die photograph.

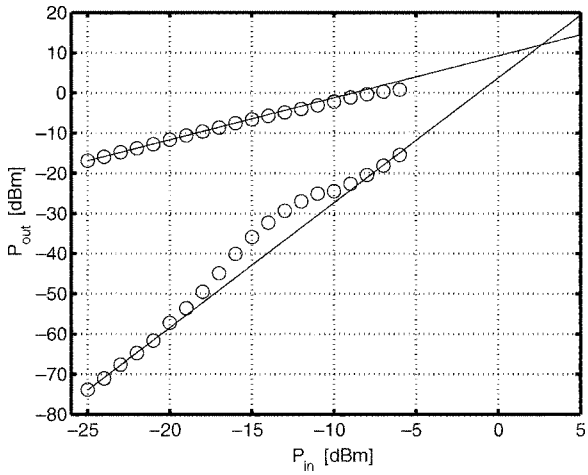


Fig. 11. Measured two-tone test at 2 GHz.

## V. Experimental Results

The three-stage DA was designed in a 0.18-$\mu$m CMOS process with a 2-$\mu$m-thick top metal. The chip occupies $1.45 \times 0.8$ mm$^2$ including pads. The die photograph is shown in Fig. 10. The DA consumes 7 mA from a 1.3-V supply. 1.3 V is the "true" supply voltage since no external RF choke or bias-T is used to bypass the drain termination resistor. This is because the voltage drop across the drain termination resistor is small thanks to low current consumption.

Ten amplifier samples were characterized on an RF probe station. The S-parameter data was measured using the Anritsu 37369C 40 GHz network analyzer; the data for different samples were very consistent and the results for a typical sample are shown in Figs. 7 and 8. Good input and output impedance match and a flat gain of $8 \pm 0.6$ dB are obtained between 40 MHz and 6.2 GHz. The lower bound of the DA bandwidth is limited by the measurement capability of the network analyzer, which is AC-coupled and has a lower limit of 40 MHz. The reverse gain, $S_{12}$, is less than $-25$ dB. The noise figure was measured using the HP8970 Noise Figure meter, and is shown in Fig. 9. As expected, noise is high at low frequencies, increases after the cutoff frequency, and is close to 5 dB in the midband. The linearity of the amplifier was verified with two-tone IIP3 and 1-dB gain compression (ICP) measurements which are reported

TABLE II
CMOS DISTRIBUTED AMPLIFIER PERFORMANCE COMPARISON

| | CMOS [$\mu$m] | Flat-Gain BW [GHz] | $S_{21}$ [dB] | $S_{11}$ [dB] | Spot NF [dB] | IIP3 [dBm] | ICP [dBm] | $P_{dc}$ [mW] | Area [mm$^2$] |
|---|---|---|---|---|---|---|---|---|---|
| This Work | 0.18 | $0.04-6.2$ | $8 \pm 0.6$ | $<$ -16 | 4.2 - 6.2 | +3 | -8.5 | 9 | 1.16 |
| [17] | 0.18 | $0.5-14$ | $10.6 \pm 0.9$ | $<$ -11 | $3.5-5.4$ | +9.4 | -0.6 | 52 | 1.60 |
| [18] | 0.18 | $0.6-22$ | $7.3 \pm 0.8$ | $<$ -8 | $4.3-6.1$ | | | 52 | 1.35 |
| [19] | 0.18 | $0.1-11$ | 8 | $<$ -12 | 2.9 | $-3.4$ | | 21.6 | 0.76 |

TABLE III
BROADBAND LNA PERFORMANCE COMPARISON

| | CMOS [$\mu$m] | 3-dB BW [GHz] | $G_{max}$ [dB] | $S_{11}$ [dB] | $NF_{min}$ [dB] | IIP3 [dBm] | ICP [dBm] | $P_{dc}$ [mW] | Area [mm$^2$] |
|---|---|---|---|---|---|---|---|---|---|
| This Work | 0.18 | $0.04-7$ | 8.6 | $<$ -16 | 4.2 | +3 | -8.5 | 9 | 1.16 |
| [4] | 0.18 | $2.3-9.2$ | 9.3 | $<$ -9.9 | 4 | -6.7 | -15 | $9+9^{\dagger}$ | 1.10 |
| [3] | 0.13 | 5.9 | 16 | $<$ -9 | 4.7 | | -24 | 38 | 0.24 |
| [5] | SiGe | $2-10$ | 21 | $<$ -10 | 2.5 | -5.5 | -11.8 | $30+45^{\ddagger}$ | 1.80 |

† 9 mW buffer stage for output match ‡ 45 mW buffer

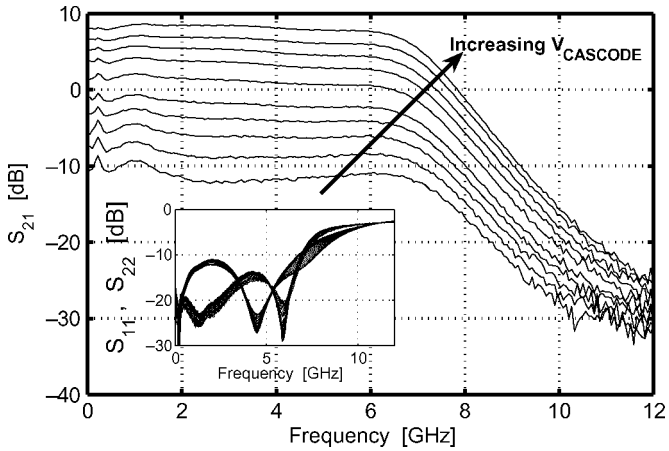


Fig. 12. Measured gain for different $V_{\rm cascode}$ voltages. Inset: measured input and output matching for different $V_{\rm cascode}$ voltages.

in Table II. The two-tone test was performed using an Agilent E4446A spectrum analyzer and two Agilent E8257D signal generators. The result is shown in Fig. 11. Fig. 12 demonstrates the programmable gain feature; gain is varied from $-10$ dB to $+8$ dB while input and output matching, and gain flatness are maintained.

## VI. DISCUSSION AND CONCLUSION

The performance of the presented amplifier is compared with other distributed amplifiers in Table II. The power consumption of the presented amplifier is significantly lower than previously published CMOS DAs, while maintaining comparable distortion, gain, and noise performance. This demonstrates that the presented design methodology is effective for lower power DA design.

Table III compares the performance of the presented amplifier with other broadband LNAs. The presented DA has a gain and noise performance comparable to the CMOS filter-match amplifier [4]. The DA's bandwidth is lower but linearity is significantly better. Both amplifiers occupy about the same area. The shunt-shunt resistive feedback amplifier in [3] has a higher gain and smaller area compared to the presented DA, but consumes much more power and has a lower linearity. The bipolar filter-match amplifier in [5] achieves a higher gain and lower noise figure at the cost of higher power consumption, lower linearity, and more expensive process.

A very low-power MOS DA design has been demonstrated. Improvement in overall DA performance is obtained through optimization of bias point in MOS devices. While this low power design approach is limited by the required bandwidth, it will become even more attractive as the $f_T$ of MOS transistors increases in scaled technologies. Thanks to the operation from DC to RF, combined with the programmable gain feature, this DA design can be used in various broadband applications including UWB and cognitive radio.

## APPENDIX I
## DA NOISE FACTOR

The noise factor, $F$, of a MESFET DA has been derived in [9], we have adapted it here for MOSFET. The derivation assumes that the source resistance, $R_s$, is matched to the gate-termination resistance, $R_g$, and the output resistance, $R_{\rm out}$, is matched to the drain termination resistance, $R_d$. In our design, all four resistances are equal to 50 $\Omega$ for optimal input and output matching and gain flatness. The main noise sources of a distributed amplifier are shown in Fig. 13, and their contribution to the total output noise is derived below.

The noise from the source resistor, $R_s$ is amplified by the forward gain, $G_F$ of the DA, therefore the output noise due to the source resistor is

$$\overline{v_{o,R_s}^2} = \left(\frac{\sqrt{4kTR_s\Delta f}}{2} g_m N \frac{1}{2} R_{\rm out}\right)^2. \qquad (13)$$

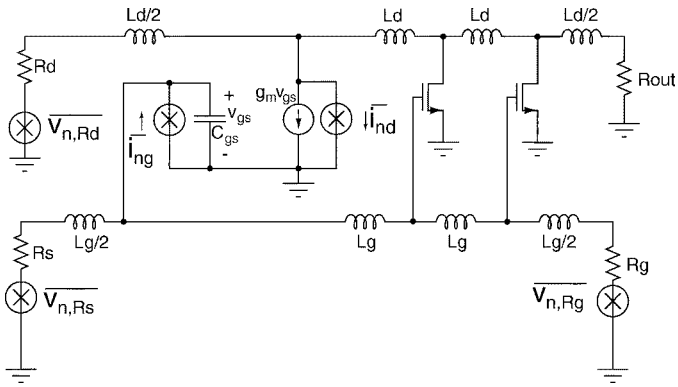


Fig. 13. DA noise sources.

The noise from the gate-termination resistor is attenuated by the reverse gain $G_R$ of the DA, therefore the output noise due to the gate termination resistor is

$$\overline{v_{o,R_g}^2} = \left(\frac{\sqrt{4kTR_g\Delta f}}{2} g_m \frac{\sin(N\beta)}{\sin\beta}\frac{1}{2}R_{\text{out}}\right)^2. \tag{14}$$

The drain termination resistor noise is split between $R_d$ and $R_{\text{out}}$, therefore the output noise due to the drain termination resistor is

$$\overline{v_{o,R_d}^2} = \left(\sqrt{4kTR_d\Delta f}\frac{1}{2}\right)^2. \tag{15}$$

The transistors have two noise sources: drain current noise $\overline{i_{nd}^2}$ and gate-induced noise $\overline{i_{ng}^2}$. These two noise sources are usually correlated with a complex correlation coefficient, $c \approx 0.395j$ [13]. The correlation coefficient is purely imaginary because the channel noise is coupled to the gate through the distributed gate capacitance. In the DA, the gate-induced current noise sees the impedance of the gate transmission line, $\sqrt{L_g/C_g}$, which is purely real,[4] therefore the correlated component of $\overline{i_{ng}^2}$ does not dissipate real power at the output [9]. As a result, we only need to consider the uncorrelated component of the gate-induced noise.

The output noise due to the drain current noise is

$$\overline{v_{o,i_{nd}}^2} = N\left(\frac{1}{2}\sqrt{\overline{i_{nd}^2}}R_{\text{out}}\right)^2 \tag{16}$$

where $\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f$, and $\gamma$ is approximately equal to 1/2 in W.I. and 2/3 in S.I.. When the transistor is biased in saturation, $g_{d0}$ can be replaced by $g_m$. Note that the total $\overline{v_{o,i_{nd}}^2}$ is a superposition of the effect of individual drain current noise sources which are uncorrelated with each other.

The expression for the gate-induced noise's contribution to the output is complicated since each gate-induced noise current source is amplified by the $G_F$ of the succeeding stages as well as attenuated by $G_R$ of the preceding stages. The output noise due to the gate-induced current noise is [9]

$$\overline{v_{o,i_{ng}}^2} = \left(\frac{g_m}{2}\sqrt{\overline{i_{ng}^2}\sum_{k=1}^{N} f(k,\beta)}\frac{R_s}{2}R_{\text{out}}\right)^2 \tag{17}$$

where $\overline{i_{ng}^2} = 4kT\delta\omega^2 C_{gs}^2/(5g_{d0})\Delta f$, and $\delta$ is a constant equal to approximately 4/3 in S.I.. The function, $f(k,\beta)$, is given by [9]

$$\begin{aligned} f(k,\beta) &= (N-k+1)^2 + \left(\frac{\sin(k-1)\beta}{\sin\beta}\right)^2 \\ &\quad + \frac{2(N-k+1)\sin((k-1)\beta)\cos(k\beta)}{\sin\beta} \\ &\approx N-K+1, \quad (\text{for large } N) \end{aligned} \tag{18}$$

where $k$ is the contribution from the $k$th stage of the DA, and $\beta = \beta_g = \beta_d$ under the condition of maximum gain. The summation term in (17), $\sum f(k,\beta)$, can be approximated by $N^3/3$ for large $N$ [9], and (17) is simplified to

$$\overline{v_{o,i_{ng}}^2} = \left(\frac{g_m}{2}\sqrt{\frac{\overline{i_{ng}^2}N^3}{2}}\frac{R_s}{2}R_{\text{out}}\right)^2. \tag{19}$$

Combining (13)–(19), the noise factor $F$ of the DA is therefore

$$F = \frac{\overline{v_{o,R_s}^2} + \overline{v_{o,R_g}^2} + \overline{v_{o,R_d}^2} + \overline{v_{o,i_{nd}}^2} + \overline{v_{o,i_{ng}}^2}}{\overline{v_{o,R_s}^2}} \tag{20}$$

$$\begin{aligned} F &= 1 + \left(\frac{\sin(N\beta)}{N\sin\beta}\right)^2 + \left(\frac{2}{Ng_mR_{\text{out}}}\right)^2 \\ &\quad + \frac{4\gamma}{Ng_mR_s} + \frac{\delta\omega^2C_{gs}^2N}{15g_m}. \end{aligned} \tag{21}$$

In the midband of the DA, only the last two terms of (21) are critical; they represent the drain current noise and the gate-induced noise, respectively. The gate-induced noise increases with frequency while the drain current noise is constant. The frequency corner at which the two noise sources are equal is of interest to the designer [9]. The gate-induced noise is directly proportional to the width of the transistor, designer can size the transistor so that this corner frequency is near or above the cutoff frequency of the pseudo-transmission lines. Equating the last two terms of the noise factor (drain current noise and gate-induced noise), we obtain the corner frequency, $f_{\text{corner}}$:

$$f_{\text{corner}} \approx \frac{1}{2\pi}\sqrt{\frac{60\gamma}{\delta}}\frac{1}{NRC_{gs1}}. \tag{22}$$

In order to identify the dominating noise source in the DA, (21) is plotted against frequency, shown in Fig. 14. The intersection circled and labeled A represents the contribution of the gate-termination noise, $F_{n,Rg}$ at low frequency compared to the

[4]The impedance of the pseudo-transmission is purely real only when ideal inductors and capacitors are used, therefore this is only an approximation.

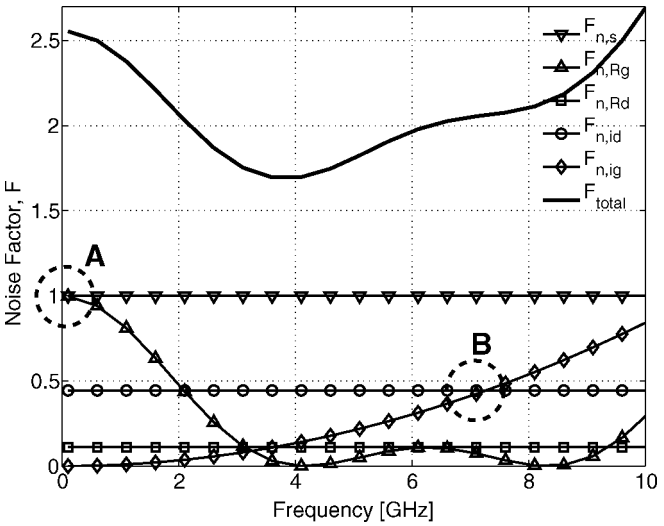


Fig. 14. DA noise factor contribution breakdown. Parameter values used in the simulation: $g_m = 40$ mS, $R = 50\ \Omega$, $C_{gs} = 800$ fF, $N = 3$, $\gamma = 2/3$, $\delta = 4/3$.

contribution of the source noise, $F_{n,s}$. As expected, the noise factor is "1" for both noise sources, resulting in the theoretical minimum F of 2 (3 dB NF). In the DA passband, the gate termination noise is attenuated by the reverse gain, $G_R$, which has its characteristic two notches (number of notches is equal to N minus 1). The intersection circled and labeled B represents $f_{\rm corner}$, the frequency at which the noise contribution from the drain current noise and the gate-induced noise are equal. From Fig. 14, it is evident that the dominant noise source in the DA passband is the drain current noise, and therefore the noise factor can be approximated by

$$F \approx 1 + \frac{4\gamma}{NRg_m}. \tag{23}$$

## Appendix II
## DA Linearity

To analyze the third-order intermodulation distortion of the DA, we assume the input signal, $V_s$, in Fig. 2 is consisted of two pure tones separated by a narrow frequency. The voltage at each gate node is a delayed version of the input. The total current into the output load is the sum of the drain currents, each delayed by the drain pseudo-transmission line. Since the two input tones are close in frequency, the phase shift in the intermodulation components is the same as the phase shift in the signals. Therefore, the intermodulation components add constructively at the output load, just as the signals do. This implies that the ratio of intermodulation distortion to signal for the DA is the same as that of a single stage. Assuming all the distortion comes from the MOS device, we can analyze the linearity of a DA by analyzing the linearity of the input transistor of a single stage.

Using the following expression for drain current $I_{ds}$ [14]:

$$I_{ds} = B\frac{X^2}{(1+\alpha X)} \tag{24}$$

where $B$ is

$$B = \frac{\mu_0 C_{ox}}{2n}\frac{W}{L}(1+\lambda V_{ds}) \tag{25}$$

and $X$ is

$$X = 2n\phi_t \ln\left\{1+\exp\left((V_{gs}-V_T)/(2n\phi_t)\right)\right\}. \tag{26}$$

In (24), $\alpha$ is the second-order effect of mobility degradation and has the unit of $[V^{-1}]$ [14]. In (26), $n$ is the subthreshold slope, $\phi_t$ is $kT/q$. $V_{gs}$, the total gate-source voltage, is the sum of its DC component, $V_{GS}$, and its small-signal component, $v_{gs}$.

In S.I., $X$ is reduced to $V_{gs}-V_T$, therefore,

$$I_{ds} = \frac{B}{1+\alpha(V_{GS}-V_T)} \cdot\left\{\frac{(V_{GS}-V_T)^2+2(V_{GS}-V_T)v_{gs}+v_{gs}^2}{1+\frac{\alpha v_{gs}}{1+\alpha(V_{GS}-V_T)}}\right\} \tag{27}$$

Using Taylor expansion, we find the fundamental and third harmonic coefficients, $C1$ and $C3$:

$$C1 = \frac{B}{1+\alpha(V_{GS}-V_T)} \cdot\left\{2(V_{GS}-V_T)-\frac{\alpha(V_{GS}-V_T)^2}{1+\alpha(V_{GS}-V_T)}\right\} \tag{28}$$

$$C3 = \frac{-B}{1+\alpha(V_{GS}-V_T)}\left\{\frac{\alpha}{1+\alpha(V_{GS}-V_T)}\right\}. \tag{29}$$

Using the following equation for IIP3 [13]:

$$\mathrm{IIP3} = \frac{2}{3}\left|\frac{C1}{C3}\right|\frac{1}{R} \tag{30}$$

where $R$ is the system impedance, 50 $\Omega$, we find IIP3 in strong inversion:

$$\mathrm{IIP3} = \frac{2}{3}\left\{\frac{2}{\alpha}(V_{GS}-V_T)+(V_{GS}-V_T)^2\right\}\frac{1}{R}. \tag{31}$$

In W.I., $X$ is reduced to $2n\phi_t\exp\{(V_{gs}-V_T)/(2n\phi_t)\}$. Again using Taylor expansion, we find $C1$ and $C3$ for W.I.:

$$C1 \approx 4Bn\phi_t\exp\left(\frac{(V_{GS}-V_T)}{n\phi_t}\right) \tag{32}$$

$$C3 \approx \frac{2}{3}\frac{B}{n\phi_t}\exp\left(\frac{(V_{GS}-V_T)}{n\phi_t}\right). \tag{33}$$

Therefore, IIP3 for W.I. is

$$\mathrm{IIP3} \approx (2n\phi_t)^2\frac{1}{R}. \tag{34}$$

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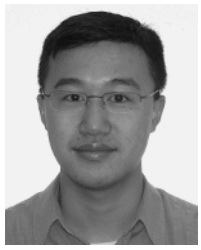

**Frank Zhang** (S'00) received the B.E. and M.S. degrees in electrical engineering from the Cooper Union for the Advancement of Science and Art, New York, NY, in 2000 and 2001, respectively. At present, he is working toward the Ph.D. degree at Columbia University, New York, NY.

From 2001 to 2003, he was an intern at Motorola's Wireless Integrated Technology Center, South Plainfield, NJ. His current research interests include analog and RF integrated circuits.

**Peter R. Kinget** (S'88–M'90–SM'02) received the engineering degree in electrical and mechanical engineering and the Ph.D. degree in electrical engineering from the Katholieke Universiteit Leuven, Belgium, in 1990 and 1996, respectively.

From 1991 to 1995, he received a graduate fellowship from the Belgian National Fund for Scientific Research (NFWO) to work as a Research Assistant at the ESAT-MICAS Laboratory of the Katholieke Universiteit Leuven. From 1996 to 1999, he was at Bell Laboratories, Lucent Technologies, Murray Hill, NJ, as a Member of Technical Staff in the Design Principles Department. From 1999 to 2002, he held various technical and management positions in IC design and development at Broadcom, CeLight, and MultiLink. In the summer of 2002, he joined the faculty of the Department of Electrical Engineering, Columbia University, New York. His research interests are in analog and RF integrated circuits and signal processing. He has published over 50 papers in journals and conferences and holds three U.S. patents with several applications under review. His research group has received funding from the National Science Foundation, the Semiconductor Research Corporation, an IBM Faculty Award, and from several grants from semiconductor companies.

Dr. Kinget has served on the Technical Program Committee of the IEEE Custom Integrated Circuits Conference (CICC) and currently serves on the Technical Program Committee of the Symposium on VLSI Circuits and the IEEE International Solid-State Circuits Conference. He has been an Associate Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS since 2003.