has one dominant pole at the output of the opamp. A folded cascode opamp has been used to ensure stability. With proper design of the loop parameters, wide frequency range of operation can be achieved.

Experimental results: To illustrate the principle, a PWLL was designed as a duty cycle adjuster for the input clock of a 10 bit, 40 MS/s pipelined analogue-to-digital converter in a 0.18μ CMOS process at 1.8 V. The power consumption is < 1 mW at 1.8 V. Fig. 4 shows the measured performance (SNRD and THD) of the ADC, both with the duty cycle adjuster turned ON and OFF at $fs = 40$ MHz and $fin = 19$ MHz. It can be seen that the SFDR and the THD remain flat as the input duty cycle is varied from 30 to 70% with the duty cycle adjuster ON. Conversely, when it is OFF, the performance drops drastically, even with 45% duty cycle. One enhancement to this design would be to use another FVC to control the coarse delay and hence a very wide operating frequency range can be achieved.

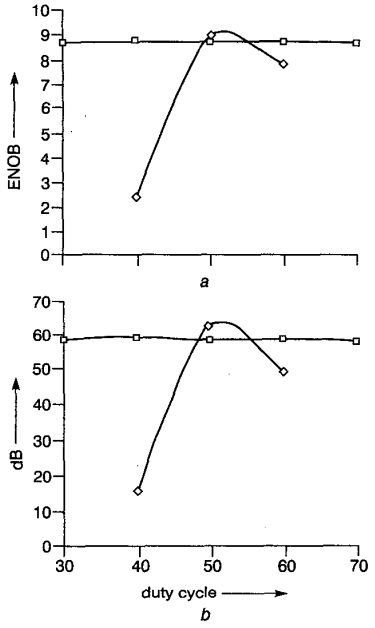

Fig. 4 *Measured data with varying input clock duty cycle*
a SNRD
b THD
—◇— DCA off
—□— DCA on

Conclusion: A novel approach based on a PWLL for the generation of a 50% duty cycle clock from an input clock with arbitrary duty cycle has been described. It can also be used to generate an output clock with duty cycles from 25 to 75%. The design has been shown to achieve this performance without affecting the jitter on one (sampling) edge of the input clock, which is very important for high-performance switched capacitor-based designs.

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Low power Schmitt trigger circuit

S.F. Al-Sarawi

Three new Schmitt trigger circuits are described. The first circuit is a truly low power, while the second and third circuits are derived from the first circuit and provide smaller hysteresis width. Measurement results for the new Schmitt trigger circuits are presented.

Introduction: In most published Schmitt trigger circuits [1–7] the aspect of low power operation is not considered, this being sometimes due to the methodology used in designing such circuits or because this aspect is irrelevant to the targeted application. Such circuits are suitable for medium power applications, but the emergence of applications which can be sustained for many years on the energy available from a small battery or from a rectified RF signal, means that truly low power circuits must be developed.

All the designed circuits are simulated using HSPICE with level 28 model parameters for a 1.2 μm standard CMOS technology.

Low power prototype CMOS Schmitt trigger circuit: The prototype lower power Schmitt trigger circuit is shown in Fig. 1*a*. The prototype circuit consists of six transistors arranged in a complementary CMOS structure. Fig. 1*b* and *c* represent two variants of the first type with less hysteresis width.

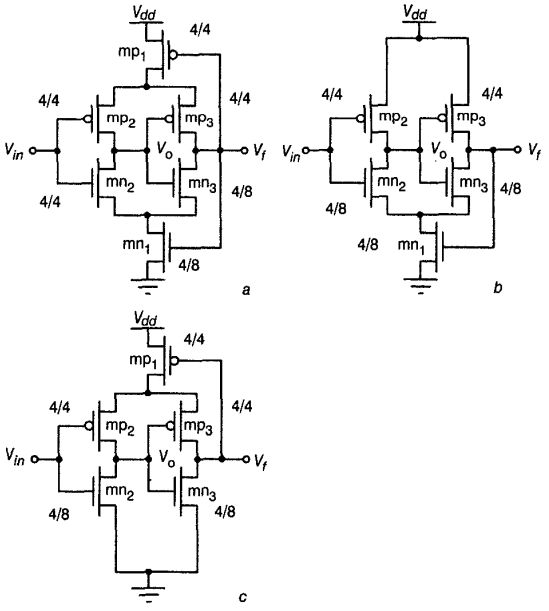

Fig. 1 *Three different Schmitt trigger circuits*
Number next to each transistor represents width to length ratio in microns
a Prototype low power circuits
b Circuit derived from *a*
c Second circuit derived from *a*

The operation of the prototype circuit can be understood as follows. When at first V_{in} is low, mn_2 is OFF, mp_2 is ON, which forces mn_3 to be ON, mp_3 OFF, and mp_1 ON.

As the input voltage rises, the input voltage V_{hl} at which the output switches from high to low then depends on the voltage at node V_n and

switching point of the inverter structure which consists of mn_2 and mp_2. The result is

$$V_{hl} = V_n + \frac{V_{dd} + V_{th}(R-1) - V_n}{R+1} \quad (1)$$

where $R = \sqrt{(\beta_{n2}/\beta_{p2})}$, β_{i_n} corresponds to the transconductance of transistor type i and number n in the schematic diagram. To simplify the analysis $V_{th} = |V_{t_n}| = |V_{t_p}|$, where V_{t_n} corresponds to the threshold voltage of a transistor n. The voltage at V_n can be found as a function of R_n and can be written as

$$V_n = \frac{V_{in}}{R_n + 1} + V_{th}\frac{(R_n - 1)}{(R_n + 1)}, \quad (2)$$

where $R_n = \sqrt{(\beta_{n1}/\beta_{n2})}$.

Substituting (2) and $V_{in} = V_{hl}$ in (1), we obtain

$$V_{hl} = V_{dd}\frac{(R_n + 1)}{R_n(R+1)+1} + V_{th}\frac{R_n(2R-1)-1}{R_n(R+1)+1} \quad (3)$$

(3) states the relation between the switching and supply voltage and the dependence of V_{hl} on the nMOS transistors geometry. From (3) it is possible to cancel the threshold voltage effect on the hysteresis by making $\beta_n = \beta_p$.

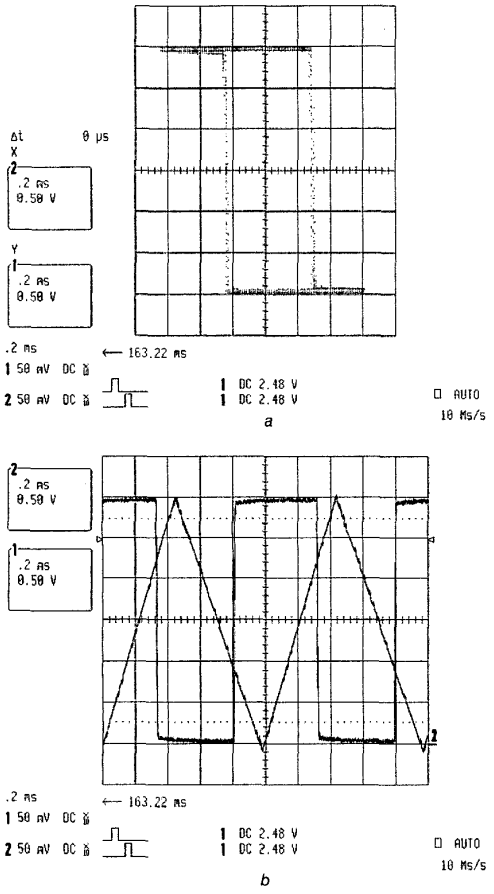

Fig. 2 *Measured characteristics of fabricated low power Schmitt trigger circuit at 3 V supply voltage and input-output characteristics against time*

a Measured characteristics
b Input-output characteristics

A similar analysis can be performed to find the switching voltage V_{lh} from low to high. The answer can, however, be obtained directly by subtracting V_{hl} from V_{dd} which is given in (4) and introducing appropriate new definitions for the R and R_n factors.

$$V_{lh} = V_{dd}\frac{R_p(R+1)}{R_p(R+1)+1} - V_{th}\frac{R_p(2R-1)-1}{R_p(R+1)+1} \quad (4)$$

The hysteresis width of the fully symmetrical, low power Schmitt trigger circuit can be calculated by subtracting (4) from (3) and letting $R_n = R_p$, resulting in

$$V_{hw} = V_{hl} - V_{lh} = V_{dd}\frac{R_n(1-R)+1}{R_n(1+R)+1} \quad (5)$$

Experimental work: The circuit shown in Fig. 1*a* was fabricated in a 2 µm double poly, double metal standard p-well process through Orbit Semiconductor. The Schmitt trigger circuit was buffered with one inverter to drive the output node.

The measured results using 3 V supply voltage are shown in Fig. 2. The designed switching points for the Schmitt trigger can be calculated using (3), (4) and (5) with $R_n = R_p = R = 1$, resulting in $V_{hl} = V_{dd}/3$, $V_{lh} = 2V_{dd}/3$ and $V_{hw} = V_{dd}/2$. The measured switching point is slightly shifted from $V_{dd}/2$ due to the difference in the ratio of the mobility of the fabricated n and p MOS transistors from the values used in the design. Although, direct measurement of the current was not possible, simulations show the short circuit current between the supply rails during switching is very small (of the order of 200 nA) using the transistor sizes shown in the schematic diagram, resulting in low fan-out. The fan-out of the Schmitt trigger circuit can be improved by buffering the output node and increasing the width of mn_2, mp_2, mn_3 and mp_3.

Conclusion: Three new Schmitt trigger circuits have been discussed, with one type having low power characteristics. Measured results verified the principle of operation and the characteristics of this low power Schmitt trigger circuit. The circuit has been used in the design of low power, very low frequency integrator oscillators.

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Efficient implementation of lifting-based discrete wavelet transform

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A recursive architecture for implementing the lifting-based discrete wavelet transform is proposed. Processing of the transform stages is interleaved, improving the hardware utilisation and efficiency.

Introduction: Factoring discrete wavelet transforms (DWT) into lifting steps can reduce the computational complexity by up to 50% [1]. Several lifting-based architectures have been proposed. Andra *et al.* [2] proposed an architecture (ACT) that uses simple functional blocks.