Low-power Sensor Interfacing and MEMS for Wireless Sensor Networks

J.A. Michaelsen, J.E. Ramstad, D.T. Wisland and O. Søråsen Nanoelectronic Systems Group, Department of Informatics, University of Oslo Norway

1. Introduction

The need for low-power and miniaturized electronics is prominent in wireless sensor network (WSN) nodes—small sensor nodes containing sensors, signal processing electronics, and a radio link. The demand for long battery life of such systems, especially if used in biomedical implants or in autonomous installations, forces the development of new circuit topologies optimized for this application area. Through a combination of efficient circuit topologies and intelligent control systems, keeping the radio idle when signal transmission is not needed, the radio link budget may be dramatically reduced. However, due to the demands for continuously monitoring of the sensor in many critical applications, the sensor front-end, analog-to-digital converter (ADC), and the control logic handling the radio up/down-link may not be turned off, and for systems with long intervals between transmissions, the energy consumed by these parts will have a large impact on battery life. In this chapter, we focus on Frequency $\Delta\Sigma$ Modulator (FDSM) based ADCs because of their suitability in WSN applications. Using FDSM based converters, both sensors with analog and frequency modulated outputs may be conveniently interfaced and converted to a digital representation with very modest energy requirements. Microelectromechanical systems (MEMS) integrated on-die with CMOS circuitry enables very compact WSN nodes. MEMS structures are used for realizing a wide range of sensors, and form vital components in radio circuits, such as mixers, filters, mixer-filters, delay lines, varactors, inductors, and oscillators. In this chapter a MEMS oscillator will be used to replace Voltage Controlled Oscillators (VCOs). The MEMS oscillator is made using a post-CMOS process. Before the die is packaged, the CMOS die is etched in order to release the MEMS structures. The top metal layers in the CMOS process acts as a mask to prevent CMOS circuitry from being etched in addition to be used as a mask to define the MEMS structures. The resulting MEMS structure consists of a metal-dielectric stack where its thickness is determined by the number of metal layers available in the CMOS process. In this chapter, we will use a deep sub-micron CMOS process to illustrate the possibility for combining MEMS and CMOS in a small die area. The MEMS oscillator is to be used as a frontend for the FDSM.

FDSM and MEMS integrated in CMOS is a versatile platform for miniaturized low-power WSN nodes. In this chapter we illustrate the benefits of this approach using simulation, showing the potential for efficient miniaturized solutions.

2. Background

Within the international research community and industry, large research and development efforts are taking place within the area of Wireless Sensor Networks (WSN) (Raghunathan et al., 2006). Wireless sensor nodes are desirable in a wide range of applications. From a research perspective, power consumption and size are main parameters where improvements are needed. In this chapter we will focus on methods and concepts for low-voltage and low-power circuits for sensor interfacing in applications where the power budget is constrained, along with MEMS structures suitable for on-die CMOS integration. These technologies enable wireless sensor network nodes (WSNNs) with a very compact size capable of being powered with a depletable energy source due to its potential for low voltage and low power consumption.

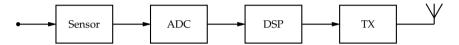


Fig. 1. Wireless sensor network node

The key components of a wireless sensor node are: 1) The sensor performing the actual measurement (pressure, light, sound, etc.), producing a small analog voltage or current. 2) An analog-to-digital (A/D) converter (ADC) converting and amplifying the weak analog sensor output to a digital representation. 3) A digital signal processing system, performing local computations on the aquired data to ready it for transmission, and for deciding when to transmit. 4) A radio transceiver for communicating the measurements. This is depicted in figure 1. The sensor readout circuitry, namely the ADC and processing logic, must continuously monitor the sensor readings in order to detect changes of interest and activate the transceiver only when needed to conserve power. For digital CMOS circuitry, an efficient way of saving power is to reduce the supply voltage, resulting in subthreshold operation of MOSFET devices, as their conductive channel will only be weakly inverted (Chen et al., 2002). In standard nanometer CMOS technology, safe operation is possible with supply voltages down to approximately 200mV (Wang & Chadrakasan, 2005). Conventional analog circuit topologies are not able to operate on these ultra low supply voltages, especially with the additional constraint of a scarce power budget (Annema et al., 2005). As a result, the ADCs currently represents a critical bottleneck in low-voltage and low-power systems, accentuating the need for new design methodologies and circuit topologies.

The sensor readout circuit must satisfy certain specifications like sufficient gain, low distortion and sufficient signal-to-quantization-noise ratio (SQNR). When studying existing Nyquist-rate ADCs, it is obvious that the analog precision is reduced as the power supply voltage is lowered (Chatterjee et al., 2005). This is mainly due to non-ideal properties of the active and passive elements, and process variations. In order to increase the SQNR, oversampled converters employing noise shaping $\Delta\Sigma$ modulators are used, trading bandwidth for higher SQNR (Norsworthy et al., 1996). ADCs are implemented either using continuous-time (CT) or Switched Capacitor (SC) components for realizing the necessary analog filter functions. SC realizations have generally been preferred for CMOS implementations as the method does not rely on absolute component values which are difficult to achieve without post-fabrication trimming. During the last few years, the power supply has moved down to 1 V in state-of-the art technologies making it hard to implement switches with sufficient conduction required for SC-filters. As a result, current SC realizations switch the opamp, eliminating the need

for CMOS switches in the signal path. This method is referred to as the Switched Opamp technique (Sauerbrey et al., 2002). As a result, the most important building block for both CT and SC based $\Delta\Sigma$ modulators are the opamp, which is also the limiting component with respect to conversion speed and signal-to-noise and distortion ratio (SINAD). As mentioned earlier, the sensor readout circuitry in a battery operated wireless sensor node should allow for operation far below 1V to facilitate low power consumption. This requirement eliminates both conventional CT and SC $\Delta\Sigma$ modulators as these approaches require large amounts of power at low supply voltages to attain reasonable performance.

Several low-power ADC topologies adapted for sensor interfacing have been reported in the last few years (Yang & Sarpeshkar, 2005; Kim & Cho, 2006; Wismar et al., 2007; Taillefer & Roberts, 2007). Among them, some are utilizing the time-domain instead of the amplitude-domain to reduce the sensitivity to technology and power supply scaling (Kim & Cho, 2006; Wismar et al., 2007; Taillefer & Roberts, 2007).

The non-feedback modulator for A/D conversion was introduced in Høvin et al. (1995); Høvin et al. (1997). In contrast to earlier published $\Delta\Sigma$ based ADCs, this approach does not require a global feedback to achieve noise shaping giving new and additional freedom in practical applications. This property is particularly useful when the converter is interfacing a sensor (Øysted & Wisland, 2005). The non-feedback $\Delta\Sigma$ modulator has two important properties which make it very suitable for low-voltage sensor interfacing. First, the topology has no global feedback which opens up for increasing the speed and resolution compared to conventional methods. Second, and most important, the analog input voltage is converted to an accumulated phase representing the integral of the input signal, thus moving the accuracy requirements from the strictly limited voltage domain, to the time domain, which is unaffected by the supply voltage. The conversion from analog input voltage to accumulated phase is performed using a Voltage Controlled Oscillator (VCO). As this solution uses frequency as an intermediate value, the non-feedback ADC using a VCO for integration is normally referred to as a Frequency Delta Sigma Modulator (FDSM).

Until recently, the FDSM has mainly been used for converting frequency modulated sensor signals with no particular focus on low supply voltage. In Wismar et al. (2006), an FDSM based ADC, fabricated in 90 nm CMOS technology, is reported to operate properly down to a supply voltage of 200 mV with a SINAD of 44.2 dB in the bandwidth from 20 Hz to 20 kHz (the audio band). The measured power consumption is 0.44 μW . The implementation is based on subthreshold MOSFET devices with the bulk-node exploited as input terminal for the signal to be converted.

At the RF front-end in WSN nodes, bulky off-chip components are usually used to meet the RF performance requirements. Such components are typically external inductors, crystals, SAW filters, oscillators, and ceramic filters (Nguyen, 2005). Micromachined components have been shown to potentially replace many of these bulky off-chip components with better performance, smaller size and lower power consumption. The topic of combining MEMS directly with CMOS has been of great interest in the past years (Fedder et al., 2008). The direct integration of MEMS with CMOS reduces parasitics, reduces the packaging complexity and the need for external components becomes less prominent. It turns out that integrating MEMS after the CMOS die has been produced has been most successful which is proven by Carnegie Mellon University (Chen et al., 2005; Fedder & Mukherjee, 2008), National Tsing Hua University (Dai et al., 2005), University of Florida (Qu & Xie, 2007) and University of Oslo (Soeraasen & Ramstad, 2008; Ramstad et al., 2009). The concept of CMOS-MEMS is maturing and seems to be versatile and

offer the flexibility of possibly replacing RF-front end components or sensors, both relevant in the context of WSNN.

3. Frequency Delta-Sigma Modulators

An FDSM based converter (Høvin et al., 1997) can conveniently be used in WSNNs for converting frequency modulated signals to a quantized and discrete bitstream, where the quantization noise is shaped away from the signal band. Overall, this results in frequency-to-digital (F/D) conversion with equivalent $\Delta\Sigma$ noise shaping.

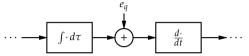


Fig. 2. FDSM overview

In the time domain, the input to the modulator, a frequency modulated (FM) signal, is $x_{\rm fm}(t) = \cos[\theta(t)]$, where the instantaneous phase is,

$$\theta(t) = 2\pi \int_0^t f_c + f_d \cdot x(\tau) d\tau \tag{1}$$

 f_d is the maximal deviation from the carrier frequency, f_c , while $x(\tau)$ represents the physical quantity we are measuring; assumed to be limited to ± 1 . The integral of the input signal and a constant bias is now represented by the phase, $\theta(t)$. The cosine function wraps the phase every 2π , effectively performing modulo integration. By using a counter, triggered by the zero-crossings of the $x_{\rm fm}$ signal, the integral of the input signal is quantized to a digital value which in turn is sampled at regular intervals, $T_s = f_s^{-1}$. A digital representation of the input, x, is recovered by differentiating the quantized phase signal. This is depicted in figure 3(a).

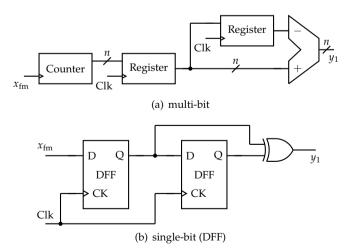


Fig. 3. First order FDSM topologies

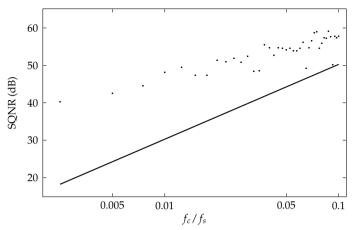


Fig. 4. Theoretical performance (solid line) and time-domain simulated performance (dots) as a function of carrier frequency and sampling frequency ratio

An important property is that quantization noise occurs after the integration, resulting in first order noise shaping of the quantization noise sequence, while the input signal is not altered. This is illustrated in figure 2, where e_q represents the quantization noise. Second order noise shaping can be obtained by integrating the quantization error from the first order FDSM. While the second order system requires a higher circuit complexity which incurs an increase in power consumption, it can be shown that the increase in performance in some cases outweighs the additional requirements (Michaelsen & Wisland, 2008).

The FDSM is inherently an oversampled system, meaning that the output bitrate, f_s , is much higher than the bandwidth of the input signal, f_b . Quantization noise is suppressed in the signal band through noise shaping. In the case of first order converters, the quantization noise will be shaped with a slope of 20 dB/decade.

If the number of zero-crossings of the FM signal during T_s is less than two, it is possible to realize the structure in figure 3(a) with only two D-flipflops (DFFs), and an XOR-gate used for subtraction, as illustrated in figure 3(b). Due to its simple implementation, the first order single-bit FDSM is a viable choice for WSNN applications because of its potential for low power consumption and low voltage operating requirements (Wismar et al., 2007). In this case, the resolution of the converter is given by (Høvin et al., 1997)

$$SQNR_{dB} = 20\log_{10}\left(\frac{\sqrt{2}f_d}{f_s}\right) - 10\log_{10}\left(\frac{\pi^2}{36}\left(\frac{2f_b}{f_s}\right)^3\right)$$
 (2)

However, in cases where $f_s/f_c\gg 1$, the actual performance may be better than predicted by equation 2. As illustrated in figure 4, this discrepancy can be significant. In this plot, f_s was held constant at 20 MHz, with $f_d=f_c\cdot 10\,\%$, and $f_b=19$ kHz. The solid line represents the performance predicted by equation 2 while the dots indicate the performance from a difference equation simulation of the converter. The underlying assumption in equation 2 is that the quantization noise sequence is a white noise sequence. However, this assumption in not accurate, and it is possible to exploit pattern noise valleys for significantly improving performance (Høvin et al., 2001).

Before further processing of the digital sensor signal in the WSNN, it is usually desirable to have an output frequency that is equal to, or slightly higher than, $2f_b$. To achieve this the output bitstream is decimated by first bandlimiting the signal using a low-pass filter. This removes the out-of-band noise to avoid aliasing. After low-pass filtering, only every N-th sample is kept, where $N = \frac{f_s}{2f_b}$. During and after decimation, each sample must be represented by more bits to avoid quantization noise being a limiting factor. The decimation usually requires a significant amount of computation. This task is therefore done in stages, where computationally efficient filters run at the input frequency, while more accurate filters run at lower frequencies. The first stage is usually a \sin^m -filter, where m is the order of the filter, named after its $(\sin(x)/x)^m$ shaped frequency response. This class of filter has a straight forward hardware implementation (Hogenauer, 1981; Gerosa & Neviani, 2004) capable of high frequency operation. It can be shown that a \sin^{L+1} filter is sufficient for an order L $\Delta\Sigma$ modulator (Schreier & Temes, 2004). At later stages, more complex filters can be used to correct for the non-ideal features of the sinc filter such as passband droop (Altera Corporation, 2007).

The frontend of the FDSM—be it a VCO in the case of an ADC, or a device which directly converts some physical quantity to a frequency modulated signal—will to some extent have a non-linear transfer function. A non-linear FM source will in turn give rise to harmonic distortion present in the output signal. Although quantization noise is shaped away from the signal band, harmonic distortion will not be suppressed as it is impossible for the F/D converter to distinguish between what is the actual signal and what is noise and distortion. This non-linearity deteriorates the effective resolution of the measurement system. However, several digital post-processing schemes and error correction systems have been devised that are able to recover linearity to some extent (Balestrieri et al., 2005). Care must be taken when designing the post-processing system so that aliasing of values and missing output codes does not present a problem. Another issue with the FDSM frontend is phase noise, also referred to as jitter. This noise will directly add to the input signal and therefore not undergo noise shaping; raising the noise floor at the output. 1/f noise has shown to be particularly problematic, and careful attention to issues related to noise is critical when designing the oscillator circuit. This is especially challenging in deep sub-micron CMOS technologies.

4. Using a MEMS resonator as a VCO

4.1 The micromechanical resonator

A resonator is a component which is able to mimic full circuit functions such as filtering, mixing, line delays, and frequency locking. The resonator is a mechanical element that vibrates back and forth where the displacement of the micromechanical element generates a time varying capacitance which in turn results in an ac current at the output node. The maximum output current occurs when stimulating the resonator with an input ac voltage with a frequency equal to the resonance frequency of the resonator. The micromechanical resonator can be represented as an LCR circuit (see figure 5) where the equations describing these passive components are related to physical parameters such as mass, damping, and stiffness (Senturia, 2001; Bannon et al., 2000).

Figure 5 is a simple LRC circuit which can be described as,

$$V_i = \ddot{q}(t)L_x + \dot{q}(t)R_x + q(t)\frac{1}{C_x}$$
(3)

where L_x , R_x and C_x are the passive element values for a maximum displacement x of the resonator. V_i and V_0 are the input and output voltages as shown in figure 5. q(t) is the charge

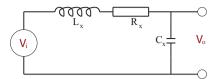


Fig. 5. A simple LCR circuit

on the capacitor which depends on the time t. By using the relationship between the output and the input $(H(t) = V_0/V_i)$ from the circuit of figure 5 and by using $q = C_x V$ results in the derivation of the resonance frequency of this system:

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{1}{L_x C_x}} \tag{4}$$

From the transfer function, the maximum throughput exists when the reactances of the inductor and the capacitor is equal to each other and opposite, thus this defines the resonance frequency for this micromechanical system. For RF front-end components and oscillators, it is desirable to have a good transfer of the signal through the component. A good throughput is possible by having a good Q-factor which is described by,

$$Q = \frac{\omega_0 L_x}{R_x} \tag{5}$$

where equation 5 is derived from the transfer function of figure 5 and ω_0 is the resonance frequency of the resonator ($\omega_0=2\pi f_0$). A large Q-factor is usually desirable to get good resonator performance. As explained in section 4.5, the resulting MEMS structures consists of a laminate of metal and dielectric, so the resulting Q-factor will be limited mostly by intrinsic material loss and gas damping which will be discussed later. A top view of a micromechanical resonator is shown in figure 6.

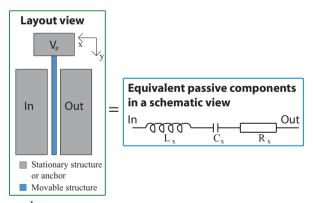


Fig. 6. The resonator analogy

Figure 6 shows a long and thin cantilever beam (fixed at one end, free to move at the other end) with two electrodes next to it. The left electrode is the input electrode while the right electrode is the output electrode. The gray areas indicate stationary elements (the anchor and

the electrodes) while the blue area indicates a part which is able to move freely (the resonator). The thin and long cantilever beam moves back and forth laterally above the silicon substrate towards the two electrodes in the x-direction. At the resonance frequency of this resonator, the maximum vibration towards the electrode is x. The thickness of the beam is not shown here as this is a top view. The V_P signal applied to the beam itself is a high DC voltage which is used to cancel unwanted frequency terms and to amplify the signal of the resonator. By separating the V_P signal from the input and output ac signals, the V_P signal will not be superimposed on either of the two signals. The gap g between the resonator and the electrodes is an important parameter which will decide vital aspects of the resonator as will be shown later.

4.2 The electromechanical analogy

4.2.1 The electromechanical coupling coefficient

The micromechanical resonator is attracted due to electrostatic forces creating a capacitive coupling between the resonator and the input electrode (Kaajakari et al., 2005). A large electrode area that covers the resonator is desirable where the capacitance C is described as,

$$C = \frac{\varepsilon_0 W_r W_e}{g} \tag{6}$$

where ε_0 is the permittivity in air, W_r is the resonator width (vertical thickness, not visible in figure 6), W_e is the electrode length, and g is the gap between the resonator and the electrode. The capacitance equation is related to the electrostatic force equation (F). The electrostatic force F is derived from the potential energy equation $U = \frac{1}{2}CV^2$ which results in:

$$F = \frac{dU}{dx} = \frac{1}{2} \frac{dC}{dx} V^2 \tag{7}$$

where V is the signal voltage. ${}^{dC}\!/_{dx}$ is the capacitance change due to a small change in the gap size g because the resonator bends towards the electrode with a displacement x. The force is proportional to the square of the voltage V which will introduce a $\cos(2\omega t)$ term (the derivation of this is not shown here). The $\cos(2\omega t)$ term will introduce oscillation at $\omega = {}^{\omega_0}\!/_2$, half the resonance frequency. In order to avoid this nonlinear relationship, a polarization voltage V_P is applied to the beam. When splitting V into $V_P + v \cdot \cos(\omega t)$ the resulting electrostatic force becomes,

$$f = V_P \frac{dC}{dx} v \tag{8}$$

Equation 8 describes the relationship between the force f and the voltage v (small signal values) that now has a linear relationship. It is now possible to derive the coefficient known as η :

$$\eta = V_P \frac{dC}{dx} \approx V_P \frac{\varepsilon_0 W_r W_e}{g^2} \tag{9}$$

 η is a coefficient which describes how well the signal from the electrode is transferred to the resonator. It is an equation that is a result of the electrostatic force equation so that the force f has a linear relationship to the voltage v. A larger η results in a larger signal of the resonator. It is desirable with a large electrode area ($A_{el} = W_r W_e$) and a small gap g. Because η is inversely proportional to the square of the gap between the electrode and resonator, it is desirable to have an extremely small gap size. Both the electrode area A_{el} and the gap size g are limited by process constraints. Notice that equation 9 is a simplified equation of η as the derivation of the capacitance C with respect on the gap g is done by assuming that the gap is the same throughout the g-axis of the resonator (throughout the resonator length g-axis of g-axis of

4.2.2 Resonator output current

The output current due to the capacitive coupling explained in section 4.2.1 can be written as:

$$i_0 = V_P \frac{dC}{dt} + C \frac{dv}{dt} \approx V_P \frac{dC}{dt} \tag{10}$$

The output current in equation 10 consists of two parts: One part which is amplified with the polarization voltage V_P , and one part which consists of the (small) sinusoidal voltage v. Equation 10 was derived by using $i_0 = {}^d/_{dt}(C \cdot V)$ (Bannon et al., 2000). It is possible to further simplify this equation by neglecting the $C^{dv}/_{dt}$ part because the voltage V_P is much larger than v:

$$i_o = V_P \frac{dC}{dx} \frac{dx}{dt} \approx \eta \omega_0 x$$
 (11)

Equation 11 was derived by using the relationship ${}^{dx}\!/_{dt} = \omega_0 x$. By using V_P , the output current i_0 can be amplified as shown in equation 11. However, when increasing V_P , ω_0 will be reduced while the displacement x increases. This means that the current will have an exponential-like increase as V_P is increased and not a linear increase of i_0 which could be expected. The fact that the operational (resonance) frequency of the resonator decreases when V_P is increased is due to an effect known as "spring-softening" which will be discussed later (Bannon et al., 2000). This spring-softening effect will be utilized in order to use the micromechanical resonator as a voltage-controlled oscillator (VCO).

4.2.3 The LCR equivalents

By using the principle of electromechanical conversion as explained in section 4.2.1, it is possible to derive formulas for L_x , C_x and R_x .

$$L_x = \frac{m_{eff}}{\eta^2} \tag{12}$$

$$C_x = \frac{\eta^2}{k_r} \tag{13}$$

$$R_x = \frac{\sqrt{k_r m_{eff}}}{Q \eta^2} \tag{14}$$

where k_r is the effective spring stiffness and m_{eff} is the effective mass of the resonator. Q is the Q-factor of the resonator which is inverse proportional to the total damping of the micromechanical resonator. All three LCR components are dependent on the square of η . This indicates a square dependence of the electrode area A_{el} and a g^4 dependence of the gap between the resonator and the electrode. The electrical equivalents of the components are not straightforward to interpret due to complicated relationships between the mass, stiffness and damping of the resonator, as well as complicated relationship due to the electrostatic force.

4.3 The resonance frequency and its implications

4.3.1 The nominal resonance frequency

The natural frequency of the resonator with no voltage applied is given by equation 15 below (Senturia, 2001):

$$f_{0(eff)} = \frac{1}{2\pi} \sqrt{\Lambda_n \frac{k}{m}} \tag{15}$$

where k is the static beam stiffness and m is the static beam mass of the micromechanical system. Λ_n is a constant depending on mode number. A mode is a certain frequency in which the resonator will have a maximum vibration amplitude. A micromechanical resonator may have several modes at distinct frequencies. Λ_n has different values for different modes. For example, Λ_1 =1.0302 for mode 1, Λ_2 =40.460 for mode 2, Λ_3 =317.219 for mode 3 etc. The resonator is operated in the first mode (Λ_1). Both k and m depends on the geometry and structural material of the resonator. The values for Λ_n used here is valid only for the cantilever beam architecture, other types of resonators will have different values of Λ_n .

4.3.2 The effective resonance frequency and Q-factor

The movable parts of the resonator will all vibrate back and forth with the resonance frequency ω_0 . The tip of the beam will have a longer distance to move and will thus have a higher velocity \dot{v} compared to the part of the cantilever beam which is closer to the anchor. Because the kinetic energy ($E_k = \frac{1}{2} m_{eff} \dot{v}^2$) must be the same throughout the beam when it vibrates, the effective mass along the beam in the y-direction in figure 6 will vary. The effective mass is defined as m_{eff} where the largest value appears close to the anchor while the smallest value appears at the tip of the beam. The derivation of m_{eff} is not shown here but can be developed by using the equation for kinetic energy. By using equation 15 and rearranging, the mechanical spring stiffness can be defined as:

$$k_m(y) = \left(2\pi f_{0(eff)}\right)^2 m_{eff}(y) \tag{16}$$

Equation 16 shows the pure mechanical spring stiffness of the beam when it vibrates. $k_m(y)$ varies along the beam in the y-direction with a maximum value close to the anchor and a minimum value close to the tip of the beam. However, when applying a DC voltage V_P to the beam, the total spring stiffness of the beam will be reduced. The resulting effective spring stiffness value k_r is reduced due to an electric spring value k_e . Because of this fact, the resonance frequency of the cantilever beam will be reduced as described in the following equation:

$$f_0 = f_{0(eff)} \sqrt{1 - \frac{k_e}{k_m}} \tag{17}$$

where the relationship ${}^{k_e}\!/_{k_m}$ determines the amount of reduction of the original nominal resonance frequency $f_{0(eff)}$. The effective spring stiffness k_r is defined as:

$$k_r = k_m - k_{\varrho} \tag{18}$$

where k_r is known as the effective beam stiffness. k_r is the result of subtracting the electrical spring stiffness k_e from the effective mechanical spring stiffness k_m (spring-softening). The effective beam stiffness is more precisely defined as,

$$k_r = \left(2\pi f_{0(eff)}\right)^2 m_{eff}(y) - \int_{W_{e1}}^{W_{e2}} V_p^2 \frac{\varepsilon_0 W_r dy'}{[g(y')]^3}$$
 (19)

where the second term of equation 19 describes the electrical spring stiffness at a specific location y' centered on an infinitesimal length of the electrode dy'. The k_e part consists of integrating from the start of the electrode (W_{e1}) to the end of the electrode (W_{e2}). The variable part of the k_e equation is the gap which varies along the y-axis throughout the beam length. The

 k_e equation is derived from the potential energy equation $U = \frac{1}{2}CV_p^2$. The gap as a function of y can be described as (Bannon et al., 2000):

$$g(y) = g_0 - \frac{1}{2} V_p^2 \varepsilon_0 W_r \int_{W_{e1}}^{W_{e2}} \frac{1}{k_m(y') [g(y')]^2} \frac{X_{mode}(y)}{X_{mode}(y')} dy'$$
(20)

where g_0 is the static electrode-to-resonator gap with $V_P = 0$. X_{mode} is an equation that describes the shape of how the cantilever beam bends. The second term describes the displacement of the resonator towards the electrode at various locations of y. As can be seen in equation 18, if k_e becomes equal to k_m , the resonance frequency should become zero. However, before that would occur, the resonator will enter an unstable state which will pull the beam towards the electrode instead. This effect is known as the "pull-in" effect. Due to the reduction of the original natural frequency of the resonator, the Q-factor will also be reduced in a similar manner. The Q-factor is mainly affected by four factors: Anchor loss, environmental (viscous gas) damping, thermoelastic damping or internal (material) energy loss. The topic of damping mechanisms for MEMS resonators is not trivial, therefore it is typical to do crude estimates for the nominal Q-factor as a starting point for analysis (Bannon et al., 2000).

$$Q_{eff} = Q_{nom} \sqrt{1 - \frac{k_e}{k_m}} \tag{21}$$

From equation 17 and equation 21 we can conclude that when increasing the V_P value, both the resonance frequency and the Q-factor of the resonator are reduced. For oscillators, a high Q-factor is desirable, therefore it is important to also include this reduction of the Q-factor for correct modeling.

4.4 Nonlinear behavior

As described by equation 17, the oscillation frequency is tuned by using V_P . In order to get a good tuneability of the MEMS resonator, it is designed to be soft so that it can operate at low voltages and at the same time have a reasonable tuning range. However, when a beam is too soft, non-linear effects become more dominant. We can classify two different types of resonator non-linearities (Kaajakari et al., 2005; 2004):

- Mechanical non-linearity: Typically non-elasticity due to geometrical and material effects
- Capacitive non-linearity: Introduced due to an inverse relationship between the displacement and the "parallel" plate capacitance

Mechanical non-linearity will be more prominent in other resonator architectures such as the clamped-clamped beam, we will therefore focus on the capacitive non-linearities for this analysis. In order to develop an understanding of the introduction of the capacitive nonlinearity, we must take a look at the equation describing the motion of the resonator:

$$m_{eff}\ddot{x} + b\dot{x} + k_r x = F(t) \tag{22}$$

Equation 22 describes the equation of movement of the resonator due to an external force. This equation is basically the same as equation 3 where the external force is the electrostatic force. The equation of movement is related to the effective mass m_{eff} , the damping b (which is inverse proportional to Q), and the effective spring stiffness k_r . In this equation k_r has a mechanical

term k_m and an electrical term k_e as described earlier. For a case where k_e is linear, the motion of the amplitude becomes:

 $X_0 = \frac{FQ_{eff}}{k_r} \tag{23}$

Equation 23 shows the displacement of the tip of the beam at resonance. However, when the resonator has a low mechanical stiffness k_m , and is at the same time operated with large V_P values, the linear k_e model becomes inaccurate. Therefore the following equation is used instead:

$$k_e(x) = k_{e0} \left(1 + k_{e1}x + k_{e2}x^2 + ...k_{en}x^n \right)$$
 (24)

From equation 24, we can see that the spring stiffness consists of higher order terms that all are related to the displacement x (Kaajakari et al., 2005). The k_{e0} term is the first term and is linear. k_{e1} and k_{e2} are square and cubic electrical spring coefficients respectively:

$$k_{e0} = -\frac{V_p^2 C_0}{g^2}, k_{e1} = \frac{3}{2g}, k_{e2} = \frac{2}{g^2}$$
 (25)

The $k_e(x)$ terms contribute to reducing or increasing the frequency depending on which term that dominates. When operating the resonator with high vibration amplitudes, the square and cubic spring stiffness terms will become more dominant. Because the amplitude-frequency curve no longer becomes a single valued function, the oscillation may become chaotic once the amplitude is larger than a critical value known as x_c . The maximum usable vibration value is extracted from the largest value that appears before a bifurcation (hysteresis of the curve). The bifurcation amplitude and critical amplitude are respectively (Kaajakari et al., 2005):

$$x_b = \frac{1}{\sqrt{\sqrt{3}Q|\kappa|}}, x_c = \frac{2}{\sqrt{3\sqrt{3}Q|\kappa|}}$$
 (26)

where

$$\kappa = \frac{3k_{e2}k_{e0}}{8k} - \frac{5k_{e1}^2k_{e0}^2}{12k^2} \tag{27}$$

Figure 7 is an example of how κ will affect the response out from the resonator. κ_1 is the lowest value and κ_3 is the largest value. In this example, κ is positive and contributes to increase in the resonance frequency as well as tilting the curve to the left. κ_1 is the lowest value and shows less tilting of the curve. When κ is too large (see κ_3), the curve enters a state of hysteresis. At the point when the hysteresis starts, the bifurcation amplitude κ_b is reached. For any curve with a hysteresis, the maximum usable amplitude of vibration is κ_c as shown in figure 7b. κ_c is always larger than κ_b and ultimately sets the limit for the maximum vibration amplitude as well as it sets the maximum output current from the resonator. Because κ is a factor which will contribute to a modified resonance frequency due to the spring stiffness non-linearities, the new resonance frequency is therefore expressed as,

$$\omega_{0(effective)} = \omega_0 \left(1 + \kappa X_0^2 \right) \tag{28}$$

From equations 27 and 28 we can see that κ will either increase (resonator becomes more stiff) the operational resonance frequency or decrease the resonance frequency. The resonator used here will have a positive κ , thus the capacitive non-linearities will contribute to stiffen the

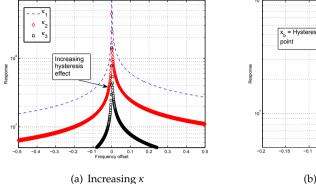


Fig. 7. Bifurcation and critical bifurcation

resonator. Because κ contributes to "stiffen" the output response, more V_P must be applied than first estimated in equation 17. By using equation 26 and 27, an expression for the maximum output current possible from the resonator is developed:

$$i_o^{max} = \eta \omega_0 x_c \tag{29}$$

 i_o^{max} sets the limit for how much current that can be registered at the output electrode before bifurcation. The difference between equation 10 and equation 29 is that the maximum current is limited by the critical vibration x_c instead. It is also possible to define the maximum energy stored in the resonator by using x_c in a similar manner.

$$E_{stored}^{max} = \frac{1}{2}k_0 x_c^2 \tag{30}$$

where k_0 is a linear spring constant ($k_0 = k_m - k_{e0}$). The maximum energy stored also determines the energy dissipation out from the resonator which is,

$$P_{dissipated} = R_x i_o^2 = \frac{\omega_0 E_{stored}^{max}}{O}$$
 (31)

In order to understand the stability of the resonance frequency, the phase-noise of the system can be evaluated. This is possible by using Leeson's equation to model the phase-noise-to-carrier ratio in an ideal oscillator:

$$\mathcal{L}(\Delta f) = 10 \log \left[\frac{kT}{\pi E_{stored}^{max}} \frac{Q}{f_0} \left(1 + \left(\frac{f_0}{2Q\Delta f} \right)^2 \right) \right]$$
(32)

where k is Boltzmann's constant and T is the absolute temperature (Shao et al., 2008). It is common to relate equation 32 to equation 31 and also add a buffer noise source from the amplifier following the resonator as given by (Kaajakari et al., 2004):

$$\mathcal{L}(\Delta\omega) = \frac{2kT}{P_{dissipated}} \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 + \frac{P_N^{buffer}}{2P_{dissipated}}$$
(33)

where P_N^{buffer} is buffer noise from an amplifier source. This value can be set to $-155^{dBm}/\sqrt{Hz}$ (or $v_n = 4n^V/\sqrt{Hz}$ for a 50Ω system). The equation for phase noise will be shown in a practical example in section 5.2.

4.5 Integration of MEMS in CMOS

There are three main methods of integrating MEMS in a CMOS process: 1. Insert the MEMS before the CMOS is made. 2. Insert the MEMS in between CMOS process steps. 3. Insert the MEMS after the CMOS has been made. In this demonstration, we will focus on the third step where the MEMS is made after the CMOS has been made which is known as post-CMOS. We will not go into the details of the process here for the sake of simplicity.

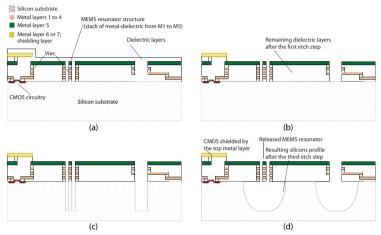


Fig. 8. The CMOS-MEMS process steps

The CMOS-MEMS process demonstrated here is inspired by previous work done at some universities (Ramstad, 2007; Fedder & Mukherjee, 2005; Sun et al., 2009). For low-power applications it is interesting to try to integrate MEMS in a deep sub-micron CMOS process. Figure 8 shows the process steps that have been used for a general deep sub-micron CMOS process. The steps a) to d) consist of the following:

- a) The wafer before etching
- b) Anisotropic etching of the dielectric
- c) Etching of silicon using DRIE
- d) Isotropic release-etch of silicon

This list shows the steps performed in order to etch and release MEMS structure(s). From figure 8 it can be seen that the top metal layer will act as a mask and define the MEMS structures. The MEMS resonator and electrodes consist of a stack of metals and dielectrics from metal layer 1 to metal layer 5. Areas that are not to be etched must be protected by a top metal layer (i.e. metal layer 6 or 7). The cross-section reveals that the CMOS must be placed a certain distance away from the open areas where the MEMS structures are etched and defined. The thickness of the resulting MEMS structure depends on the amount of metal layers that are used. The thickness of the metal-dielectric stack influences the smallest possible gap between a resonator and an

electrode. There are also rules which define the smallest possible width of a structure and the largest possible width of a structure. There are more CMOS-MEMS rules than discussed here, but these are some of the most important ones when combining CMOS and MEMS on-chip by making MEMS structures from the metal layers offered by a general CMOS process.

4.6 The oscillator circuit

The MEMS resonator described in section 4.1 is made using a conventional 90 nm CMOS process using the same process steps as described in section 4.5. By putting the micromechanical resonator in a feedback loop with an amplifier, we get the basic oscillator circuit as shown in figure 9 below:

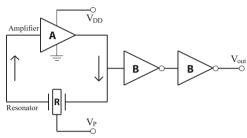


Fig. 9. Basic oscillator circuit

An oscillator is defined as a circuit that produces a periodic output signal at a fixed frequency. The resonator is the element in the circuit which defines the resonance frequency while the amplifier is the active element which sustains oscillation. The bias voltage V_P applied to the resonator is used to tune the frequency of this voltage-controllable oscillator. In this demonstration, the Q-factor of the resulting metal-dielectric MEMS structure is lower compared to state-of-the-art MEMS and will contribute to increase the motional impedance R_x which is seen in series with the amplifier. The low Q-factor will also lead to a large phase-noise. Both these two factors are not critical here as this is a demonstration to show MEMS directly combined with CMOS processing that could lead to future interesting applications. Even though R_x is large, the amplifier will be able to initiate and sustain oscillation. In order for the oscillator to start up the impedance from the amplifier has to be negative and at least three times larger than the total impedance that is in series with the amplifier. The total impedance consists of parasitics in the circuit plus the motional impedance from the resonator. More details of how to start up and sustain oscillation is not described here but can be investigated further in reference (Ramstad, 2007; Vittoz et al., 1998). In figure 9, element A is realized as a Pierce Amplifier, element R is realized as the resonator described in section 4.1, while the two B elements are buffers to amplify the signal for the following FDSM stage.

5. System simulation

In order to investigate the viability of our proposed system, and to discover potential problems, we devised a simulation model of the system. In this section, we first present our simulation of the full FDSM and MEMS system. We then go on to describe our experiment, and finally we discuss the simulation results.

5.1 Method

As the output frequency of the MEMS oscillator in this case is low, a first-order oversampled FDSM as the F/D converter is appropriate. A detailed simulation model would be too computationally demanding to be of practical use. It would also require a mechanical simulation for the MEMS part in co-simulation with the electrical FDSM netlist. We therefore implemented the simulation model using Verilog-A (Accellera Organization, Inc., 2008) building blocks running on a commercial SPICE simulator. An outline of the simulation model is depicted in figure 10. The output from this model is a sampled single-bit bitstream, y[n]. The bitstream was then decimated to a stream of output words, which were finally post-processed to compensate for the non-linearity of the MEMS resonator. In the following subsections we describe the components of our simulation model in more detail.

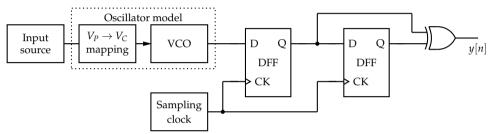


Fig. 10. Simulation model outline

5.1.1 The oscillator circuit

The modeling of the resonator has mostly been done by using analytical scripts from the equations described in section 4. Due to the non-linearity of the MEMS resonator for large values of V_P , the need for a more sophisticated simulation tool became apparent. By using a Finite Element Method (FEM) software tool, an accurate simulation of the resonance frequency and beam displacement as a function of the V_P voltage is performed. The results from the FEM simulations are back annotated into the analytical script in order to develop correct RLC equivalents, resonator output current as well as a correct model of the phase-noise. The total VCO model is then described by using Verilog-A. The VCO model is in itself a linear VCO. The non-linearity (arising from the MEMS resonator) is applied as a pre-distortion of the input signal, mapping the tuning voltage, V_P , to a VCO control voltage, V_C , using a table_model construct in Verilog-A code. This gives the designer, flexibility and makes it easy to switch between different VCO characteristics.

Figure 11 shows the implementation of the MEMS resonator where this cantilever beam is $100\mu m$ long, $1\mu m$ wide and a few microns thick. This is a resonator which is easy to tune in frequency because its mechanical stiffness is rather low. A fixed-fixed beam would allow a higher operational frequency, but is in turn more difficult to tune. A different resonator architecture as a tunable MEMS resonator can be developed, however in this chapter we focus on a simple MEMS architecture in order to point out the non-linearity problem and the resulting phase-noise of this CMOS-MEMS resonator.

The amplifier in the oscillator circuit is a Pierce amplifier which is a single-ended solution. The Pierce amplifier is a simple topology that has low stray reactances and little need for biasing resistors which would lead to more noise. By tuning the bias current in the Pierce amplifier, the gain (or equivalent negative impedance) increases. The MEMS resonator is typically the

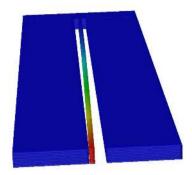


Fig. 11. 3D plot for the 1st vibrational mode of the MEMS resonator

element which limits the phase-noise, not the Pierce amplifier. However, the Pierce amplifier needs to be flexible enough in order to initiate and sustain oscillation of the MEMS resonator. For a variation of Q-factor of the MEMS resonator and possible process variations, the Pierce amplifier has been made to start up oscillation for R_x values up to a few M Ω as the Pierce amplifier can be represented as a negative impedance value of up to around ten M Ω . It would be possible to make a full differential amplifier and resonator configuration for low noise applications, however this has been left out as future work.

5.1.2 FDSM circuit

The FDSM circuit is a first-order single-bit DFF FDSM. The FDSM circuit is made up of two DFFs whose outputs are XOR-ed. The DFFs and XOR gate are implemented as individual Verilog-A components interconnected in a SPICE sub-circuit. The FDSM circuit also contains an ideal sampling clock source.

5.1.3 Decimation and digital post-processing

As we used an FDSM with first order noise shaping, we used a sinc^2 filter with N=8 in the first stage, see figure 12. In the second stage, we used sinc^4 filter with N=32, and finally a FIR filter with a decimation ratio of 2. This is depicted in figure 13. The sinc^4 filter in the second stage was used to give better rejection of excess out-of-band quantization noise. We did not correct for the passband droop incurred by the sinc filters.

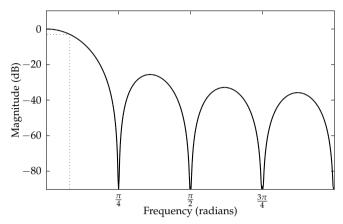


Fig. 12. Magnitude response of the first stage decimation filter

The non-linearity of the oscillator's transfer function gives rise to a significant harmonic distortion, which deteriorates the performance of the ADC. In this case, we used a simple lookup table (LUT) (Kim et al., 2009), to map every possible intermediate output, to a final quantized and corrected value. The non-linearity was characterized by applying a known linear input sequence, which in turn was used to build the inverse mapping LUT.

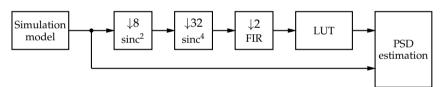


Fig. 13. Bitstream decimation and post-processing

Both decimation and post-processing was implemented outside the simulation model and no quantization was performed until after the post-processing.

5.1.4 Spectral estimation and performance measurement

The output data collected from the simulation model, and from the decimation and post-processing was analyzed using a Fast Fourier Transform (FFT) according to the guidelines in Schreier & Temes (2004).

5.2 Results

In section 4.4, the reason for the critical vibration amplitude x_c was shown and discussed. Varying V_P will eventually make the theoretical amplitude cross the x_c around 6.5V as shown in figure 14a.

If the resonator is initially placed in an environment with some pressure, reducing the pressure to a vacuum state will result in an increase in the Q-factor and x_c can cross the theoretical resonator displacement amplitude x quicker than anticipated. The resonator used here is used in a low-pressure environment, but placing it in vacuum will not increase the Q-factor significantly due to internal material loss. The critical vibration amplitude results in a small

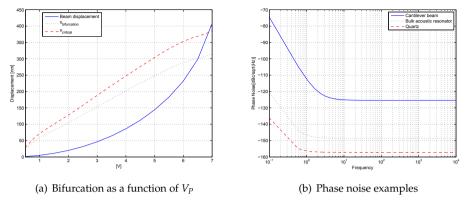


Fig. 14. Bifurcation and phase noise

buffer before the hysteresis amplitude x_b is reached. By using x_c and Leeson's equation for phase noise as shown in section 4.4, we can plot the phase noise as a function of offset from the carrier frequency. Figure 14b shows some examples of other VCO components and how much noise they have compared to the resonator used in this CMOS-MEMS demonstration. The phase-noise example is calculated using equation 33, although this noise model has not been implemented in the total VCO model.

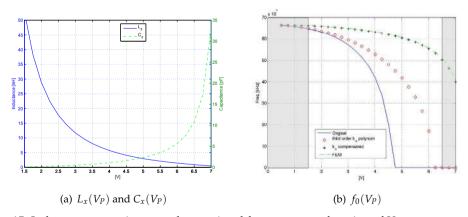


Fig. 15. Inductance, capacitance and operational frequency as a function of V_P

When varying V_P , the RLC equivalent that represents the MEMS resonator in the oscillator circuit will vary. An example of this is shown in figure 15a where the inductance decreases and the capacitance increases when V_P is increased. The variations of these two components are exactly opposite. From figure 15a, it can be seen that there is an exponential tendency of both values at the ends of the graph. This exponential behavior sets a "starting limit", thus the

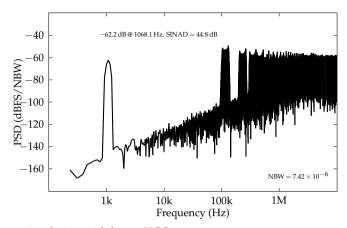


Fig. 16. Reference simulation with linear VCO

critical vibration amplitude x_c ultimately determines the maximum tunable frequency of the VCO as shown in figure 15b.

The k_e compensated term in figure 15b is extracted from the FEM simulation tool in order to develop the correct k_e . A first and third order polynomial k_e is also shown in order to demonstrate that the analytical formulas become too coarse grained for such a soft beam, thus the need for combining FEM results and analytical results becomes more important. The resulting operational area for the VCO gives an input range $V_P = 1.5 \rightarrow 6.5$ V, which gives $f_c = 58546$ Hz, and $f_d = 7743.7$ Hz. We used a sampling frequency, f_s , of 20 MHz for the FDSM circuit, and defined the signal bandwidth, f_b , to be 19 kHz. Equation 2 predicts SQNR_{dB} = 22 dB. All spectral plots were plotted using 2^{18} samples for the full spectrum, and 2^9 samples for the decimated spectra.

After characterizing the MEMS resonator, we built the LUT by applying 16 equally spaced DC inputs to the system spanning the input range. To estimate the corresponding output codes we averaged each output sequence, which was truncated to 2⁹ samples after decimation.

We then simulated the full system for 16.4 ms using a full-scale sine wave input. In the first experiment we used a linear transfer function for the VCO to serve as reference. The result from this experiment is plotted in figure 16. In this case, the signal to quantization noise and distortion (SINAD) ratio is 44.8 dB.

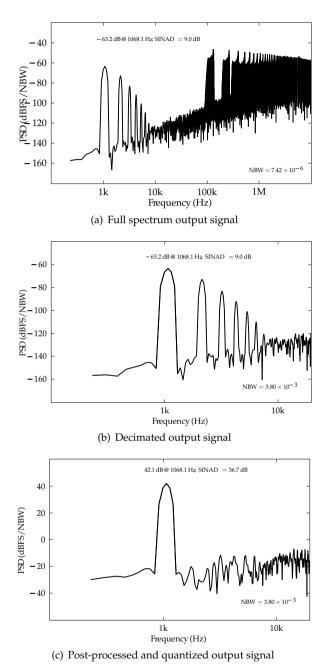


Fig. 17. Simulations with MEMS resonator non-linearity

In the second experiment we used the transfer function obtained from the MEMS resonator

simulation. The results from this experiment are shown in figure 17. The full spectrum is shown in figure 17a, the spectrum after decimation is shown in figure 17b, and the post-processed signal is plotted in figure 17c, quantized to 8 bits. After linearization and quantization, the SINAD is 36.7 dB.

5.3 Discussion

From figure 16, we can see that quantization noise is shaped with a slope of 20 dB/decade as expected and that the spectrum is smooth in the in-band part of the signal. The difference between the simulated SINAD and SQNR_{dB} predicted by equation 2 is 22.8 dB which is significant. However, $f_c/f_s \approx 0.003$, so this discrepancy is supported by the data in figure 4. Given the modest frequency tuning range of the MEMS resonator the overall resolution of the converter is very reasonable, because of the high sampling frequency with respect to the carrier frequency, which compensates for the potential impact on performance. This indicates that the overall system performance can be recovered by shifting the burden to digital circuits—in accordance with the long standing trend in CMOS technology where each new technology generation is geared towards allowing for aggressive performance scaling of digital circuitry, at the expense of analog and mixed signal performance.

As expected, the non-linearity of the MEMS resonator is clearly visible as harmonic distortion in figure 17a and 17b. By comparing figure 17b and 17c, it is evident that the LUT based correction scheme to a large extent recovers overall linearity; approximately one effective bit of resolution is lost. This further supports that relying on digital processing for achieving sufficient resolution is feasible in this system. As explained, the LUT processing scheme was applied before quantization. Thus, in a hardware realization, tradeoffs will have to be made. However, the results presented in this section indicate that given sufficient resources, linearity can to a certain degree be recovered. Another important consideration when using this scheme for linearization is that it gives rise to a non-linear dynamic range—electrical noise will have varying impact on the spectrum due to the non-linear gain.

6. Conclusion

In this chapter, we have presented CMOS MEMS and FDSM as a platform for WSNNs. CMOS MEMS can be used for building a wide range of sensors for use in WSNs, and have application in communication subsystems. FDSM provides a simple and robust means of digitizing the sensor signal. In all, this enables compact low-power WSNNs.

While we have outlined the feasibility of this scheme, more research is needed to further investigate this approach. Currently, we are working on more sophisticated methods for achieving linearity. A higher frequency resonator would enable the application of second order noise shaping, which is beneficial for high resolution, low-power applications. Also, a higher resonator tuning range and better linearity would directly benefit the system's performance. The phase noise needs more attention to investigate the system level impact, and the tuning voltage of the resonator is too high to be compatible with deep sub-micron CMOS transistors. We are currently working towards a prototype implementation of the system.

7. References

Accellera Organization, Inc. (2008). Verilog-AMS Language Reference Manual. Altera Corporation (2007). Application Note 455: Understanding CIC Compensation Filters.

- Annema, A.-J., Nauta, B., van Langevelde, R. & Tuinhout, H. (2005). Analog circuits in ultra-deep submicron CMOS, *IEEE Journal of Solid-State Circuits* **40**(1): 132–143.
- Balestrieri, E., Daponte, P. & Rapuano, S. (2005). A State-of-the-Art on ADC Error Compensation Methods, *IEEE Transactions on Instrumentation and Measurement* **54**(4): 1388–1394.
- Bannon, F., Clark, J. & Nguyen, C.-C. (2000). High-Q HF Microelectromechanical Filters, *Solid-State Circuits, IEEE Journal of* **35**(4): 512–526.
- Chatterjee, S., Tsividis, Y. & Kinget, P. (2005). 0.5-V analog circuit techniques and their application in OTA and filter design, *IEEE Journal of Solid-State Circuits* **40**(12): 2373–2387.
- Chen, F., Brotz, J., Arslan, U., Lo, C.-C., Mukherjee, T. & Fedder, G. (2005). CMOS-MEMS resonant RF mixer-filters, pp. 24–27.
- Chen, O.-C., Sheen, R.-B. & Wang, S. (2002). A low-power adder operating on effective dynamic data ranges, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* **10**(4): 435–453.
- Dai, C.-L., Chiou, J.-H. & Lu, M. S.-C. (2005). A maskless post-CMOS bulk micromachining process and its applications, *Journal of Micromechanics and Microengineering* 15: 2366–2371.
- Fedder, G., Howe, R., Liu, T.-J. K. & Quevy, E. (2008). Technologies for Cofabricating MEMS and Electronics, *Proceedings of the IEEE* **96**(2): 306–322.
- Fedder, G. K. & Mukherjee, T. (2005). Integrated RF Microsystems with CMOS-MEMS components, *in Proceedings of MEMSWAVE*, pp. 111–115.
- Fedder, G. & Mukherjee, T. (2008). CMOS-MEMS Filters, pp. 110–113.
- Gerosa, A. & Neviani, A. (2004). A low-power decimation filter for a sigma-delta converter based on a power-optimized sinc filter, Vol. 2, pp. II–245–248.
- Hogenauer, E. B. (1981). An Economical Class of Digital Filters for Decimation and Interpolation, *IEEE Transactions on Acoustics, Speech, and Signal Processing* **ASSP-29**(2): 155–162.
- Høvin, M., Olsen, A., Lande, T. S. & Toumazou, C. (1995). Novel second-order Δ -Σ modulator frequency-to-digital converter, *Electronics Letters* **31**(2): 81–82.
- Høvin, M. E., Wisland, D. T., Marienborg, J. T., Lande, T. S. & Berg, Y. (2001). Pattern Noise in the Frequency $\Delta\Sigma$ Modulator, **26**: 75–82.
- Høvin, M., Olsen, A., Lande, T. & Toumazou, C. (1997). Delta-Sigma Modulators Using Frequency-Modulated Intermediate Values, *IEEE J. Solid-State Circuits* **32**(1): 13–22.
- Kaajakari, V., Koskinen, J. & Mattila, T. (2005). Phase noise in capacitively coupled micromechanical oscillators, *Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions* on 52(12): 2322–2331.
- Kaajakari, V., Mattila, T., Oja, A. & Seppa, H. (2004). Nonlinear limits for single-crystal silicon microresonators, *Microelectromechanical Systems*, *Journal of* **13**(5): 715–724.
- Kim, J. & Cho, S. (2006). A Time-Based Analog-to-Digital Converter Using a Multi-Phase Voltage Controlled Oscillator, *Proc. IEEE International Symposium on Circuits and Systems ISCAS* 2006, pp. 3934–3937.
- Kim, J., Jang, T.-K., Yoon, Y.-G. & Cho, S. (2009). Analysis and Design of Voltage-Controlled Oscillator-Based Analog-to-Digital Converter, *IEEE Transactions on Circuits and Systems I: Regular Papers*. Accepted for future publication.
- Michaelsen, J. & Wisland, D. (2008). Towards a Second Order FDSM Analog-to-Digital Converter for Wireless Sensor Network Nodes, *NORCHIP*, 2008., pp. 272–275.
- Nguyen, C.-C. (2005). MEMS Technology for Timing and Frequency Control, Vol. 54, p. 11.
- Norsworthy, S. R., Schreier, R. & Temes, G. C. (1996). Delta-Sigma Data Converters, IEEE Press.

- Qu, H. & Xie, H. (2007). Process Development for CMOS-MEMS Sensors With Robust Electrically Isolated Bulk Silicon Microstructures, *Microelectromechanical Systems*, *Journal of* 16(5): 1152–1161.
- Raghunathan, V., Ganeriwal, S. & Srivastava, M. (2006). Emerging techniques for long lived wireless sensor networks, *IEEE Communications Magazine* **44**(4): 108–114.
- Ramstad, J. E. (2007). System-on-Chip micromechanical vibrating resonator using post-CMOS processing, Master's thesis, University of Oslo, Department of Informatics.
- Ramstad, J. E., Kjelgaard, K. G., Nordboe, B. E. & Soeraasen, O. (2009). RF MEMS front-end resonator, filters, varactors and a switch using a CMOS-MEMS process, pp. 170–175.
- Sauerbrey, J., Tille, T., Schmitt-Landsiedel, D. & Thewes (2002). A 0.7-V MOSFET-only switchedopamp Sigma Delta modulator in standard digital CMOS technology, *IEEE Journal of Solid-State Circuits* 37(12): 1662–1669.
- Schreier, R. & Temes, G. C. (2004). *Understanding Delta-Sigma Data Converters*, Wiley-IEEE Press.
- Senturia, S. (2001). Microsystem Design, Springer Science and Business Media, Inc., chapter 7-10.
- Shao, L., Palaniapan, M., Khine, L. & Tan, W. (2008). Nonlinear behavior of Lamé-mode SOI bulk resonator, pp. 646–650.
- Soeraasen, O. & Ramstad, J. E. (2008). From MEMS Devices to Smart Integrated Systems, Microsystem Technologies, Journal of 14(7): 895–901.
- Sun, C.-M., Wang, C., Tsai, M.-H., Hsieh, H.-S. & Fang, W. (2009). Monolithic integration of capacitive sensors using a double-side CMOS MEMS post process, *Journal of Micromechanics and Microengineering* **19**(1): 15–23.
- Taillefer, C. & Roberts, G. (2007). Delta-Sigma Analog-to-Digital Conversion via Time-Mode Signal Processing, *Proc. IEEE International Symposium on Circuits and Systems ISCAS* 2007, pp. 13–16.
- Vittoz, E., Degrauwe, M. & Bitz, S. (1998). High-Performance Crystal Oscillator Circuits: Theory and Application, *Solid-State Circuits*, *IEEE Journal of* **23**(3): 774–783.
- Wang, A. & Chadrakasan, A. (2005). A 180-mV Subtreshold FFT Processor Using a Minimum Energy Design Methology, *IEEE Journal of Solid-State Circuits* **40**(1): 310–319.
- Wismar, U., Wisland, D. & Andreani, P. (2007). A 0.2V, 7.5μW, 20kHz ΣΔ modulator with 69 dB SNR in 90 nm CMOS, *Proc. ESSCIRC 33rd European Solid State Circuits Conference*, pp. 206–209.
- Wismar, U., Wisland, D. T. & Andreani, P. (2006). A 0.2V 0.44μW Audio Analog to Digital ΣΔ Modulator with 57 fJ/conversion FoM, *Proceedings of the 32nd European Solid-State Circuit Conference*, Switzerland, pp. 187–190.
- Yang, H. & Sarpeshkar, R. (2005). A Time-Based Energy-Efficient Analog-to-Digital Converter, *IEEE J. Solid-State Circuits* **40**(8): 1590–1601.
- Øysted, K. & Wisland, D. (2005). Piezoresistive CMOS-MEMS Pressure Sensor with Ring Oscillator Readout Including Δ - Σ Analog-to-Digital Converter On-chip, *Proc. Custom Integrated Circuits Conference the IEEE 2005*, pp. 511–514.



Wireless Sensor Networks

Edited by

ISBN 978-953-307-325-5 Hard cover, 342 pages Publisher InTech Published online 29, June, 2011 Published in print edition June, 2011

How to reference

In order to correctly reference this scholarly work, feel free to copy and paste the following:

J.A. Michaelsen, J.E. Ramstad, D.T. Wisland and O. Sorasen (2011). Low-power Sensor Interfacing and MEMS for Wireless Sensor Networks, Wireless Sensor Networks, (Ed.), ISBN: 978-953-307-325-5, InTech, Available from: http://www.intechopen.com/books/wireless-sensor-networks/low-power-sensor-interfacing-and-mems-for-wireless-sensor-networks

INTECH

open science | open minds

InTech Europe

University Campus STeP Ri Slavka Krautzeka 83/A 51000 Rijeka, Croatia Phone: +385 (51) 770 447

Fax: +385 (51) 686 166 www.intechopen.com

InTech China

Unit 405, Office Block, Hotel Equatorial Shanghai No.65, Yan An Road (West), Shanghai, 200040, China 中国上海市延安西路65号上海国际贵都大饭店办公楼405单元

Phone: +86-21-62489820 Fax: +86-21-62489821 © 2011 The Author(s). Licensee IntechOpen. This chapter is distributed under the terms of the <u>Creative Commons Attribution-NonCommercial-ShareAlike-3.0 License</u>, which permits use, distribution and reproduction for non-commercial purposes, provided the original is properly cited and derivative works building on this content are distributed under the same license.