Low Power Sequential Circuit Design by Using Priority Encoding and Clock Gating*

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Abstract

This paper presents a state assignment technique called priority encoding, which uses multi-code assignment plus clock gating to reduce power dissipation in sequential circuits. The basic idea is to assign multiple codes to states so as to enable more effective clock gating in the sequential circuit. Practical design examples are studied and simulated by PSPICE. Experimental results demonstrate that the priority encoding technique can result in sizable power saving.

I. Introduction

Synthesis of sequential circuits for low power[1~5] is an area of research that promises to result in large power savings. The sequential circuit design process can be divided into the following steps: (1) State reduction (to minimize the number of state variables); (2) State assignment (to determine the relationship between states); (3) Choice of flip-flops (to determine the state transition diagram by using state variable values); (4) Design of the combinational circuit part (to produce the outputs and next states). State assignment plays an important role in determining the structure and complexity of the resulting finite state machine in terms of the number of nodes required to implement the output and next logic. State assignment also affects the switching activity of the state variables and hence the internal signals in the circuit.

During the low-power design of the combinational circuits; it has been found that blocking the redundant signals and shutting off the redundant parts of the circuit is an effective method to lower the energy dissipation [6]. If some part of the circuit has no effect on the circuit functionality during some time period, then this part is functionally redundant in that period. If the part is made inactive (by cutting off the power supply or by fixing its input signals), then power can be saved. This technique of exploiting redundancy can be applied to combinational logic part of a finite state machine. A sequential circuit is however different from a combinational one in a number of important aspects:

(i) A sequential circuit has flip-flops, which store state signals.

(ii) A sequential circuit receives a special signal called clock, which is used to synchronously trigger the flip-flops.

(iii) States are assigned by encoding the state variables.

We next describe three restraining techniques with respect to each of these aspects.

(i) Traditional flip-flops are single-edge triggered flip-flips (SETFF), which are sensitive to either rising or falling edge of the clock. So half of the clock transitions do not have any impact on the circuit and thereby create redundant behaviors, which in turn results in wasted power dissipation in the flip-flops. For this reason, a double-edge triggered flip-flop (DETFF) can be used, which utilizes both transition edges of the clock, and thereby achieves power saving. [6-8]

(ii) The function of the clock is to force all flip-flips to synchronously change their state (from present state to next state). During this switching process, if the next state of a certain flip-flop is the same as its present state, then this flip-flip will be in a holding mode. The clock's triggering action for this flip-flop becomes redundant and can be masked. Therefore, clock gating technique can be used to lower the power dissipation. [9-13]

(iii) During state assignment, k state variables are used to express 2^k different states. However, if the number of functional states l is not equal to 2^k, i.e., $l \le 2^k$, then there will exist $(2^k - l)$ redundant states. These redundant states can be beneficial in reducing the complexity of the combinational circuit, but reliability of the circuit may be adversely affected. We must consider the system behavior if it enters one of these redundant

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states and make the system self-corrective. Theoretically, there should be a technique for avoiding the redundant states, which also saves power dissipation. We have however not found any work on this subject.

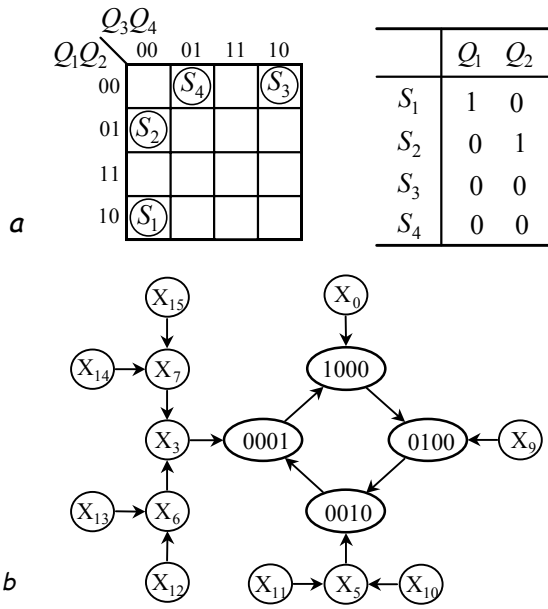
This paper proposes a priority encoding technique to eliminate any unused state code. The result is that some states do not require binary assignment of all state variables. When the system is in such a state, the unused state variables become redundant. Because the corresponding flip-flop outputs are not used, these flip-flops can be isolated from the clock to reduce their power dissipation.

The paper is organized as follows. In the next section we present the design principle of multi-code state assignment by using priority encoding. A practical example of ring counter will be presented to show that restraining redundant states can lead to power saving. In section III, we take two sequential circuits in common use as examples to describe the effect of the number of redundant states and the state probabilities on the multi-code state assignment. Section IV is dedicated to the conclusions.

II. Priority encoding by using redundant states

In combinational circuit design, the existence of redundant states is helpful in generating a large prime implicant during Boolean function minimization. If the implicant contains 2^m minterms, a maximum of m variables may be eliminated from the product-form. If we use k state variables to express l different states ($l \le 2^k$), there will be $(2^k - l)$ redundant states. These redundant states may be utilized to make some states multi-coded e.g., two-coded, four-coded, etc. These state assignments give rise to large implicants during combinational circuit optimization, thus reducing the complexity of the combination circuit implementation.

An example of sequential circuit with a lot of redundant states is the **one-hot ring counter**, where each state corresponds to a state variable. Take the four-state (S_1, S_2, S_3, S_4) counter as an example. Fig. 1(a) shows the state assignment Karnaugh map and the state assignment table of the four states corresponding to state variables (S_1, S_2, S_3, S_4). Notice that each state is encoded by a state variable minterm. The result is a set of twelve $(12 = 2^4 - 4)$ redundant states, which are depicted by empty rooms in Fig. 1(a). Although these redundant states can be used to simplify the excitation functions ($D_1 = Q_4$, $D_2 = Q_1$, $D_3 = Q_2$, $D_4 = Q_3$), the problem is that the design will not be self-corrective. We must change D_1 function to $D_1 = \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3$, to meet this requirement. The complete state diagram of the revised circuit is shown in Fig. 1b. One can easily verify that if the circuit enters one of the invalid states, it will return to the valid working cycle in a period no more than three clock cycles.



	Q_1	Q_2	Q_3	Q_4
S_1	1	0	0	0
S_2	0	1	0	0
S_3	0	0	1	0
S_4	0	0	0	1

Figure 1 Design of a one-hot ring counter

(a) K-map and tabular of state assignment

(b) Complete state diagram of the self-corrective design

We can use these twelve redundant states to realize the multi-code state assignment, as shown in Fig. 2(a). Note that encodings for (S_1, S_2, S_3, S_4) are Q_1, $\overline{Q}_1 Q_2$, $\overline{Q}_1\overline{Q}_2 Q_3$ and $\overline{Q}_1\overline{Q}_2\overline{Q}_3$, hence state variable Q_4 is immaterial and can be omitted. Because state S_4 is encoded by three zero state variables, the ring counter has evolved from a one-hot type to a **one-zero-hot** type.[14] Because we use D flip-flops, $Q_i' = D_i$, hence the next state equations and the excitation functions of the three flip-flops can be derived based on the state table shown in Fig. 2(b):

$$D_1 = \overline{Q_1 + Q_2 + Q_3},\ D_2 = Q_1,\ D_3 = Q_2$$

These equations may be used to realize a ring counter with correct functionality, but without any clock gating. Our goal is however to find a low power (i.e. clock gated) ring counter circuit. To do so, we need to derive the clock-gating functions as discussed next.

In Fig. 2(b) S_1 is four-coded and S_2 is two-coded whereas S_3 and S_4 are uni-coded. We find that Q_1 has the highest priority, which means that when Q_1=1, Q_2 and Q_3 are don't cares. Similarly, Q_2 has the second highest priority because when Q_1=0 and Q_2=1, then Q_3 is don't care. Therefore, in the corresponding circuit, $Q_1 = 1$ can be used to restrain the switching of Q_2 and Q_3, whereas $Q_2 = 1$ can be used to restrain the switching of Q_3. The restraining functions can be realized by a clock-gating technique, as shown in Fig.2(c). The signal for gating the clock signal to the second flip-flop must be D_1, and not Q_1. The reason is that when the clock to

the second flip-flop arrives, $D_1=1$ will force $Q_1=1$, which will subsequently block the clock to the second and third flip-flop immediately. Similarly, we use $D_1=1$ and $D_2=1$ to mask the clock to the third flip-flop as opposed to using Q_1 and Q_2. If delays of the two NOR gates that produce the gated clock signals clk_2 and clk_3 are the same as that of the inverter which produces clk_1, then the three flip-flops will all work synchronously. Notice that the omitted fourth flip-flop is replaced by the NOR gate that produces Q_2.

The circuit of Fig. 2(c) has been simulated by PSPICE. Fig. 3(a) shows waveforms of the clock and the output signals. The three derived clocks clk_1, clk_2, clk_3 are quasi-synchronous. The output waveforms show the circuit functionality is correct.

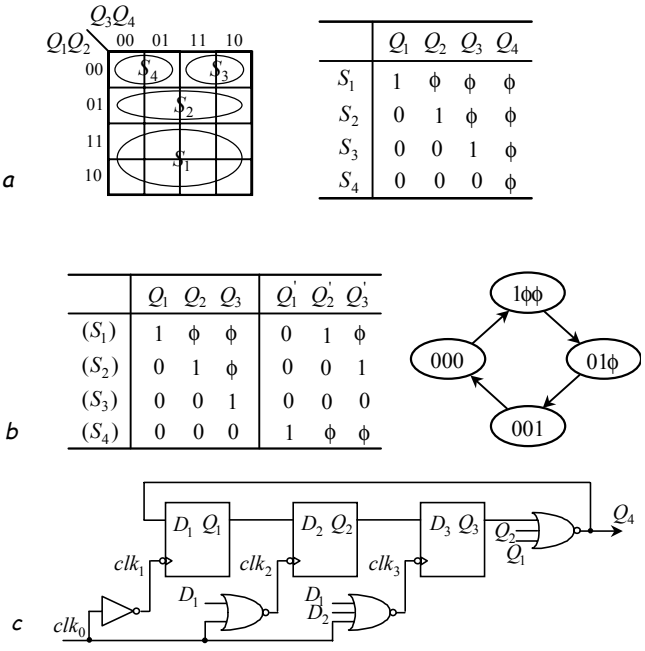


Fig. 2 Design of a one-zero-hot ring counter

(a) Karnaugh-Map and tabular description of state assignment

(b) State table and state diagram

(c) Gated-clock design

Now let's discuss the power dissipation of the new design. The state assignment table in Fig.1(a) shows that the four flip-flops receive 16 triggering actions from the clock in one cycle. However, the state assignment table in Fig. 2(b) shows that the three flip-flops receive only 9 triggering actions from the clock in one cycle. Consequently, the maximum power saving due to reduction of one flip-flop and clock gating is (16-9)/16 = 43%. The energy dissipation curve of the two circuits in Fig. 3(b) show that the power saving is in fact 33%. The disparity is produced because of the energy dissipation in the NOR gates used for gating clock.

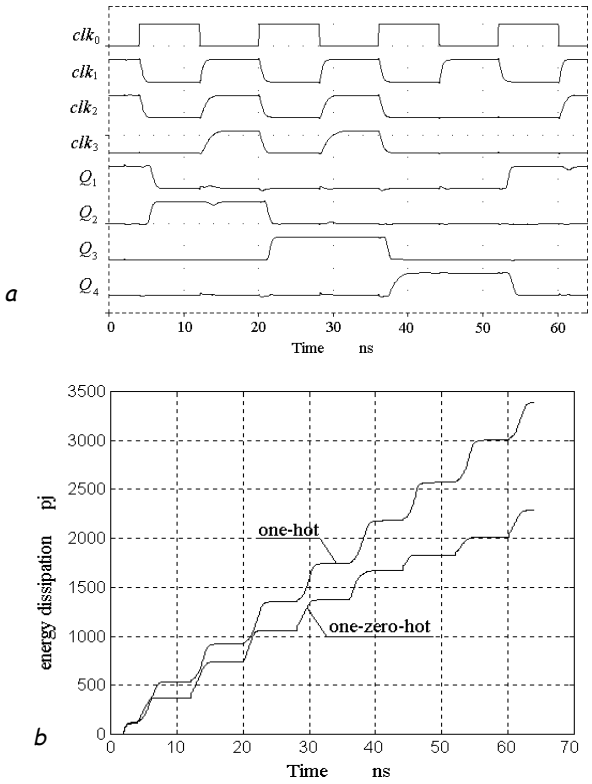


Fig. 3 Simulation of the one-zero-hot ring counter

(a) Clock and signal waveforms

(b) Energy dissipation curves

Finally, it should be pointed out that the design of Fig. 2(c) not only simplifies the circuit realization and saves energy dissipation, but also improves the circuit reliability because it eliminates the unused states. The complete state diagram in Fig. 2(b) shows this advantage.

III. Multi-code state assignment with clock gating

The uni-code state assignment corresponds to a minterm of the state variable space. In contrast, the multi-code state assignment contains 2^m minterms of the state variable space, thereby eliminating 2^m-1 redundant states. In general, we can decompose the set of redundant states into groups of 2^i-1 states and determine the corresponding multi-code state assignments. In the previous section, there were 12 redundant states when using four state variables (Q_1, Q_2, Q_3, Q_4). The non-redundant state assignment in Fig. 2(a) was obtained according to the grouping 7+3+1+1=12. If we used three state variables (Q_1, Q_2, Q_3) instead, then the number of redundant states would be reduced to 4. Since 4 =

3+1, the non-redundant state assignment in Fig. 2(b) would be achieved. Obviously, the inclusion of redundant states increases the complexity of the state assignment procedure. We consider two popular sequential circuits as examples to discuss the state assignment algorithm.

Example 1 Decimal up-counter

In this counter, the counting states (0, 1,…, 9) are encoded with the conventional 8421 BCD encoding, as shown on the leftmost column of Table 1. Notice that there are 6 redundant states: (1010, 1011, 1100, 1101, 1110, 1111).

Table 1: Two encodings of a decimal up-counter

	8421 BCD encoding				Priority-encoding			
digit	D	C	B	A	D	C	B	A
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	0
3	0	0	1	1	0	0	1	1
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	0	1	1	1
8	1	0	0	0	1	ϕ	ϕ	0
9	1	0	0	1	1	ϕ	ϕ	1

From the above table, the excitation functions for the four flip-flops are derived as:

$$D_D = CBA + D\overline{A},$$
$$D_C = C\overline{B} + C\overline{A} + \overline{C}BA, \quad (1)$$
$$D_B = \overline{D}\cdot\overline{B}A + B\overline{A},$$
$$D_A = \overline{A}.$$

We now discuss the priority encoding using six redundant states. Since 6 = 3+3, two states among the ten digits can be four-coded. Analyzing the original 8421BCD state encoding table, states 8 and 9 can be four-coded, as shown on the right side of Table 1. This new scheme maintains the characteristics of the original circuit. When $D=1$, the state variables C and B become don't cares, therefore the priority of D is higher than C and B. In the circuit realization, when the input of flip-flop D is 1, this input can be used to isolate the clock that triggers flip-flops C and B so as to reduce the corresponding energy dissipation. The new excitation functions for the four flip-flops are:

$$D_D = \overline{D}CBA + D\overline{A},$$
$$D_C = \overline{D}C + \overline{D}BA, \quad (2)$$
$$D_B = \overline{D}\cdot\overline{B}A + B\overline{A},$$
$$D_A = \overline{A}.$$

Comparison between eqn.1 and eqn.2 shows that D_B and D_A are the same in both sets. However, in the latter design, a literal $\overline{D}$ is added to D_D and the form of D_C is simplified. The result is that the combinational circuit part is simpler and the power dissipation is lower. As for the energy dissipation of flip-flops, the occurrence probability of each state in any cycle is 10%. From the right part of Table 1, flip-flops C and B are don't cares in states 8 and 9. During a complete 0-9 count, we save 20% of power dissipation for flip-flops B or C. For the same counting cycle, we thus reduce the power dissipation in all four flip-flops by 10%. Note however that the extra clock gating NOR gate results in some energy dissipation.

In the above example, the occurrence probability of each state was the same. In a general sequential circuit, however, steady state probabilities are not the same. To obtain the maximum power saving, we should therefore choose states with higher occurrence probability and multi-encode them first.

Example 2 8421 BCD detector

An 8421 BCD detector receives a serial input T forming a group of four bits (the least significant bit arrives first). When the detector receives a non-8421 BCD group of bits, the output is $R=1$. The state table for the BCD detector after state reduction is shown in Table 2.

Table 2: state of detector

Present state	Next state		Output R	
	$T=0$	$T=1$	$T=0$	$T=1$
A	B	B	0	0
B	C	D	0	0
C	E	F	0	0
D	F	F	0	0
E	A	A	0	0
F	A	A	0	1

A conventional state assignment using state variables (x, y, z) is shown by the conventional encoding column in Table 3. Since the states are all uni-coded, there are two redundant states. From this state assignment, the excitation functions of the three flip-flips and the output function are:

Table 3: state assignment

State	Conventional encoding			Priority encoding		
	x	y	z	x	y	z
A	0	0	0	ϕ	0	0
B	0	0	1	ϕ	0	1
C	1	1	1	1	1	1
D	0	1	1	0	1	1
E	1	1	0	1	1	0
F	0	1	0	0	1	0

$$D_x = \overline{T}xz + \overline{T}\overline{y}z,$$
$$D_y = z,$$
$$D_z = \overline{y},$$
$$R = T\overline{x}y\overline{z}. \quad (3)$$

We now discuss the priority encoding by using the two redundant states. Since 2 = 1+1, two-code assignments for two of the states are possible. To obtain the maximal power saving, the occurrence probabilities of these two states should be as high as possible. Suppose a, b, c, d, e, f are occurrence probabilities of the six states *A*, *B*, *C*, *D*, *E*, *F*, and τ is the probability of input variable $T = 1$. In line with the relationship between the present states and the next states, we obtain the following probability relations:

$$a = e + f$$
$$b = a$$
$$c = b \cdot (1 - \tau) \quad (4)$$
$$d = b \cdot \tau$$
$$e = c \cdot (1 - \tau)$$
$$f = c \cdot \tau + d$$

Take the first equality in eqn.4 as example. From Table 2, we find that the next state will be *A* if and only if the present state is *E* or *F*, thus $a = e + f$ is obtained. Other equalities in eqn.4 are similarly obtained. Due to Eq.(4), we have

$$a = b = c + d = e + f \quad (5)$$

Furthermore, according to the normalization of probability values, we have:

$$a + b + c + d + e + f = 1 \quad (6)$$

So $a = b = 0.25$ are the maximal state probabilities, c, d, e, f have lower state probabilities and are dependent on the probability of input *T*. Therefore we chose states A and B to carry out the two-coded assignments. The priority encoding scheme is shown on the right side of table 3. The state variable *y* represents priority over x, that x is redundant and can be suppressed when $y = 0$. The excitation functions of flip-flops and the output function by using scheme II are as follows:

$$D_x = \overline{T}x + \overline{T}\overline{y}$$
$$D_y = z \quad (7)$$
$$D_z = \overline{y}$$
$$R = T\overline{x}y\overline{z}$$

Compared the above equation with eqn.3, D_y, D_z and R are the same, while D_x is clearly simplified. The result is to reduce the area of combinational circuit as well as the power dissipation. Above all, when the system is in state A or state B, $y = 0$ can be used to isolate the clock that triggers flip-flop x so as to save 50% of the energy dissipation of the flip-flop x. As for all three flip-flops, the total energy saving is about 16.7%.

IV. Conclusions

State assignment of sequential circuits influences the complexity of their combinational circuit realization, to which designers attach a lot of importance. The state assignment also influences the switching behavior of the state variables, and hence the power dissipation in these circuits. Previous research has resulted in low power state assignment that would assign codes with minimum Hamming distances to states with high transition probabilities. This paper in contrast proposed a priority-based state assignment technique that exploits the redundant state codes to mask the clock to some of the flip-flops. Priority encoding thus not only eliminates the redundant state codes, but also improves the finite machine reliability. Three practical design examples were presented to show that this technique is feasible and can significantly reduce the energy dissipation.

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