Low Power, Testable Dual Edge Triggered Flip-Flops

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Abstract

Power dissipation is an important parameter in the design of VLSI circuits, and the clock network is responsible for a substantial part of it (upto 50%). Two main approaches have been suggested to reduce clock dissipation: clock gating and low power flip-flops. In this article we address the latter. We demonstrate that the usage of double edge triggered flip-flops results in a power reduction of 50% in the clock net, and in a reduction of upto 45% inside the flip-flops. Furthermore, we consider other flip-flop parameters, like setup and hold times, propagation delay and testability.

1 Introduction and Motivation

With the growing integration of today's VLSI circuits, power dissipation is gaining importance. Power dissipation is becoming one of the limiting factors for further integration, since high dissipation values lead to high temperatures and reduce the lifetime of integrated circuits (ICs). Furthermore, battery-powered applications require low-energy consuming ICs.

The power dissipation in synchronous VLSI circuits is contributed by several factors: i.e. memory, IO, logic and clock power dissipation. The *memory* power dissipation can be reduced by designing less power consuming memories, and/or by reducing the number of memory accesses of the implemented algorithm [Cha95]. A similar approach must be followed for the *IO* power dissipation. There are many ways to reduce the *logic* power dissipation [Dev95], and this is the field towards most research on low power design is targeted. *Clock* dissipation is divided into three major contributions: that of clock wires, clock buffers and flip-flops. Each of these contributions is described in the following paragraph.

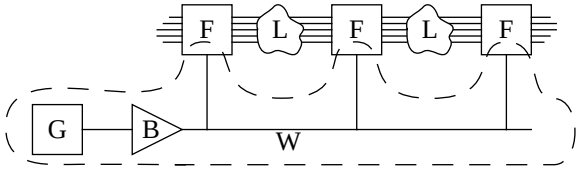

Figure 1: A synchronous digital circuit.

Consider the schematic representation of a synchronous digital circuit as shown in Figure 1. The clock path consists of a clock generator (G), a set of buffers (B), the clock wires (W) and the flip-flops (F). The flip-flops are driven by the combinational logic (L) through the data input and controlled by the clock signal. The total capacitance (C_{clk}) seen by the clock network (dashed part in Figure 1) consists of the clock generator (C_g), the buffers (C_b), the interconnect (C_w) and the input capacitive clock load of the flip-flops (C_l). Figure 2 shows a schematic representation of a flip-flop, containing two paths, a datapath (horizontal arrow) and a clockpath (vertical arrow). Let $C_{ff,clk}$ be the capacitance of the clockpath, and $C_{ff,data}$ that of the datapath.

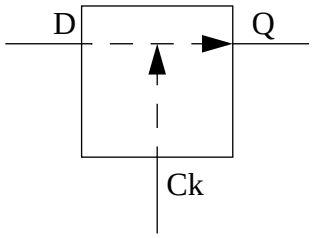

Figure 2: A schematic representation of a flip-flop.

The total power dissipation of the clock network can be computed as follows:

$$P_{clk} = V_{dd}^2 \cdot \{f_{clk} \cdot (C_{clk} + C_{ff,clk}) + f_{data} \cdot C_{ff,data}\} \quad \textbf{(EQ 1)}$$

Here, f_{clk} stands for the clock frequency, and f_{data} for the average data frequency. As it is clear from this equation, one part of the power dissipation is clock dependent, and the other data dependent.

Normally, ICs are based on single edge triggered (SET) flip-flops. However, double edge triggered (DET) flip-flops are attractive to reduce the clock power dissipation [Lu90, Afg91, Gag93 and Hos94]. The following section provides a brief review of different SET and DET flip-flops. In this article we carry out a quantitative assessment of different SET and DET flip-flops in terms of power dissipation, set-up and hold times, propagation delay times and testability. All these evaluations are carried out in Section 3. Finally, in Section 4 we summarize the results and draw conclusions.

2 SET and DET Flip-Flops

The advantages of using edge triggered flip-flops in VLSI

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system design are well known. With this technique the setup time for data inputs is independent of the clock-pulse width, and the circuit implementation is a great deal simpler. A SET flip-flop changes its output on only one of the two clock edges, hence leaving idle a part of the circuit during the remaining clock transitions. On the other hand, a DET flip-flop changes its output at every clock edge. Therefore, the frequency of the clock signal can be halved while maintaining the same data throughput. As will be shown in Section 3, this can lead to a significant reduction in power dissipation.

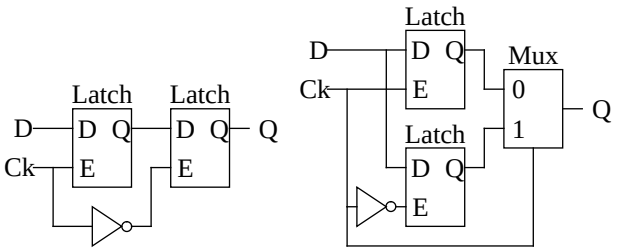

Figure 3: Schematics of a SET and a DET flip-flop.

Figure 3 illustrates the difference between a SET and a DET flip-flop. The former consists of a master and a slave latch serially connected, whereas the latter is based on two parallel connected latches driving the inputs of a multiplexer.

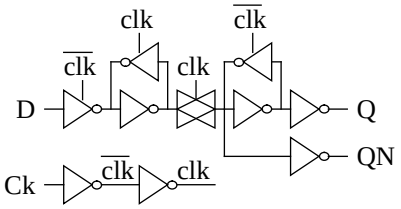

Figure 4: Conventional implementation of a SET flip-flop.

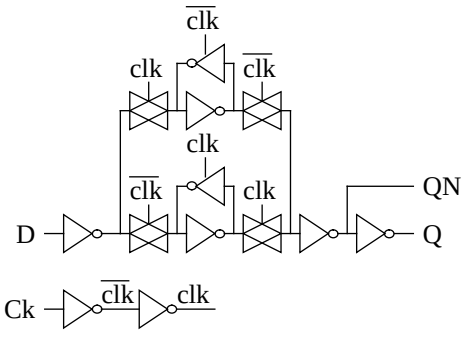

Figure 5: Conventional implementation of a DET flip-flop.

Both dynamic and static implementations of the SET and DET flip-flops have been reported in the literature [Hos94]. However, since the dynamic implementations are more power consuming, we address only the static ones. Figure 4 and 5 show the implementation proposed by [Hos94], after modification of the single n-transistor transmission gates into complementary transmission gates. In this article these implementations will be referred to as SET1 and DET1

However, as will be described in Section 3.4, these implementations suffer from I_{DDQ} testability problems. Improved implementations of the SET and DET flip-flops are illustrated in Figures 6 (SET2) and 7 (DET2). In these configurations, the data transfer between latches is made unidirectional. The unidirectional nature of this transfer improves the I_{DDQ} testability, as well as the performance. These aspects will be discussed in Sections 3.4 and 3.2, respectively.

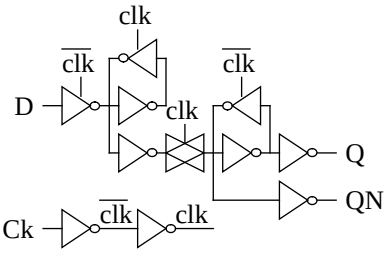

Figure 6: Improved implementation of a SET flip-flop.

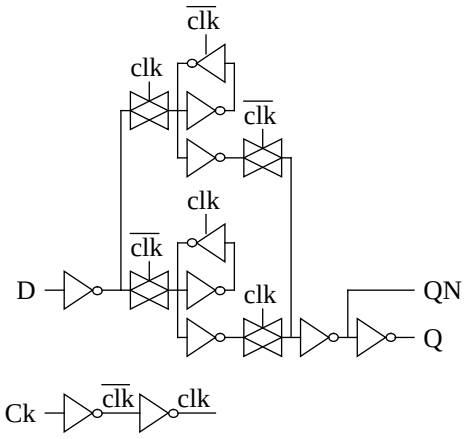

Figure 7: Improved implementation of a DET flip-flop.

3 Performance Parameters

The performance of a flip-flop is determined by its propagation delay, setup and hold times, power dissipation, its ability to withstand the clock skew and its area. In the following subsections we will give a more detailed treatment on these topics. Furthermore, we will also address testability.

3.1 Power Dissipation

As stated before, SET flip-flops change their output only on one of the two clock edges, hence leaving idle a part of the circuit during the remaining clock transitions, although changes do occur in parts of the elements inside the flip-flop. Equation 1 can be rewritten for a SET flip-

flop as:

$$P_{SET,\,clk} = 2f \cdot (E_{clk} + E_{SET,\,clk}) + 2f_{data} \cdot E_{SET,\,data} \quad \textbf{(EQ 2)}$$

Here, f stands for the clock frequency of the SET flip-flop. Furthermore, E_{clk}, $E_{SET,\,clk}$ and $E_{SET,\,data}$ are introduced for simplification of the equation and are equal to $V_{dd}^2 \cdot C_{clk}/2$, $V_{dd}^2 \cdot C_{SET,\,clk}/2$ $V_{dd}^2 \cdot C_{SET,\,data}/2$, respectively. They represent the dissipation of the clock network per clock edge, the dissipation inside the SET flip-flops per clock edge and the dissipation inside the SET flip-flops per data edge, respectively. On the other hand, DET flip-flops change their output at every clock edge. Therefore the clock frequency can be halved while keeping the same data throughput as the SET flip-flops. A similar equation can be written for a DET flip-flop.

$$P_{DET,\,clk} = f \cdot (E_{clk} + E_{DET,\,clk}) + 2f_{data} \cdot E_{DET,\,data} \quad \textbf{(EQ 3)}$$

Here, $E_{DET,\,clk}$ and $E_{DET,\,data}$ represent the dissipation inside the DET flip-flops per clock edge and the dissipation inside the DET flip-flops per data edge, respectively. They are equal to $V_{dd}^2 \cdot C_{DET,\,clk}/2$ and $V_{dd}^2 \cdot C_{DET,\,data}/2$, respectively. In this analysis we assume that the input capacitive clock load (C_l) of the SET flip-flop is equal to that of the DET flip-flop. Since in both flip-flops the clock signal is locally buffered by equal sized inverters, this is a reasonable assumption.

Comparing Equations 2 and 3 leads to the following conclusions. The power dissipation of clock network of a DET flip-flop is equal to the half of that of a SET flip-flop for the same data throughput. Though the total clockpath capacitance inside a DET flip-flop is larger in comparison with that of a SET flip-flop, however, it is (dis)charged at half the rate of that of a SET flip-flop. In order to get a better understanding of the dissipation inside the flip-flops the schematics of the four previously presented (Section 2) flip-flops with no load have been simulated for a 0.5 micron technology using an in-house SPICE-like simulator (PSTAR). All rise and fall times were assumed to be equal to 2 ns. The following table presents the dissipation per clock and data edge of the conventional SET and DET flip-flops (SET1 and DET1) and the improved ones (SET2 and DET2).

	SET1	SET2	DET1	DET2
$E_{ff,clk}$	7.30 fJ	7.30 fJ	7.80 fJ	7.80 fJ
$E_{ff,data}$	13.1 fJ	13.5 fJ	18.2 fJ	19.2 fJ

Table 1: Flip-flop dissipation per clock and data edge.

From Table 1 the following conclusions can be drawn. Firstly, the dissipation per clock and data edge of the DET flip-flops is larger than that of the SET flip-flops. This can be explained due to larger number of transistors in the DET flip-flops. Secondly, comparing the SET1 and SET2 flip-flops. The dissipation per clock edge is the same, which agrees with the fact that both flip-flops have the same amount of clock capacitance. The dissipation per data edge of the SET2 flip-flop is 3% larger, although the number of transistors has been increased by more than 7%. This can be explained by the bidirectional behavior of the transmission gate, in combination with the finite rise and fall times of the clock signals. The gated inverter in the SET1 slave feedback loop (dis)charges a larger capacitance than the same inverter of the SET2 feedback loop, since the capacitance of the master feedback loop is also partially (dis)charged. In the SET2 flip-flop, the unidirectional behavior of the additional inverter reduces this amount of capacitance. Thirdly, comparing the DET1 and DET2 flip-flops. The dissipation per clock edge of the DET flip-flops, analogous to the SET case, is also equal. The dissipation per data edge of the DET2 flip-flop is 5% larger than that of the DET1 flip-flop, in spite of an increase of 13% in transistor count. This can be explained analogously. In the case of the DET1 flip-flop the output multiplexer is realized by two transmission gates. Owing to the bidirectional behavior of the transmission gates in combination with the finite rise and fall times of the clock signals driving these transmission gates, a larger capacitance is (dis)charged at every clock transition. In the DET2 flip-flop, the unidirectional behavior of the gated inverters reduces this amount of capacitance.

Another method to compare the SET and DET flip-flops is to compute the power dissipation as a function of the data activity $alpha = f_{data}/f_{clk}$. While carrying out this comparison, we should bear in mind that DET flip-flops require half the clock frequency in order to maintain the same data throughput. Figure 8 plots the normalized power dissipation for these four flip-flops as a function of the data activity.

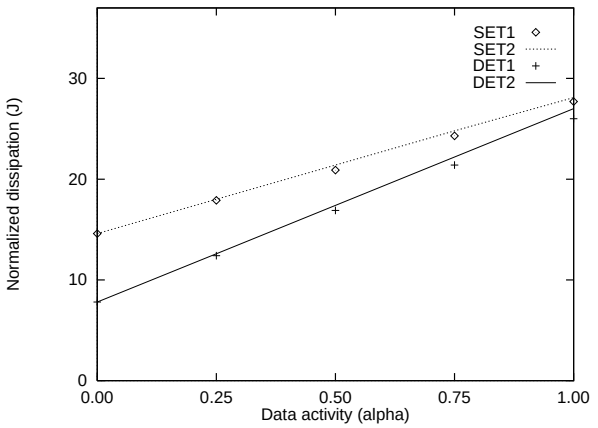

Figure 8: Dissipation as a function of data activity.

From this graph it can be seen that at low data activities ($alpha$ around 0.0) the usage of DET flip-flops results in a flip-flop power saving of 45%. However, at high data activities ($alpha$ around 1.1) there is no appreciable difference in flip-flop power dissipation. Nevertheless one

should remember that in the case of DET flip-flops the dissipation of the clock network is reduced by a a factor of 2, owing to the halved clock frequency.

3.2 Propagation Delay, Setup and Hold Times

The propagation delay of a flip-flop is defined as the elapsed time between the clock signal and the output Q. It is calculated from the time instance when the active edge of the clock reaches $V_{dd}/2$ to the time instance when Q reaches $V_{dd}/2$. The maximum toggle rate of a flip-flop is inversely proportional to its propagation delay. The maximum toggle rate has been determined by connecting the inverted output (QN) to the data input (D), and by increasing the clock frequency till it fails to latch data properly. The computed toggle rates are shown in Table 2.

	SET1	SET2	DET1	DET2
f_{max}	1.33 GHz	1.35 GHz	0.55 GHz	0.51 GHz

Table 2: Maximum toggle rates.

Several conclusions are drawn from these results. Firstly, the SET1 and SET2 flip-flops show comparable toggle rates. The same applies for the DET1 and DET2 flip-flops. The unidirectional behavior of the improved flip-flops compensates the increase in capacitance due to the larger number of transistors. Secondly, the toggle rates of the DET flip-flops are lower in comparison with those of the SET flip-flops. However, in the case of DET flip-flops, the data output switches twice per clock cycle. Therefore, the maximum toggle rates should be multiplied by a factor of two in order to compare them with SET flip-flops. This leads to the following values: 1.10 GHz and 1.02 GHz for the DET1 and DET2, respectively.

The setup time is defined as the time *before* which the data should be stable with respect to the edge of the clock. Similarly, the hold time is defined as the time *after* which the data should be stable with respect to the edge of the clock. For the determination of the setup time, a given flip-flop is initially simulated with relaxed setup time. Subsequently, data is changed successively closer to the active edge of the clock while the output of the flip-flop is kept under observation. At the instance when the output of the flip-flop fails to register the change in input data, the time difference between input data and the clock edge is considered to be its setup time. This time difference is calculated from midpoints ($V_{dd}/2$) of these signals. The hold time of a given flip-flop is also calculated similarly. Initially, the flip-flop is simulated with relaxed hold time. Subsequently, after the active edge of the clock, data is changed successively closer to the active edge while the output of the flip-flop is observed. At the instance when the output of the flip-flop fails to register the change in input data, the time difference between the clock edge and data edge is considered to be its hold time. Table 3 shows the simulated setup and hold times of the SET and DET flip-flops.

	SET1	SET2	DET1	DET2
Setup	0.28 ns	0.26 ns	0.32 ns	0.18 ns
Hold	0.02 ns	-0.09 ns	-0.04 ns	-0.08 ns

Table 3: Setup and hold times.

As illustrated in Table 3, the unidirectional data path within flip-flops improve their setup and hold times. Due to the unidirectionality, the parasitic capacitance in the latch that has to be (dis)charged is reduced significantly. The reduced parasitic capacitance leads to improved setup and hold times. For example, the setup time of the DET flip-flop is improved from 0.32 ns to 0.18 ns and hold time from -0.04 ns to -0.08 ns by the application of unidirectional data path.

3.3 Clock Skew

The ability of a flip-flop to withstand clock-skew is an important parameter in robust, timing insensitive designs. The same reasoning is applicable to SET and DET flip-flops for clock skew. However, for DET flip-flops the high and low parts of a clock cycle should be equal, since the data changes at every clock edge. Therefore, care must be taken to use symmetrical clock buffers while using DET flip-flops.

3.4 Testability

Typical defects in CMOS processes include shorts and opens in conducting layers, gate oxide defects, p-n junction leakage defects, etc. In the modern CMOS processes, the occurrence of open defects is significantly less compared to that of shorts. Shorts or bridging faults are poorly represented by the stuck-at fault model. A class of shorts in flip-flops are not detected by I_{DDQ} testing [Rod94]. Recently [Sac95], I_{DDQ} testable SET flip-flop configurations have been proposed. The basic idea is to make master to slave latch data transfer unidirectional. The unidirectionality is achieved by adding either an extra inverter or a clocked inverter instead of transmission gate. As shown in Sections 3.2 and 3.3, these configurations also have improved data setup and hold times, and can withstand larger clock skew [Sac95].

The I_{DDQ} testing has been widely recognized as the most effective test method in catching defects. Therefore, a similar concept is utilized to make DET flip-flops I_{DDQ} testable as well as to enhance their timing performance. However, DET flip-flops do not have a master-slave arrangement; the output is multiplexed by the clock signal. The I_{DDQ} testability is achieved by making the path from latch outputs to the output multiplexer unidirectional. This can be further explained by Figure 9. The figure illustrates the conventional DET and a short causing the SA fault in the DET. In CMOS technology,

flip-flops are made economically using switches or transmission gates. These switches are alternately closed or opened to ensure the master-slave operation of the flip-flop. The bidirectional nature of transmission gates is the reason why bridging faults in the slave latch are not detected by I_{DDQ} [Sac95]. At the instance of clock transition, a positive regenerative feedback via a pair of back to back inverters allows a fault-free DET flip-flop to ride through this transitory phase.

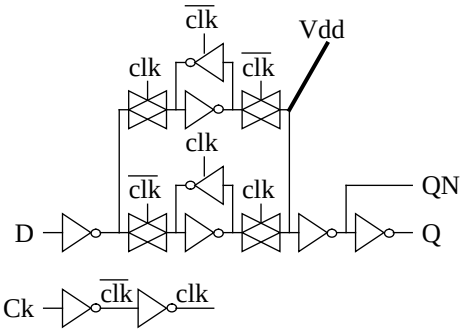

Figure 9: A short to the power supply node.

Due to the bridging the faulty node is constantly driven to V_{dd} (V_{ss}) level. In the case of a low resistive bridging fault, the voltage driving strength through the fault is much stronger than that of the conflicting inverter, and as a result the latch is over-written by this drive. This operation is similar to the Write operation carried out over a SRAM cell. Therefore, in the steady-state condition no current flows and the fault is not detected by the I_{DDQ} test technique. Similarly, there are other bridging faults (e.g. gate oxide defects) in the output drivers that are not detected by I_{DDQ} test technique. The voltage detection of these faults depends on circuit level parameters, fault resistance, *observability conditions*, etc. A detailed discussion on this subject is beyond the scope of this article. An interested reader is referred to [Sac95] for a detailed discussion.

3.5 Area

The number of transistors of the SET and DET flip-flops is shown in the following table.

	SET1	SET2	DET1	DET2
Trans.	26	28	30	34

Table 4: Number of transistors per flip-flop.

As explained in Section 3.4, in order to achieve I_{DDQ} testability data transfer out of the latches requires unidirectionality. Therefore two respectively four extra transistors will be needed per flip-flop. This explains the difference in area between SET1 and SET2 on one hand and DET1 and DET2 on the other. In general DET flip-flops, due to extra multiplexing require more transistors than their SET counterparts. This represents an increment of approximately 15% to 20%. This increment agrees with the reported 17% of [Hos94].

4 Conclusions

In this article several SET and DET flip-flops are presented. A comparison is made between these flip-flops, in terms of power dissipation, propagation delay, setup and hold times, clock skew, area and testability.

The usage of DET flip-flops leads to a reduction of 50% in power dissipation of the clock net, and a reduction of upto 45% in the power dissipation inside the flip-flops. Furthermore, DET flip-flops show similar propagation delay and setup and hold time results in comparison with SET flip-flops. However, the area of DET flip-flops is 15% to 20% larger, and their usage requires symmetrical clock buffers.

Testability is also an important design parameter. The importance of unidirectional data transfer inside the flip-flops is emphasized for performance as well as for I_{DDQ} testing.

5 References

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