Low-Power Wireless Transceiver With 67-nW Differential Pulse-Position Modulation Transmitter

Mika Pulkkinen, *Graduate Student Member, IEEE*, Tuomas Haapala, *Graduate Student Member, IEEE*, Jarno Salomaa, and Kari Halonen, *Member, IEEE*

***Abstract*— This article presents a low-power wireless narrowband (NB) transceiver consisting of a 434-MHz NB transmitter (NBTX) and a 434-MHz NB receiver (NBRX) implemented in 0.18 μm CMOS. The NBTX utilizes differential pulse-position modulation (DPPM) to decrease consumed energy per bit (EPB) by up to 67% compared to on-off keying (OOK). The packet error performance of DPPM with a soft-decision decoding scheme is analyzed. According to the results, the packet error ratio (PER) does not deteriorate compared to OOK except at very low signal-to-noise levels. The lowest power consumption of the NBTX is 8.3 μW when DPPM data is transmitted continuously. Utilizing packet-mode transmission, the average power consumption is 67 nW at a data rate of 4.8 kbps. The transmitted data was received with a PER of 0.1% by a receiver placed at a 30-meter distance from the NBTX. With a higher power consumption of 2.5 μW at the same data rate, the estimated line-of-sight (LOS) uplink range is up to 200 meters. The NBRX is a mixer-first uncertain-IF receiver. A temperature-compensated ring oscillator (TCRO) is utilized as a local oscillator. Its measured deviation of frequency is from +0.1% to –1.2% over a temperature range from –40 to +85 °C. The NBRX utilizes Manchester encoding and the sensitivity is –87 to –82 dBm over the temperature range at a data rate of 40 kbps. The NBRX consumes 85 μW.**

***Index Terms*— Narrowband, transceiver, transmitter, receiver, energy efficiency, Internet of Things, temperature compensation, ring oscillator, uncertain-IF, differential pulse-position modulation, on-off keying, soft-decision, hard-decision.**

I. Introduction

THE modern society is going through a wireless revolution. A connection is embedded in a growing number of wireless objects such as mobile phones, tablets, laptops, car keys, smart watches, fitness trackers, wireless headphones and wireless sensors. These kinds of devices are powered by a battery or an energy harvester that can only provide a limited amount of energy and power. A limited power source combined with high power consumption leads to a reduced operating time and problems such as the frequent need to replace or recharge batteries, or discontinuous operation with harvested energy. The power consumption of the devices should therefore be minimized. In wireless devices, and particularly sensor nodes [1], a significant amount of power can be consumed by radios. Thus, transmitter and receiver solutions with minimal power consumption have been sought.

Numerous narrowband (NB) transmitters with sub-mW power consumption [2]–[9] have been published that could improve the operating time of devices. Such transmitters have typically utilized binary modulations such as on-off keying (OOK), binary frequency-shift keying (BFSK) or binary phase-shift keying (BPSK) that encode one bit per symbol. Due to reduced hardware complexity and low output power requirements, these modulations have enabled low power consumption and a low consumed energy per bit (EPB). Thus, sub-mW NB transmitters have rarely utilized M-ary modulations that encode multiple bits per symbol. They could, however, decrease the EPB even further by decreasing the active time per bit of high-power circuits in the utilized RF front-end. Due to the decreased active time, less energy could be consumed per bit e.g. by carrier generation which typically dominates the total power budget in ultra-low power transmitters [8].

In this work, we utilize a direct-RF OOK transmitter front-end [6] with M-ary differential pulse-position modulation (DPPM) [10], [11] to encode up to 6 bits per transmitted RF pulse. This reduces the active time of the front-end per bit and calculations predict that the EPB and average power consumption decrease by up to 67% and 94%, respectively, compared to OOK. This improvement is also observed in our measurement results. With DPPM, soft-decision decoding [12] can be utilized at the receiver side to improve error performance compared to hard-decision decoding. The error performance with soft-decision decoding is analyzed regarding the transmission of data in small packets. The results suggest that, without increasing the peak output power, DPPM enables a lower packet error ratio (PER) than OOK except at very low signal-to-noise levels. Thus, EPB is improved without deteriorating the error performance.

The implemented narrowband transmitter (NBTX) can be configured to transmit DPPM data in packets with up to 63 symbols per packet. When 6 bits are encoded per symbol and 48-bit packets are transmitted at a rate of 100 packets per second, the average power consumption is 67 nW. In the measurements, the data transmitted in this mode was received

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Mika Pulkkinen, Tuomas Haapala, and Kari Halonen are with the Department of Electronics and Nanoengineering, Aalto University, 02150 Espoo, Finland (e-mail: mika.pulkkinen@aalto.fi; kari.halonen@aalto.fi).

Jarno Salomaa is with Emberion Oy, 02130 Espoo, Finland.

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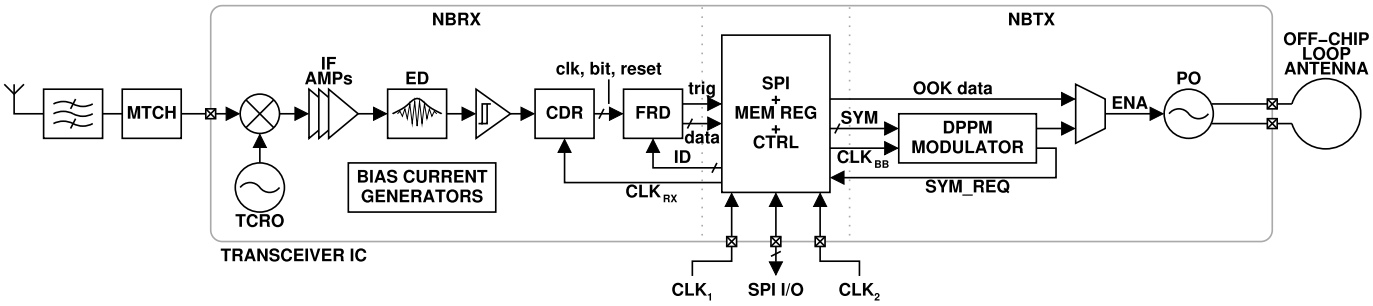

Fig. 1. Block diagram of the transceiver system of this work.

at a distance of 30 meters. With higher power consumption and EPB, the estimated uplink range is 200 meters. When data is transmitted in continuous mode, the lowest average power consumption and EPB are 8.3 μW and 11.6 pJ/bit, respectively.

We also present a mixer-first uncertain-IF [13] narrowband receiver (NBRX). A temperature-compensated ring oscillator (TCRO) is utilized as a local oscillator (LO). Its deviation of frequency is from +0.1% to –1.2% over a temperature range from –40 to +85 °C. Also an on-chip demodulator for a Manchester-encoded signal is included. The receiver consumes 85 μW of power and the sensitivity of the measured unit is from –87 to –82 dBm at a data rate of 40 kbps over the temperature range.

II. Transceiver System

The transceiver of this work is intended to be used in a low-power wireless device for communicating with a base station device. The block diagram of the transceiver system is shown in Fig. 1. The system consists of the NBTX and the NBRX, a serial peripheral interface (SPI), memory registers (MEM REG) and digital control signal generator circuitry (CTRL). The trim bits, transmit data and received data are stored in the MEM REG and are read and written through the SPI. During RF data transmission, the CTRL provides clock, data and other signals to the NBTX and enables transmission of data both continuously and in short packets. In this prototype, transmission of a packet is initiated by giving a trigger command through the SPI. When the signals to the NBTX are disabled, it only consumes a minor standby power. The CTRL gates the CLK_{RX} of the receiver, derived from an off-chip clock CLK_1. The clock and the NBRX bias current generators can be disabled for a low NBRX standby power.

The uplink utilizes M-ary DPPM to reduce the EPB through decreased active time of the transmitter front-end per bit. A low-leakage direct-RF narrowband transmitter front-end [3], [6] is utilized. Due to its low standby power and fast startup, duty cycling and DPPM can be performed efficiently. As DPPM does not require symbol synchronization [11], a stable baseband frequency reference such as a crystal oscillator is not required for transmission. In DPPM, the data is effectively encoded in time intervals between the transmitted RF pulses. A timing reference can be transmitted as a part of the data packet and a receiver can resolve the data by calculating the time delays between the pulses in proportion to the timing reference [14]. This allows for significant variation in the baseband clock frequency and, thus, a low-power ring oscillator could be used to clock the DPPM modulator. DPPM is discussed in more detail in Section III. An OOK transmission mode has also been included. In this test system, the modulators are clocked using an external clock CLK_2.

The downlink utilizes Manchester encoding which enables use of a low-complexity low-power receiver architecture. It also removes the need for an accurate baseband frequency reference at the receiver side. The receiver front-end is based on a mixer-first topology [13]. Placing a passive mixer at the beginning of the signal chain comes with a significant penalty in the noise figure (NF) but removes the need for RF amplifiers which saves a significant amount of power. Using a ring oscillator as the LO, the RF signal can be mixed with a reduced power to an IF signal band for amplification. The temperature sensitivity of frequency, typical to uncompensated ring oscillators, would make the RF signal mix to a band outside of the –3 dB band of the IF amplification chain and deteriorate sensitivity significantly at low and high temperatures. This is avoided by utilizing the TCRO. The amplified IF signal is fed to an envelope detector (ED) whose output is first amplified and then quantized by a comparator with hysteresis.

The comparator output is fed to a digital oversampling clock and data recovery circuit (CDR) that extracts clock and data signals from a Manchester-encoded signal. The CDR was implemented as a digital block as this enables its use with a wide range of data rates simply through adjustment of the frequency of the oversampling clock, CLK_{RX}. With the implemented CDR algorithm, the frequency of the oversampling clock may vary by at least ±20% if the input is an ideal Manchester-encoded signal. The CDR feeds the received bits to a 30-bit shift register (SR) in a communication frame detector (FRD). A valid packet consists of a 14-bit chip identifier (ID) followed by 16 bits of data. The FRD checks if the 14 MSBs in the SR match with a programmable ID. If they do, the 16 LSBs are triggered to the MEM REG after which the data is available to an external controller device.

III. Differential Pulse-Position Modulation

A. Modulation Considerations in Low-Power Transmitters

Among published low-power transmitters, the EPB has been a popular metric for energy efficiency. It has often been reduced by utilizing a binary modulation with a high data

rate [3]–[5], [15]. With binary modulations such as OOK, BPSK and BFSK, one bit is transmitted in one baseband clock cycle $T_{BB} = 1/f_{BB}$. With a high f_{BB} such as 40 MHz as used in [15], the high-power circuits of the transmitter are active only for a short time per bit and the EPB is low. However, increasing f_{BB} comes with a significant drawback – according to the dilation property of Fourier transform [16], signal bandwidth increases directly proportionally to f_{BB}. This assumes that, as T_{BB} is scaled down, the whole baseband signal with any envelope shaping is compressed which also maintains spectral shaping. The signal power is spread over a wider bandwidth and the power spectral density (PSD) of the signal decreases. Thus, increasing f_{BB} decreases the signal-to-noise ratio (SNR), error performance and uplink range. For example, increasing f_{BB} tenfold decreases the SNR by 10 dB.

Increasing f_{BB} may, however, be beneficial if the output power is scaled up by an equal factor to maintain the SNR and uplink range. Transmitter architectures generally consume most power in LO generation and power amplification [1]. Moreover, the carrier generation typically dominates the power budget in ultra-low power transmitters [8]. Increasing both f_{BB} and output power may decrease the EPB if LO power consumption need not be increased. To examine the improvement, let us consider LO and PA power consumption of example transmitters TX1 and TX2 that are capable of equal uplink range. Both of these transmitters use the same binary modulation method and the same RF oscillator whose power consumption is $P_{OSC} = 100\ \mu$W. They transmit one bit per $T_{BB,1} = 10\ \mu$s and $T_{BB,2} = 1\ \mu$s, respectively. The output power of TX1 is 10 μW. Due to tenfold f_{BB} and bandwidth, the output power of TX2 is 100 μW which enables an equal PSD with TX1 and, ideally, an equal uplink range. The PA efficiency is 20% and the PA power consumptions are therefore $P_{PA,1} = 50\ \mu$W and $P_{PA,2} = 500\ \mu$W, respectively. The EPB of TX1 is $\text{EPB}_1 = (P_{OSC} + P_{PA,1}) \cdot T_{BB,1} = 1.5$ nJ/bit. Similarly, we get $\text{EPB}_2 = 0.6$ nJ/bit for TX2. In this case using a high f_{BB} and increased output power enables a lower EPB and is favorable. Here we did not consider the fact that the achieved PA efficiencies are generally higher at higher output powers [1] which could improve the EPB of TX2 even further. Nevertheless, increasing f_{BB} can only be exploited limitedly as bandwidths are in practice regulated by local authorities and a wideband spectrum may violate such standards [1].

In addition to utilizing a high f_{BB}, the EPB may be reduced using an M-ary modulation which, in a similar fashion, effectively decreases the active time of the RF front-end per bit. The high-power RF circuits consume power P_{RF} and are active for T_{BB} per symbol. As each symbol carries B bits, the EPB can be written as

$$EPB = P_{RF} \cdot T_{BB}/B. \tag{1}$$

This suggests that a low EPB can be achieved by deploying a low-power transmitter front-end and by increasing B, i.e. by encoding more bits per symbol. Low P_{RF}, however, requires that the M-ary modulation is such that the RF signal with high B can be generated with low-power circuits. Additionally, the output power requirement of the modulation should be low, i.e. demodulation of the signal should only require a low SNR to achieve a given error performance.

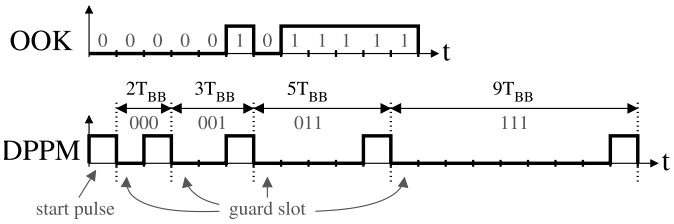

Fig. 2. Examples of OOK and 8-DPPM data packets.

For low P_{RF}, such transmitter architectures can be utilized that minimize the number of high-power blocks. One option is a direct-modulation architecture where the major blocks are a carrier synthesizer, a modulator, and a PA [1], [5]. Another option is a direct-RF power oscillator (PO) topology that consists of two major blocks: a modulator and a PO [1], [3], [6]. These architectures have been popular in published sub-mW narrowband transmitters and have enabled low EPBs. However, binary modulations such as OOK and BFSK have generally been used. For further reduction of the EPB, we propose the use of M-ary DPPM which is compatible with these architectures and enables increasing B.

In DPPM, the data is effectively encoded in time intervals between the transmitted RF pulses. A low-power OOK transmitter front-end can be utilized to generate the pulses. The modulation can be performed using, for instance, a low-power digital block based on a counter [14] and operating at baseband clock frequency f_{BB} that defines the timing of the pulses. According to an analysis given in Section III-C, if a DPPM receiver applies soft-decision decoding [12] and B is sufficiently low, packet error performance with DPPM is better than with OOK except at very low carrier-to-noise levels. Thus, if DPPM is used instead of OOK, the output power need not be increased and low P_{RF} is maintained. By choosing B properly, DPPM enables a lower EPB than OOK without deteriorating the error performance. The average power consumption and average transmitted power with DPPM are significantly lower than with OOK due to a decreased rate of transmitted pulses. Circuit design for high values of B requires mainly only incrementing the word length of the digital modulator. For these benefits, DPPM is a considerable modulation for low-power transmitters.

B. Differential Pulse-Position Modulation

In DPPM, the data is defined by the temporal position of a pulse within a symbol. Alternatively, the data can be considered to be encoded in the time delay between the pulses in two consecutive symbols. B bits are encoded per symbol. When a guard slot is included, a symbol is divided to up to $L_{s,max} = 2^B + 1$ slots. The length of a single slot is one baseband clock cycle, T_{BB}. A DPPM data packet consisting of 3-bit symbols with a guard slot is depicted in Fig. 2. For reference, an OOK packet consisting of the same data is depicted. A DPPM symbol consists of "off" slots and one "on" slot in which an RF pulse is transmitted. The pulse is set

to one of 2^B different slots to indicate which B-bit value the symbol represents. As opposed to PPM, a DPPM symbol ends immediately after the "on" slot. A DPPM data packet consists of N_s symbols and, in practice, there must be one "start" pulse before the first symbol which the timing of the pulse in the first symbol is referenced to. The guard slot helps a receiver to distinguish two consecutive pulses when the shortest symbol (000 when $B = 3$) is transmitted.

Theoretically, there is no limit to how many bits are encoded per symbol. However, this affects the symbol times and average data rate. When a guard slot is utilized, the minimum and maximum symbol time are $T_{s,min} = 2 \cdot T_{BB}$ and $T_{s,max} = L_{s,max} \cdot T_{BB}$, respectively. With equiprobable symbols, the average symbol time is their average:

$$T_{s,avg} = \frac{T_{s,min} + T_{s,max}}{2} = \frac{2^B + 3}{2} \cdot T_{BB}. \tag{2}$$

As B bits are transmitted per symbol, the average data rate is

$$\overline{R_b} = \frac{B}{T_{s,avg}} = \frac{2 \cdot f_{BB} \cdot B}{2^B + 3} \tag{3}$$

when data is transmitted continuously. This is lower than with OOK whose data rate is f_{BB} [bits/s]. With a fixed f_{BB}, the data rate with DPPM e.g. with $B = 4$ and $B = 6$ is 58% and 82% lower than with OOK, respectively.

With OOK, $\frac{1}{2}$ pulses are transmitted per bit on average if bits 0 and 1 are equiprobable. With DPPM, $\frac{1}{B}$ pulses are transmitted per bit regardless of data content when the "start" pulse is neglected. If $B > 2$, a DPPM transmitter transmits less pulses for a given amount of data bits compared to OOK, e.g. 50% and 67% less with $B = 4$ and $B = 6$, respectively. Thus, if most power is consumed for generating the RF pulses, DPPM can significantly decrease the EPB compared to OOK.

Assuming equiprobable bits and symbols, OOK and DPPM transmitters transmit pulses at rates $R_{p,ook} = \frac{1}{2} \cdot f_{BB}$ and $R_{p,dppm} = 1/T_{s,avg} = 2 \cdot f_{BB}/(2^B + 3)$ on average, respectively. Thus, with a given f_{BB}, a DPPM transmitter transmits e.g. 79% and 94% less pulses per second with $B = 4$ and $B = 6$, respectively. If generating the RF pulses consumes the most power, this is the estimated decrement of power consumption with DPPM. It is also an estimate for the decrement of average output power.

C. Soft-Decision DPPM Decoding Error Performance

A lower EPB does not improve the overall performance of a transmitter if it decreases error performance. Although increasing B decreases the EPB with DPPM, it can not be increased arbitrarily as it increases the number of slots in a symbol. This increases the probability that, in a received DPPM signal, the amount of noise and interference in one of the "off" slots exceeds the signal amplitude in the "on" slot which produces a symbol error. To study the effect of white Gaussian noise in the signal band and to compare error performance with OOK, let us calculate the PERs with OOK and DPPM. This PER analysis assumes that a noncoherent narrowband receiver with an envelope detector is utilized to receive the signal [17]. With this assumption, when bit 1 is received, the distribution of the ED output voltage (the probability that output amplitude is r) according to [17] is

$$p_1(r) = \frac{r}{\sigma^2} e^{-(r^2+A^2)/2\sigma^2} I_0\left(\frac{rA}{\sigma^2}\right) \tag{4}$$

where A is the signal envelope, σ is the standard deviation of additive white noise and $I_0(z)$ is the modified Bessel function of the first kind and zeroth order [12], [17]. When bit 0 is received, the distribution of the ED output voltage [17] is

$$p_0(r) = \frac{r}{\sigma^2} e^{-r^2/2\sigma^2}. \tag{5}$$

An OOK receiver samples the ED output once per bit and compares the value to a threshold b_0 to decide whether the bit is 0 or 1. The threshold is ideally set to a value that statistically minimizes the probability of bit 0 being interpreted as 1 or vice versa. For OOK, the BER as given in [17] is

$$BER_{ook} = \frac{1}{2}[1 - Q(\sqrt{2\gamma}, b_0)] + \frac{1}{2} e^{-b_0^2/2}, \tag{6}$$

where $Q(a, b)$ is the Marcum-Q function and $\gamma = A^2/2\sigma^2$ is the average SNR in the ED output while the carrier is being received. $b_0 = \sqrt{2 + \gamma/2}$ is a decent approximation for the optimal threshold at a given γ [12], [17]. When N_b bits are transmitted per packet, the PER with OOK is

$$PER_{ook} = 1 - (1 - BER_{ook})^{N_b}. \tag{7}$$

With DPPM, let us consider a packet-level soft-decision decoding (PL-SDD) scheme. The PL-SDD scheme extends a symbol-level soft-decision decoding scheme discussed e.g. in [12] to decoding one packet at a time. With N_s symbols per packet, a DPPM receiver knows that, with the "start" pulse, $N_O = N_s + 1$ "on" slots are contained in $L_{p,max}$ slots. $N_s = N_b/B$ is the number of symbols per packet and $L_{p,max} = 1 + N_s \cdot L_{s,max} = 1 + N_s \cdot (2^B + 1)$ is the maximum number of slots in a packet. Ideally, a PL-SDD receiver samples the ED output once per slot and stores the amplitudes of $L_{p,max}$ slots. The receiver sets the decision threshold adaptively to the value of the $(N_s + 1)$th highest amplitude among all the slots to limit the number of "on" slots to N_O. At decent SNR levels, it is statistically probable that the (N_s+1)th highest amplitude in the "on" slots is higher than the highest amplitude in the "off" slots produced by noise. As the threshold adapts to the actual received amplitudes within a packet, the PER is improved compared to using a statistically optimum threshold.

The PER with DPPM with the PL-SDD scheme can be derived with probability calculations. Let $\boldsymbol{O}$ and $\boldsymbol{Z}$ be arrays containing the ED output amplitudes corresponding to the "on" and "off" slots, respectively. The numbers of elements in the arrays are N_O and $N_Z = L_{p,max} - N_O$, respectively. A packet error occurs if any element in $\boldsymbol{O}$ is lower than the highest element in $\boldsymbol{Z}$ in which case at least one "off" slot is interpreted as an "on" slot. The PER is

$$PER_{dppm} = \int_0^\infty P(\max\ \boldsymbol{Z} = r) \cdot P(\min\ \boldsymbol{O} \le r)\, dr \tag{8}$$

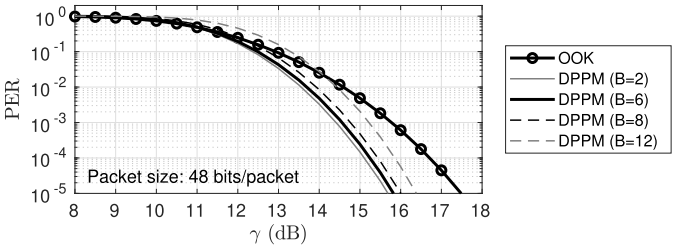

Fig. 3. Packet error ratio with OOK with hard-decision decoding and DPPM with a packet-level soft-decision decoding scheme.

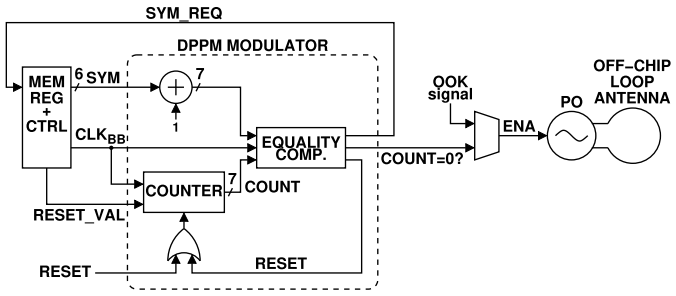

Fig. 4. Block diagram of the NBTX with a detailed DPPM modulator.

where $P(\max\ \boldsymbol{Z} = r)$ is the probability density function of the maximum value in $\boldsymbol{Z}$ and is given by

$$P(\max\ \boldsymbol{Z} = r) = \frac{d}{dr}\left[\int_0^r p_0(r)\ dr\right]^{N_Z}. \tag{9}$$

$P(\min\ \boldsymbol{O} \leq r)$ is the probability that the minimum value in $\boldsymbol{O}$ is less than or equal to r, given by

$$P(\min\ \boldsymbol{O} \leq r) = 1 - \left[1 - \int_0^r p_1(r)\ dr\right]^{N_O}. \tag{10}$$

By substituting (5) and (4) to (9) and (10), respectively, and substituting the results to (8) yields:

$$\begin{aligned} PER_{dppm} &= \int_0^\infty \frac{N_Z r}{\sigma^2} e^{-r^2/2\sigma^2}\left[\int_0^r \frac{r}{\sigma^2} e^{-r^2/2\sigma^2}\ dr\right]^{N_Z-1} \\ &\cdot \left\{1 - \left[1 - \int_0^r \frac{r}{\sigma^2} e^{-(r^2+A^2)/2\sigma^2} I_0\left(\frac{rA}{\sigma^2}\right) dr\right]^{N_O}\right\} dr \end{aligned} \tag{11}$$

In this form, the derivative shown in (9) has been solved.

The result of (11) can be evaluated, for instance, using numerical integration. Fig. 3 shows the PERs with a packet size of $N_b = 48$ bits/packet obtained using (7) and (11) for OOK and DPPM with B values 2, 6, 8 and 12. DPPM with B values up to 8 offers a better PER when γ is greater than 11–12.5 dB. With $B = 12$, γ must be greater than 14 dB for DPPM to outperform OOK. Thus, the results suggest that DPPM with $B \leq 8$ enables a better error performance than OOK at such values of γ that are in any case required for PER $< 10\%$ with OOK. At low values of B, the peak output power requirement does not increase strongly with B which allows for low P_{RF}. Looking at (1), this property makes DPPM a favorable M-ary modulation for EPB reduction.

DPPM offers a better error performance compared to OOK and also a lower EPB and lower power consumption. Also compared to other modulations, use of DPPM is an efficient way to reduce the EPB as it decreases the active time of the transmitter front-end per bit. This decreases the energy consumed per bit by both LO and PA. Additionally, it can be performed with low transmitter complexity. Therefore, DPPM is a good candidate as the modulation method for low-power transmitters. However, some of its shortcomings are that: 1) a PL-SDD DPPM receiver is more complex than an OOK receiver; 2) due to the increased temporal packet length, data rate is lower, a DPPM receiver needs to be active for a longer time per bit and also the probability of occurrence of an interferer is greater; 3) spectral efficiency is lower than with OOK and; 4) noise and interference can produce insertion and deletion errors [19] and one error in a single slot can corrupt data in multiple symbols.

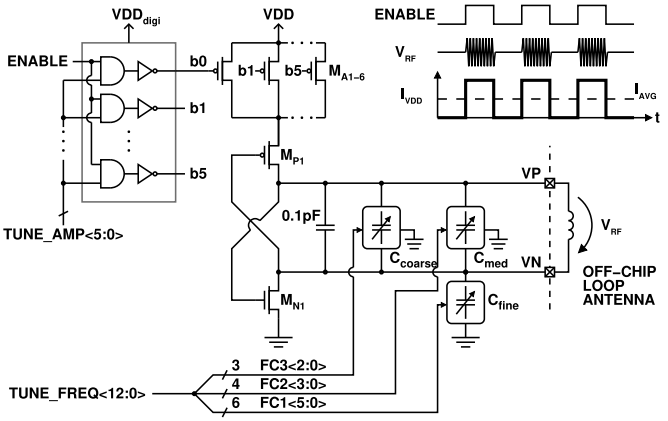

Fig. 5. Schematic of the power oscillator (modified from [6, Fig. 1]).

IV. Narrowband Transmitter

A block diagram of the NBTX is shown in Fig. 4. It consists of a DPPM modulator, a multiplexer for choosing between OOK and DPPM modulation, and a power oscillator (PO). The PO design has been presented earlier in [6]. A carrier frequency of 434 MHz is used for reduced free-space loss [20] compared to, for example, 2.4 GHz used in [3]. The OOK modulator is included in the CTRL block. OOK modulation is performed so that the CTRL feeds data bits one by one, clocked at f_{BB}, to the ENABLE input multiplexer of the PO. DPPM is the primary modulation due to a reduced EPB.

A schematic of the PO is shown in Fig. 5. A current-reusing LC oscillator topology similar to [18] is utilized. Its core is a cross-coupled transistor pair (XCP) i.e. M_{P1} and M_{N1} that is connected to an LC tank. Using a PMOS-NMOS XCP instead of an NMOS-NMOS XCP, less power is consumed to produce a given oscillation amplitude. Setting the ENABLE signal to logic one allows current flow through part of the transistors M_{A1}-M_{A6} as selected using the control word TUNE_AMP. This enables the oscillation. Supply voltage is 1.2 V. The LC tank consists of digitally tunable on-chip capacitors C_{coarse}, C_{med} and C_{fine} and an off-chip copper loop that operates both as the inductor and the TX antenna. The tuning capacitors enable 13-bit tuning of the resonant frequency of the tank.

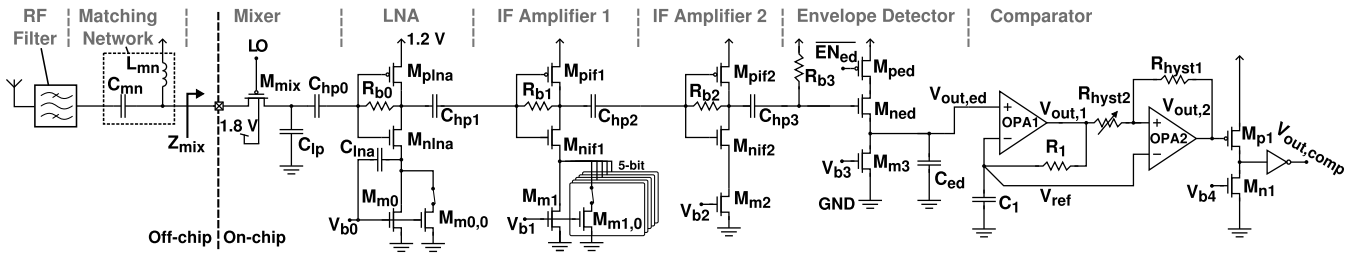

Fig. 6. Receiver front-end.

A more detailed description of the front-end, the capacitors and the antenna is provided in [6].

A functional block diagram of the DPPM modulator is included in Fig. 4. It consists of an adder, a clocked counter and an equality comparator. The modulator enables transmission of DPPM packets as depicted in Fig. 2 with a "start" pulse and up to 63 symbols per packet. The 6-bit symbol SYM and clock signal CLK_{BB} are provided by the CTRL and MEM REG blocks. The number of bits per symbol can be set from $B = 1$ to $B = 6$ utilizing SYM values limited from 0 to 2^B–1. The adder increases the SYM by one to add a guard slot in the symbol. CLK_{BB} is a gated version of an off-chip clock CLK_2. When the transmitter is off, the counter value is at maximum value, 1111111_2, and CLK_{BB} is disabled. Transmission is initiated by enabling the clock signal. At the first rising clock edge, the counter value changes to zero. When the output of the counter is equal to zero, a pulse the length of one CLK_{BB} cycle is output to the ENABLE input of the PO. Simultaneously, a new symbol is requested from the MEM REG. The counter, clocked by CLK_{BB}, counts up until the count is equal to SYM+1 after which the counter is reset to zero, a pulse is output and a new symbol is requested. The amount of transmitted symbols is calculated in the CTRL. When N_s symbols have been transmitted, the CTRL disables CLK_{BB} and gives a signal to reset the counter back to 1111111_2.

The supply voltage of the digital blocks is 1.2 V. The functionality of the DPPM modulator was written in VHDL code that was synthesized and place-and-routed. The block contains 148 standard logic cells and its logic cell core area is 0.002 mm^2. High-Vt digital cells were utilized to reduce standby power. In simulations, the modulator consumes 25 nW and 1.26 μW when the frequency f_{BB} of CLK_{BB} is 100 kHz and 5 MHz, respectively. This is relatively little compared to the PO whose measured active power was 378 μW in [6].

V. Narrowband Receiver

A. Front-End

The implemented receiver front-end, shown in Fig. 6, is based on an envelope-detecting mixer-first topology. The front-end is similar to the implementation presented in [21] but we use a single programmable IF signal chain with a modified low-noise amplifier (LNA) design and push-pull IF amplifiers. The use of just one IF signal chain saves power but comes with a noise penalty. We use push-pull amplifiers rather than common source amplifiers because they provide more gain for the same power. While the use of push-pull stages decreases the linear range of the IF chain, envelope-detecting receivers benefit from relaxed linearity requirements due to the inherent non-linearity of the envelope detection process [13].

The mixer is passive and single-ended. We use a PMOS-type mixer transistor with its n-well biased to 1.8 V. The source–bulk junction of an NMOS-type mixer transistor could become forward-biased in case of a strong input signal, at worst causing a latch-up. Because of non-quadrature mixing, the receiver requires a discrete RF band-pass filter (BPF) that attenuates the mirror frequencies of the input signal band and attenuates LO signal leakage from the single-ended mixer to the RF input. The BPF is also required to considerably improve the selectivity and interference performance of the receiver front-end that is dictated by the transfer function from the BPF input to the ED output, as shown in [13]. The high input impedance of the mixer, Z_{mix}, is translated to 50 Ω by a simple off-chip L-type matching network composed of capacitor C_{mn} and inductor L_{mn}. Due to this impedance conversion from high to low, the matching network offers some voltage gain that counteracts the conversion loss of the passive mixer. The matching network also provides a 1.2-V DC voltage bias for the drain and source of the mixer transistor. The channel resistance of the mixer transistor M_{mix} and the metal-insulator-metal capacitor C_{lp} form a low-pass filter that attenuates high-frequency noise and interference.

The LNA and IF amplifiers are based on a current-biased, single-ended push-pull topology. Capacitors C_{hp0}-C_{hp3} act as high-pass filters and isolate consecutive IF stages at DC. The ED translates the IF signal magnitude into a voltage at its output deploying the non-linearity of transistor M_{ned}. The current source transistors M_{m0}-M_{m3} utilize the voltage biases V_{b0}-V_{b3} generated by separate integrated current mirrors. The current mirrors are separated to suppress a potential feedback path from the IF amplifier chain to the input of the LNA through the current source transistors M_{m0}-M_{m3}. Such feedback could make the amplifier chain unstable. Resistors R_{b0}-R_{b3} provide DC voltage biasing. The gain of the LNA and the first IF amplifier can be adjusted by programmable current sources, with one and 5 tuning bits dedicated to the LNA and the first IF amplifier, respectively. The current-mirror-originated noise at node V_{b0} is attenuated by the negative feedback path composed of transistor M_{m0} and capacitor C_{lna}, which improves the NF of the LNA.

The receiver front-end was simulated post layout. The simulated voltage gain of the passive front-end before the LNA, excluding the BPF, is 13 dB. The LNA has a maximum

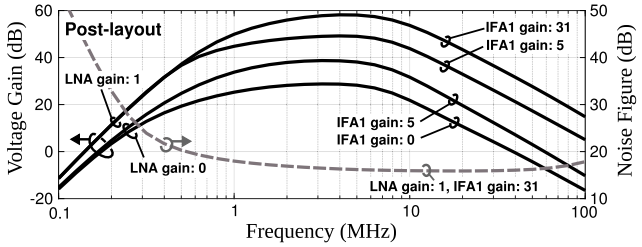

Fig. 7. Simulated gain and NF of the IF amplifier chain.

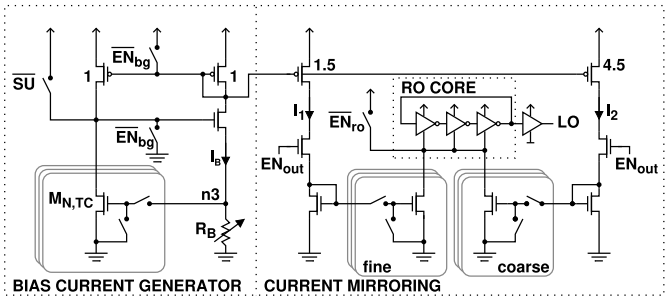

Fig. 8. Schematic of the temperature-compensated ring oscillator.

voltage gain of 22 dB with a corresponding NF of 16 dB and a current drain of 14 μA. Capacitor C_{lna} improves the NF of the LNA by about 6 dB in the middle of its passband. The NF of the full front-end is only 13.5 dB due to the early voltage gain provided by the matching network. The simulated gain and NF of the amplifier chain is presented in Fig. 7, with the NF shown for the maximum gain setting and capacitor C_{hp0} included in the simulation. The total voltage gain of the amplifier chain is tunable from 29 to 58 dB with the maximum tuning step size of 3.5 dB. The -3-dB bandwidth of the IF amplifier chain is sized moderately large, approximately 6.5 MHz, which allows for minor uncertainty in the frequency of the TCRO that generates the LO. Consequently, the front-end follows the uncertain-IF principle. The LNA, IF amplifiers and ED drain 26 μA in total, including the integrated current mirrors that generate the bias voltages V_{b0}–V_{b3}.

The comparator stage consists of differential amplifiers OPA1 and OPA2, a common-source (CS) stage and an inverter. Amplifier OPA1 is connected in negative feedback to buffer and amplify the ED output. The negative input, V_{ref}, is generated by low-pass filtering the amplifier output, $V_{out,1}$, using resistor R_1 and capacitor C_1. V_{ref} also acts as the reference voltage for the comparator, OPA2. For proper operation of the comparator, V_{ref} must settle sufficiently close to the mid-level of the ED output. To allow time for V_{ref} to settle, a received RF data stream must be preceded by a header e.g. a short Manchester-encoded bit array.

Hysteresis is implemented by setting the positive input of OPA2 to a voltage between $V_{out,1}$ and $V_{out,2}$ using voltage division through resistors R_{hyst1} and R_{hyst2}. Resistor R_{hyst1} is 10 MΩ and R_{hyst2} can be set to 0.5, 1 and 2 MΩ to adjust the amount of hysteresis. The tail transistors in OPA1 and OPA2 are biased by voltage V_{b4} that is provided by on-chip bias current generators. OPA1, OPA2 and the CS stage consume 6 μA, 0.5 μA and 1.0 μA, respectively.

B. Temperature-Compensated Ring Oscillator

The TCRO has been implemented by co-designing a bias current generator (BCG) with a tunable temperature coefficient (TC) and current mirroring together with the ring oscillator (RO) core. The schematic is shown in Fig. 8. The RO is current starved with NMOS tail transistors and, with a fixed bias current, its frequency increases with temperature. The positive TC of the RO is canceled out by the negative TC of the BCG that can be adjusted by tuning the width of transistor $M_{N,TC}$. The bias current I_B is adjusted through R_B and can be set to 100, 125 or 150 nA in the nominal corner. I_B is additionally affected by the width of $M_{N,TC}$. Thus, when the width is tuned, also the current mirroring ratio needs to be adjusted to produce the desired output frequency. I_B is mirrored to currents I_1 and I_2 with ratios 1:1.5 and 1:4.5, respectively. Furthermore, I_1 and I_2 are mirrored to the tail transistors of the RO for fine and coarse tuning of the frequency, respectively.

The simulated current consumption of the TCRO including all the blocks in Fig. 8 is 29.7 μA at a frequency of 434 MHz in the nominal corner. The supply voltage is 1.2 V. Due to process variation, a post-fabrication calibration of the output frequency and its TC is required. The frequency must be measured with different widths of $M_{N,TC}$ in at least three temperatures due to the non-linearity of the frequency as a function of temperature. Based on this measurement, an optimal width must be set that minimizes the variation of the output frequency.

C. Back-End

The back-end of the receiver consists of the CDR and FRD. The CDR extracts the clock and data signals from a Manchester-encoded input signal. A similar Manchester decoding algorithm has been presented earlier, for instance, in [22]. In the chosen convention for representing Manchester-encoded data, bits 1 and 0 are represented by 01 and 10, respectively, i.e. by a rising and a falling edge. Fig. 9 shows the signals related to the operation of the CDR at the beginning of reception of a packet. Data bits are shown on line DATA and are clocked by signal CLK. The Manchester-encoded line, comparator output $V_{out,comp}$ in this system, is shown below them with a start sequence. The Manchester signal is sampled to variable s_{new} at the rising edges of an oversampling clock $\mathrm{CLK_{RX}}$ denoted with vertical grey lines. The amount of consecutive identical samples of s_{new} is counted in variable L. The oversampling ratio is $OSR = f_{RX}/f_{CLK}$ where f_{RX} and f_{CLK} are the frequencies of $\mathrm{CLK_{RX}}$ and CLK, respectively. In the figure, OSR is 4.

The CDR algorithm is based on detecting a key feature in the Manchester signal: when DATA changes state to A, the Manchester signal is $\neg A$ for one whole cycle of CLK. As a result, L grows larger compared to when DATA remains unchanged. L is compared to a programmable threshold value L_{th}, 4 in this case. When L reaches L_{th} and s_{new} toggles,

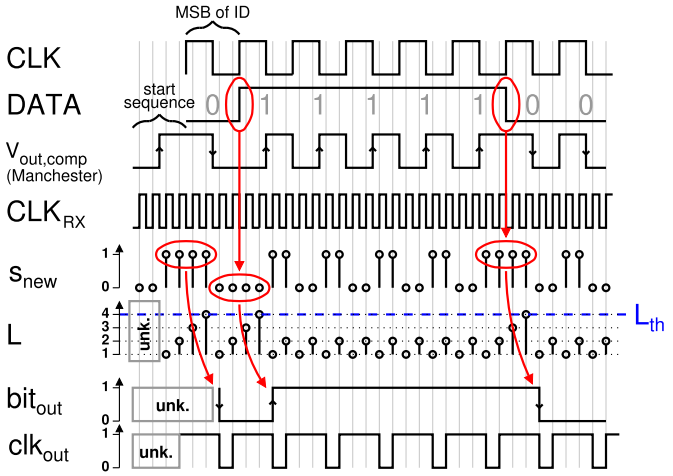

Fig. 9. Examples of clock and data signals, corresponding ideal Manchester-encoded signal (comparator output) and signals relevant to the operation of the CDR at the start of reception of a packet. (unk. = unknown state).

bit_{out} is changed to the new value of s_{new}. The value of DATA remains the same until the next time L reaches L_{th}. Until that time, a rising edge is generated on line clk_{out} every time s_{new} changes state to bit_{out}.

To produce a transition of bit_{out} to the value of the first bit in a packet (i.e. the MSB of the ID), a packet must be preceded by a start sequence. To make L reach L_{th} by the middle of this first bit, the first half of the Manchester signal must be extended. Additionally, to reset L to 1 before this, this extended period must be preceded by a short period where the Manchester line is at the opposite value. Thus, in the case of the first bit, bits 0 and 1 need to be preceded by sequence 01 and 10, respectively. The timing of the start sequence could be varied depending on f_{RX} and L_{th}. However, as a transmitter may not know these values, a valid timing can be produced by using an inverted MSB of the ID as the start sequence.

The FRD is functionally a 30-bit shift register with some additional logic. The first register is the LSB register and its data input is bit_{out}. The registers are clocked at the rising edges of clk_{out}. The 14 MSBs of the SR are compared with the programmable 14-bit ID received from the memory registers. When the 14 MSBs match with the ID, the payload in the 16 LSBs is triggered to the memory register. Simultaneously, the SR is reset to zero as a precaution. Noise and interference in the RF input following the packet can cause toggling of $V_{out,comp}$. Furthermore, this can cause toggling of clk_{out} and bit_{out} and trigger random data to the SR. The reset after triggering the payload prevents the rest of the bit content from being forwarded in the SR and reduces false triggering due to the contents of the packet.

To reduce false ID matches when data is not received, a reset-if-short feature has been added: the CDR gives a reset signal to the FRD if s_{new} changes state and L is only 1. This way, with a fully random input to the CDR, the SR is reset to zero once in eight CLK_{RX} cycles on average. This is relatively often compared to the full length of a packet which is $30 \cdot OSR$ cycles of CLK_{RX}, for example, 120 cycles with $OSR = 4$. Thus, bits randomly triggered to the SR reach the 14 MSBs less frequently and the probability of a false ID match is decreased. However, because the comparator has hysteresis, s_{new} may toggle sparsely in the presence of noise-only RF input to the system. Therefore, a feature could be added that resets the SR also if s_{new} remains at the same value for longer than expected. Errors due to random input could additionally be reduced by adding a means for error detection such as parity bits, and by preventing triggering of data to the memory register in case of erroneous data. Because of the reset-if-short feature, OSR must be at least 4 so that two rising CLK_{RX} edges are produced per half a cycle of CLK. This avoids unintended resetting of the SR during reception.

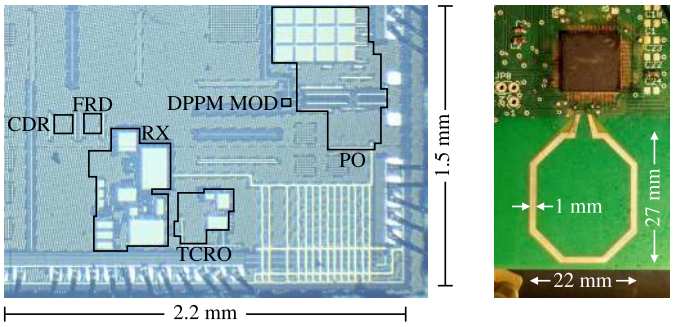

Fig. 10. Micrograph of the implemented blocks (left) and packaged chip with the off-chip loop antenna (right).

For a given value of L_{th}, the algorithm accepts a wide range of CLK_{RX} frequencies. The frequency must be greater than $L_{th} \cdot f_{CLK}$ and less than $2 \cdot (L_{th} - 1) \cdot f_{CLK}$. If the frequency is too low, L does not reach L_{th} in one cycle of CLK near the transitions of DATA line. If it is too high, L reaches L_{th} in half a cycle of CLK when DATA line does not toggle. According to functional simulations in Questa Sim from Mentor Graphics, with $L_{th} = 4$, f_{RX} can vary by $\pm 20\%$. The allowed variation increases slightly as L_{th} increases. The frequency limits apply to an ideal Manchester-encoded signal where the line changes state exactly at the beginning of a cycle of CLK or in the middle of it. In practice, the receiver front-end and e.g. RF signal envelope shaping affect the timing of the comparator output and the frequency limits.

The functionality of the CDR and FRD were written in VHDL code and they were synthesized and place-and-routed. The CDR and FRD contain 151 and 91 standard logic cells, respectively. High-Vt devices were utilized for lower standby power. With Manchester-encoded input data at 50 kbps, the simulated power consumption in the nominal corner is 0.55 μW with $L_{th} = 4$ and $f_{RX} = 250$ kHz. With $L_{th} = 8$ and $f_{RX} = 500$ kHz, it is 1.00 μW. The combined area of the logic cell cores is 0.02 mm^2.

VI. Narrowband Transmitter Measurements

Fig. 10 shows a micrograph of the NBTX and NBRX blocks on the left and a QFN100-packaged chip with the off-chip loop antenna on the right. The areas of the receiver with the TCRO and the transmitter including the modulator and demodulator blocks are 0.35 mm^2 and 0.34 mm^2, respectively. The following measurements have been performed in room temperature unless otherwise mentioned.

For NBTX measurements the amplitude tuning word of the PO was set to TUNE_AMP = 001000_2, less than maximum,

for reduced power consumption. The standby currents of the PO and the DPPM modulator are 1.0 nA and 0.2 nA, respectively.

A. Output Power

As the PO directly drives the loop antenna and does not have a 50 Ω output, the output power of the transmitter was estimated by performing link measurements. The NBTX was set to generate the carrier wave continuously and the power received by a $\lambda/4$ whip antenna was measured using a spectrum analyzer. The received power is affected by reflections. Thus, the measurement was repeated 105 times at several distances between 19 to 24 meters to obtain an estimate for the output power by averaging. The RX antenna was connected to a spectrum analyzer whose resolution bandwidth was set to 10 kHz. The received power values ranged from –89.9 to –72.5 dBm. The power of the radiated carrier, $P_{c,rad}$, was estimated using equation [6, eq. (1)]:

$$P_{c,rad} = P_r - G_r - D_t + FSPL + L_r. \tag{12}$$

P_r is the power delivered to the spectrum analyzer. $G_r \approx 2.0$ dBi is the simulated gain of a receiving $\lambda/4$ monopole antenna without a groundplane. $D_t \approx 2.4$ dBi is the simulated directivity of the transmitting antenna towards the direction of the receiver. $FSPL$ is the free-space loss [20] as predicted by

$$FSPL\ [dB] = 20 \cdot log_{10}(\frac{4\pi \cdot r}{\lambda}). \tag{13}$$

Here r is the separation of the two antennas and λ is the wavelength. $L_r = 7.1$ dB is the loss at the receiver side i.e. the sum of the measured cable loss, 1.6 dB, and mismatch loss of the utilized receiving antenna, 5.5 dB. The estimates of $P_{c,rad}$ range from –37 to –22 dBm and the average of the estimated powers in watts is $P_{c,rad} = 3.5\ \mu$W. Based on these measurements, the output power of the transmitter is approximately –25 dBm.

B. Frequency Tuning and Supply Sensitivity

The measured frequency tuning range of the PO is 117.1 MHz from 515.7 MHz down to 398.6 MHz. The frequency resolution is less than 120 kHz throughout the tuning range. The tuning characteristics of the frequency are similar to those of the measured unit from an earlier process run that were presented by the authors of this work in [6, Fig. 6–7]. The measured supply sensitivity of the PO is –8.83 kHz/mV in a voltage range from 1.0 to 1.4 V. The frequency change with supply voltage is practically linear in this range.

C. Output Spectrum

Examples of the output spectrum with OOK and DPPM modulated signals are shown in Fig. 11(a) and 11(b) with f_{BB} set to 100 kHz and 5 MHz, respectively. The transmitter was set to transmit OOK and DPPM data continuously with the center frequency tuned to 434 MHz. A receiving $\lambda/4$ whip antenna was placed a few centimeters apart from the on-PCB

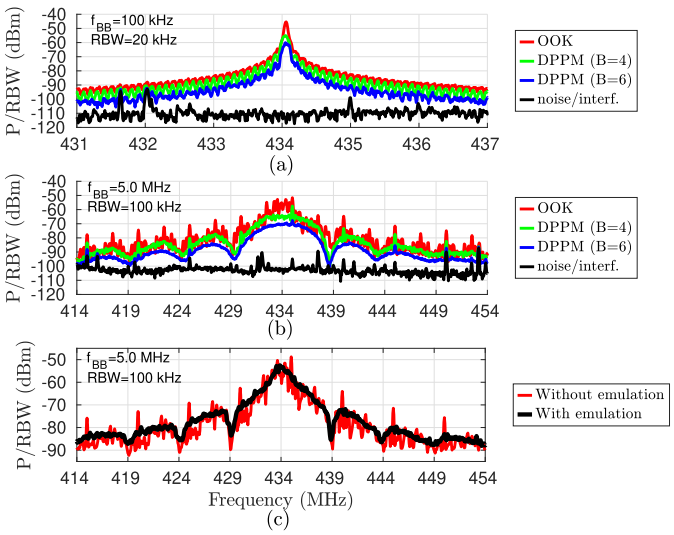

Fig. 11. Examples of narrowband transmitter output spectra in continuous OOK and DPPM transmission modes when baseband clock frequencies are (a) 100 kHz, and (b) 5.0 MHz, plotted with noise floor and local interferers. (c) Output spectrum with OOK-modulated data with and without emulated baseband clock jitter. (RBW: resolution bandwidth).

loop antenna and the spectra were measured using a spectrum analyzer. With a given f_{BB}, the null-to-null bandwidth with both OOK and DPPM is the same. With DPPM, RF pulses are transmitted less frequently and the average output power is lower. This, however, does not imply a lower uplink range – what matters more is the radiated power, $P_{c,rad}$, when the carrier signal is generated, i.e a pulse is transmitted to represent bit 1 in OOK or to designate the start or end time of a symbol in DPPM. The packet error analysis of section III-C predicts that DPPM with $B \leq 8$ enables a better PER than OOK except at low carrier-to-noise levels.

Spikes in the spectra are mainly local interferers and mixing products of the baseband clock at harmonics of f_{BB}. The spikes at multiples of f_{BB} are lowered if the frequency is provided by a ring oscillator or other clock generator with a higher amount of jitter compared to the utilized Keysight 33250A clock generator. This was tested by emulating jitter by rapidly switching the baseband clock frequency f_{BB}, generated by the 33250A, during transmission. Fig. 11(c) shows an example of how the output spectrum improves in the case of OOK modulated data with $f_{BB} = 5.0$ MHz.

D. Current Consumption / Continuous-Mode Transmission

For current measurements, the frequency of the PO was tuned to 434 MHz. The average current consumption of the PO during continous-wave transmission is 230 μA. With OOK or DPPM modulated data, the PO is off part of the time and the current consumption decreases significantly. With OOK modulated data consisting of equal amount of ones and zeros, the average current is 115.6 μA, 116.3 μA and 119.3 μA at data rates of 0.1 Mbps, 1.0 Mbps and 5 Mbps, respectively. These values include the current consumption of the digital amplitude control logic gates in Fig. 5. The corresponding EPBs are 1.39 nJ/bit, 140 pJ/bit and 28.6 pJ/bit, respectively.

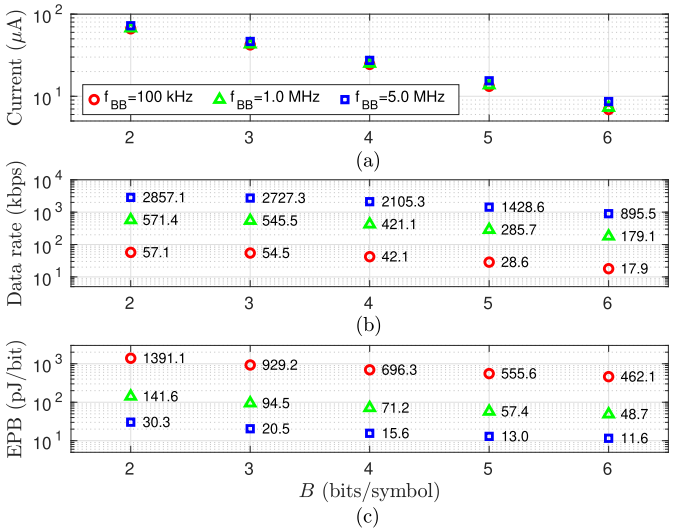

Fig. 12. Narrowband transmitter current consumption, average data rate and average energy per bit as a function of B when DPPM data is transmitted continuously.

With DPPM, the average current is brought even lower and the EPB is improved. The current consumption is plotted in Fig. 12(a). These values include the consumption of the PO, its logic gates and the DPPM modulator. The mean data rates are shown in Fig. 12(b) and are calculated according to (3). EPB values are shown in Fig. 12(c) and are calculated with equation EPB $= V_{DD} \cdot I / \overline{R_b}$. The EPB is lowest, 11.6 pJ/bit, with $f_{BB} = 5$ MHz and $B = 6$. This is 59% lower than with OOK at the same baseband clock frequency, i.e. with the same null-to-null bandwidth. Nevertheless, the transmitted energy per RF pulse is the same and a better PER is enabled with DPPM using a soft-decision decoding DPPM receiver. With a high f_{BB}, the proportion of the EPB consumed by the DPPM modulator starts to be significant as the PO consumes less energy per pulse due to a shorter pulse length. With $f_{BB} = 5$ MHz and $B = 6$, the modulator consumes 1.25 μA of the total current which is 8.63 μA. Therefore reduction of the EPB is lower than 67% that was predicted in section III-B.

Results are also shown for $f_{BB} = 100$ kHz which improves the SNR and uplink range compared to 5 MHz at the cost of the EPB. With this clock frequency, the EPB ranges from 1.39 nJ/bit at $B = 2$ to 462 pJ/bit at $B = 6$. This is up to 67% better than with OOK at the same clock frequency. Thus, the use of DPPM can be beneficial when either low or high bandwidth is available. The current consumption is lowest, 6.9 μA, with $f_{BB} = 100$ kHz and $B = 6$. This is 94% less than with OOK with the same clock frequency. With this f_{BB}, the DPPM modulator consumes a smaller portion of the total current, e.g. 42 nA and 27 nA with $B = 2$ and $B = 6$, respectively. Thus, the decrement of power consumption and EPB match the predictions of section III-B.

E. Current Consumption / Packet-Mode Transmission

The transmitter is intended to be used to transmit data in packets. The average current consumption was measured while the transmitter was triggered to transmit one 48-bit packet every 10 milliseconds. Thus, the data rate was 4.8 kbps. OOK data packets consisted of 50% of ones i.e. 24 RF pulses in total which produces an average current consumption with OOK. With DPPM, B was set to 6 bits and one packet consisted of 9 RF pulses – one for each of the eight 6-bit symbols and one "start" pulse. DPPM symbols were set so that the average symbol time was close to the average, 33.5 clock cycles with $B = 6$ according to (2), which produces an average current consumption with DPPM. With 100 packets per second, 100·24 = 2 400 and 100·9 = 900 pulses are transmitted per second using OOK and DPPM, respectively. With DPPM, the number is constant. With OOK, the number depends on the data and can vary from 0 to 4 800.

TABLE I
MEASURED NBTX PERFORMANCE / PACKET-MODE

Packet Rate Data Rate	100 packets/s 4.8 kbps	
f_{BB}	100 kHz	5 MHz
Average PO Duty Cycle (OOK) Power Consumption (OOK) Energy Per Bit (OOK)	2.4% 6.61 μW 1.38 nJ/bit	0.048% 143 nW 29.8 pJ/bit
PO Duty Cycle (DPPM) Power Consumption (DPPM) Energy Per Bit (DPPM)	0.9% 2.48 μW 0.517 nJ/bit	0.018% 67.1 nW 14.0 pJ/bit
EPB improvement with DPPM	**63%**	**53%**

The packet-mode measurement results are summarized in Table I. The PO duty cycle is calculated by dividing the number of pulses transmitted per second by f_{BB}. With $f_{BB} = 100$ kHz, the use of DPPM decreases the power consumption and EPB by 63% compared to OOK despite the fact that the data rates are equal. With $f_{BB} = 5$ MHz, the power and EPB are decreased by 53%. The energy efficiency improvements are slightly smaller than in continuous-mode transmission as generating the "start" pulse consumes additional energy when data is transmitted in packets. Again, it is notable that the decrement of the EPB achieved through the use of DPPM instead of OOK does not degrade error performance unlike the decrement achieved through increasing f_{BB}.

While the EPB with DPPM is the lowest with $B = 6$, it should be noted that the jitter of the baseband clock will introduce symbol errors [14]. Thus, a reasonable value of B and packet size must be selected based on the jitter of the baseband clock. The smaller the B and packet size, the more jitter is allowed.

F. Other Remarks

In the PO, the off-chip copper loop antenna also acts as the LC tank inductor. Thus, the frequency is sensitive to the surroundings of the copper loop as has been addressed in [2] and [6]. For example, placing a hand near the antenna can shift the frequency by several hundreds of kHz. Unless an effective frequency control loop is utilized to avoid emission in unwanted bands as was done in [2], use of another type of inductor in the LC tank is recommended and the antenna should be separated from the oscillator, for instance, by using a PA stage.

VII. NBTX RADIO LINK MEASUREMENTS

A. Description of the PL-SDD Receiver and Measurement

Line-of-sight (LOS) uplink measurements were performed to verify that the DPPM data transmitted by the NBTX

can be received over a wireless link and to roughly test the maximum uplink range. A PL-SDD DPPM receiver base station (BS) was built using a laptop, a USRP-2901 software defined radio device [23], a 433-MHz SAW filter [24] and an omni-directional +2 dBi $\lambda/4$ monopole antenna for the 433-MHz band. In receive mode, a USRP-2901 downconverts and digitizes the in-phase (I) and quadrature-phase (Q) components of the received signal [25]. Its NF is from 5 to 7 dB [23]. A PL-SDD algorithm was implemented in LabVIEW, a software tool by National Instruments, to extract the received data from the USRP output.

The NBTX was set to transmit randomized 48-bit data packets using DPPM and was configured for minimum energy consumption per bit, i.e. $B = 6$ and $f_{BB} = 5.0$ MHz. Thus, one packet consisted of 8 RF pulses for the 6-bit symbols and one "start" pulse. The LabVIEW program randomized the eight 6-bit data words (i.e. symbols W_1-W_8) and programmed them to the on-chip memory. The maximum packet length was $L_{p,max} = N_s \cdot L_{s,max} + 1 = 8 \cdot 65 + 1 = 521$ slots, i.e. baseband clock cycles. The sampling rate of the USRP was set to $f_s = 15$ MSPS, three times f_{BB}, to enable calculation of the time between the received energy peaks with a higher accuracy. LO frequency was set to $f_{LO} = 431$ MHz and the received signal band was therefore 423.5–438.5 MHz.

An external trigger was used to trigger the USRP to record 20 000 samples of the IQ data. It also triggered an FPGA to send a transmit command to the NBTX through the SPI. The LabVIEW algorithm read the IQ samples and utilized a complex finite impulse response BPF to limit the signal bandwidth to 6 MHz from 431 to 437 MHz. This covers enough of the bandwidth of the DPPM signal and attenuates noise and interference outside of the band. Fig. 13(a) shows examples of the IQ signals after the BPF. After the filtering, the signal energy was computed using equation $E_n = I_n^2 + Q_n^2$ where n is the index of the complex sample. A moving sum filter (MSF) was applied to the signal energy array $\boldsymbol{E}$ using a sliding window of 3 samples which equals the length of the transmitted RF pulse. Fig. 13(b) shows an example of the data after the MSF, corresponding to IQ signals in Fig. 13(a).

The PL-SDD was performed on the output of the MSF in clips of 1 963 samples. The USRP generated three samples per baseband clock cycle and the maximum length of one packet was $3 \cdot L_{p,max} = 1563$ samples. The clip size was set to greater than $3 \cdot L_{p,max}$ so that the clips could be picked iteratively from the 20 000-sample data starting from the first sample in steps of 200 to speed up the processing. In each clip, the algorithm interpreted the 9 highest energy peaks as the RF pulses. In this case a peak refers to a sample whose preceding and following sample have lower energies. The time delays between these peaks were calculated. The received words W_1'-W_8' were derived based on the delays and compared with the transmit data W_1-W_8 to check if a packet had been received correctly.

B. Uplink Measurement Results

The PER was first tested with the distance between the transmitting and receiving antennas set to 10 meters. At the

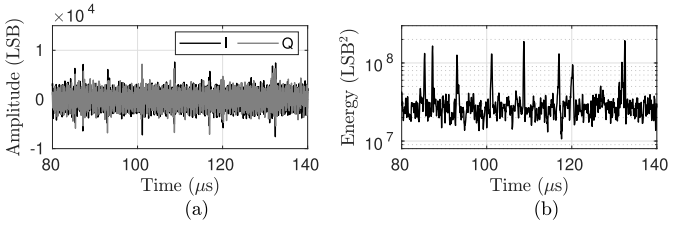

Fig. 13. (a) Received I and Q signals after the complex bandpass filter in a 30-meter link measurement, and (b) corresponding IQ signal energy (output of the moving sum filter). One whole DPPM packet is shown.

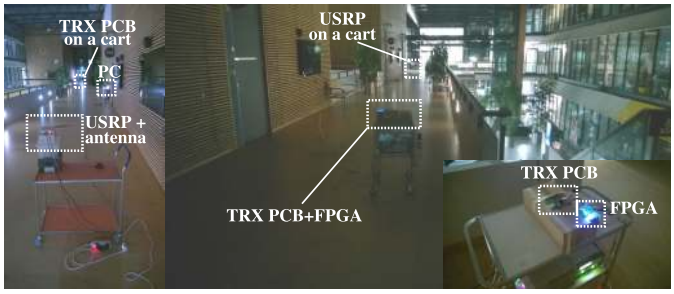

Fig. 14. Measurement setup in the 30-meter radio link measurement with view from the receiver towards the transmitter (left) and the other way around (right). The transceiver PCB with an FPGA on a cart is shown in the bottom right.

output of the MSF, the carrier-to-noise-and-interference ratio (CNIR)[1] was typically 22 to 24 dB which should enable a low PER (see Fig. 3). However, high-power out-of-band interferers appeared occasionally that blocked the DPPM signal and disrupted the IQ signal despite the use of the SAW filter. 40 000 packets were first transmitted and the BS was able to receive and decode the data with a PER of 0.19%. In this measurement, all the errors occurred during the presence of interferers. The effect of out-of-band interferers could be reduced by performing steeper (e.g. analog) bandpass filtering at the receiver before analog-to-digital conversion. To emulate operation without the blockers, the LabVIEW program was changed so that it neglected the received packet if a blocking signal could be detected in the baseband signal and transmission of the packet was performed again. In this measurement, 100 000 packets were received with zero errors. 75 packets were neglected and re-transmitted due to the presence of a blocker.

Additional PER measurements were performed with a 30-meter distance between the antennas. The setup is shown in Fig. 14. CNIR values in the range from 8.2 to 17 dB were observed. The signals of Fig. 13 were obtained in this setup and, in the figure, the CNIR is 8.2 dB. In this measurement, 3 000 packets were transmitted and received with three erroneous packets suggesting that the PER is roughly 0.1%. Analysis of the IQ signals of the received erroneous packets suggests that the errors were induced by noise.

In the 30-meter test setup, signal quality was tested also with $f_{BB} = 100$ kHz which improves the SNR due to decreased bandwidth. The sampling rate of the receiver was maintained at 15 MSPS, the bandwidth of the complex BPF was decreased

[1]Here CNIR refers to the ratio between the energy of unmodulated carrier wave and noise per T_{BB}, estimated from the energy in the "on" and "off" slots in the MSF output.

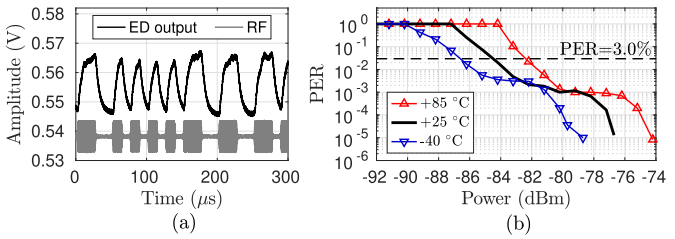

Fig. 15. (a) Envelope detector output with Manchester-encoded RF input signal with average power of −82 dBm. Amplitude of the RF signal is not in scale. (b) Measured packet error ratio of the narrowband receiver with a calibrated TCRO versus average RF signal power with Manchester-encoded input signal.

to 120 kHz and the window size of the MSF was changed to 150 samples (i.e. the length of the RF pulse). In the presence of white Gaussian noise only, noise power is expected to decrease by $10{\cdot}\log_{10}(6\text{ MHz}/120\text{ kHz}) \approx 17$ dB. In the measurement, the CNIR increased by roughly 16 dB which is well in line with the expected decrement of noise. The result suggests that, in this configuration, signal power could decrease by 16 dB for a similar PER performance with the previous 30-meter measurement that was performed with $f_{BB} = 5$ MHz. A 16-dB decrement of power corresponds to the increment of free-space loss when link distance is increased from 30 meters to 200 meters. Thus, it can be estimated that the maximum LOS link distance in this configuration could be as high as 200 meters with a moderate PER performance.

VIII. Narrowband Receiver Measurements

For receiver PER measurements, the LNA and IF amplifier gains and the comparator hysteresis were set to maximum. A Manchester-encoded RF signal was generated at a carrier frequency of 434 MHz using a USRP-2901 and was fed to the RF input of the NBRX through the matching network. The bit rate was 40 kbps and the CDR oversampled the comparator output with a clock frequency $f_{RX} = 380$ kHz with L_{th} set to 8. An example of the ED output with –82 dBm RF input signal power is shown in Fig. 15(a). One packet was fed to the NBRX at a time, followed by a period where the received data was read to a computer through the SPI and compared with randomized data of the RF signal. A 300–μs header consisting of a data bit array 101010101010_2 was added before each packet to allow time for the comparator reference voltage V_{ref} to settle. To reduce premature ID matches due to the consecutive ones and zeros received because of the header, the four MSBs of the ID were always set to 1100_2. The 10 LSBs of the ID were randomized for each packet. The last bit of the header also acted as a start sequence for the CDR.

The measured PER of the receiver is plotted against the average power of the Manchester-encoded RF input signal in Fig. 15(b). The measurement was performed in a temperature chamber in –40, +25 and +85 °C. With IDs 11001010101011_2 and 11001010101010_2, errors were produced with an increased probability. The reason for this could be premature ID matches due to similarity between the ID and the header and the flipping of early header bits which can occur due to an unsettled V_{ref}. One way to reduce these errors is to use parity bits or other mechanism for validating the content of the packet before triggering data to the memory register. Without such mechanism in this system, another way is to modify either the header or the ID to avoid similarity. Errors due to these problematic IDs are neglected in the results of Fig. 15(b). The sensitivity of low-power receivers has commonly been reported at a BER of 0.1%. With 30-bit packets, the corresponding PER is PER = 1-(1-BER)$^{30} \approx 3.0\%$. With a calibrated TCRO, this PER was achieved with RF signal powers from –87 to –82 dBm over the temperature range. The measured power consumption of the receiver including the front-end, its bias current generators, CDR and FRD without the TCRO in this configuration is 43.0 μW.

TABLE II
Comparison of Temperature-Compensated Oscillators

Reference	Frequency [MHz]	Frequency Deviation	Temperature Range [°C]	Power [μW]
[26]	1800	±0.23%	7–62	87
[27]	1250	±5.0%	–40–125	19 800
[28]	2400	–1.0–1.3%†	–40–120	19 200
[29]	24–80	±0.03%	–40–150	359–720‡
[30]	13.56	±0.88%	0–125	6800
[31]	8.05–257.6	–40–50ppm	–40–80	27 000
This work	**431**	**–1.19–0.06%**	**–40–85**	**41.9**

† Approximated based on [28, Fig. 8].
‡ Calculated from values given in [29, Table III]. Minimum supply voltage is assumed here.

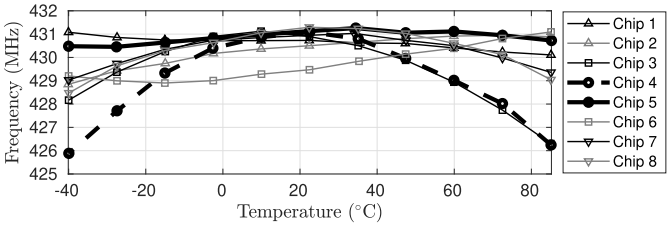

Fig. 16. Measured frequency of the temperature-compensated ring oscillator (TCRO) versus temperature after calibration.

The measured temperature stability of the TCRO after calibration for minimal TC and a maximum frequency of 431 MHz is shown in Fig. 16. Eight chips were measured. The best stability is achieved with chip 5 whose frequency deviation compared to the target frequency of 431 MHz is +0.06% to –0.13%. The worst is achieved with chip 4 whose deviation is +0.02% to –1.19%. The power consumption of the TCRO including the bias current generator, current mirroring and the RO core is 41.9 μW. The phase noise is –72.8, –82.5 and –122.6 dBc/Hz at 100 kHz, 1 MHz and 10 MHz, respectively. Table II summarizes the measured power and frequency stability of this TCRO and existing state-of-the-art.

The acceptable frequency limits of the TCRO are set by the IF amplifier bandwidth. If the RF signal is mixed to a band outside of the IF amplification band, the RF-to-baseband conversion gain is lower and sensitivity degrades. The measured conversion gain of chip 1 is plotted against the LO frequency at different temperatures in Fig. 17 with a Manchester-encoded RF input signal at 434 MHz. The conversion gain reduces with increasing temperature. The total gain reduction is approximately 5 dB at +85 °C with the reduced conversion gain and an LO frequency drop to 426 MHz, as can be seen in Fig. 16. This can be considered

TABLE III
SUMMARY OF MEASURED TRANSCEIVER PERFORMANCE AND COMPARISON

		This work	**[7]**	**[9]**	**[3]**	**[4]**	**[8]**	**[21]**	**[33]**
	Technology	**0.18 μm**	40 nm	65 nm	0.18 μm	0.13 μm	0.13 μm	65 nm	65 nm
	Supply Voltage (V)	**1.2**†	0.5	0.8	0.8–1.0	0.2–0.8	N/A	0.75	0.5
RX	Modulation	**Manchester**	OOK	OOK	-	-	-	OOK/Manch.	OOK
	Freq. Band (MHz)	**434**	315	13.56	-	-	-	2450	2400
	Data Rate (kbps)	**40**	1000	100	-	-	-	650/250	10/50
	Power Cons. (μW)	**84.9**	38	42.5	-	-	-	50	99
	Standby Power (nW)	**5.3**	N/A	N/A	-	-	-	N/A	18
	Sensitivity (dBm)	**–87 to –82**	–55	–72	-	-	-	–71/–88	–97/–92
	Temperature Range	**–40 to +85 °C**	N/A	N/A	-	-	-	N/A	N/A
TX	Modulation	**OOK/DPPM**	OOK	OOK	OOK/FSK	BPSK	BFSK	-	-
	Freq. Band (MHz)	**434**	315	13.56	2400	400	400	-	-
	Data Rate (kbps)	**17.9–5 000**	1 000	100	5 000	20 000	200	-	-
	Power Cons. (μW)‡	$\geq$ **8.3**	52	21	191/374	330	90	-	-
	Standby Power (nW)	**1.5**	N/A	N/A	0.0397	N/A	N/A	-	-
	Output Power (dBm)‡	**–28 (OOK)**	–21 (OOK)	N/A	–29 (OOK)	–15 (BPSK)	–17 (BFSK)	-	-
		–40 (DPPM,B=6)			–26 (FSK)			-	-
	Energy/bit (pJ/bit)‡	$\geq$ **11.6**	52	210	38	16.5	450	-	-
	LOS Uplink Range	**30–200 m**	-	-	-	-	-	-	-

† Additionally 1.8 V bias required by the mixer.
‡ When data is transmitted continuously.

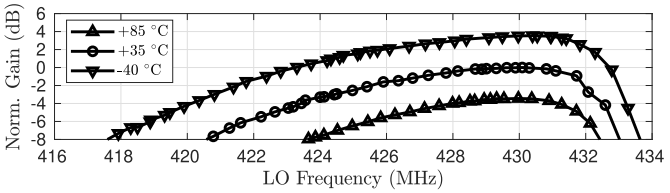

Fig. 17. Measured RF-to-baseband conversion gain of the IF amplifiers and the envelope detector of the receiver versus LO frequency at different temperatures. Gain is normalized so that maximum gain is 0 dB at +35 °C.

as a rough estimate of the worst case sensitivity degradation of the NBRX over the temperature range.

The total power consumption of the receiver with the front-end, TCRO, their bias current generators, CDR and FRD is 84.9 μW. With this level of active power, the NBRX may require duty-cycling in ultra-low power applications. A commercial 6.5 cm^2 photovoltaic array, for instance, may produce only tens of microwatts of power under office illumination [32], a portion of which is consumed by necessary energy harvesting and power management circuitry. The total standby power of the NBRX is 5.3 nW.

IX. CONCLUSION

This article presented a low-power transceiver and discussed the benefits of M-ary DPPM in terms of transmitter energy efficiency. DPPM decreased the transmitter energy consumption per bit by up to 67% compared to OOK. The error performance of DPPM with soft-decision decoding and OOK were analyzed. The results suggest that the use of DPPM instead of OOK does not deteriorate error performance at decent SNR levels when a sufficiently low amount of bits is encoded per symbol. The implemented transmitter consumes 67 nW of power when transmitting DPPM data in packets at a data rate of 4.8 kbps. The data transmitted in this mode was succesfully demodulated by a USRP-based receiver placed at a distance of 30 meters from the transmitter. The on-chip Manchester receiver consumes 84.9 μW and the measured sample showed a sensitivity from –87 to –82 dBm over the temperature range from –40 to +85 °C.

The measured performance of the transceiver is summarized in Table III with transceivers, receivers and transmitters with sub-mW active power consumption. This work shows the lowest transmitter power consumption when modulated data is transmitted continuously. The RX power consumption and sensitivity are well in line with previous works. Among these works, this RX is the only one whose sensitivity was characterized over a wide temperature range.

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Mika Pulkkinen (Graduate Student Member, IEEE) received the B.Sc. degree in electrical engineering from the Aalto University School of Electrical Engineering, Espoo, Finland, and the M.Sc. degree in micro- and nanotechnology from the Aalto University School of Electrical Engineering in 2014. He is currently pursuing the Ph.D. degree with the Electronic Circuit Design Group, Department of Electronics and Nanotechnology, Aalto University. His professional interest includes the design of low-power digital, analog, and RF circuits.

Tuomas Haapala (Graduate Student Member, IEEE) received the M.Sc. degree in biotronics from Aalto University, Espoo, Finland, in 2015, where he is currently pursuing the Ph.D. degree under the supervision of Prof. K. Halonen.

He joined the Department of Electronics and Nanoengineering, Aalto University, in 2011. In 2018, he was a Visiting Ph.D. Student under the supervision of Prof. A. Liscidini at the University of Toronto, Toronto, ON, Canada. His research interest includes low-power analog, digital, and RF circuits for the massive IoT.

Jarno Salomaa received the B.Sc. degree (Hons.) in electrical engineering and the M.Sc. degree (Hons.) in electronics and applications from the Aalto University School of Electrical Engineering, Espoo, Finland, in 2011 and 2012, respectively.

He was with the Electronic Circuit Design Group, Department of Electronics and Nanoengineering, Aalto University, from 2008 to 2019, and held a visiting student researcher position with the Berkeley Wireless Research Center, Department of Electrical Engineering and Computer Sciences, UC Berkeley, in 2016 and 2018. Since 2019, he has been with Emberion Oy, Espoo, as a Principal Engineer. His research interests include the analog and mixed-signal design of sensor circuits and systems, energy harvesting, and power management.

Kari Halonen (Member, IEEE) received the M.Sc. degree in electrical engineering from the Helsinki University of Technology, Finland, in 1982, and the Ph.D. degree in electrical engineering from Katholieke Universiteit Leuven, Belgium, in 1987. Since 1988, he has been with the Electronic Circuit Design Laboratory, Helsinki University of Technology (since 2011 Aalto University). Since 1993, he has been an Associate Professor at the Faculty of Electrical Engineering and Telecommunications, Aalto University, where he has been a Full Professor since 1997. He became the Head of the Electronic Circuit Design Laboratory in 1998. He was appointed as the Head of the Department of Micro and Nano Sciences, Aalto University, from 2007 to 2013. He specializes in CMOS and BiCMOS analog and RF integrated circuits, particularly for telecommunication and sensor applications. He has authored or coauthored over 450 international and national conference and journal publications on analog and RF integrated circuits. He has served as a TPC Member of ESSCIRC and ISSCC. He received the Beatrice Winner Award at the ISSCC Conference 2002. He has been an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, a Guest Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, and the Technical Program Committee Chairman for the European Solid-State Circuits Conference 2000 and 2011.