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Citation: J. Vac. Sci. Technol. B **35**, 01A107 (2017); doi: 10.1116/1.4972870
View online: http://dx.doi.org/10.1116/1.4972870
View Table of Contents: http://avs.scitation.org/toc/jvb/35/1
Published by the American Vacuum Society

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Low-temperature atomic layer deposition-grown Al_2O_3 gate dielectric for GaN/AlGaN/GaN MOS HEMTs: Impact of deposition conditions on interface state density

Milan Ťapajna,[a] Lukáš Válik, Filip Gucmann, Dagmar Gregušová, Karol Fröhlich, Štefan Haščík, and Edmund Dobročka
Institute of Electrical Engineering, Slovak Academy of Sciences, Dúbravská cesta 9, SK-84104 Bratislava, Slovakia

Lajos Tóth and Béla Pécz
Institute of Technical Physics and Materials Sciences, EK MTA, Konkoly T. M. út 29-33, H-1121 Budapest, Hungary

Ján Kuzmík
Institute of Electrical Engineering, Slovak Academy of Sciences, Dúbravská cesta 9, SK-84104 Bratislava, Slovakia

(Received 30 August 2016; accepted 5 December 2016; published 22 December 2016)

The oxide/semiconductor interface state density (D_{it}) in Al_2O_3/AlGaN/GaN metal-oxide-semiconductor high-electron mobility transistor (MOS-HEMT) structures with gate oxides grown by atomic layer deposition at low deposition temperature is analyzed in this work. MOS-HEMT structures with Al_2O_3 gate oxide were deposited at 100 and 300 °C using trimethylaluminum precursor and H_2O and O_3 oxidation agents. The structures were found to show negative net charge at oxide/barrier interface with density (N_{int}) of $10^{13}\,cm^{-2}$, which was attributed to the reduction of barrier surface donor density (N_{DS}). D_{it} was determined using capacitance transient techniques, and the results were assessed by the simulations of the capacitance–voltage characteristics affected by interface traps. The results indicate a lower interface quality of the sample with Al_2O_3 grown using O_3 agent compared to those with H_2O, even though the former provided lowest gate leakage among the analyzed structures. Moreover, to uncover the N_{DS} nature, D_{it} distributions determined here were compared to that reported previously on devices with N_{int} close to zero, i.e., with fully compensated surface barrier polarization charge by N_{DS} [Ťapajna *et al.*, J. Appl. Phys. **116**, 104501 (2014)]. No clear correlation between D_{it} and N_{DS} was concluded, indicating the nature of N_{DS} to be different from that of interface states in the energy range analyzed here. *© 2016 American Vacuum Society.*
[http://dx.doi.org/10.1116/1.4972870]

I. INTRODUCTION

Recently, GaN high-electron mobility transistors (HEMTs) have been considered to replace Si power switching transistors in high-efficiency AC/DC and DC/DC converters due to lower ON-state resistance and superior dynamic properties of the GaN devices.[1–3] For switching devices, enhancement-mode transistors with threshold voltage (V_{th}) as high as $\sim$5 V are often required from the system level.[4] Owing to inherent depletion-mode character of the GaN HEMTs, a great effort has been devoted toward the development of enhancement-mode (or normally-off) devices for switching applications.[1–6] Although several concepts for normally-off GaN HEMTs have been proposed in the literature,[2,5,6] fabrication of such devices with sufficiently high V_{th} ($\sim$5 V) and uncompromised current driving capability (compared to normally-on counterparts) remains a challenge. Application of a metal-oxide-semiconductor (MOS) gate structure in GaN HEMTs (MOS-HEMTs) offers a promising approach to overcome the existing trade-off between V_{th} and output current of the device, providing sufficiently high negative polarization charge ($>1.8\times10^{13}\,cm^{-2}$) is left uncompensated at the oxide/barrier interface.[7–9] In this case, normally-off device operation can be achieved, and, moreover, V_{th} can be increased by oxide thickness (t_{ox}) increasing to a desired value.[8,10,11] However, polarization charge at the barrier surface is fully compensated in most of the cases by the charge referred here to as surface donors, while its origin and nature has not been understood yet.

One of the possibilities to partially suppress the surface donors' formation in GaN MOS-HEMTs is to employ atomic layer deposition (ALD) for growth of the gate dielectric. Recently, Al_2O_3 and HfO_2 grown by ALD at 100 °C provided normally-off operation of InAlN/GaN MOS-HEMT with positive V_{th} shift compared to the reference Schottky-gated structure and V_{th} increase with the increase in t_{ox}.[11] This has been attributed to the reduction of the surface donors' density from 4.5 to about $1\times10^{13}\,cm^{-2}$ as a result of low deposition temperature (T_D) during ALD.[11] It has been proposed by several authors that surface donors are located at or close to oxide/III-N barrier interface.[7–9] Therefore, a possible relationship between N_{DS} and distribution of the oxide/barrier interface traps (D_{it}) represents a relevant question, yet not explored in more detail in the

[a]Electronic mail: milan.tapajna@savba.sk

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literature. In this work, we investigated $D_{it}(E)$ distribution in Al_2O_3/GaN/AlGaN/GaN MOS-HEMT structures with gate oxide grown by ALD. D_{it} distribution was measured on samples with Al_2O_3 deposited at 100 and 300 °C using trimethylaluminum (TMA) precursor and two oxidation agents: H_2O and O_3. First, the structural properties of the processed structures are presented, and the methodology for D_{it} determination using capacitance techniques is discussed. Experimentally determined D_{it} distributions were then compared to that of MOS-HEMTs with fully compensated surface polarization charges reported previously.

II. EXPERIMENTAL PROCEDURES

The Al_2O_3/GaN/AlGaN/GaN MOS-HEMT structures were fabricated on commercial (Cree) GaN/$Al_{0.29}Ga_{0.71}$N/GaN heterostructures (from top 3 nm/17 nm/1.7 μm) grown on 4H-SiC substrate by metal-organic chemical vapor deposition (MOCVD). After Ti/Al/Ni/Au Ohmic contacts evaporation and annealing (850 °C, 1 min), Al_2O_3 gate dielectrics were grown by ALD at 100 and 300 °C using TMA as Al precursor and H_2O as oxidation agent (referred to as H_2O-100 °C and H_2O-300 °C in the following) and at 100 °C using O_3 oxidation agent (O_3-100 °C). For all three sets of samples, Al_2O_3 films with thickness of 10, 20, and 30 nm (nominal thickness) were deposited to allow analysis of the charge distributions in the gate stack. All structures then underwent postdeposition annealing step performed at 400 °C for 15 min. Fabrication of MOS-HEMT structures was accomplished by Ni/Au (40 nm/50 nm) gate evaporation and patterning using optical lithography and lift-off process.

The structural and chemical properties of the prepared dielectric films were studied using high-resolution transmission electron microscopy (HR-TEM) and x-ray photoelectron spectroscopy (XPS) on bare samples with 10-nm thick Al_2O_3 films grown on GaN/AlGaN/GaN heterostructures. The samples underwent similar postdeposition annealing step as to MOS-HEMT devices. For HR-TEM study, specimens embedded in a Ti disk were mechanically ground and polished down to 50 μm, followed by 7 kV Ar^+ ion milling until perforation. JEOL 3010 was used operating at 300 kV with a point resolution of 0.17 nm. XPS measurements were performed using Perkin Elmer PHI 1600 system equipped with a spherical capacitor analyzer and a monochromated AlKα radiation source ($h\nu = 1486.6$ eV) with a 23.5 eV of pass energy. To determine the stoichiometry of the Al_2O_3 films, the O/Al area ratio was calculated from the single peaks deconvoluted from the O1s and Al2p spectra (not shown in detail). The O/Al ratio ranges from 1.7 to 1.9 (as summarized in Table I), that is, slightly higher compared to stoichiometric Al_2O_3 (1.5). Similar values have been reported in the literature for thin Al_2O_3 films oxide that was attributed to excess of O atoms close to the surface.[12] X-ray reflectivity (XRR)[13] was used for oxide thickness (t_{ox}) measurement using Al_2O_3 layers deposited on commercial SiO_2/Si substrates in the same run as MOS-HEMT devices. For XRR measurements, Bruker AXS-D8 Discover equipment with Cu Kα radiation generated by an x-ray tube with a rotating anode operating at 12 kW was used.

Table I. Summary of Al_2O_3 films thickness measured by HR-TEM (10-nm thick films only) and XRR, static dielectric constant extracted from the *CV* measurements, and O/Al ratio determined from the XPS analysis.

	Al_2O_3 thickness (nm)					
	Nominal					
	10		20	30		
	HR-TEM[a]	XRR			ε_{ox}[b]	O/Al ratio[a]
O_3-100 °C	9.0	9.4	23.1	34.3	9.6	1.86
H_2O-100 °C	12.0	11.3	22.0	32.9	9.6	1.94
H_2O-300 °C	11.5	11.4	22.9	33.7	8.3	1.72

[a]Determined on bare Al_2O_3 films deposited on GaN/AlGaN/GaN heterostructure using the same conditions as for the MOS-HEMT devices.
[b]Extracted from the dependence of total capacitance of MOS-HEMT structure as a function of Al_2O_3 thickness.

DC current–voltage (*IV*), capacitance–voltage (*CV*), and capacitance transients of MOS HEMT devices were performed on circular diode structures with diameter of 80 μm. All the capacitance measurements were performed using AC signal with an amplitude of 30 mV and a frequency of 100 kHz. As will be discussed in Sec. III D, all three set of samples showed reduced N_{DS} by about 50% compared to full compensation of the surface polarization charge, resulting in the oxide/barrier net charge density (N_{int}) ranging from -1.1 to -1.2×10^{13} cm^{-2} (see Table II). Note that for fully compensated surface polarization charge by N_{DS}, the net charge N_{int} tends to be close to zero.[7–9,14]

D_{it} distribution was determined on MOS-HEMT structures with $t_{ox} = 10$ nm only, as it is expected to be independent of t_{ox}. Two complementary techniques were used: (1) D_{it} in the energy range of E_C-$E = 0.5$–1.0 eV was determined using V_{th}-transients, deduced from the capacitance transients measured at $V_g \approx V_{th} - 0.5$ V at temperatures of 25, 75, and 125 °C. Only relative change (ΔV_{th}) between V_{th} transients measured after "filling" pulse $V_F = 0$ (no filling) and $V_F = 1.5$ V (interface traps filling) was used for D_{it} determination, to cancel out possible bulk trapping process (i.e., V_{th} drift) previously discussed in Ref. 15. $D_{it}(E)$ was determined from the time derivative of ΔV_{th}-t. (2) Filtered light-assisted V_{th} transient technique was used to determine D_{it} distribution of very deep interface states in the range of 1.75–3.25 eV below E_C. Here, the difference between V_{th} transient measured in the dark and after light exposure was taken into account. The light from the broad-band Xe-lamp (SP, ASB-XE-175) was filtered using band-pass metal interference filters with FWHM spectral transmittance ranging from 17.5 to 5 nm for light energy of 1.75 to 3.25 eV, respectively. In contrast to Ref. 15, the light was exposed 50 s after beginning of the transient and kept exposed until the termination of the measurement. Finally, the *C-V* curves of the MOS-HEMT structures were calculated using a numerical solver of the one-dimensional Poisson equation with the Shockley–Read–Hall statistics

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TABLE II. Summary of V_{th}-t_{ox} slopes extracted from the *C-V* measurements on set of MOS-HEMT structures with $t_{ox} = 10$, 20, and 30 nm, together with resulting Q_{eff}. Also listed are polarization charge in the quantum well, P_{QW}, net charge density at Al_2O_3/barrier interface, N_{int}, metal/Al_2O_3 SBH, and position of Fermi level in the equilibrium ($V_g = 0$ V) $E_{F,0}$ in respect to the bottom of the GaN-cap conduction band.

Sample	V_{th}-t_{ox} slope (V/cm)	Q_{eff}/q (cm^{-2})	P_{QW}/q (cm^{-2})	N_{int} (cm^{-2})	SBH (eV)	E_C-$E_{F,0}$ (eV)
O_3-100 °C	−0.035	1.34×10^{12}	1.27×10^{13}	-1.14×10^{13}	3.55	1.85
H_2O-100 °C	−0.025	1.09×10^{12}		-1.16×10^{13}	3.45	1.75
H_2O-300 °C	−0.011	8.0×10^{11}		-1.22×10^{13}	3.3	2.0

accounting for the interface traps response, taking the measurement time into account.[16]

III. RESULTS AND DISCUSSION

A. Structural analysis

Cross-sectional HR-TEM images of samples with 10-nm thick Al_2O_3 deposited by different ALD conditions on GaN/AlGaN/GaN heterostructures are depicted in Figs. 1(a)–1(c). Atomically flat interface between Al_2O_3 and III-N semiconductor can be inferred for all three samples. H_2O-300 °C sample [Fig. 1(b)] shows notably smoother Al_2O_3 surface compared to films grown at 100 °C [Figs. 1(a) and 1(c)]. The Al_2O_3 thicknesses (t_{ox}) measured by HR-TEM and XRR techniques are summarized in Table I. Similar t_{ox} (within the experimental error) was obtained from HR-TEM and XRR analyses for oxide films with nominal thickness of 10 nm grown on AlGaN/GaN and SiO_2/Si substrates, respectively. Therefore, t_{ox} determined from the XRR measurement on all sets of samples was considered in the analysis described below. The barrier thickness (comprised of the GaN-cap and AlGaN layers) was found to be about 19 nm, in agreement with the nominal thickness.

Interestingly, despite low deposition temperature, all Al_2O_3 films were found to have polycrystalline structure with the mean grain size of 15–20 nm. Most of the crystal grains are well oriented to the GaN substrate with a face centered cubic structure (a = 0.79 nm). However, the crystallinity of the Al_2O_3 films needs to be confirmed by the x-ray diffraction that is currently under investigation. It is worth mentioning that to avoid artifacts, special care was taken during the thinning procedure by using low temperature glue (>100 °C) and the ion bombardment with a decreased ion energy of 7 kV (instead of standard 10 kV). Crystallization of the ALD layers due to possible heating of electron beam during the TEM observation is unlikely in the experimental conditions used here.

B. I-V and C-V measurements

Figure 2(a) shows typical *I-V* characteristics of MOS-HEMT structures with $t_{ox} = 10$ nm. Sample O_3-100 °C shows lowest gate leakage (I_g) of $\sim 10^{-5}$ A/cm^2 at $V_g = -5$ V, while it increases for devices with ALD-grown Al_2O_3 using H_2O to $\sim 10^{-3}$ A/cm^2 at $V_g = -5$ V. At positive V_g-s, a sharp increase in I_g can be observed. To understand this behavior, *I-V* measurements at different temperatures were performed as shown in Fig. 1(b). Weak temperature dependence of the exponential I_g-V_g characteristics at $V_g > 1$ V indicates tunneling

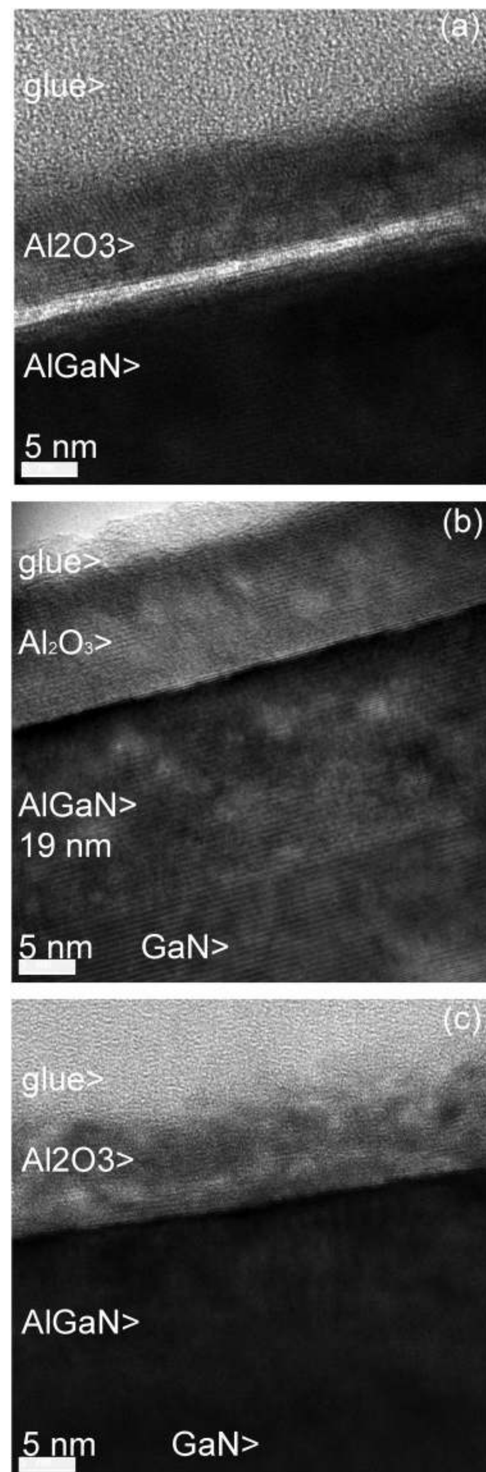

FIG. 1. (a) HR-TEM micrographs of H_2O-100 °C (a), H_2O-300 °C (b), and O_3-100 °C (c) Al_2O_3 grown on GaN/AlGaN/GaN heterostructures taken on cross sectional thinned specimens.

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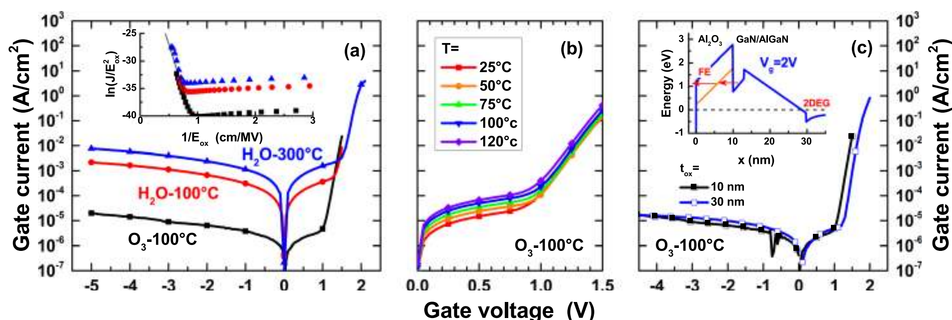

FIG. 2. (Color online) (a) Typical *I-V* characteristics of Al_2O_3/GaN/AlGaN/GaN MOS-HEMT structures with O_3-100 °C, H_2O-100 °C, and H_2O-300 °C Al_2O_3. The inset shows the Fowler–Nordheim plot of *I–V* data at positive V_g-s resulting in tunneling barrier height of 0.92 eV using $m^* = 0.28m_0$ (Ref. 17). (b) *I–V* characteristics of structure O_3-100 °C measured at temperatures ranging from 25 to 120 °C. (c) Comparison between *I–V* characteristics of MOS-HEMT structures with 10 and 30-nm thick Al_2O_3. The inset of (c) depicts band diagram of the gate stack with sketch of field emission of electrons from bulk traps into Al_2O_3 conduction band.

effects. Therefore, the *I-V* data at positive V_g-s were plotted in the so-called Fowler–Nordheim plot depicted in the inset of Fig. 2(a). From the high-field linear part of the plot, barrier height of 0.92 eV was extracted using effective electron tunneling mass of $m^* = 0.28m_0$,[17] assuming electron tunneling from GaN into Al_2O_3 conduction band through a triangular barrier. However, the resulting barrier height is more than two-times lower than the reported conduction band discontinuity between GaN and ALD grown Al_2O_3, ΔE_C [$\sim$2.2 eV (Ref. 18)]. Moreover, *I–V* measurements on samples with different thickness depicted in Fig. 1(c) show similar gate voltage onsets of the I_g exponential increase, in contrast to its expected increase with t_{ox} (i.e., similar electric field in the oxide). Instead, this behavior can be explained by the field emission of electrons from trap centers in Al_2O_3 located 0.92 eV below the conduction band minimum, as depicted in the inset of Fig. 2(c). We assume that for $V_g > 1$ V, electrons are first injected from the channel into trap centers in Al_2O_3 located near Al_2O_3/GaN-cap interface and then emitted into conduction band of the oxide. An important implication of the gate leakage onset at $V_g > 1.5$ V is expected inability to form a free-electron accumulation in the AlGaN barrier upon higher positive V_g.[19,20] This effect excludes application of any AC admittance techniques for $D_{it}(E)$ determination (such as that reported by Hori *et al.* in Ref. 21) in this voltage region, as leakage paths in Al_2O_3/AlGaN gate stack will effectively screen the capture-emission processes of interface traps.[22]

Figure 3 shows typical *C-V* characteristics of MOS-HEMT structures measured from depletion toward accumulation and backward with sweep rate of 0.2 V/s. From the *C-V* characteristics, the following features can be deduced:

(1) As expected, similar V_{th} of -2.6, -3.0, and -3.3 V was extracted from the *C-V* curves (determined graphically in the depletion part similar to Refs. 15 and 23, cf. Fig. 3) for samples H_2O-100 °C, O_3-100 °C, and H_2O-300 °C, respectively.
(2) MOS-HEMT structure O_3-100 °C shows notable *C-V* (thus V_{th}) hysteresis of $\sim$0.2 V, while structures with oxide grown using H_2O show essentially no hysteresis.
(3) While samples with O_3-100 °C and H_2O-100 °C Al_2O_3 show similar and relatively steep *C-V* depletion, *C-V* curve for sample H_2O-300 °C is stretched-out in the depletion part.
(4) All three *C-V* curves show sign of capacitance increase at $V_g > 1.1$ V (O_3-100 °C) and $V_g > 1.5$ V (H_2O-100 °C, H_2O-300 °C) resembling *C-V* behavior for the so-called spill-over regime. In this case, population of free electrons in the AlGaN barrier leads to capacitance rise up to the gate oxide capacitance, C_{ox}. However, the capacitance increase may be also related to the gate leakage onset, as it appears at similar V_g-s [cf. Fig. 2(a)]. Moreover, 2DEG density extracted from the integration of the *C-V* curve in the range from $V_g \sim V_{th}$ to spill-over regime would give sheet carrier density ranging from 6 to 7×10^{12} cm^{-2} that is almost two-times lower than the expected value of 1.3×10^{13} cm^{-2} given by AlGaN/GaN polarization charge.[24]

To analyze oxide/semiconductor interface quality in the processed MOS-HEMTs and its possible relation to the effects described above, first, we determined D_{it} distributions for all studied structures. Then, the MOS-HEMT *C-V* behavior as well as V_{th} hysteresis was simulated using 1D Poisson

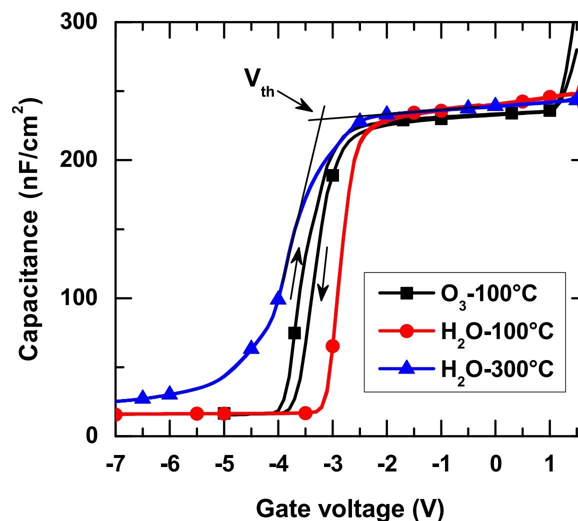

FIG. 3. (Color online) Typical *C-V* characteristics of the Al_2O_3/GaN/AlGaN/GaN MOS-HEMT structures with $t_{ox} = 10$ nm.

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calculation taking capture/emission processes of interface traps into account.

C. $D_{it}(E)$ determination

D_{it} distributions were measured using V_{th}-transient and photoassisted V_{th}-transient techniques on MOS-HEMT structures with $t_{ox} = 10$ nm. Typical V_{th}-transients measured at $T = 25\,°C$ are compared in Fig. 4(a). Note that V_{th} increases with elapsed time for all three samples, suggesting electron capture rather than electron emission from interface traps expected to take place at negative bias. This can be understood as a result of electron injection from the gate electrode into bulk traps in the Al_2O_3 similar to Ref. 15. To cancel this parasitic trapping out, only the difference between V_{th}-transients with $V_F = 1.5$ V (interface traps filling) and $V_F = 0$ V (no filling) was used to calculate D_{it} distribution for a given temperature. As expected, application of positive filling pulse induced more negative V_{th} shift at the beginning of the transients due to enhanced electron emission from filled traps. By repeating such measurements for $T = 75$ and 125 °C, D_{it} in the energy range of E_C-$E = 0.6$–1 eV was determined and is summarized in Fig. 5 for all studied structures. Although ΔV_{th} transient includes emission from electron traps located also in the AlGaN and Al_2O_3 aligned with the Fermi level, interface trap emission is expected to dominate, as evidenced in Refs. 23 and 25 by comparing V_{th} transients of Schottky- and MOS-gated HEMT structures.

The photoassisted V_{th} transient measurement is exemplified in Fig. 4(b) for sample O_3-100 °C upon exposure of light with energy centered around 1.75 eV. Similar to V_{th} transients, V_{th} increases with elapsed time due to parasitic electron trapping. Therefore, V_{th} transient was first recorded in the dark and then repeated with light exposure. Light was exposed 50 s after beginning of transient measurement so that alignment between the two transients can be adjusted, as depicted in Fig. 4(b). Both measurements were stopped at $t = 150$ s, when the difference between the two transients (i.e., ΔV_{th}) saturated. This procedure was then repeated for higher light energies. D_{it} was calculated from ΔV_{th} and

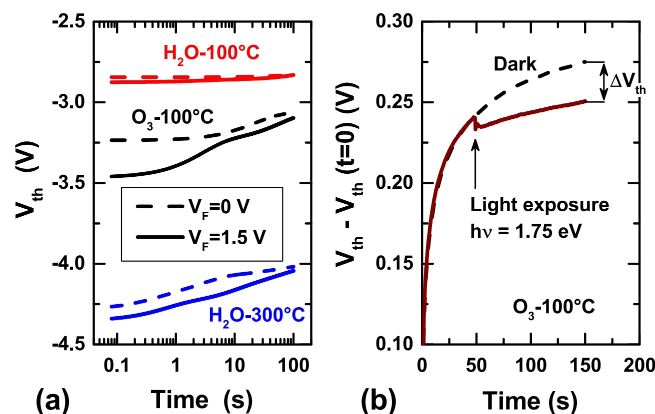

FIG. 4. (Color online) (a) Comparison of V_{th} transients measured at room temperature using $V_{meas} = V_{th}$–0.5 V, without ($V_F = 0$ V, dashed lines) and with filling pulse ($V_F = 1.5$ V, solid lines) for separation of the parasitic bulk trapping effect. (b) V_{th} transients measured at the same voltage as in (a) upon dark condition and after exposure of filtered light at $t = 50$ s.

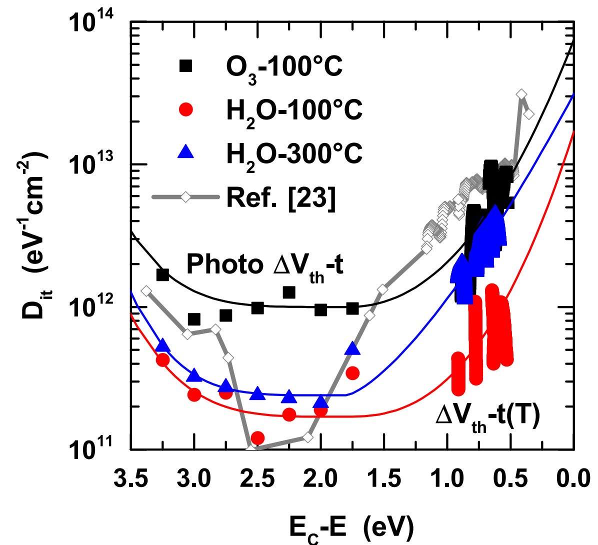

FIG. 5. (Color online) Summary of D_{it} distributions determined on Al_2O_3/GaN/AlGaN/GaN MOS-HEMT structures analyzed here (symbols) and that reported in Ref. 23 (lines with symbols). Also shown are approximated D_{it} distributions (lines) used as input parameters for C-V simulations.

difference between two adjacent light energies as $D_{it}(h\nu) = (\varepsilon_{ox}/t_{ox})[\Delta V_{th}/q(h\nu_i - h\nu_{i-1})]$. Light energy $h\nu$ was considered for E_{it}, as measured from the bottom of GaN conduction band. Capture of electrons (i.e., hole emission) from GaN valence band by interface traps for $h\nu > E_g/2$ was not considered for simplicity.

The resulting D_{it} distributions of the analyzed MOS-HEMT structures are shown in Fig. 5. MOS-HEMT structures O_3-100 °C show highest D_{it} among the analyzed structures with a value of about $10^{12}\,eV^{-1}\,cm^{-2}$ in the range of E_C-E = 3.25–1.75 eV that increases to a value of $10^{13}\,eV^{-1}\,cm^{-2}$ in the range of E_C-$E = 0.9$–0.5 eV. As compared to O_3-grown sample, both samples grown with H_2O show an order of magnitude lower D_{it} of about $2 \times 10^{11}\,eV^{-1}\,cm^{-2}$ in the range of E_C-$E = 3.25$–1.75 eV. Interestingly, despite lower deposition temperature, MOS-HEMT structure H_2O-100 °C shows lower D_{it} of 2×10^{11}–$10^{12}\,eV^{-1}\,cm^{-2}$ in the range of E_C-$E = 0.9$–0.5 eV compared to D_{it} ranging from 2 to $5 \times 10^{12}\,eV^{-1}\,cm^{-2}$ for sample H_2O-300 °C in the same energy range. Our data therefore indicates that application of O_3 oxidation agent during ALD growth of Al_2O_3 at low deposition temperature provides lower interface quality compared to H_2O, even though it gives the lowest gate leakage among the oxides analyzed here. Regarding the deposition temperature, our data suggest higher D_{it} in the range of E_C-$E = 0.9$–0.5 eV for the structure with Al_2O_3 grown with H_2O at higher temperature, while the deposition temperature seems to have a minor impact on the gate leakage. Further, keeping in mind similar D_{it} distribution in the range of E_C-$E = 0.9 - 0.5$ eV for O_3-100 °C and H_2O-300 °C, one may expect similar C-V hysteresis for both MOS-HEMT structures. This is because interface traps in this energy range have been shown to re-emit electrons with time constant similar to duration of the V_g back-sweep (tenths of seconds).[16,23] However, while structure O_3-100 °C showed C-V hysteresis of about 0.2 V, sample H_2O-300 °C showed negligible hysteresis (cf. Fig. 3).

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D. *C-V* simulations

In order to support our hypothesis of the I_g-related capacitance increase at $V_g = 1.5$ V and to understand discrepancies between *C-V* hysteresis and D_{it} distribution for sample H_2O-300 °C, we performed the simulations of the *C-V* curves and corresponding hysteresis using the experimentally determined D_{it}. For the simulation, one needs to know exact charge distribution across the MOS-HEMT gate stack. While theoretical values can be used for the estimation of polarization charges at III-N interfaces, the net charge at oxide/III-N interface (Q_{int}) has to be determined experimentally. To do so, we used dependence of V_{th} as a function of t_{ox}, similar to Refs. 8, 23, and 26. Following an analytical model for V_{th} in GaN MOS-HEMT structures,[9] the slope of V_{th}–t_{ox} dependence can be expressed as

$$\frac{dV_{th}}{dt_{ox}} = -\frac{Q_{eff}}{\varepsilon_{ox}} = -\frac{1}{\varepsilon_{ox}}(P_S + P_{QW} + qN_{DS} + qN_{ox} + qN_{it}), \quad (1)$$

where P_S is the surface polarization charge (that includes GaN-cap surface and GaN-cap/AlGaN interface polarization charge), P_{QW} is the polarization charge in the AlGaN/GaN quantum well, N_{DS} is the ionized surface donors density (partially or fully compensating P_S), N_{ox} is the sheet oxide fixed charge, and N_{it} is the interface trapped charge.[9] Q_{eff} represents an effective charge and it simply quantifies electrostatic impact of the charges residing in MOS-HEMT structure to V_{th} changes due to t_{ox} variation. Note that P_S, N_{DS}, N_{ox}, and N_{it} are assumed to be located at or close to oxide/III-N interface. From Eq. (1), it can be then defined that

$$Q_{eff} - P_{QW} = P_S + qN_{DS} + qN_{ox} + qN_{it} = Q_{int}. \quad (2)$$

This means that the net oxide/III-N charge ($Q_{int} = qN_{int}$) can be calculated from Q_{eff} (extracted from the slope of V_{th}-t_{ox} dependence) and polarization charge in the quantum well.

The dielectric constant of Al_2O_3 films used in the simulations was also determined experimentally from the dependence of MOS-HEMT total capacitance (C_{tot}) as a function of t_{ox}, similar to techniques used in Si MOS structures with high-*k* dielectrics.[27] As C_{tot} is given by the serial combination of the barrier and oxide capacitance, the static dielectric constant of the latter (ε_{ox}) can be determined from the slope of C_{tot}-t_{ox} dependence using the calculated barrier capacitance from known barrier thickness (TEM) and its dielectric constant (8.8).[24] The values of ε_{ox} for ALD-grown Al_2O_3 films are summarized in Table I. It ranges from 8.3 to 9.6 in reasonable agreement with the value reported for amorphous Al_2O_3 (9).[28] All III-N material properties were taken from Ref. 16.

Using MOS-HEMT structures with 10, 20, and 30 nm, we determined Q_{eff} from the V_{th}-t_{ox} dependences for all three set of samples, and the results are summarized in Table II. Then, P_{QW} and metal/Al_2O_3 Schottky barrier height (SBH) were adjusted to account for the experimental V_{th} and its variation with t_{ox}. The same P_{QW} of 1.27×10^{13} cm^{-2} for all structures and SBH at Ni/Al_2O_3 interface ranging from 3.3 to 3.55 eV were found to fit the experimental data. This procedure is reasonable, keeping in mind the same AlGaN/GaN wafer used for the sample processing. On the other hand, variation in the quality of the oxide surface can result in variation of the metal/oxide SBH (Ref. 29) and it compares well to the value reported in the literature for Ni/Al_2O_3 interface [3.5 eV (Ref. 30)]. Somewhat smaller P_{QW} compared to a theoretical value [1.6×10^{13} cm^{-2} (Ref. 24)] can be attributed to slight differences between nominal and actual Al composition and/or presence of defects, such as dislocations, reducing crystal quality, and thus polarization charge density.

Simulated *C-V* curves for analyzed MOS-HEMT structures with oxide thickness of 10 nm are shown in Fig. 6. Beside the experimental curve, we plotted also *C-V* curve considering $D_{it} = 0$ (dashed line) and D_{it} distribution similar to that determined experimentally (solid lines). For the calculation, actual D_{it} distribution was approximated by two exponential functions, as plotted in Fig. 5 by solid lines. To simulate the *C-V* hysteresis, also shown is the *C-V* curve calculated after setting the steady-state to $V_g = 1.5$ V (dotted line). In this state, all traps are allowed to capture or emit charge carriers according to its position to Fermi level at this voltage. This is similar to the experimental condition at $V_g = 1.5$ V, where mostly shallower traps are available and elevated leakage current further promotes charge capture/emission processes. Note that in previous simulations, thermal equilibrium was set to $V_g = 0$ V, as the first measurement steps from the equilibrium state.

Let us first discuss the gate voltage at which free electrons spill-over into the AlGaN barrier (V_{spill}) that is characteristic by second increase of the capacitance. We note here that this voltage can be also referred to as flat-band voltage V_{FB}, as AlGaN bands become flat at this condition. Simulation data suggest that V_{spill} can be expected at $V_g = 3$ V for an "ideal" structures without considering oxide/barrier interface traps. The presence of interface traps further shifts V_{spill} to higher positive voltages due to capture of electrons by (acceptor-like) interface traps which in turn stretches-out the *C-V* curve of the MOS-HEMT structure. V_{spill} increases by 0.5 V for H_2O-100 °C and by 3 V for O_3-100 °C and H_2O-300 °C, depending on D_{it} in the energy range of E_C-$E < E_{F,0}$ ($E_{F,0}$ is the Fermi level position measured from GaN conduction band at oxide/barrier interface at $V_g = 0$ V), i.e., correlating with shallower D_{it} distribution measured by V_{th} transients. Therefore, it can be concluded that *C-V* simulations support our hypothesis of gate leakage related capacitance increase at positive V_g-s, rather than being related to spill-over regime.

Regarding the *C-V* hysteresis, good agreement between experimental data and simulations can be inferred from Fig. 6 for samples O_3-100 °C (0.2 and 0.21 V, respectively) and H_2O-100 °C (<10 and 70 mV, respectively). As evidenced in Ref. 23, electron emission from interface traps centered around E_C-$E = 0.6$ eV dominantly determines the value of hysteresis upon sweep conditions used here (0.2 V/s), neglecting the effect of other traps, such as

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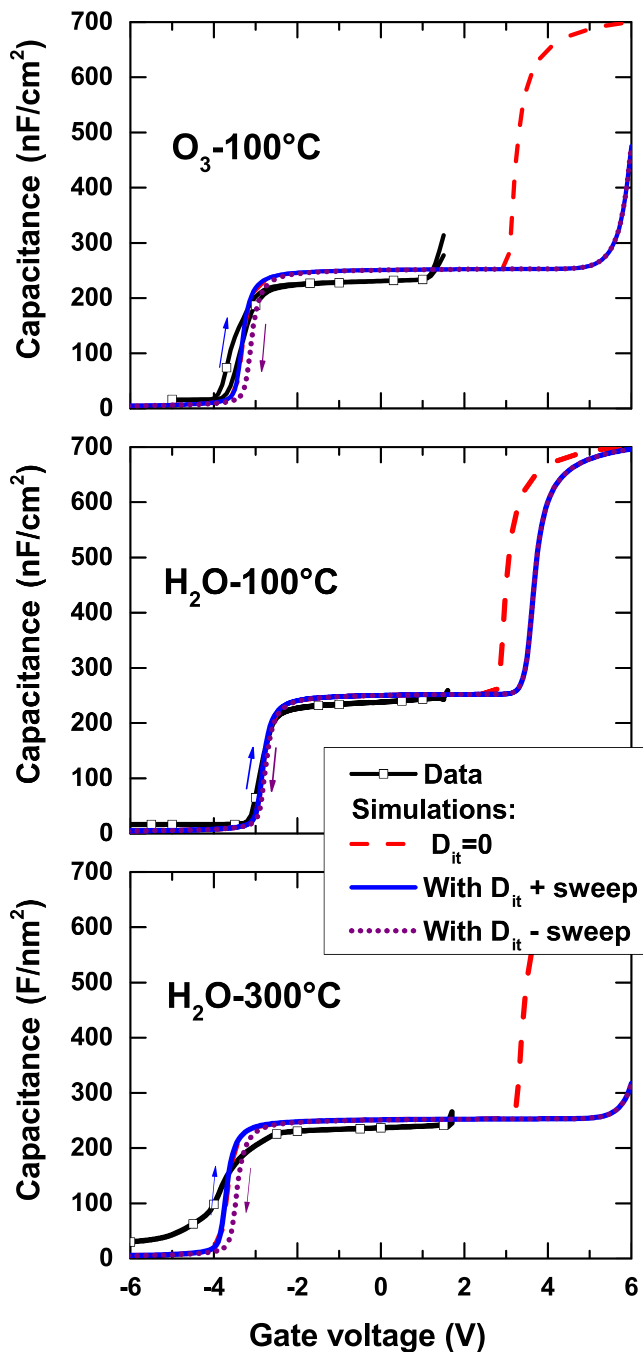

FIG. 6. (Color online) Experimental and calculated *C*-*V* curves for Al_2O_3/GaN/AlGaN/GaN MOS-HEMT structures analyzed here. Lines with symbols represent experimental data and dashed lines shows calculated curves assuming $D_{it} = 0$. Full and dotted lines depicts simulations with approximated D_{it} shown in Fig. 5 accounting for forward (from −6 to 6 V) and backward (from 6 to −6 V) measurements, respectively (see the text for details).

border traps. However, a large discrepancy between experimental (<10 mV) and simulated *C*-*V* (0.25 V) hysteresis can be inferred from Fig. 6(c) for structure H_2O-300 °C. We believe that the absence of any hysteresis can be attributed to coaction of parasitic electron trapping and interface trap emission during *C*-*V* sweeps at T = 300 °C.

Having experimentally determined $D_{it}(E)$ of samples with reduced N_{DS}, we can compare our results with $D_{it}(E)$ measured on AlGaN/GaN MOS-HEMT structures with fully compensated P_S in order to follow possible correlation between D_{it} and N_{DS}. Also plotted in Fig. 5 is D_{it} reported in our previous work[23] on Al_2O_3/GaN/AlGaN/GaN MOS-HEMTs with Al_2O_3 grown by MOCVD at 600 °C. As detailed in Ref. 23, this structure shows N_{int} of $-3 \times 10^{12}\,cm^{-2}$, i.e., almost an order of magnitude lower N_{int} compared to structures analyzed here ($\sim -1 \times 10^{13}\,cm^{-2}$). Keeping in mind an order of magnitude difference between D_{it} in the range of E_C-E = 3.25–1.75 eV for O_3-100 °C sample and those grown using H_2O while featuring similar N_{int} (thus N_{DS}), variation of D_{it} for structure with MOCVD grown Al_2O_3 in this energy range can be disregarded in terms of correlation with N_{DS}. Comparing the shallower traps (E_C-E = 0.9–0.5 eV), sample from Ref. 23 shows similar D_{it} to that determined for O_3-100 °C sample, except the energy range of E_C-E = 0.9–0.7 eV, in which MOCVD grown structure shows slightly higher D_{it} (from 7 to $4 \times 10^{13}\,eV^{-1}\,cm^{-2}$) compared to O_3-100 °C structure (from 5 to 1 $\times 10^{13}\,eV^{-1}\,cm^{-2}$). However, D_{it} differs by an order of magnitude for structures H_2O-100 °C and O_3-100 °C in the same energy range, while both samples showed similar N_{DS}. For more quantitative comparison, the difference of N_{it} obtained from D_{it} distributions as $N_{it} = \int_{E_C-0.5\,eV}^{E_C-0.9\,eV} D_{it}(E)dE$ gives the ΔN_{it} of $1.4 \times 10^{12}\,cm^{-2}$, which is much lower value compared to $\Delta N_{int} = 8 \times 10^{12}\,cm^{-2}$. Therefore, it can be concluded that, in the energy range considered, there is no clear correlation between D_{it} and N_{DS} for samples analyzed here and that reported previously.[23] Nevertheless, this conclusion does not mean that possible correlation between D_{it} and N_{DS} can exist for shallow traps located close to the conduction band edge.

Finally, let us point out the stretch-out of the *C*-*V* curve for structure H_2O-300 °C in the region corresponding to 2DEG depletion. As pointed out by several authors,[16,23] it is unlikely to attribute the stretch-out in this region to interface traps, as the Fermi level at oxide/barrier interface coincide with very deep traps (E-E_C > 1 eV) featuring much longer time constant in respect to the measurement time. Instead, traps in the GaN channel or spatial inhomogeneity of the gate oxide can account for this effect. Again, keeping in mind the same wafer used for the device processing and the absence of such effect for O_3-100 °C and H_2O-100 °C, the latter effect is more likely. Local inhomogeneity in Al_2O_3 thickness can induce variation in gate oxide electric field which in turn smears-out the pinch-off voltage of the structure.

IV. CONCLUSIONS

$D_{it}(E)$ distribution in Al_2O_3/AlGaN/GaN MOS-HEMT structures with low-T_D ALD grown oxides and reduced N_{DS} was analyzed. Although our results indicates lower interface quality for Al_2O_3 deposited on III-N heterostructure using O_3 oxidation agent compared that with H_2O, the former gives the lowest gate leakage among the structures analyzed here. From the comparison between D_{it} determined here and those reported in the literature, there seems to be no correlation between D_{it} and N_{DS}. Also, the methodology for D_{it} determination using capacitance techniques was discussed,

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focusing on enhanced forward gate leakage constraints on the application of the AC admittance techniques for D_{it} determination. Finally, we described a simple experimental methodology for the extraction of the MOS-HEMT gate charge distribution using experimental V_{th}-t_{ox} dependence and theoretical polarization charge in the quantum well that can be used for C-V simulations.

ACKNOWLEDGMENTS

This work was supported by V4-Japan joint call on advanced materials (project SAFEMOST), Slovak projects VEGA 2/0138/2014 and project "CENTE I" (1/2, ITMS code 26240120011) funded by Structural Funds of the EU by means of the Agency of the Ministry of Education, Science, Research and Sport of the Slovak republic. L. Tóth and B. Pécz thank the financial support from OTKA Project Nos. 118201 and 108869. The authors would like to thank Roman Stoklas and Tamotsu Hashizume (RCIQE, Hokkaido University, Japan) for providing XPS measurements and analysis.

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