

Low Temperature Fabrication of Immersion Capacitive Micromachined Ultrasonic Transducers on Silicon and Dielectric Substrates

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Abstract—A maximum processing temperature of 250°C is used to fabricate capacitive micromachined ultrasonic transducers (CMUTs) on silicon and quartz substrates for immersion applications. Fabrication on silicon provides a means for electronics integration via post-complementary metal oxide semiconductor (CMOS) processing without sacrificing device performance. Fabrication on quartz reduces parasitic capacitance and allows the use of optical displacement detection methods for CMUTs. The simple, low-temperature process uses metals both as the sacrificial layer for improved dimensional control, and as the bottom electrode for good electrical conductivity and optical reflectivity. This, combined with local sealing of the vacuum cavity by plasma-enhanced, chemical-vapor deposition of silicon nitride, provides excellent control of lateral and vertical dimensions of the CMUTs for optimal device performance. In this paper, the fabrication process is described in detail, including process recipes and material characterization results. The CMUTs fabricated for intravascular ultrasound (IVUS) imaging in the 10–20 MHz range and interdigital CMUTs for microfluidic applications in the 5–20 MHz range are presented as device examples. Intra-array and wafer-to-wafer process uniformity is evaluated via electrical impedance measurements on 64-element ring annular IVUS imaging arrays fabricated on silicon and quartz wafers. The resonance frequency in air and collapse voltage variations are measured to be within 1% and 5%, respectively, for both cases. Acoustic pressure and pulse echo measurements also have been performed on 128 $\mu\text{m} \times 32 \mu\text{m}$ IVUS array elements in water, which reveal a performance suitable for forward-looking IVUS imaging at about 16 MHz.

I. INTRODUCTION

CAPACITIVE micromachined ultrasonic transducers (CMUTs) have been developed as an alternative to piezoelectric ultrasonic transducers, particularly for microscale and array applications [1]. Because CMUTs are surface micromachined, they can be fabricated into one- or two-dimensional arrays and customized for specific applications; and they can have performance comparable to piezoelectric transducers in terms of bandwidth and dy-

amic range [2]. A single element of a CMUT array consists of compliant membranes with electrodes suspended above an electrically conductive substrate. To transmit an acoustic wave, an alternating current (AC) signal and a large direct current (DC) bias are applied to the membrane. The DC voltage pulls down the membrane where the transduction is efficient and linearizes the device response. The AC voltage sets the membrane into motion at the desired frequency and generates an acoustic wave in the surrounding fluid. To receive an acoustic wave, the capacitance change is measured when an impinging acoustic wave sets the membrane into motion. If the elements of the CMUT array have a small, mechanically active area covered with an electrode, the change in capacitance also will be small and can be overwhelmed by parasitic capacitance.

Parasitic capacitance can be found in two different areas, each requiring a unique solution. The first source of parasitic capacitance is the area in which the bond pads and metal traces overlap the bottom electrode. Because standard CMUT processes make use of a doped silicon bottom electrode, parasitic capacitance can dominate the active capacitance of the device. To reduce this on-chip capacitance, a patterned metal-bottom electrode can be used. The use of the metal-bottom electrode also allows CMUTs to be fabricated on dielectric substrates such as quartz. With a transparent quartz substrate, optical detection schemes, which are independent of device capacitance, can be implemented to improve the CMUT performance [3], [4]. Although materials such as doped polysilicon or amorphous silicon also could be used for the bottom electrode, metals have higher electrical conductivity and optical reflectivity, which is important for optical detection. The second source of parasitic capacitance comes from the electrical interconnects to the amplifying electronics. This source of parasitic capacitance can be reduced only through hybrid or monolithic integration with the electronics that would typically be implemented using complementary metal oxide semiconductor (CMOS) technology.

The original CMUT process makes use of low-pressure chemical vapor depositions (LPCVD) for membrane formation and sealing [5]. Because the high process temperatures (900°C) make postprocess CMOS integration impossible, through wafer vias have been developed to allow CMUTs to be flip-chip bonded to a signal-processing

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chip as a means for hybrid integration [6], [7]. A major drawback to this approach is the complicated fabrication process. A recently developed process based on PECVD silicon nitride generates a relatively large gap, 4000 Å or larger, requiring high DC bias voltages, and the process temperature is somewhat high for CMOS integration, 400–500°C, due to an annealing step for the silicon nitride [8]. A recently developed approach to CMUT fabrication makes use of wafer-bonding techniques to improve membrane uniformity [9]. However, the high temperatures required for bonding make postprocess CMOS integration impossible.

Another approach to electronics integration is to fabricate the CMUT out of the layers of a standard CMOS process [10]. Although this constitutes the ultimate in electronics integration, the CMUTs cannot be fabricated directly over the electronics, wasting valuable real estate on the chip. A second approach to electronics integration involves postprocessing CMUTs directly over CMOS electronics [11]. This process makes use of polymer sacrificial layers under a silicon nitride membrane formed with plasma-enhanced, chemical-vapor deposition (PECVD), but generates gaps in the 1–2 μm range, which is not suitable for efficient CMUT operation at high frequencies. To operate CMUTs at high frequencies, the membranes must be small and stiff to achieve the desired resonant frequency. These stiff membranes, coupled with large gaps, may require prohibitively high-collapse voltages for efficient CMUT operation.

In this paper, we present a low-temperature, CMOS-compatible CMUT fabrication process without any performance tradeoffs and a reduced number of process steps as compared to hybrid integration using through wafer vias. The equipment required for the whole process consists of a PECVD system, a dry etching system, a metal sputtering system, standard wet bench, and photolithography equipment. The process makes use of low-temperature PECVD processes for the deposition of the low-stress silicon nitride structural layer at 250°C, which is the maximum process temperature when a metal sacrificial layer is used. Alternatively, an amorphous silicon sacrificial layer deposited at 300°C can be used as the sacrificial layer. These process temperatures enable postprocess CMOS electronics integration without compromising CMUT performance. Because a dielectric membrane is used, the electrode size and location can be changed to reduce parasitic capacitance and optimize performance [12], [13]. The membranes are sealed using PECVD silicon nitride, allowing for immersion operation and eliminating the need for long-sealing channels required for LPCVD silicon nitride sealing. Additionally, the process allows CMUTs to be fabricated on optically transparent dielectric substrates using a patterned metal bottom electrode for reduced parasitic capacitance and providing an opportunity for optical detection.

In the following sections, we first describe the details of the low-temperature fabrication process we used for the fabrication of interdigital CMUTs for microfluidic applications and ring-annular CMUT arrays for forward-looking intravascular ultrasound (IVUS) imaging applications. We

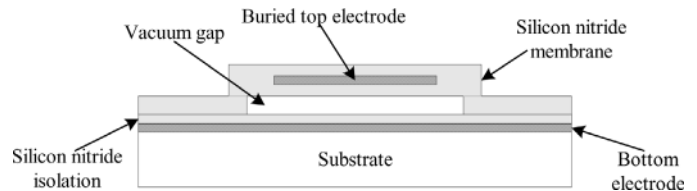


Fig. 1. Schematic of completed CMUT fabricated with the low-temperature, CMOS compatible process.

then present experimental characterization results of individual device performance as well as process uniformity on the IVUS arrays fabricated on both silicon and quartz substrates.

II. LOW-TEMPERATURE CMUT FABRICATION PROCESS

The cross section of an immersion CMUT fabricated using a low-temperature, CMOS compatible process is illustrated in Fig. 1. The device consists of a silicon nitride membrane suspended above a vacuum-sealed gap. Electrodes on the surface of the substrate and buried in the membrane allow electrostatic forces to be applied to the membrane. The fabrication process is illustrated in Fig. 2 and will be described in the following sections. The letters in the figure correspond to the following section headings.

A. Bottom Electrode

The first step in the fabrication process forms the bottom electrode. This electrode can be formed either by doping the silicon substrate or by patterning a thin layer of metal. With a doped silicon bottom electrode, all non-moving parts of the top electrode act as parasitic capacitance degrading device performance, and the use of optical detection techniques is prohibited for most of the optical spectrum.

To alleviate these problems, a patterned, metal-bottom electrode is used. By patterning the metal-bottom electrode, the parasitic capacitance can be significantly reduced. Also, a metal-bottom electrode allows CMUTs to be fabricated on dielectric substrates, such as quartz. The reduced process temperature is advantageous when postprocessing CMUTs over CMOS circuitry. In Fig. 3, micrographs of completed transducers are shown with a doped, silicon-bottom electrode and patterned, metal-bottom electrodes.

Aluminum, chromium, and gold were investigated for use as the bottom electrode. The film thickness for all metals was 1500 Å. Aluminum was investigated for its ease in deposition and patterning. When depositing the PECVD silicon nitride isolation layer, the aluminum was observed to form hillocks when placed on the heated platen of the PECVD system. This hillock formation, which has been well documented in literature, is evident from the speckled appearance of the aluminum bottom electrode in Fig. 3(b)

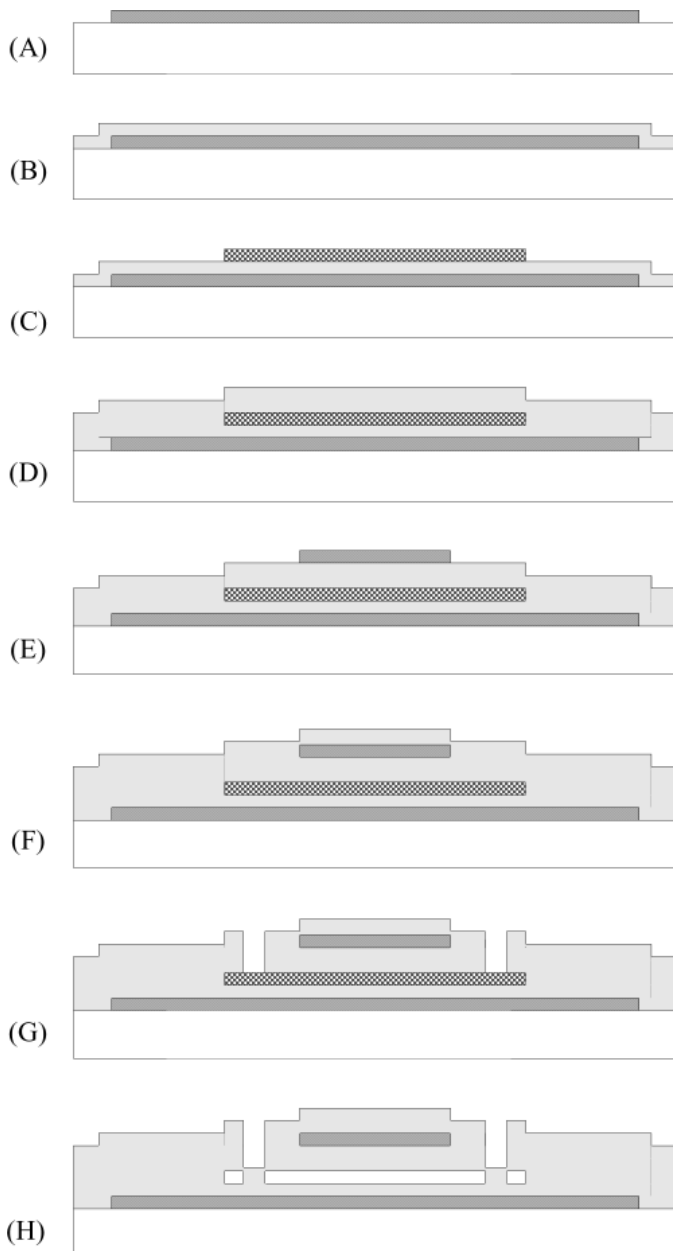


Fig. 2. Illustration of low-temperature process flow for immersion CMUTs.

[14]. This process produced roughness two to three times the thickness of the original aluminum layer as seen in the atomic force microscope (AFM) image in Fig. 4(a). This surface roughness is transferred to the subsequent layers and results in membranes with nonuniform gaps. When the sacrificial layer is etched away, the motion of the membrane is obstructed by the defects.

Chromium also was considered because of the ease of deposition and patterning and its resistance to oxidation. After depositing the silicon nitride isolation layer, no oxidation of the chromium was observed, making it an attractive bottom-electrode material, as seen in Figs. 3(c) and 4(b). The only drawback is the high resistivity compared to aluminum and gold. The CMUTs were successfully fabricated and tested using a chromium bottom electrode.

Gold was investigated as a bottom-electrode material because of its low-electrical resistance and low rate of oxidation when depositing silicon nitride. Gold also is preferred over chrome and aluminum as it is not readily attacked by the etchants used during the membrane release.

B. Silicon Nitride Isolation Layer

A silicon nitride layer, 1500 Å thick, is deposited to protect the bottom electrode or silicon substrate from the etchants used for the membrane release. When a doped silicon bottom electrode is used in conjunction with an amorphous silicon sacrificial layer, the silicon nitride layer is needed to prevent the tetramethylammonium hydroxide (TMAH) from etching the silicon substrate. If a chromium sacrificial layer is used on a doped silicon substrate, the isolation layer is not needed. Whenever a patterned, metal-bottom electrode is used, the isolation layer is required.

C. Sacrificial Layer

The sacrificial layer, used to form the gap under the membrane, can be formed out of either PECVD amorphous silicon or sputtered metal. Amorphous silicon can be deposited at temperatures as low as 300°C but must be patterned with a reactive ion etch (RIE). The process parameters for the amorphous silicon deposition can be found in Table I, and the etch recipe can be found in Table II. The PECVD amorphous silicon has a low surface roughness (approximately 4 Å) and does not oxidize when coated with silicon nitride. This film has been used to form gaps as small as 1000 Å. The only disadvantage in using amorphous silicon is the poor selectivity of TMAH during the membrane release.

The use of metal sacrificial layers also was investigated. As previously discussed, aluminum is a poor choice due to the severe oxidation when coated with silicon nitride. Other researchers have successfully used aluminum as a sacrificial layer [15]. However, for those applications the gap height is large, on the order of 1 μm, and surface oxidation is of little concern. Chromium does not oxidize in the PECVD chamber and is easily patterned using commercially available wet etchants. The chromium etchant is very selective to silicon nitride and, therefore, is a suitable release agent. Gaps as small as 1300 Å have been fabricated using this chromium sacrificial layer, but this does not constitute the lower limit. In practice, the gap height is limited by the static deflection of the membrane due to atmospheric pressure and residual stresses, stiction, and the surface roughness of the sacrificial layer. The static deflection due to residual stresses can be overcome through proper design and the stiction problem can be overcome by releasing a thicker membrane, and then thinning it back to the desired thickness after sealing. The surface roughness of the sacrificial layer is on the order of nanometers and represents the ultimate limit of the gap height.

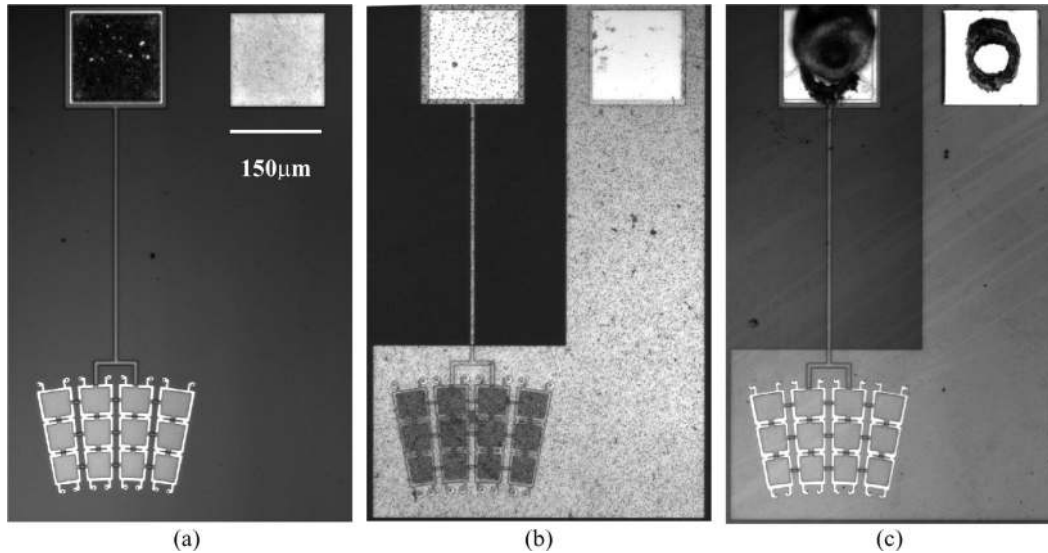


Fig. 3. Micrographs of completed CMUTs fabricated on (a) silicon with a doped silicon bottom electrode, (b) silicon with a patterned, aluminum-bottom electrode, and (c) quartz with a patterned, chromium-bottom electrode.

TABLE I
RECIPES FOR PECVD OF SILICON NITRIDE AND AMORPHOUS SILICON.¹

Parameter	Silicon nitride	Amorphous silicon
5% SiH ₄ in He	200 sccm	1000 sccm
NH ₃	8 sccm	—
He	560 sccm	—
N ₂	150 sccm	—
Pressure	1100 mTorr	900 mTorr
Power	50 W	50 W
Temperature	250°C	300°C
Deposition rate	100 Å/minute	75 Å/minute

¹The silicon nitride and amorphous silicon films were patterned using RIE. The process parameters can be found in Table II.

TABLE II
RECIPES FOR REACTIVE ION ETCH OF SILICON NITRIDE AND AMORPHOUS SILICON.¹

Parameter	Silicon nitride	Amorphous silicon
Etch gas 1	45 sccm CHF ₃	30 sccm SiCl ₄
Etch gas 2	5 sccm O ₂	20 sccm Cl ₂
Pressure	40 mTorr	30 mTorr
Power	200 W	150 W
Etch rate	650 Å/minute	500 Å/minute

¹The recipe for silicon, nitride-etched nitride is approximately five times faster than amorphous silicon, and the recipe for amorphous, silicon-etched silicon approximately 15 times faster than silicon nitride.

D. Membrane Formation

Depositing PECVD silicon nitride over the sacrificial layer forms the vibrating membrane of the CMUT. The thickness of this layer varies, depending upon the application; but 6000 Å is a typical value. To prevent defects in this layer of silicon nitride, it is important to completely remove any photoresist residue before the deposition. When

amorphous silicon is used as the sacrificial layer, a standard RCA or Piranha clean is used. However, if a metal sacrificial layer is used, the standard cleaning processes (RCA or Piranha) cannot be used because they will degrade or remove the metal layer. Instead, the photoresist residue is removed by immersing the wafers in a beaker of acetone in an ultrasonic bath. Commercially available photoresist strippers also could be used. The wafer is removed after soaking for 10–15 minutes and rinsed with acetone, methanol, and deionized water. After drying the wafer, the membrane silicon nitride can be deposited.

E. Top Electrode Formation

Again, aluminum is a poor choice for the top electrode material because it will oxidize with subsequent silicon nitride depositions. Chromium is also a poor choice because of its high resistivity and high residual stress. However, the combination of the two materials produces a suitable top electrode. Depositing 1200 Å of aluminum followed by 300 Å of chromium forms the top electrode. The aluminum provides good electrical conductivity, and the chromium protects the aluminum from oxidation.

F. Second Membrane Deposition

Another deposition of silicon nitride is carried out to increase the thickness of the membrane and protect the top electrode from the etchants used during release. This layer of silicon nitride is typically 6000 Å thick.

G. Membrane Release

To allow the etchants to reach the sacrificial layer, holes are etched through the layers of silicon nitride using RIE. When an amorphous silicon sacrificial layer is used, one must be aware of the selectivity of the etch process to silicon. If the process has low selectivity, one can easily

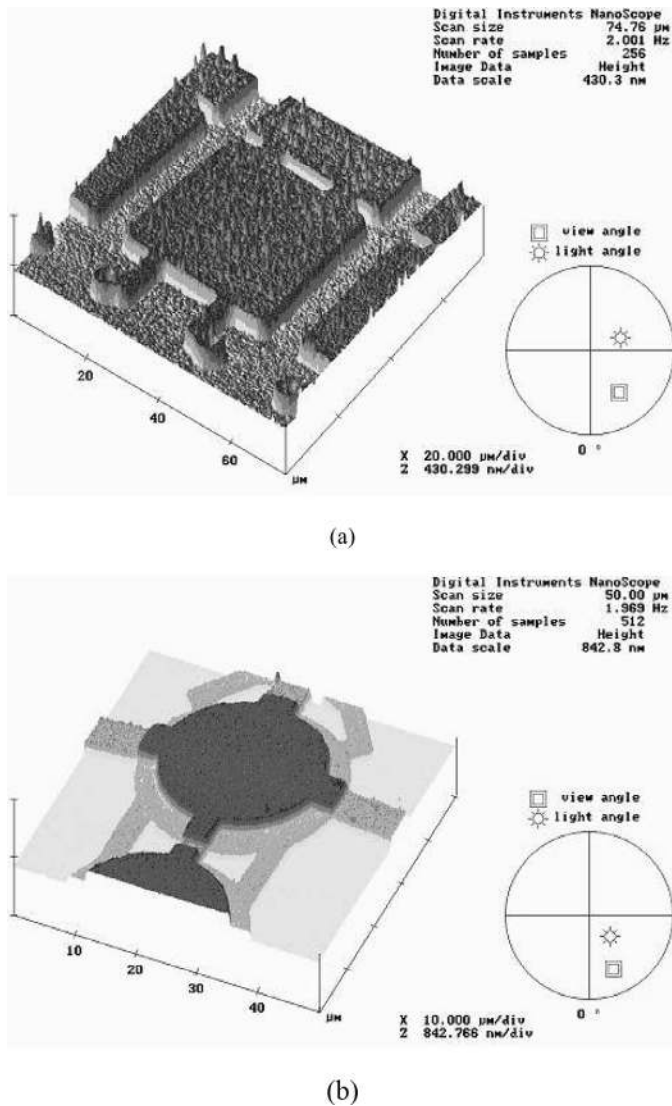


Fig. 4. AFM images of (a) surface roughness of aluminum resulting from oxidation on the heated PECVD platen, and (b) smooth surface resulting from use of chromium-bottom electrode.

etch through the thin sacrificial layer, the thin silicon nitride isolation layer, and down to the silicon substrate. If this occurs, the silicon etchant used for release will attack the substrate and destroy the devices. The recipe used for selectively etching the silicon nitride can be found in Table II. When a metal sacrificial layer is used, the selectivity of the reactive ion etch is of little importance because the metal layer acts as an etch stop.

When using amorphous silicon, the release is performed by immersing the wafer in a beaker of 4 wt% TMAH doped with 13.5 gm/L of silicon. The TMAH was used rather than KOH because of its CMOS compatibility, and the solution is doped to improve the selectivity to silicon nitride [16]. Although the etch rate of the silicon nitride is low, approximately 40–80 $\text{\AA}/\text{hour}$, it can be significant during long releases that take 10–12 hours. The slow attack of the silicon nitride results in a membrane with a nonuniform gap that leads to device performance that is difficult

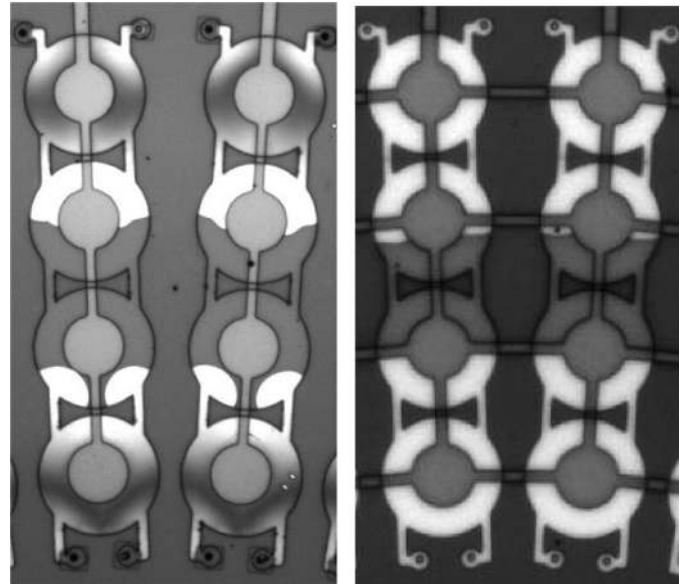


Fig. 5. Micrographs showing partially released 32- μm diameter membranes with (a) nonuniform thickness resulting from attack of silicon nitride by TMAH, and (b) uniform thickness due to low etch rate of silicon nitride in chromium etchant.

to predict. When the etch rate of silicon nitride was high (80 $\text{\AA}/\text{hour}$), the etch rate of amorphous silicon was slower than normal, compounding the problem. For devices with a long lateral etch length, the attack of silicon nitride results in different thickness membranes on the same transducer as shown in Fig. 5(a).

When chromium is used for the sacrificial material, commercially available chromium etch is used to release the membranes. The progression of the membrane release is shown in Fig. 5(b). The etch rate of silicon nitride in the chromium etchant was too low to be measured, and thus the gaps resulting from the chromium sacrificial layer have a uniform thickness. With a uniform membrane thickness, the device performance can be more accurately modeled and predicted. For devices with large or thin membranes, the small gaps may cause some problems resulting from stiction. This effect can be mitigated by rinsing the wafer with methanol before drying or by using a supercritical dryer.

H. Membrane Sealing

The membranes are sealed for immersion applications by depositing another layer of PECVD silicon nitride. This silicon nitride sealing layer is typically much thicker than the gap height (4500 \AA vs. 1500 \AA) to ensure complete membrane sealing in a single deposition. The CMUTs are typically sealed using LPCVD silicon nitride depositions, but this necessitates long etch channels to prevent deposits on the underside of the membrane. Other materials such as LPCVD silicon dioxide also result in more localized sealing than silicon nitride, but the high temperatures prohibit post-CMOS electronics integration. Because PECVD is much more directional than LPCVD, the membranes are

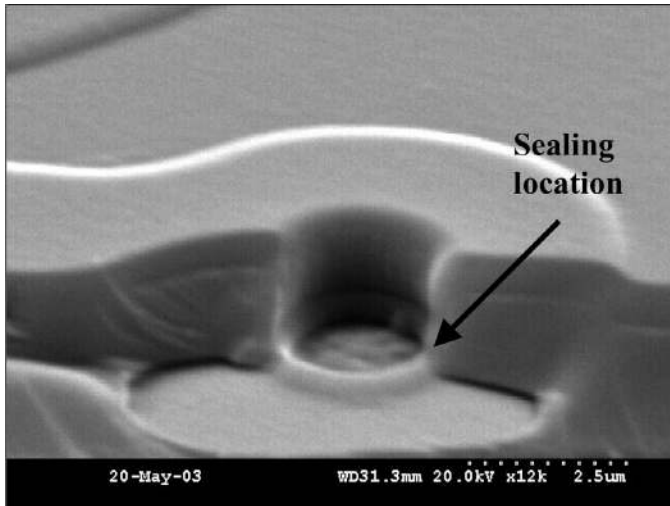


Fig. 6. SEM showing the local sealing of the CMUT membrane around the etch hole resulting from a PECVD silicon-nitride deposition.

sealed locally, in about 5000 \AA lateral distance, around the perimeter of the etch hole as seen in Fig. 6. In Fig. 6, one can see the interface between the membrane silicon nitride ($10,000 \text{ \AA}$) and the sealing layer (4500 \AA). The local sealing eliminates the need for long sealing channels and allows membranes to be packed into denser arrays. Also, additional etch holes can be placed around the perimeter of the membrane to speed the release [8].

An interesting problem arises when attempting to seal thin membranes using PECVD silicon nitride, in which fully released membranes are placed in the chamber and a short deposition is performed. After removing the samples and inspecting them under a microscope, the membranes are found to be collapsed. However, a drop of methanol placed on the wafer quickly fills the remaining gap under the membranes. This eliminates the possibility that the membranes are sealed and have collapsed due to atmospheric pressure. Finite-element simulation of the membrane yields a resonant frequency near the drive frequency of the radio frequency (RF) plasma which is at 13.56 MHz . Furthermore, membranes on the same wafer with higher resonant frequencies did not collapse. Therefore, we hypothesize that the membranes were set into resonance by the RF plasma, repeatedly impacted the substrate, and became permanently collapsed due to charge build up. This problem can be avoided by depositing a thicker membrane before the sealing process and thinning back to the desired thickness after the membrane is sealed.

The final step in the process uses RIE to etch through the silicon nitride layer covering the bond pads. This allows external electrical connections to be made with wire bonding. In some cases, gold was patterned over the bond pads to improve the reliability of the wire bonds.

I. Alternative Process Flow

An alternative process flow releases the membranes after the first membrane deposition. With this process, there

is little time invested in the wafer before performing the critical step in the process, the membrane release. Because the top electrode has not been deposited, there is no risk that pinholes in the silicon nitride could allow the top electrode to be destroyed. With this modified process, the membrane must be thick enough so that the resonant frequency is above the drive frequency of the RF plasma. Another drawback to this alternate process is that the top electrode position cannot be optimized to improve the performance of the CMUT.

Post-CMOS processing of CMUTs can be performed based on the approach used for building digital mirror devices (DMD), a commercially successful optical display made of a two-dimensional (2-D) array of electrostatically actuated mirrors [17]. In this process, a low temperature silicon oxide layer is deposited first over the existing CMOS circuitry for electrical isolation. This is followed by chemical-mechanical polishing to provide an optically flat surface, and vias are opened in the silicon oxide layer for electrical contacts. The optical micromirrors then are surface micromachined over the silicon oxide surface. In the case of CMUTs, the same base process can be followed by the low-temperature process outlined above to fabricate CMUTs directly on CMOS electronics.

III. PLASMA PROCESSING

The depositions of silicon nitride and amorphous silicon were carried out in a single Unaxis 790 PECVD system (Unaxis 790 PECVD, Unaxis Semiconductors, St. Petersburg, FL 33716) and the process parameters for both films are summarized in Table I.

All relevant properties of the PECVD silicon nitride were measured to fully characterize the transducers. The results are summarized in Table III. The residual stress was determined using the wafer bow technique. A Veeco Dektak 3030 profilometer (Veeco Instruments, Woodbury, NY) was used to measure the wafer bow before and after depositing a layer of silicon nitride. The residual stress was determined to be tensile with a value of $35 \pm 5 \text{ MPa}$ on several wafers from different process runs. The density was determined to be $2040 \pm 20 \text{ kg/m}^3$ by weighing a silicon wafer before and after depositing a known thickness of silicon nitride. This is at the very low end of the published values and indicates that the film has high porosity. This assumption is further verified by the measured relative permittivity of 6.3, lower than the high-density silicon nitride films. The Young's modulus of a $2\text{-}\mu\text{m}$ layer of silicon nitride is determined to be about 160 GPa using nanoindentation. However, measurements on CMUTs suggest a 30% lower value when experimental results are consistently fit with finite-element analysis (FEA) on devices with various dimensions. Because the literature suggest that the Young's modulus of PECVD silicon nitride would be about 160 GPa with a density of 2600 kg/m^3 and decrease with the density of the film, we believe that the lower value obtained from electromechanical measurements are more reliable [18], [19].

TABLE III
PROPERTIES OF SILICON NITRIDE FILM.

Property	Value
Residual stress	35 ± 5 MPa (T)
Density	2040 ± 20 kg/m ³
Young's modulus	160 ± 10 GPa (nanoindentation) 110 GPa (FEA fit to experimental data)
Relative dielectric constant	6.3 ± 0.1

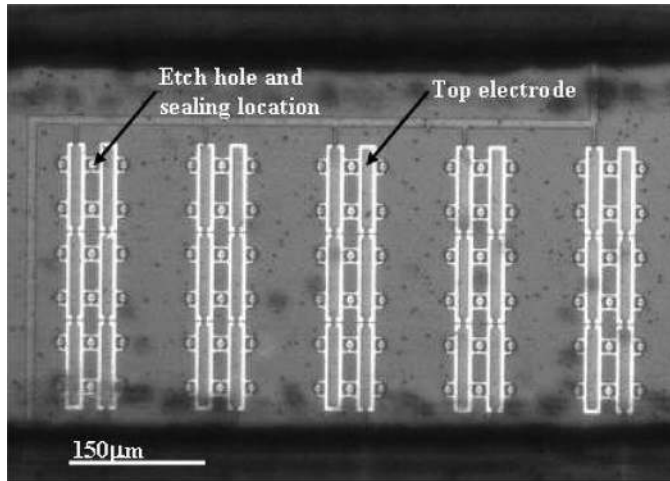


Fig. 7. Interdigital CMUT integrated into a microfluidic channel for sensing and pumping.

IV. FABRICATED CMUTS

The fabrication process described in the preceding sections was used to produce CMUTs for two distinct applications. The first uses long rectangular CMUTs to generate Scholte interface waves in microfluidic environments [20]. These CMUTs are arranged in an interdigital configuration, as seen in Fig. 7, to generate highly directional interface waves. Devices were designed and tested in water at frequencies of 5, 10, and 20 MHz. A typical device operating at 10 MHz has a width of $20 \mu\text{m}$, a length of $100 \mu\text{m}$, a thickness of 8000 \AA , and a gap height of 1500 \AA . These devices were demonstrated to perform fluid sensing and bidirectional fluid pumping in microchannels [21].

Ring annular arrays for forward-looking IVUS were the other application of CMUTs fabricated using the low-temperature process. The forward-looking IVUS arrays were designed to operate in the 10–20 MHz range with high efficiency [12]. Each array element consists of a line of four to eight circular membranes with 32 to $45 \mu\text{m}$ diameter or three to six trapezoidal membranes with 36 to $45 \mu\text{m}$ side length as seen in Fig. 8. A membrane thickness of $1.8 \mu\text{m}$ is used to provide center frequencies in the 10–20 MHz range. The dimensions are selected such that the array elements have acceptance angles suitable for forward-looking imaging at 10 to 20 MHz operation. Detailed imaging-related characterization results and initial images obtained with these IVUS arrays can be found in a recent conference article [22].

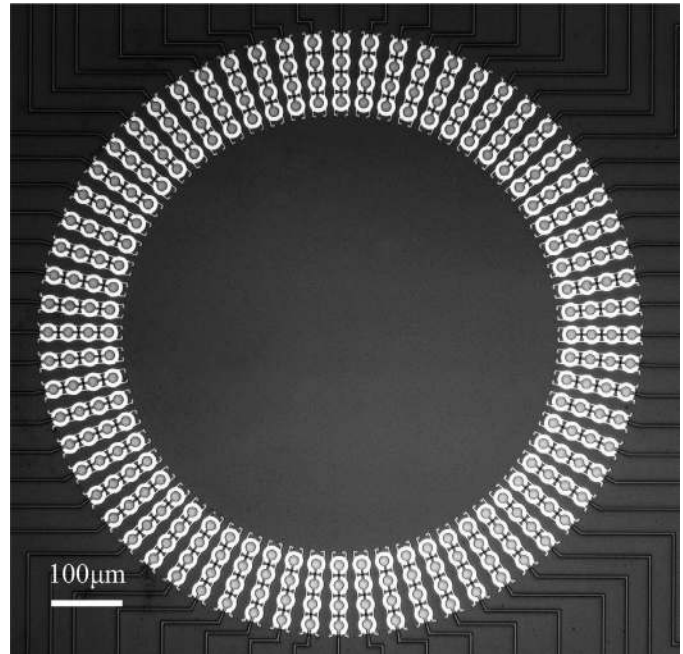


Fig. 8. Micrograph of a 64-element, ring-annular, forward-looking IVUS imaging array with 1-mm array diameter. Each element is comprised of four, $32\text{-}\mu\text{m}$ circular membranes or three $36\text{-}\mu\text{m}$ long trapezoidal membranes (as shown in Fig. 3).

V. TRANSDUCER CHARACTERIZATION

Extensive characterization was performed on the IVUS arrays with circular CMUT elements. Information on process uniformity, process repeatability, membrane material properties, and device performance was obtained through electrical and acoustical measurements.

A. Electrical Characterization

Electrical impedance and collapse voltage measurements provide valuable information to quantify mechanical and electrical properties of CMUTs. Because the CMUTs behave as resonators with high quality factors in air, small variations in the membrane properties result in noticeable changes in the resonance frequency. We use the resonance frequency as a way of assessing process variation within an array, across a wafer, and from wafer to wafer. Fig. 9 shows the real and imaginary parts of the measured electrical impedance of a single element of the IVUS array of Fig. 8 at 70 V DC bias. The different traces indicate devices built on silicon and quartz wafers during the same

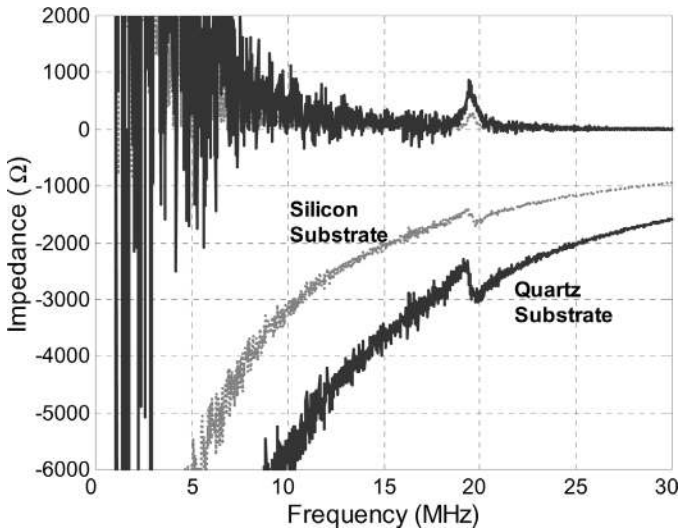


Fig. 9. Measured electrical impedance for CMUTs fabricated with and without patterned-bottom electrodes. Each device consists of four membranes each $32 \mu\text{m}$ in diameter.

process run. The resonance frequencies are within 1% of each other, which shows that our low temperature process produces mechanically identical devices from wafer to wafer even with different substrate materials. The measured maximum variation in resonance frequency across a 64-element array is found to be less than 1%, which is expected as the array diameter is only 1 mm.

The collapse voltage provides an independent measure of mechanical and electrical properties and can be used to determine the consistency of the experimental results. The collapse voltage is determined by increasing the CMUT bias until the resonant peak begins to shift downward drastically, and the maximum value of the peak starts to decrease. The intra-array and wafer-to-wafer uniformity of the collapse voltage is measured to be in the 5% range using this method.

A finite-element model predicting the resonant frequency and collapse voltage of circular CMUTs has been developed for design and verification purposes. The model uses the multiphysics capabilities of the ANSYS finite-element package (ANSYS, Inc., Canonsburg, PA) to model electrostatic collapse and the resonance frequency in air [12]. The resonance behavior of the CMUT is modeled with a harmonic analysis using the same mechanical mesh as the coupled electromechanical model. A typical device with parameters, given in Table IV, results in a resonance frequency of 21.6 MHz and a collapse voltage of 170 V, which is within 5% of the measured values. Experimental and calculated resonance frequency and collapse voltage agree within 7.5% accuracy for circular CMUT IVUS elements with different membrane thickness, gap thickness, and membrane diameter when the membrane material properties listed in Table III are used with a Young's modulus of 110 GPa. The consistency of these results suggests that the finite-element model can be used for the design and optimization of CMUTs.

TABLE IV
TYPICAL PARAMETERS OF A CMUT MEMBRANE IN AN IVUS
ARRAY ELEMENT.

Parameter	Value
Diameter	$32 \mu\text{m}$
Isolation layer thickness	$0.15 \mu\text{m}$
Gap thickness	$0.13 \mu\text{m}$
Membrane thickness below the top electrode	$0.6 \mu\text{m}$
Top electrode thickness	$0.16 \mu\text{m}$
Total membrane thickness	$1.8 \mu\text{m}$

Electrical measurements also are performed to verify the reduced parasitic capacitance of CMUTs fabricated on quartz substrates. The impedance curves shown in Fig. 9 indicate only a 57% reduction in total capacitance associated with the patterned bottom electrode because of 2 pF off-chip capacitance of the particular setup present in both measurements. These results show that the low-temperature process can be used to fabricate CMUTs with equivalent mechanical and improved electrical characteristics on quartz substrates as compared to their silicon counterparts.

B. Acoustic Characterization

The acoustic performance of the immersion CMUTs fabricated using the low-temperature process is evaluated by acoustic measurements in a water tank. The transmit performance of a single element of the IVUS array shown in Fig. 8 is evaluated in water using a hydrophone calibrated in the 1–20 MHz range (GL series hydrophone, ONDA Corp., Sunnyvale, CA 94089). Fig. 10 shows output signals measured by the hydrophone located 2.5 mm away from the transducer for 10 V-peak tone bursts at different frequencies. The DC bias is 100 V, corresponding to 60% of the collapse voltage. The measured hydrophone output corresponds to a pressure of 20 kPa/V at the CMUT surface. The results agree well with analytical calculations predicting 16 kPa/V constant pressure output in the 10–20 MHz range for this particular device.

The pulse-echo response of the CMUTs also has been measured using a flat aluminum block as a target 1 mm away. The top graph in Fig. 11 shows the pulse-echo signal obtained on a device consisting of 16 $32\text{-}\mu\text{m}$ membranes when it is excited with an 8 ns, 30 V peak signal with 100 V DC bias. The receive electronics used for these measurements is based on two cascade connected AD603 low-noise amplifiers (Analog Devices, Norwood, MA) resulting in 90 MHz bandwidth and 60 dB total gain. The frequency spectrum of the first echo, shown in Fig. 11(b), indicates that the transducers have 60% fractional 6 dB bandwidth centered on 16 MHz. The broad bandwidth of the receiver electronics allows one to observe a second peak at about 55 MHz, corresponding to the second antisymmetric vibration mode of the CMUT membranes. Note that this measurement has been performed with a setup with a

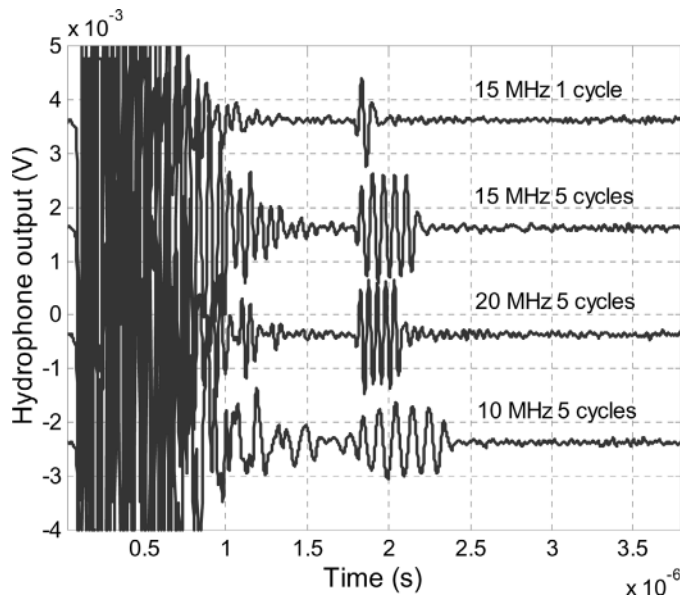


Fig. 10. Measured hydrophone output signals corresponding to tone burst signals at 10, 15, and 20 MHz input to a single element of the IVUS array shown in Fig. 8.

parasitic capacitance nearly an order of magnitude larger than the array element, resulting in an overall bandwidth smaller than cited for CMUTs in the literature. Nevertheless, the results show that the performance of the CMUTs fabricated with the low-temperature process is suitable for IVUS imaging. Obviously, one can expect a much broader bandwidth and improved performance with CMUTs integrated with electronics by post-CMOS fabrication.

VI. CONCLUSIONS

In this paper we have presented in detail a fabrication process for CMUTs with a maximum processing temperature of 250°C. This process would allow transducers to be postprocessed directly onto CMOS electronics without compromising the performance of the CMUT or the electronics. Due to the low-process temperature, it also is possible to fabricate CMUTs on quartz substrates to reduce parasitic capacitance and to enable optical detection. The transducers are sealed for immersion applications using PECVD silicon nitride, which eliminates the need for long sealing channels and allows for more dense arrays. The properties of the silicon nitride films, which is critical for device design and performance, have been characterized and found to be consistent from wafer to wafer.

The characteristics of the CMUTs on quartz and silicon substrates have been determined through electrical measurements, and the process uniformity is evaluated on forward-looking IVUS imaging arrays. Both the resonant frequency and collapse voltage variation are found to be suitable for building CMUT imaging arrays. The transmit pressure and pulse-echo response measurements in water suggest that the CMUT arrays are suitable for IVUS imaging at about 16 MHz center frequency. We currently are working on monolithic CMOS electronics-CMUT integra-

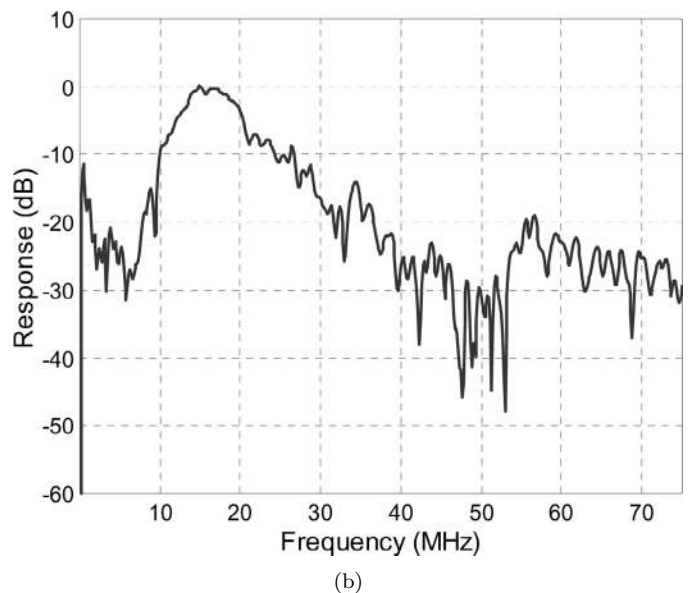
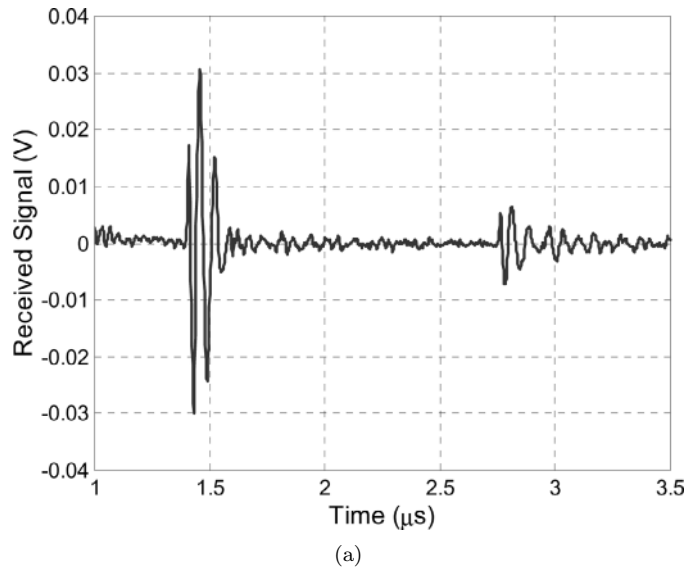


Fig. 11. (a) The pulse-echo response of a CMUT consisting of 16–32- μm diameter membranes. (b) The frequency spectrum of the first echo signal in (a) showing 60% fractional bandwidth at about 16 MHz.

tion for high-performance IVUS arrays. We believe that this approach will be economical due to small silicon area per array and will open up the possibility for further integration of various sensors with CMUT imaging arrays.

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